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# Front-end electronics for high rate, position sensitive neutron detectors<sup>☆</sup>

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## Abstract

Advanced neutron detectors for experiments at new spallation sources will require greater counting rate capabilities than previously attainable. This necessitates careful design of both detector and readout electronics. As part of a new instrument for protein crystallography at LANSCE, we are constructing a detector whose concept was described previously (IEEE Trans. Nucl. Sci. NS-46 (1999) 1916). Here, we describe the signal processing circuit, which is well suited for <sup>3</sup>He detectors with a continuous interpolating readout. The circuit is based on standard charge preamplification, transmission of this signal over 20 meters or so, followed by sample and hold using a second order gated baseline restorer. This latter unit provides high rate capability without requiring pole-zero and tail cancellation circuits. There is also provision for gain-adjustment. The circuits are produced in surface mounted technology. © 2001 Elsevier Science B.V. All rights reserved.

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## 1. Introduction

Neutron scattering experiments are an important complement to X-ray scattering in the determination of structure of a wide range of materials, particularly in biology, solid state

physics and material science. We are fabricating an advanced, position sensitive, neutron detector [1] for protein crystallography studies at Los Alamos National Laboratory. The detector is based upon our previous experience in this field [2,3], covers 120°, provides time-of-flight information and an increased count-rate capability.

A block diagram of a section of the detector and readout system is shown in Fig. 1. Some important features are:

- (1) The detection process is based on neutron absorption in high pressure <sup>3</sup>He, followed by charge multiplication at an anode. A signal

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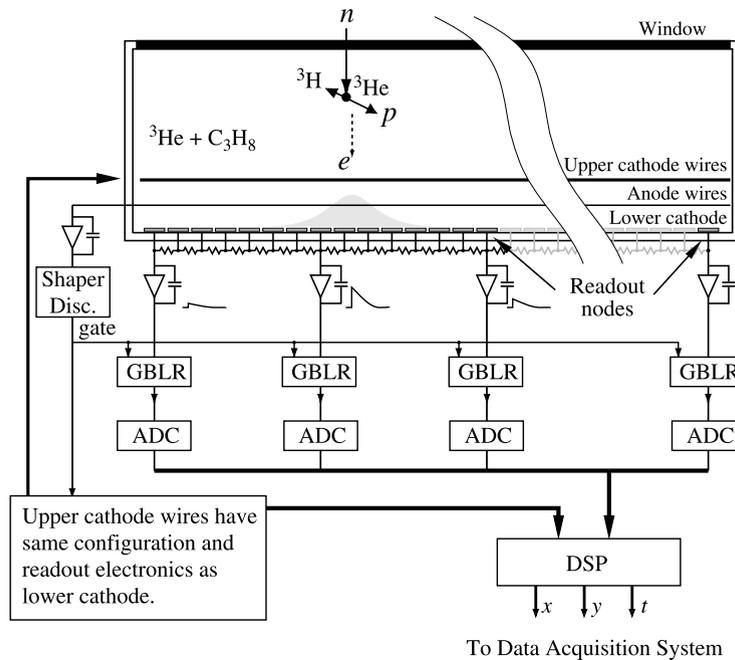


Fig. 1. Block diagram of the detector readout system — part of one axis of one detector segment. (The detector has 8 segments, with  $15X$  and  $17Y$  readout nodes each for a total of 256 channels.)

sampling time of no less than  $1 \mu\text{s}$  is required to ensure that approximately half of the induced charge has been collected.

- (2) Position readout between nodes is accomplished with resistive charge division. A shaping time of  $1 \mu\text{s}$  has been chosen to satisfy condition (1), which also provides optimized preamplifier noise and position linearity.
- (3) Approximately 300 electronic channels are required.

A low noise charge to voltage circuit, incorporating a second order gated baseline restorer (GBLR), has been designed to meet these considerations. For simplicity and cost considerations, fabrication with surface mount technology has been adopted.

## 2. Front-end electronics

The front-end electronics chain (Fig. 2) is designed to read-out the detector signals and to

feed them to ADCs for position analysis (centroid finding) which will be performed by DSP. It is composed of:

- (1) a preamplifier, which integrates the detector current signal,
- (2) a buffer circuit, which provides a gain of about 16 and a differential output to drive twisted-pair cable,
- (3) a shaping circuit composed of:
  - (a) a line receiver which drives a delay line of  $750 \text{ ns}$  to delay the signal for appropriate gating,
  - (b) a one step integrator with  $0.3 \mu\text{s}$  time constant,
  - (c) a second order gated base line restorer to provide correction for both the instantaneous value and the slope of the baseline. It is a time variant, double differentiation equivalent filter,
  - (d) a sample & hold circuit (analog memory stage) to maintain the measured value until digitization.

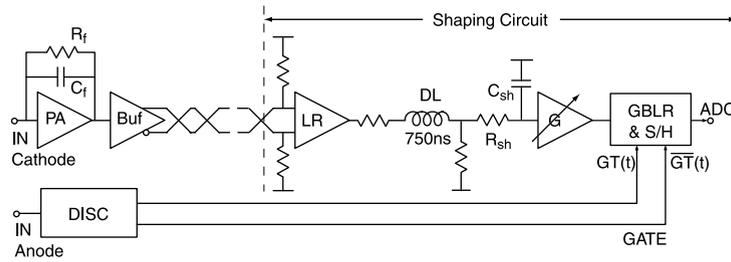


Fig. 2. Schematic of the analog front-end electronics (1 channel).

### 2.1. The preamplifier

This is a charge sensitive preamplifier, Fig. 3, with feedback capacitance  $C_f = 4.7$  pF, feedback resistance  $R_f = 2$  M $\Omega$ . The input impedance of the preamplifier is

$$R_{in} = \frac{1}{g_m} \frac{C_0 + C_f}{C_f} \approx 93 \Omega \quad (1)$$

where the dominant pole capacitance  $C_0 = 2$  pF and the input FET transconductance  $g_m = 15$  mA/V. A relatively high value of the  $C_f$  is chosen in order to minimize  $R_{in}$  whose value is required to be negligible ( $\leq 0.5\%$ ) compared with the inter-node resistance of the charge division resistive chain, for position linearity considerations.

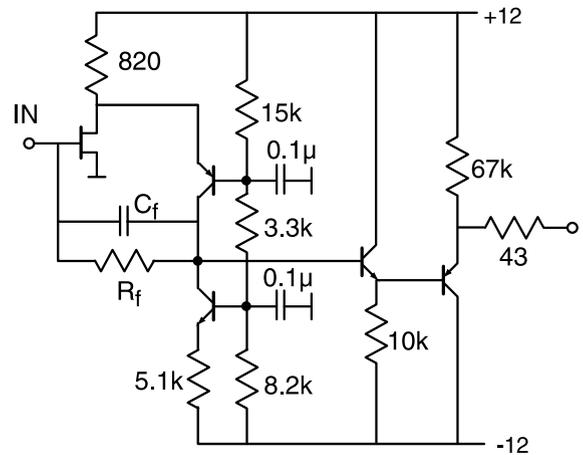


Fig. 3. The preamplifier circuit diagram.

### 2.2. The buffer circuit

Because of the low gain in the preamplifier (0.213 V/pC with  $C_f = 4.7$  pF), a buffer circuit is added to provide voltage gain (Fig. 4). It also provides differential drive for a twisted pair cable connecting the preamplifier to the rest of the front-end electronics.

It is composed of a first stage that has a gain of 4 and a second stage that has differential output with a gain of 4 (from the input to one of the differential outputs). Thus, the total buffer gain is 16. For example, 20 mV at the input will give 320 mV across the buffer outputs when terminated in 100  $\Omega$ .

### 2.3. The shaping circuit

The input of the shaping circuit is a line receiver with  $2 \times 50 \Omega$  input for proper termination of the

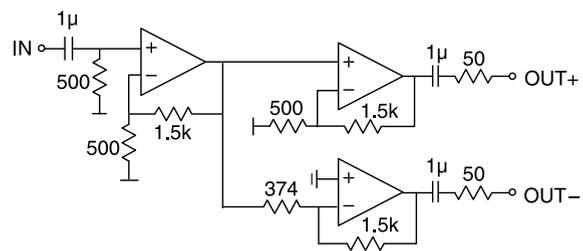


Fig. 4. Buffer schematic diagram.

twisted pair cable. The line receiver gain is about 1.6 and it drives a 750 ns, 100  $\Omega$  delay line which is terminated at both ends. This is followed by RC integration of  $\tau_{sh} = 0.3 \mu s$ .

A digitally controlled, variable gain amplifier precedes the gated base line restorer to provide a

nominal signal level of about 1 V. The gain is defined by software control and can be set to four different values: 4, 8, 12 and 16. This permits the input voltage of the GBLR to be maintained in an appropriate range for different detector gas gains.

The principles of the gated base line restorer [3–5] are explained using the simplified circuit diagram in Fig. 5. It is a second order time variant filter, as reflected by the high input impedance of the GBLR when the switch SW is open, and near-zero input impedance when SW is closed. When there is no selected event SW is closed and the GBLR input voltage  $V_s(t)$  is maintained close to zero. When an event of interest is selected, SW opens during  $T_g$ , the width of the gate pulse, and the circuit provides two types of correction:

- (1) If the base line, prior to  $C_1$ , at the GBLR input is a constant DC voltage, the current  $I_{C1}(t)$  supplied by the OTA amplifier to  $C_1$  is zero. The DC voltage of the base line is memorized on  $C_1$  during  $T_g$ , and added to the signal at the S/H input.
- (2) If the base line is slowly moving, the current  $I_{C1}(t)$ , supplied by the OTA to  $C_1$  is not zero and its amplitude, defined by the voltage memorized on  $C_2$  depends on the base line slope at gate opening time. This constant current will give linear approximation, of the base line change at the gate opening time, and will correct for the preamplifier decay, for the tail of the detector signal and pile-up effects.

Both corrections (1 & 2) acts in addition.

With the sample and hold, the GBLR is equivalent to triple correlated sampling circuit.

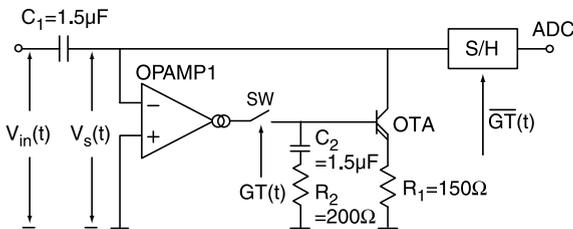


Fig. 5. Simplified diagram of the GBLR.

The closed loop transfer function, for this case is given by

$$\frac{V_s(p)}{V_{in}(p)} = \frac{p^2}{(p - \alpha_1)(p - \alpha_2)} \quad (2)$$

where

$$\alpha_{1,2} = \frac{-GR_2}{2R_1C_1} \pm \frac{\sqrt{G}\sqrt{GR_2^2C_2 - 4R_1C_1}}{2R_1C_1\sqrt{C_2}}. \quad (3)$$

$G$  is the transconductance gain of OPAMP1.

With an input defined by

$$V_{in}(p) = \frac{1}{p - \alpha_e} \quad (4)$$

the output will be

$$V_s(p) = \frac{p^2}{(p - \alpha_e)(p - \alpha_1)(p - \alpha_2)} \quad (5)$$

and in the time domain

$$\begin{aligned} V_s(t) = & \frac{\alpha_e^2}{(\alpha_e - \alpha_1)(\alpha_e - \alpha_2)} e^{\alpha_e t} \\ & + \frac{\alpha_1^2}{(\alpha_1 - \alpha_e)(\alpha_1 - \alpha_2)} e^{\alpha_1 t} \\ & + \frac{\alpha_2^2}{(\alpha_2 - \alpha_e)(\alpha_2 - \alpha_1)} e^{\alpha_2 t}. \end{aligned} \quad (6)$$

With  $\alpha_1 \ll \alpha_e$  and  $\alpha_2 \ll \alpha_e$ , and with  $\alpha_1 \approx \alpha_2$ , the long tail ( $\alpha_e$ ) part of Eq. (6) will be negligible, as will be the base line fluctuation due to the background pulses.

During the decay of  $V_{in}(t)$  there will be a current  $I_{C1}(t) = C_1 dV_{in}(t)/dt$  discharging  $C_1$ .

When a valid event arrives (on the tail of a preceding one), the switch will open ( $\approx 50$  ns before). The capacitor  $C_2$  will retain the voltage necessary to maintain the correction current through  $C_1$ , compensating for the slope of the input baseline. This is in addition to the instantaneous value of the baseline stored on  $C_1$ .

The sample and hold (S/H) switch operates in conjunction with the base line restorer switch and will forward the pulse amplitude to the ADC.

The current in  $C_2$  is defined by

$$I_{C2}(t) = GV_s(t). \quad (7)$$

Using Eq. (6)  $I_{C2}(t)$  has been calculated and is presented in Fig. 6.

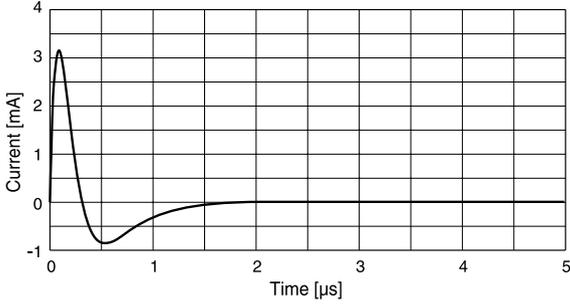


Fig. 6. Charging current of  $C_2$ .

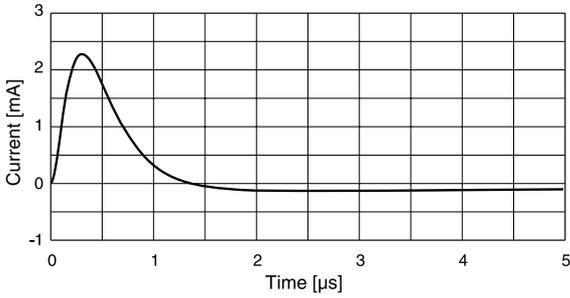


Fig. 7. Charging current of  $C_1$ .

The current capability of OPAMP1 is 2.2 mA.  $I_{C2}(t)_{\max}$ , Fig. 6, is 3.1 mA. The small saturation for input events giving an output larger than 0.7 V can be tolerated.

The voltage on the capacitor  $C_2$  is given by

$$V_{C2}(t) = \frac{G}{C_2} \int_{-\infty}^t V_s(t) dt. \quad (8)$$

The current charging  $C_1$  presented in Fig. 7, is given by

$$I_{C1}(t) = \frac{V_{C2}(t)}{R_1}. \quad (9)$$

The maximum of the charging current  $I_{C1}(t)_{\max} = 2.3$  mA, much less than the OTA output current capability ( $\approx 22$  mA).

#### 2.4. Noise

To calculate the noise, the weighting function of the time variant circuit [6] has to be calculated first. The weighting function will be obtained by

separating the time intervals corresponding to the switching periods of the GBLR circuit. The time scale for the weighting function will start from the right-hand side going to the left. To calculate the contribution of an elementary noise impulse, at the time when the signal is sampled, the calculation proceeds in 2 steps:

- (1) For impulses arriving at  $u > T_g$ , where  $u = -(t - T_g)$ . The switch SW (Fig. 5) is closed.
  - (a) Just before the opening of the switch, the voltage on  $C_1$ ,  $V_{in}(u - T_g)$  will be subtracted from  $V_{in}(u)_{u>T_g}$ . Hence, the sampled signal will be:  $V_{in}(u)_{u>T_g} - V_{in}(u - T_g)$ .
  - (b) At the moment the switch is opened, the value  $V_s(u - T_g)$ , Eq. (6), has to be added.
  - (c) The correction voltage  $V_{cr}$  created on  $C_1$  by the integration during  $T_g$ , of the current  $I_{C1}(t)$ , Eq. (9), has to be subtracted at the sampling time. Since  $V_{C2}(u - T_g)$ , constant during  $T_g$ , is the sampled voltage on  $C_2$ ,

$$V_{cr}(u - T_g) = \frac{1}{C_1} \int_0^{T_g} \left[ \frac{V_{C2}(u - T_g)}{R_1} \right] dt = \frac{T_g}{R_1 C_1} V_{C2}(u - T_g). \quad (10)$$

- (2) For impulses arriving at  $0 \leq u \leq T_g$ , the output voltage, after the switch is opened, will follow  $V_{in}(u)$ . The sampled value will be  $V_{in}(u)$ . We can, now, write the expression for the weighting function, giving the noise contribution at sampling time. By adding the four terms from (1) and (2) and by replacing the variable  $u$  with  $-(t - T_g)$ ,

$$w(t) = V_{in}[-(t - T_g)] - V_{in}(-t) + V_s(-t) - \frac{T_g}{R_1 C_1} V_{C2}(-t). \quad (11)$$

The complete weighting function for the whole readout chain has to include the RC integration shown as  $R_{sh}C_{sh}$  in Fig. 2. This is not included in Eq. (11) for simplicity. The convolution of Eq. (11) and the RC integration, normalized to the maximum response for an impulse (delta function) input at  $t = 0$ , is shown in Fig. 8. This is the

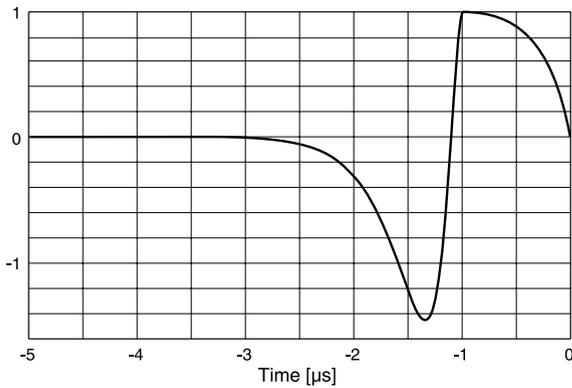


Fig. 8. Weighting function for the overall readout chain. The negative lobe can be made smaller, but longer, by increasing  $R_1 C_1$ , in the GBLR.

weighting function of the whole chain and is similar to a bipolar shaping. The base line occupation of around  $3 \mu\text{s}$  defines the count-rate limit for one readout segment.

Using the weighting function from Fig. 8, the theoretical equivalent noise charge (ENC) of the overall chain is calculated by Eq. (12) [4,7] and plotted in Fig. 9 as a function of the detector capacitance per node ( $C_D$ ).

$$\sigma_q = \left[ 2kTR_s \left( \frac{C_D}{2} + C_s + C_{\text{FET}} \right)^2 \int_{-\infty}^{\infty} [w'(t)]^2 dt + \frac{4kTC_D}{\alpha T_g} \int_{-\infty}^{\infty} w^2(t) dt \right]^{1/2}. \quad (12)$$

$C_D$  is the detector cathode capacitance per node,  $C_s$  is the capacitance from connections and feedthroughs etc., and  $C_{\text{FET}}$  is the capacitance of the input FET. The equivalent noise parallel resistor  $R_P = R_D/2 \sim 25 \text{ k}\Omega$  in this detector.  $R_D$  is the value of the total resistive chain over a readout node, which in turn is determined by the detector electrode capacitance and the integration time (in this case, gate width  $T_g$ ):  $R_D C_D \sim T_g = 1 \mu\text{s}$ . The coefficient  $\alpha < 1$  (in our case 0.86) has been added to compensate for the effect on noise to the distributed  $R_D$ . The equivalent serial input noise resistor  $R_s$  is assumed to be  $100 \Omega$ . The noise obtained, for  $C_D = 20 \text{ pF}$  and  $C_s + C_{\text{FET}} = 40 \text{ pF}$ , is  $\approx 4900$  electrons RMS.

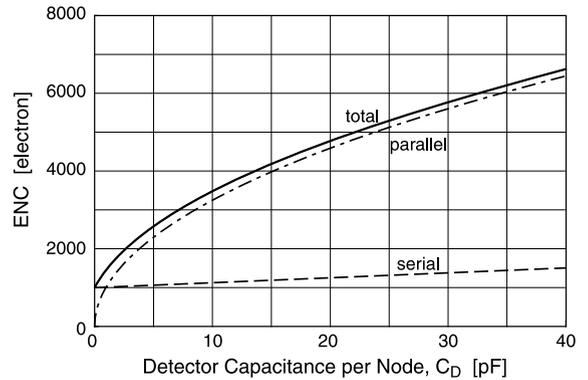


Fig. 9. Calculated noise for the front-end circuit.

The noise generated by  $R_D$  will be dominating and due to relation  $T_g \geq R_D C_D$  which has to be satisfied to get good position linearity, the noise will depend on essentially the detector  $C_D$ . For a given  $T_g$ ,  $C_D$  must be made as small as possible!

Fig. 10 shows the principal analog signals: the delay line output  $V_{\text{DL}}(u)$ , the gating signal  $GT(t)$  and a method to interpret the influence of the weighting function  $w(t)$  on the output of the GBLR.

Measurements at the S/H output give the following noise contributions:

- (1) GBLR, with no cable at the GBLR input, of 0.65 mV RMS,
- (2) noise when the buffer circuit is added, but without the preamplifier, of 1 mV RMS,
- (3) noise contribution for the overall chain with  $C_D = 20 \text{ pF}$  and  $R_P = 25 \text{ k}\Omega$  of 8 mV RMS which, after calibration by  $\delta(t)$  current pulses, corresponds to 4800 electrons.

Thus, there is good agreement between calculated and measured noise.

## 2.5. Signal size

The design goal in position resolution of this detector is about 1.5 mm FWHM. In  $^3\text{He}$  filled neutron detectors, position resolution is ultimately limited by the neutron interaction process in the gas. The gas mixture is chosen to satisfy as closely

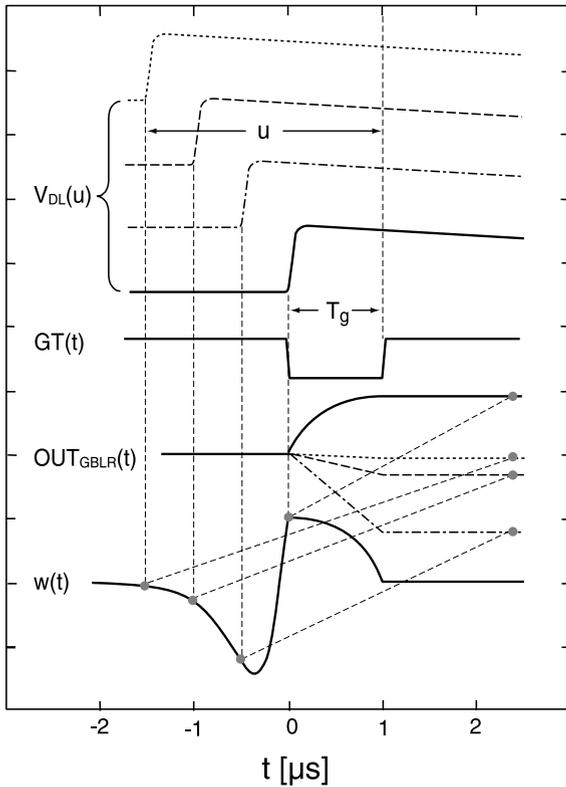


Fig. 10. Interpretation of the GBLR weighting function.

as possible the required detection efficiency and position resolution, within the constraints of the maximum allowable working pressure. A gas limit of approximately 1.3 mm FWHM is achieved in our operating mixture (6 atm  $^3\text{He}$ , 2.5 atm propane). The final resolution is represented by the quadratic addition of the gas limit and all other dispersive effects, the major factor in this device being electronic noise. We, therefore, aim for an electronic noise contribution of no more than 0.9 mm FWHM to achieve the design goal.

A detailed study of the position resolution in a detector with resistive charge division can be found in Ref. [3]. In our case, noise limited position resolution can be expressed as

$$\sigma_x = a \frac{\text{ENC}}{Q_s} L, \quad (13)$$

where  $\sigma_x$  is the RMS position resolution, ENC is the rms noise charge,  $Q_s$  is the total charge signal

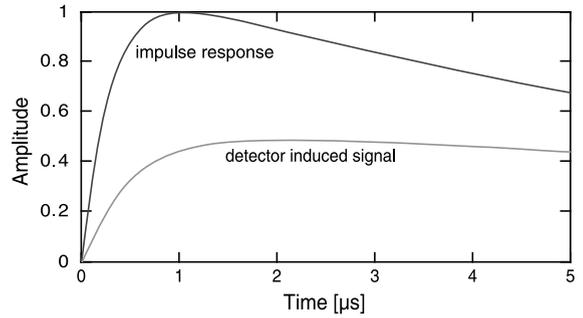


Fig. 11. GBLR input signals for a delta current impulse (upper curve) and the induced current pulse from a point charge moving away from the anode (lower curve). Both current pulses produce equal amount of charge. The RC integration time constant is 0.3  $\mu\text{s}$ .

involved in the charge division,  $L$  is the readout node spacing and  $a$  is a constant determined by the number of channels used in the centroid calculation and the characteristics of the signal filter.  $a$  is about 1.5 for the circuit used here, and  $L$  is 1.27 cm. An upper limit of 0.4 mm on  $\sigma_x$  ( $\sim 0.9$  mm FWHM) determines a lower limit on  $Q_s$  of 40 fC. To produce 40 fC on each cathode plane, an anode charge level of  $\sim 0.1$  pC measured in 1  $\mu\text{s}$  is needed.

The signal waveform in the first a few microseconds from a neutron event can be approximated by the induced current pulse of a point charge  $Q$  drifting in the cylindrical field close to the anode wire:

$$i(t) = kQ \frac{1}{t - t_0} \quad (14)$$

where  $k$  is a constant determined by electrode geometry, and  $t_0$  is a characteristic time constant, which is about 2 ns in this case. The GBLR input waveform from this induced signal is shown in Fig. 11, together with the waveform from a delta current impulse of equal net charge. The difference from unity in amplitude at  $t = 1 \mu\text{s}$  represents the ballistic deficit, about 55% in this case. Therefore, to obtain a 0.1 pC charge on the anode at 1  $\mu\text{s}$  requires a final anode charge of about 0.2 pC. The ionization from the proton and triton created in the original neutron interaction with a  $^3\text{He}$  atom releases 764 keV of kinetic energy, or close to

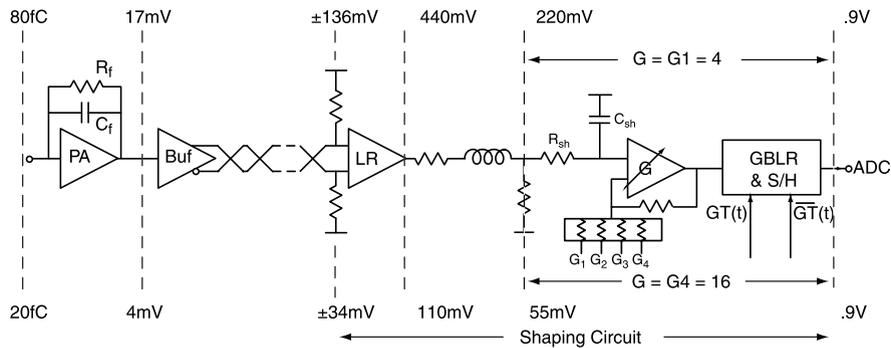


Fig. 12. Front-end amplification and shaping circuit with signal voltage indications.

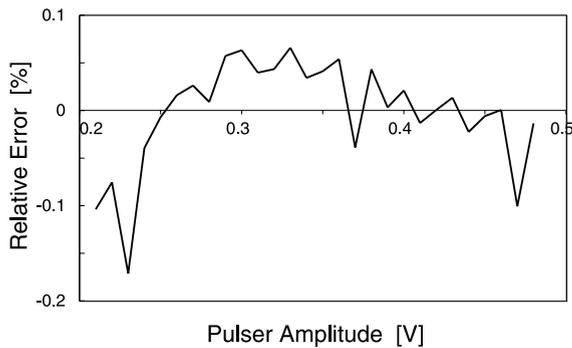


Fig. 13. Differential error from the linearity test.

$2.5 \times 10^4$  electron/ion pairs in our gas mixture. Taking account of the ballistic deficit, the detector requires a gas gain of only about 50 to generate 100 fC in 1  $\mu$ s, a value that has permitted long term, stable operation of these types of detector in many existing applications [2].

The curves in Fig. 11 reflect an  $R_{sh}C_{sh}$  integration time of 300 ns before the GBLR input (Fig. 12). The value is optimized for noise filtering and recovery time.

## 2.6. Dynamic range and linearity

In Fig. 12, the gains and signal voltage levels are shown at different stages of the overall circuit for two extreme detector gas gains. There is digital control of the electronic gain in order to compensate for different values of gas gain.

The linearity of the circuit has been measured and the differential errors are given in Fig. 13. The linearity is better than 0.3% up to 2.5 V output signal swing.

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