LSST sensor testing and front-end electronics

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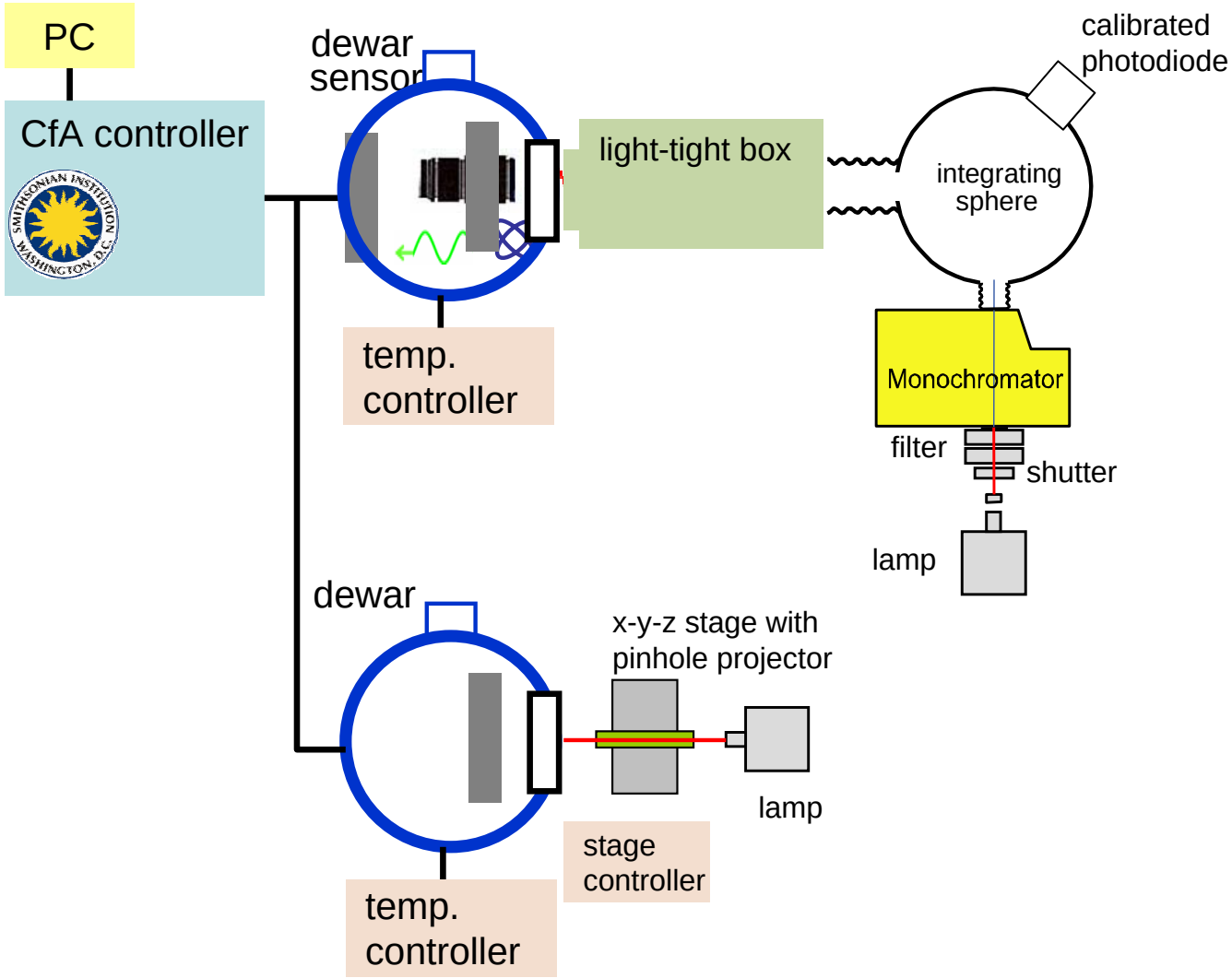
Sensor optical and electrical tests (CCD baseline)

- Imaging array
  - Cosmetics (bright/dark pixels, traps, glow)
  - Dark current vs. temperature
  - Charge transfer efficiency
  - Quantum efficiency, 400 – 1050 nm
  - Response uniformity (flat field) in *grizy* filters
  - Full well capacity
  - Point spread function/MTF
  - Remnant image
- Readout amplifiers
  - Gain
  - Read noise vs. frequency
  - Linearity
  - Crosstalk

Sensor test facility

- Develop infrastructure to operate, characterize large-area multisegment sensors
- Prepare for testing of pre-prototype LSST sensors from vendor Phase II contracts.
- Two controllers (4- and 32-channel) based on CfA MegaCam design under construction:
  - 4-channel controller is operational and being debugged
  - Boards and components for 32-channel system on hand
  - Develop capability with borrowed large-format CCD until sensors from Phase II vendor contracts arrive
- LN_2 cryostats, temp. controller, DAQ computer on hand
- 430 sq ft former Hybrid Circuits lab under renovation (shared w/raft metrology), expect to occupy space by end of October.

Sensor test facilities (prototype evaluation phase)



defects
crosstalk
imaging

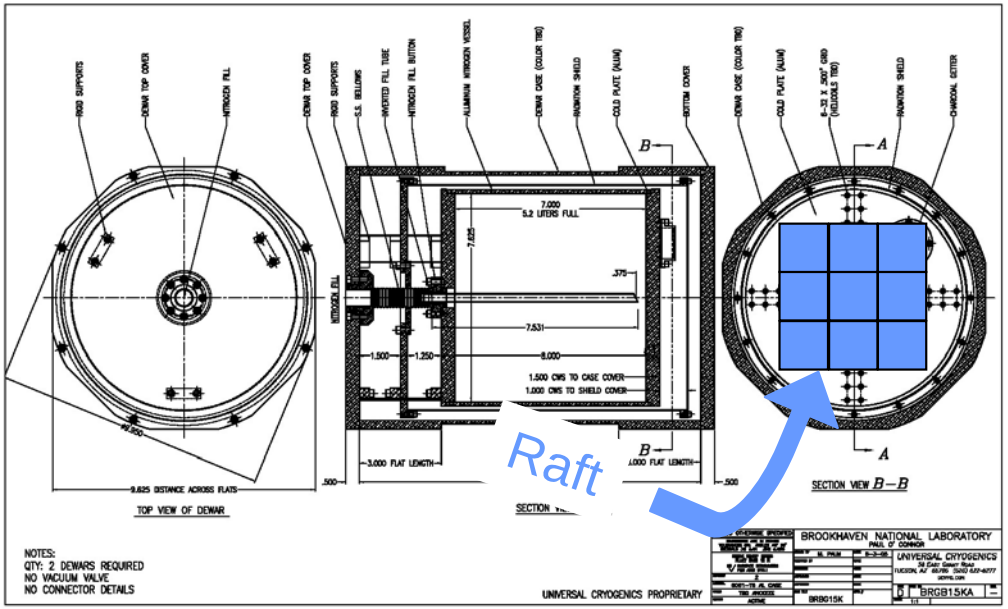
dark current
CTE
full well
noise, gain
persistent image

QE

PSF

Sensor test facility

Lab B-121B under renovation



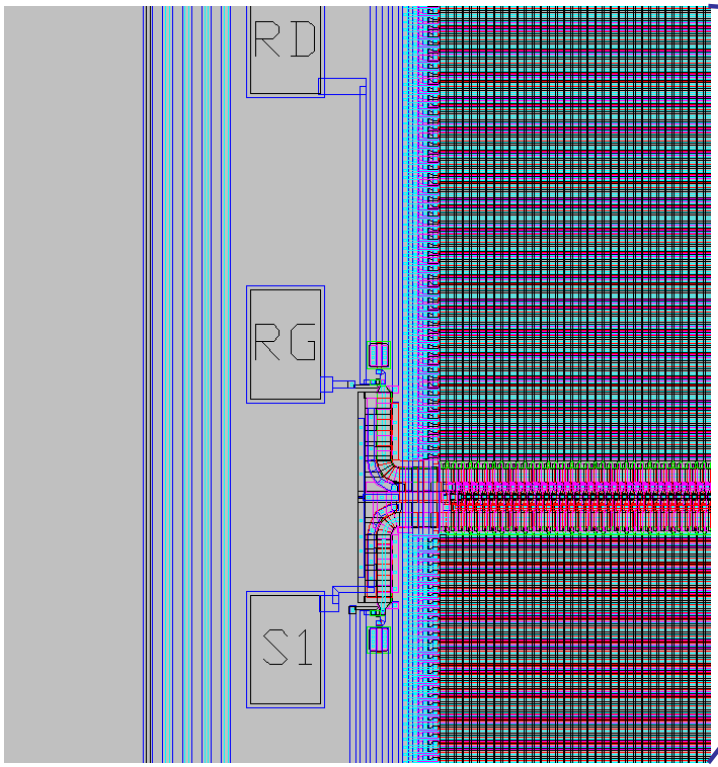
Univ. Cryogenics 8” Dewar

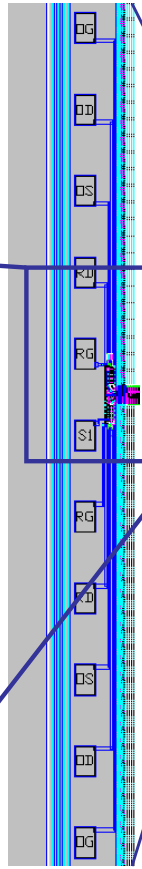
Horizontal laminar flow bench

ADC board for controller

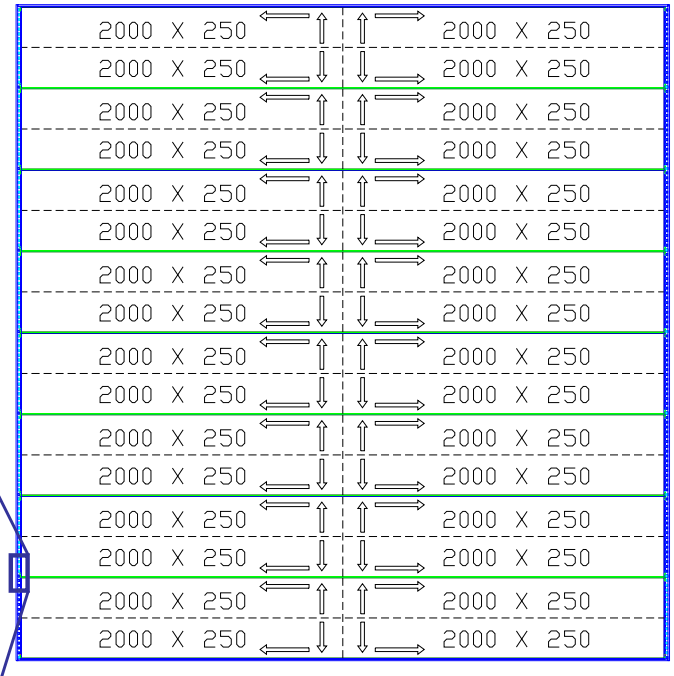
Multi-port 4K x 4K CCD strawman

Detail of output port





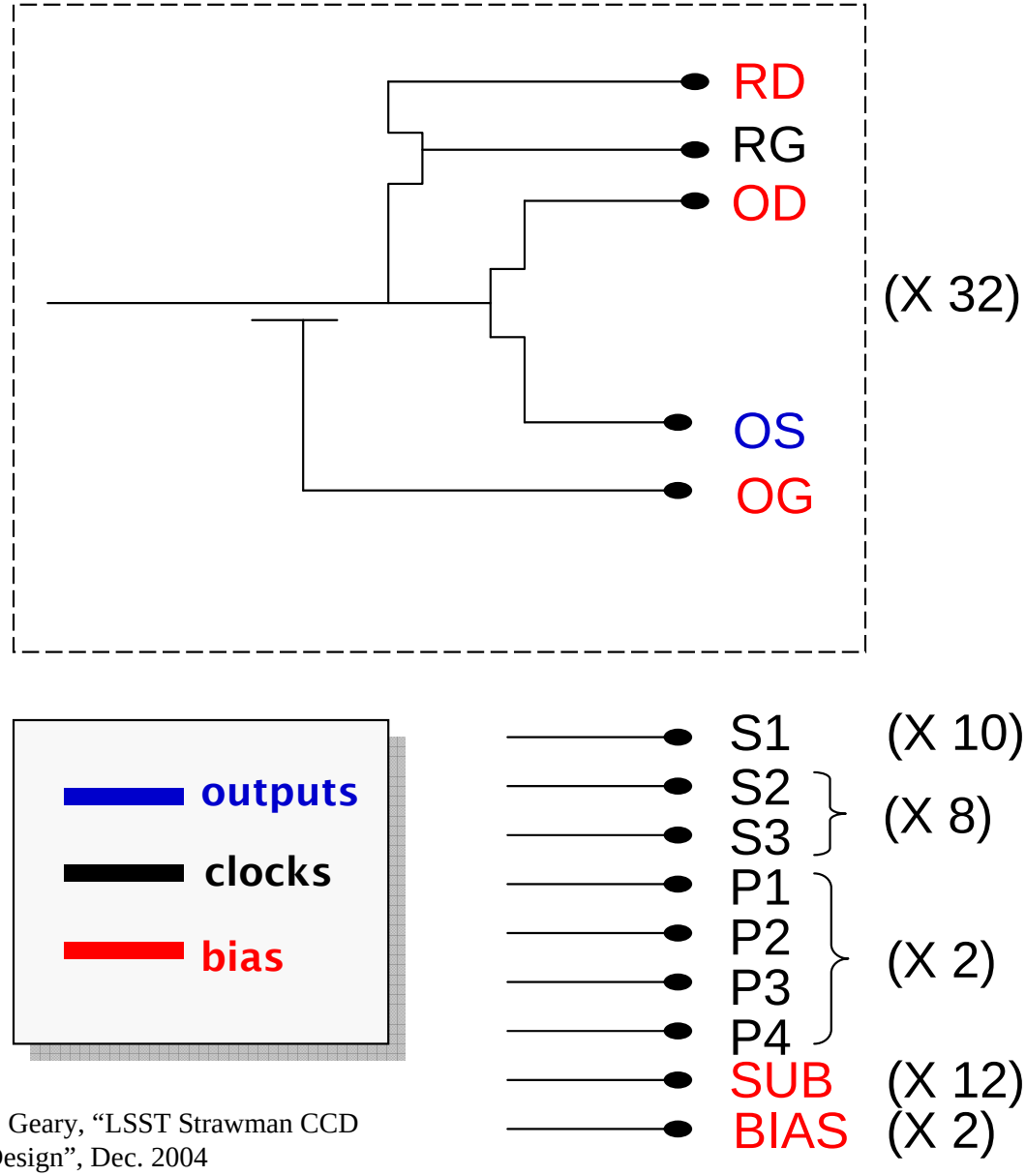
Detail of one edge



Full CCD showing segmentation. Note pads on left and right edges only

Strawman has 208 pads total

CCD connections



per CCD :

32 output
66 clock
110 bias
208 TOTAL

per raft (9 CCDs):

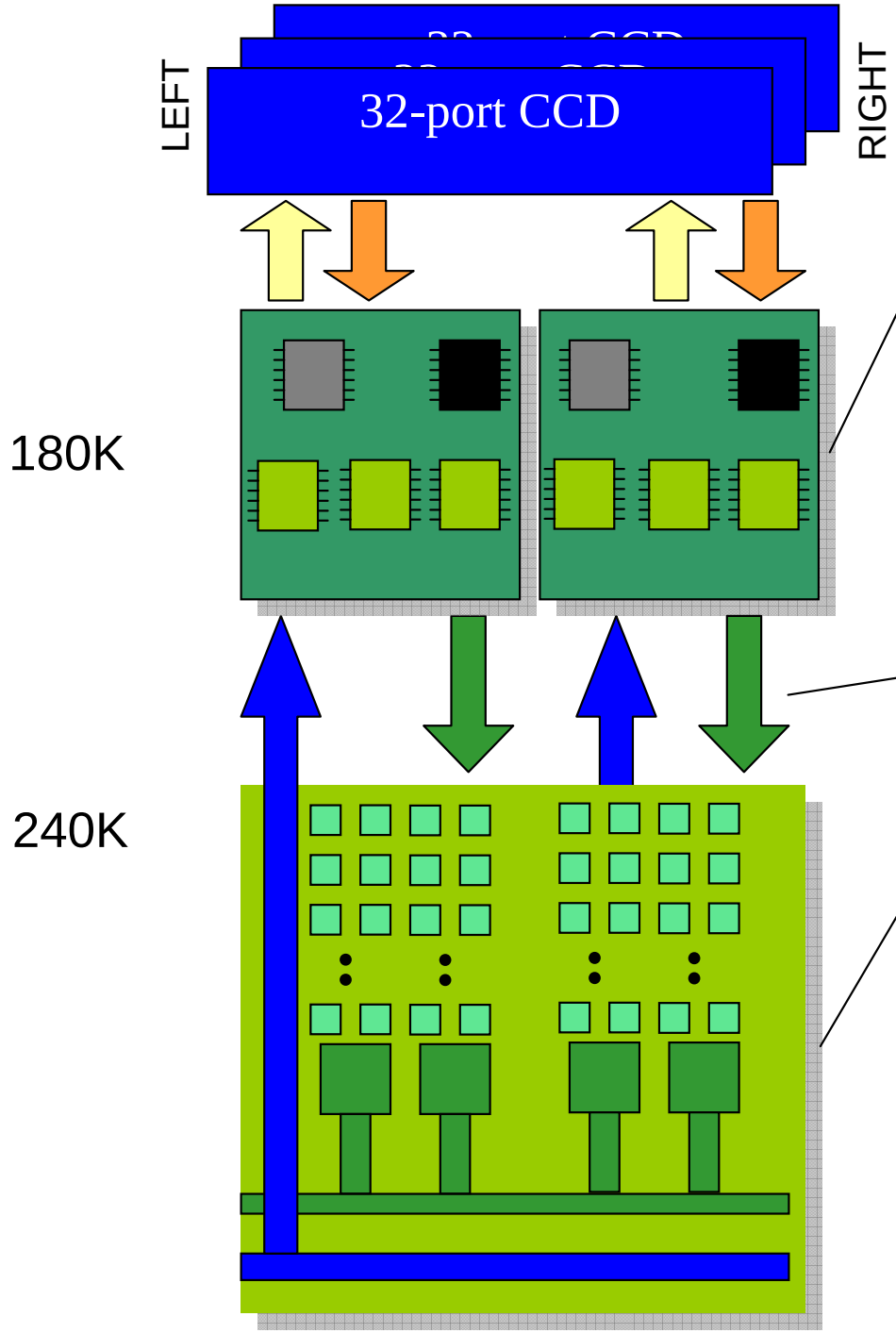
288 output
594 clock
990 bias
1872 TOTAL

per full FPA (201 CCDs):

6432 output
13266 clock
22110 bias
41808 TOTAL

J. Geary, "LSST Strawman CCD Design", Dec. 2004

In-dewar electronics partitioning (baseline)



Front End Boards (6 per raft):

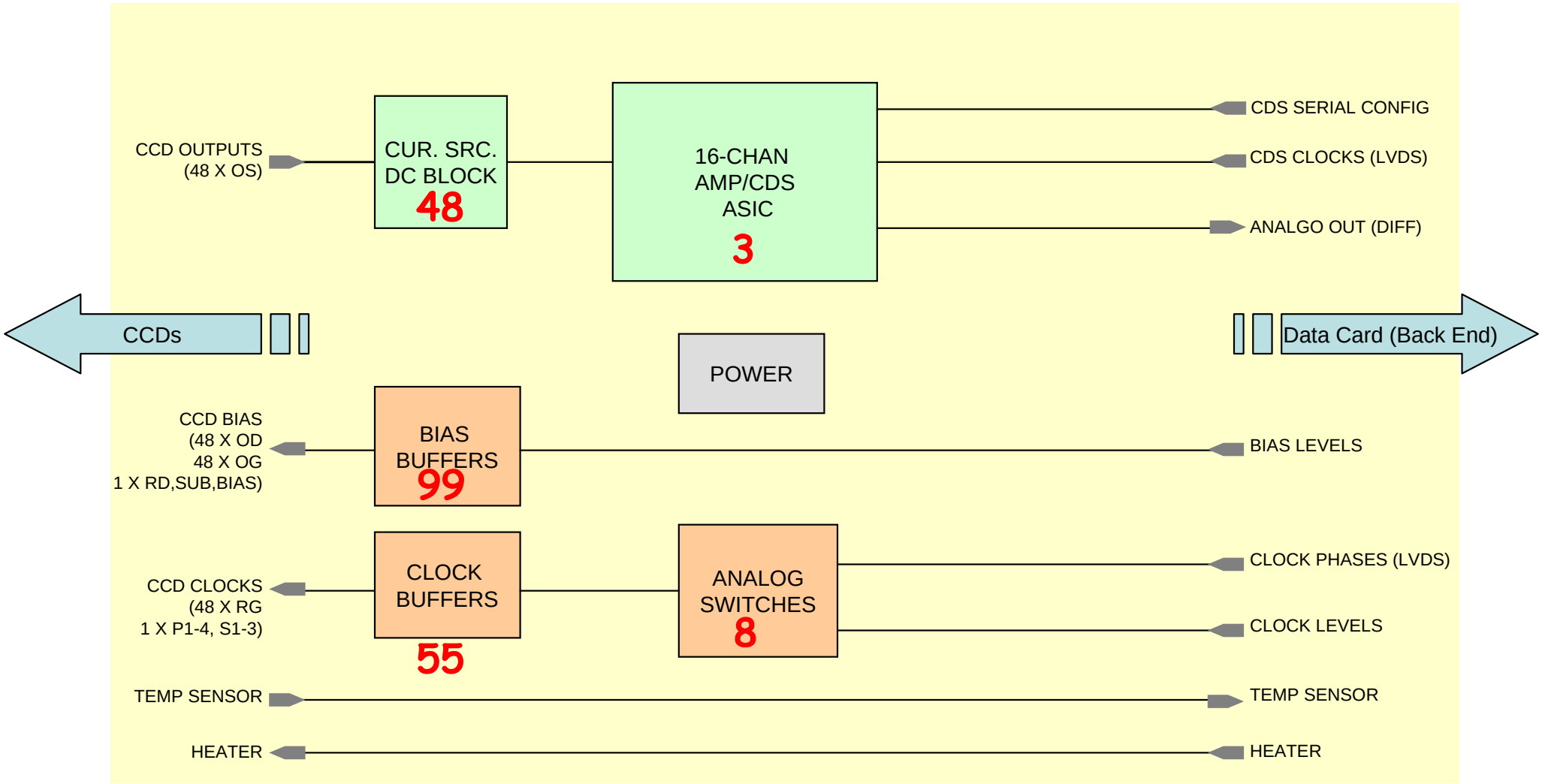
- 48-channel video signal chain through CDS processing
- clock and bias drive

Flex cables

Data Card:

- differential receiver
- signal chain ADC
- frame buffer
- data transport to optical fiber
- clock pattern generation
- clock and bias DACs

48-channel Front End Board (FEB) for CCD sensor

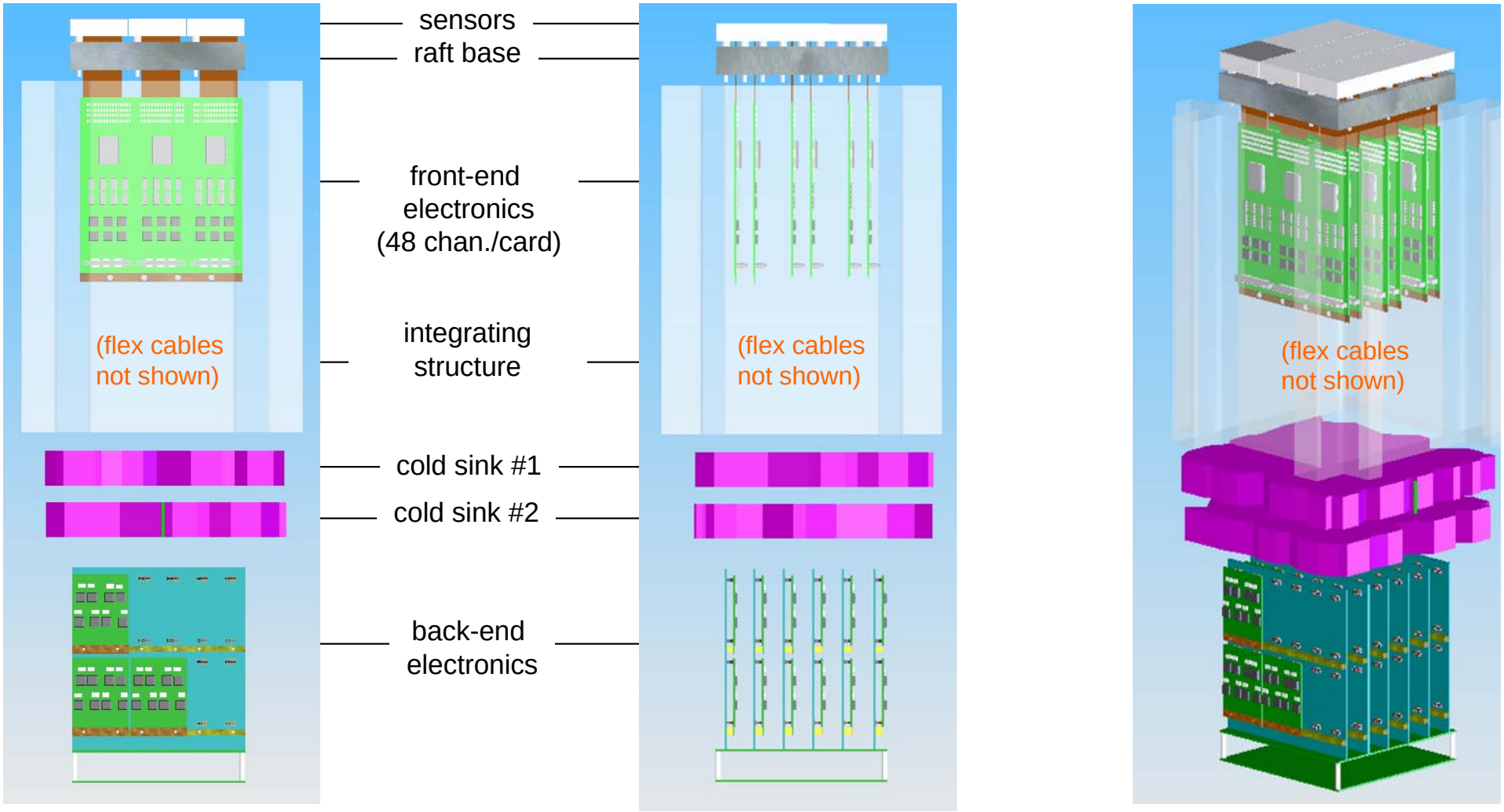


FUNCTIONS:

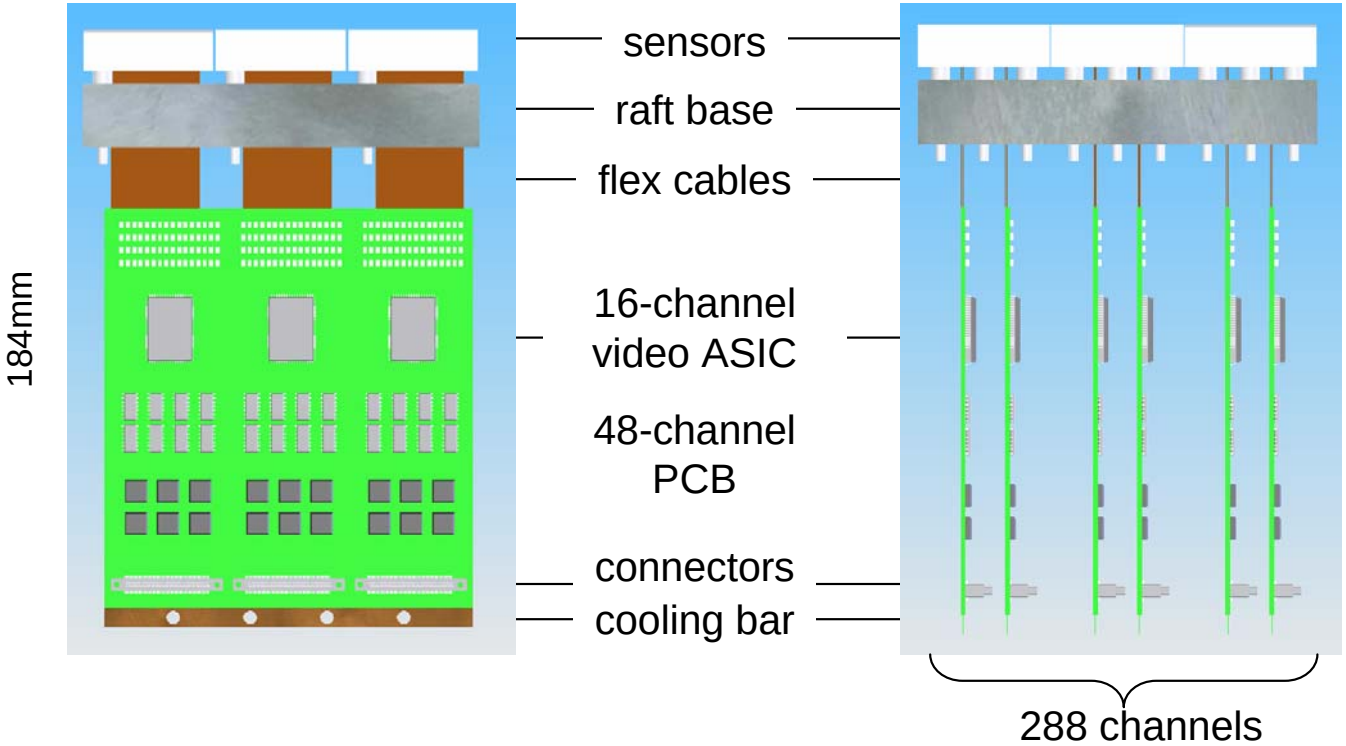
Preamplification and CDS processing
Clock and bias drivers
Temp sensor and heater

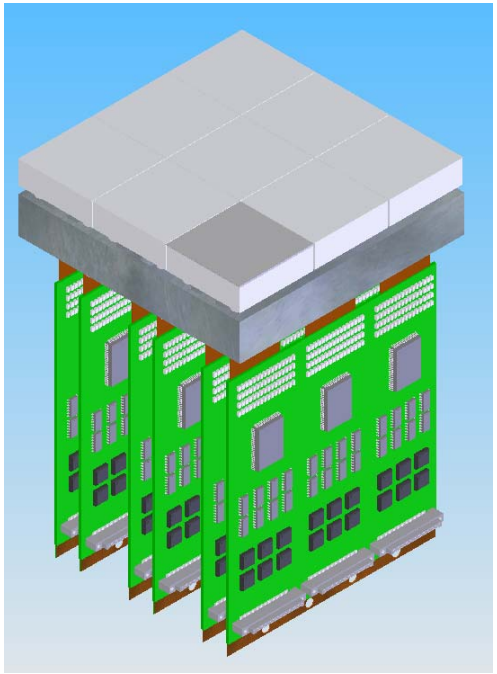
assumes bussing of all clock, bias except OD, RG, OG, which have individual buffers for each output port for isolation

Physical layout of in-dewar electronics



ASIC location on front-end card





600 – 1000 wire interface to BEE

cooling, alignment not shown

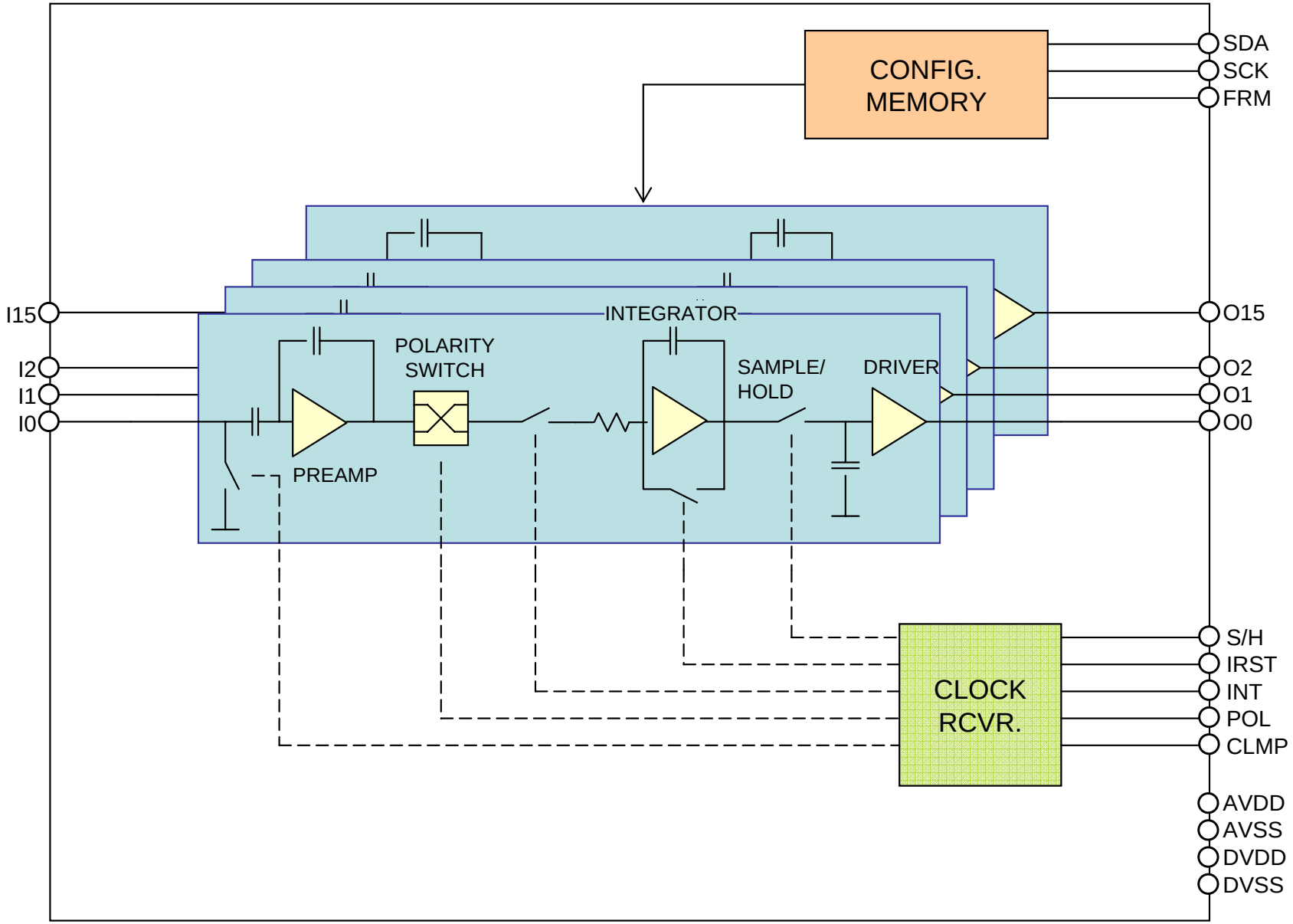
LSST signal chain ASIC

- Functions:
  - current source for CCD source follower (opt.)
  - DC block (opt.)
  - preamp
  - CDS by dual-slope integration
  - S/H
  - differential driver to back-end electronics

- Requirements:

– channels	16 (goal)
– pixel rate	250-500 kHz
– noise	> 4 e^- rms
– dynamic range	93 dB from noise to full well, single gain range
– crosstalk output-output	<< 10^{-3}
– linearity	TBD, depends on calibration scheme
– power	< 50 mW/channel
– temperature	180K and 300K
– technology	0.25 μm CMOS

Signal Chain ASIC Block Diagram

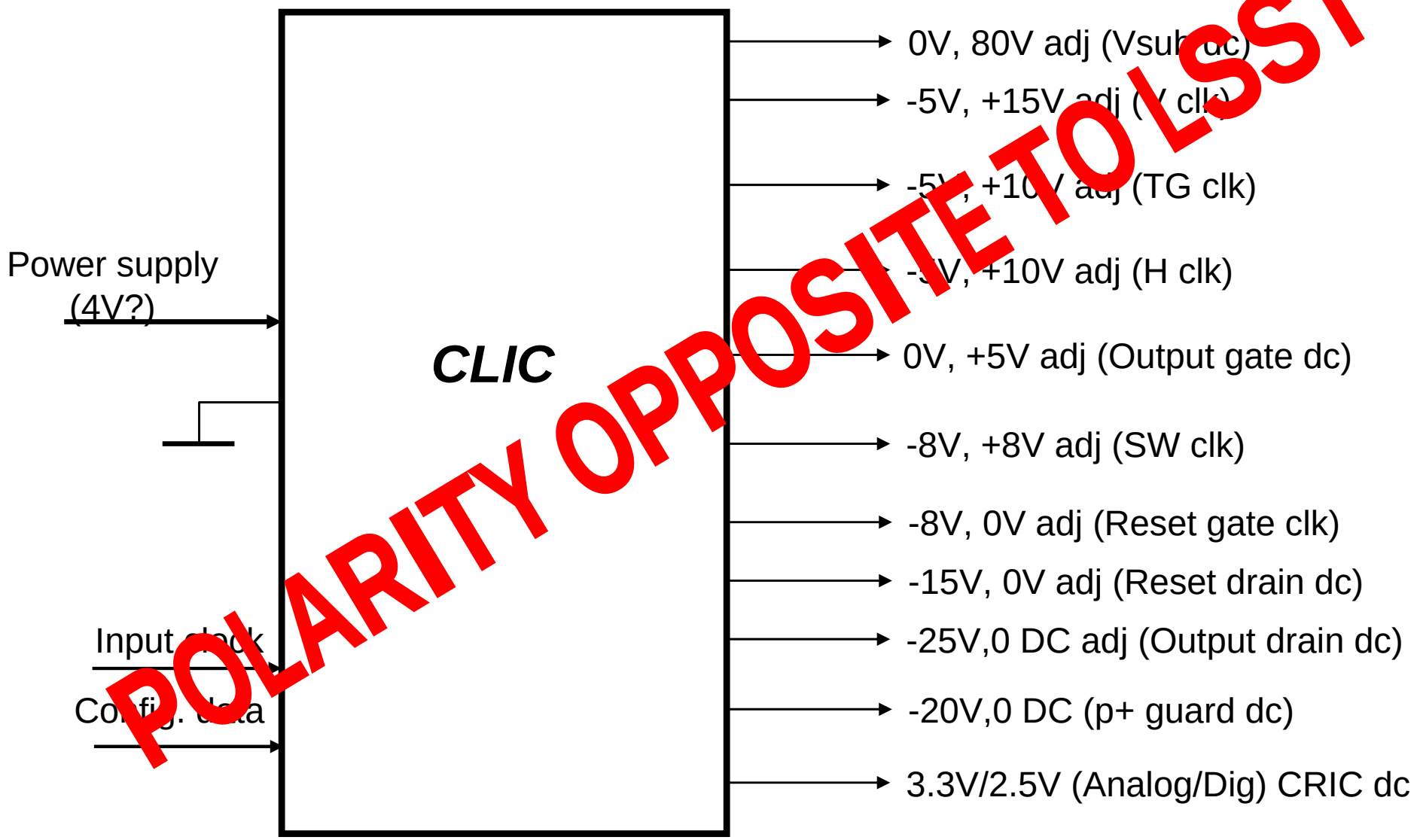


Single-ended blocks shown for clarity

CCD support ASIC

- Readout ASIC alone doesn't simplify in-Dewar electronics enough
- Need to generate, switch, buffer many CCD clock and bias signals
- ASIC solution to reduce circuit board area, active package count, cabling, thermal qualification, power(?)
- Requires high voltage ASIC technology (>20V)
- Possible functions:
  - DC to DC converters
  - Linear voltage regulators
  - DACs
  - Switched output stages
- Parallel development proposed for SNAP: CLIC chip

CLIC chip in development



POLARITY OPPOSITE TO LSST

High Voltage CMOS technology table

Features	AMS	AMS	AMIS	AMIS	ATMEL	DALSA
Min feature size	0.8um/2-3um	0.35um	0.35um	0.7um	0.5um	0.8um
Oxide thickness	17nm/51nm					
Breakdown voltage	50V	50V	80V	100V	85V	300V
Substrate	Bulk/Well		Bulk/Well (SOI avail in the future)	Bulk/well	SOI	Bulk/well
Temperature range						
Transconduct-ance						
Matching						
Noise						
Linear capacitance	Yes 50Vb					Yes 1.35fF/um^2
Linear resistors	Yes 50Vb		Yes 1000Ω/sq	Yes 1000Ω/sq		Yes 5000Ω/sq
Models	BSIM3v3					
Status	Design kit available	Available in July 04	Access through Europractice….	Access through Europractice….	NDA being signed up and Atmel visit	Available

CCD and IC supply voltages

Signal	# of copies	Type	Exposure V_L	Exposure V_H	Readout V_L	Readout V_H	Reset V_L	Reset V_H	Adj. Range V_L	Adj. Range V_H	t_{width} (μsec)	Cap (pF)	I
V1	2	ck	-3.	+5.	-3.	+5.	+9.	+9.	-5.	+15.	50.0	30000	
V2	2	ck	-3.	+5.	-3.	+5.	+9.	+9.	-5.	+15.	50.0	30000	
V3	2	ck	-3.	+5.	-3.	+5.	+9.	+9.	-5.	+15.	50.0	30000	
Transfer-gate	2	ck	-3.	+5.	-3.	+5.	-4.	+6.	-5.	+10.	50.0	30	
H1	4	ck	-4.	+6.	-4.	+6.	-4.	+6.	-5.	+10.	0.50	50	
H2	4	ck	-4.	+6.	-4.	+6.	-4.	+6.	-5.	+10.	0.50	50	
H3	4	ck	-4.	+6.	-4.	+6.	-4.	+6.	-5.	+10.	0.50	50	
Output-gate	4	dc	+2.2	+2.2	+2.2	+2.2	+2.2	+2.2	0	+5.			
Summing-well	4	ck	-5.	+5.	-5.	+5.	-5.	+5.	-8.	+8.	0.50	small	
Reset gate	4	ck	-6.	0	-6.	0	-6.	0	-8.	0	0.15	small	
Reset drain	1	dc	-12.5		-12.5		-12.5		-15.	0			
Output drain	4	dc	-22.		-22.			-22.	-25.	0			<1 mA
Video out	4	ac											
n+ substrate	1	dc		+80.		+80.		0	0	+100.			<1 μA
n+ guard	1	float											
p+ guard	1	dc	-20.		-20.		-20.		-20.	0			
Temp mon+	1	dc											10 μA
Temp mon-	1	dc											

Plus….
3.3V analog (CRIC), 3.3V/2.5V digital (CRIC) 3.3V analog/digital LV.