Low-Noise CMOS Signal Processing IC for Interpolating Cathode Strip Chambers

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Abstract

A CMOS circuit for obtaining precision amplitude and timing information from the cathodes of a proportional chamber with interpolating cathode strips has been developed. The chip performs charge amplification, shaping, analog storage and multiplexing, and generates a prompt timing pulse which can be used for trigger purposes. Novel features of the IC include: preamplifier optimized for large (40-250pF) detector capacitance, digitally programmable gain and bandwidth of the fourth-order shaper, and an array of on-chip capacitors and switches for injecting charge for calibration.

Noise is less than 1500 r.m.s. electrons with an input capacitance of 100 pF using bipolar 550 nsec shaping. Linearity is better than 0.8% over a dynamic range of 1500:1. The constant fraction discriminator has a time walk of ±2.5 nsec over the range 10-500 fC. Power dissipation is 50 mW per channel.

I. INTRODUCTION

Cathode strip chambers (CSCs) are gas multiwire proportional chambers with cathodes segmented into strips and anode-cathode spacing set so that the footprint of the induced charge spans 3-5 strips as illustrated in Figure 1. The track position is found by interpolation. Since the cathode is fabricated photolithographically the strip positions are very precise and the position resolution is typically determined by the accuracy with which charge can be measured. Hence, the electronics plays a key role in determining the resolution. The position resolution is proportional to the noise-to-signal ratio with the proportionality constant between 1.5 and 2. In addition to keeping the effects of noise and crosstalk down to a level that will not degrade the position resolution, the intercalibration of channels must also be accurate to a fraction of a percent.

During 1993 and 1994, a large prototype chamber of this type was used in beam tests to obtain position resolution of 40μm with a strip pitch of 5mm.[1]

II. ARCHITECTURE OF THE IC

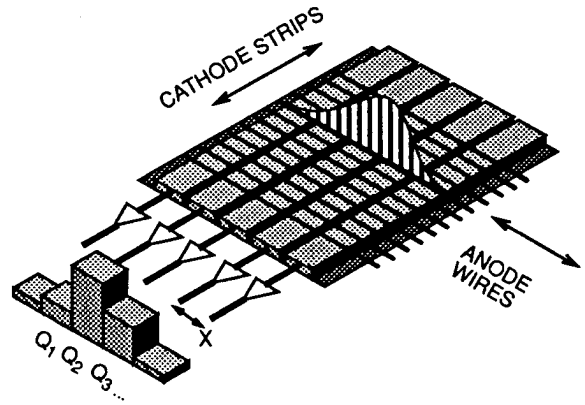

Figure 1: Cathode strip chamber showing orthogonal strips and wires, charge distribution along the wire direction, readout preamps, and charge measured on each strip. The position resolution is $\sigma_X/X = K(\sigma_Q/Q)$, where X is the spacing between readout nodes, Q is the total charge on the cathode, and K is a proportionality constant between 1.5 and 2.

optimized for minimum noise with a detector capacitance of 40-250 pF, followed by amplitude and time measurement sub-channels. The preamp design was described in [2]. The precision amplitude measurement sub-channel has a bipolar semi-Gaussian shaper which is an active filter with 2 zeros and 6 poles. The shaper time constants are set with passive components and use programmable parallel capacitor arrays to provide peaking time control. Digitally programmable gain is provided by a programmable serial resistor array following the preamp. This allows the IC to adapt to changes in experimental conditions, i.e. luminosity upgrades or modification of chamber gain.

Timing is provided by a fast (30 nsec) unipolar shaper followed by a constant fraction discriminator. For calibration purposes, we provide each channel with a 1 and 2 pF MOS capacitor that can be connected to a test pulser input by CMOS switches. The switch array is controlled by a serially-loaded shift register, allowing the user to inject 0,1,2,or 3 units of charge into any channel. This provides the ability to calibrate channels individually or in groups, or to simulate actual events in which charge is shared over three strips, and makes it easier to calibrate crosstalk effects.

All of the circuit blocks have been prototyped individually and in combinations on test chips. Results to be reported in the next section are obtained from a test chip having a complete single

[1]This research was supported by the U.S. Department of Energy: contract No. DE-AC02-76CH00016

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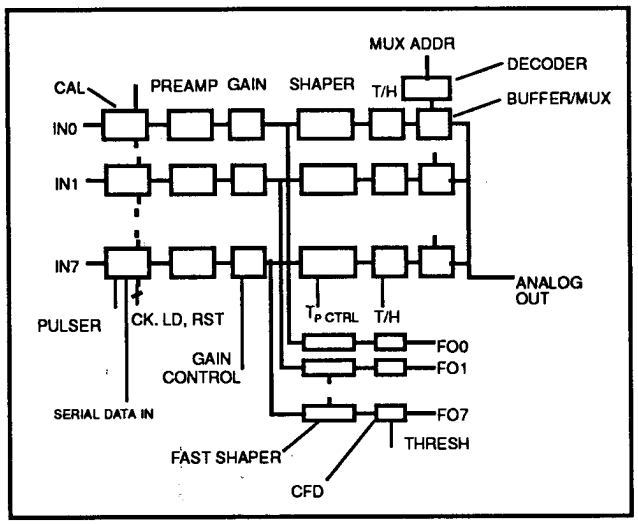

Figure 2: Block diagram of the CSC readout IC.

channel (except for the calibration circuit), unless otherwise noted. The layout of this chip is shown in Figure 3.

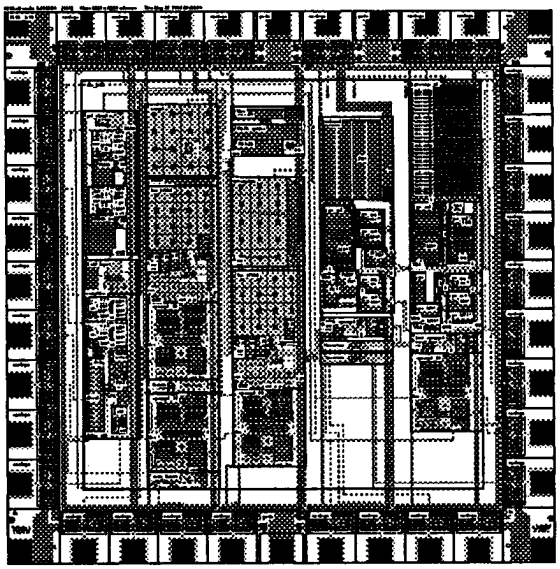

Figure 3: Layout of the CSC readout IC. Dimensions: 2.25 x 2.25 mm. Preamp input is at upper right.

III. RESULTS

1. *Amplitude Measurement Channel*

Figure 4(a) shows the impulse response waveforms at the analog output with four settings of gain control, and in Figure 4(b)

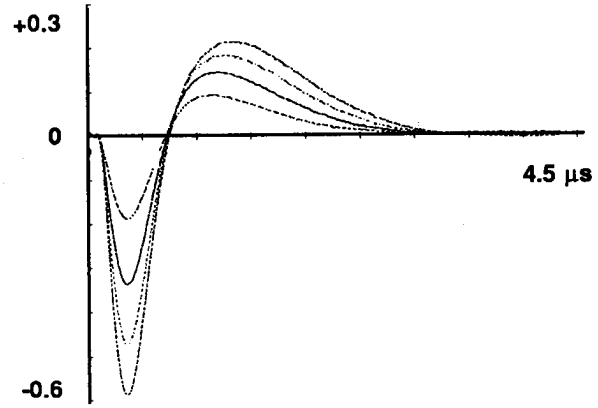

Figure 4(a): Impulse response at the analog output for four settings of the gain control. Time scale from 0 to 4µs.

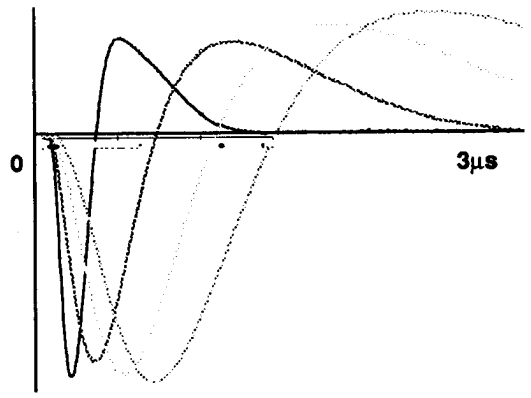

Figure 4 (b): Impulse response at the analog output for four settings of the peaking time control. Time scale from 0 to 3 µs.

four settings of peaking time control are illustrated. There are a total of sixteen settings of these controls, and measurements of the gain and 5%-100% peaking times (t_p) are shown in Figure 5. Simulated values are also shown here. It is clear from the Figure that the gain and peaking time controls are reasonably independent.

Turning to linearity, Figure 6 shows the peak output voltage from the amplitude sub-channel as a function of input charge with gain control set to its two extreme values. It can be seen that the linearity is good nearly up to the power supply rail of 2.5V, and that the chip can be tailored to work with full-scale detector charge from 150 to 500 fC. The integral nonlinearity

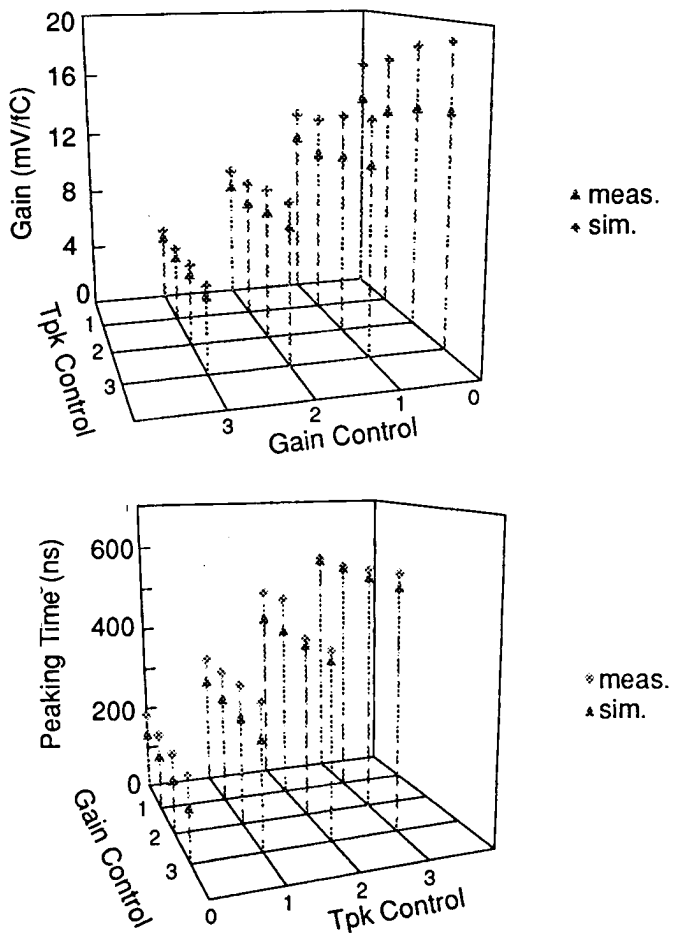

Figure 5: Top, gain as a function of gain and peaking time control settings. Bottom, peaking time (5% - 100%) as a function of the two settings. Measured and simulated values shown.

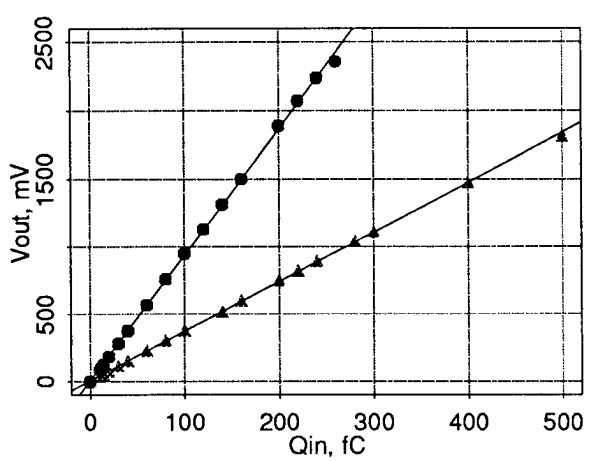

Figure 6: Linearity at different gains. Peak output voltage as a function of input charge for the two extreme settings of gain control.

has been measured for all 16 settings of the shaper control word and for output amplitudes less than ±1.5V it averages 0.8%.

The response of the shaper to current waveforms with tails similar to real gas detectors is compared to its impulse response in Figure 7. We generate a voltage waveform

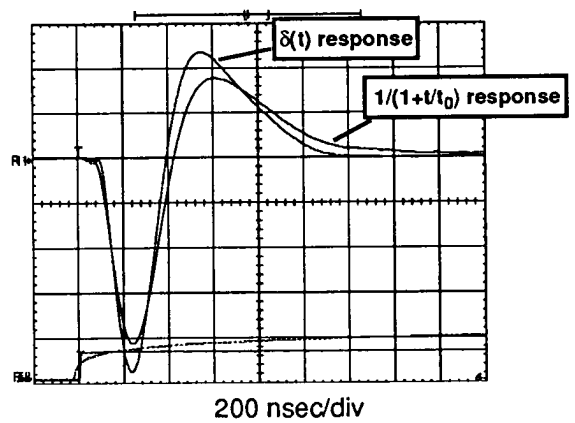

Figure 7: Comparison of impulse response and response to input current with wire-chamber-like time dependence $I_0/(1+t/t_0)$. Lower waveforms: input from pulser. Upper waveforms: shaper output. Horizontal scale: 200 nsec/div.

$V(t) = V_0 \ln(1+t/t_0)$ with an arbitrary waveform generator and apply it to the input through a 1pF capacitor. The resulting current has the form $I(t) = I_0/(1+t/t_0)$, which approximates the shape of the current from a gas detector due to positive ion drift [3]. (The constant t_0 is about 2.5 nsec for these chambers). The return to baseline increases by a few hundred nsec for the wirechamber-like input pulse.

The rate capability of this readout system will be limited either by pileup or by the deadtime due to the track-and-hold. To study the effects of pileup, we apply a two pulses of the form $I_0/(1+t/t_0)$ with the first pulse having five times the amplitude of the second. The baseline shift at the beginning of the second pulse is measured as a function of the separation between the pulses for all settings of the peaking time control. Figure 8 shows the results as a function of the ratio of separation to peaking time. For separations greater than about 10-15 times t_p, pileup effects fall below the level of 1%. This agrees with analytical and simulated results. (The scatter in the data is caused by small variations in the shape of the waveform for different gain and peaking time settings). Assuming a sustained average rate R, we set $1/R$ to $100 \bullet t_p$ to make pileup negligible. This translates to rates from 20-60 kHz per strip, which is adequate for the muon spectrometers in large collider detectors where these chambers have been proposed.

The equivalent input noise charge (ENC) is found by measuring the r.m.s. voltage noise at the output of the shaper and dividing by the gain. We measure the ENC at several input capacitances and compute the intercept ENC_0 and the noise

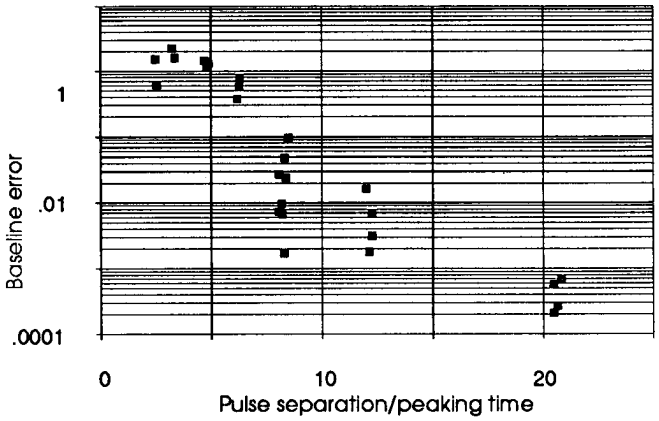

Figure 8: Pileup effect. 5X pulse is followed by 1X pulse; baseline error at start of second pulse is shown. Both pulses have $I_0/(1+t/t_0)$ "tail". Horizontal axis is ratio of separation between pulses to peaking time. Several values of peaking time control are plotted.

slope *NS*. Figure 9 shows the ENC_0 and *NS* as a function of gain and peaking time. The noise slope depends on $t_p^{-1/2}$, as expected when series noise dominates. The ENC_0 has dependence on both t_p and gain. Peaking time dependence is the same as the *NS*. The ENC_0 is greatest at low gains, indicating that there is a second-stage noise contribution from sources after the preamp. For a detector with 150pF capacitance, the total ENC would be from 1900 e^- to 3700 e^-, depending on peaking time. This is low enough so that the electronic noise will not degrade the position resolution for reasonable chamber gains. The chip's series noise resistance is about 75 Ω.

2. *Timing Channel*

The constant-fraction discriminator (CFD) is based on a two-comparator circuit similar to that described in [4]. It has adjustable threshold and pulsewidth. The circuit blocks are from a standard cell library having 5V logic swings. The CFD output waveform is shown in Figure 10.

CFD delay has been measured as a function of input charge from 10 to 500 fC. Figure 11 plots the relative delay as a function of input charge. The delay variation (time walk) has a total range of ±2.4 nsec.

To simulate timing results in an actual experiment, we used an input consisting of a sequence of pulses with Poisson-distributed arrival times with a mean rate of 25 kHz and an amplitude distribution as shown in Figure 12a. This amplitude spectrum has a long tail at the high end to crudely simulate the energy loss in a real gas detector. The resulting output timing distribution, shown in Figure 12b, has an r.m.s. width of 1.6 nsec. This is low enough to provide a beam crossing tag for the track in a real chamber.

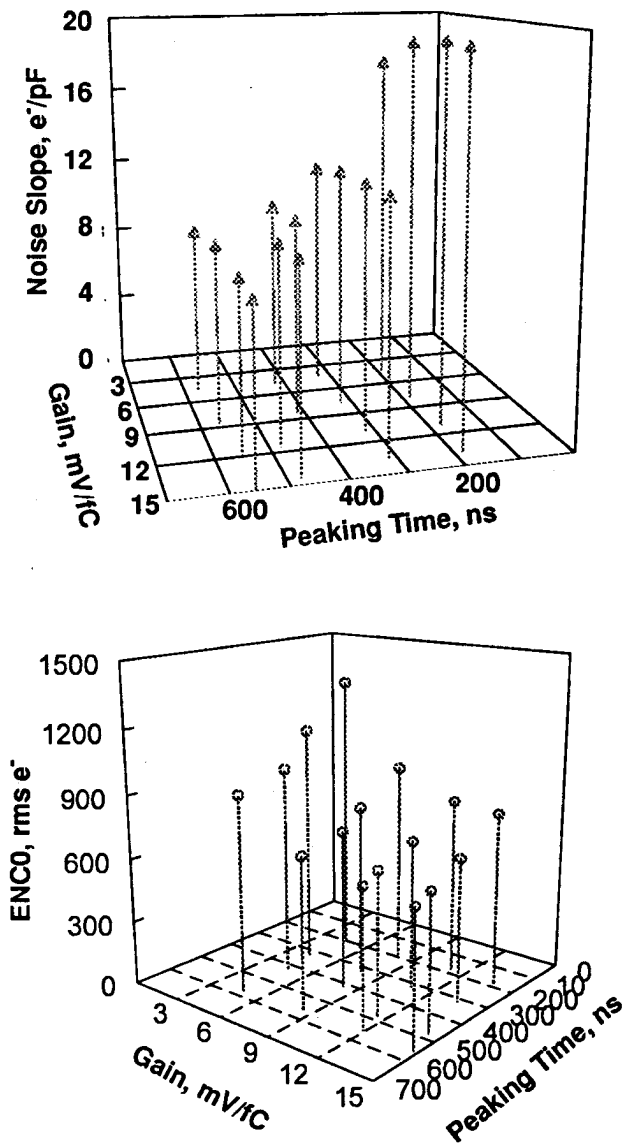

Figure 9: Noise fit parameters vs. gain and peaking time settings. Top: noise slope, *NS*. Bottom: noise intercept, ENC_0.

When the IC is packaged in a conventional 40-pin DIP, the 5V CFD output couples to the preamp input. This coupling generates an error in the peak voltage seen at the analog output of the chip. The amplitude error, expressed as an equivalent input charge, is between 3 and 30 fC depending on peaking time and gain. When the wirebond from the CFD output is removed, the error decreases to 0.02 to 0.36 fC. Hence we attribute the coupling to capacitive coupling between package pins and/or bond wires. In the next iteration of the chip we plan to modify the CFD to have a differential, low voltage swing output buffer and to use better packaging techniques to minimize digital-analog crosstalk.

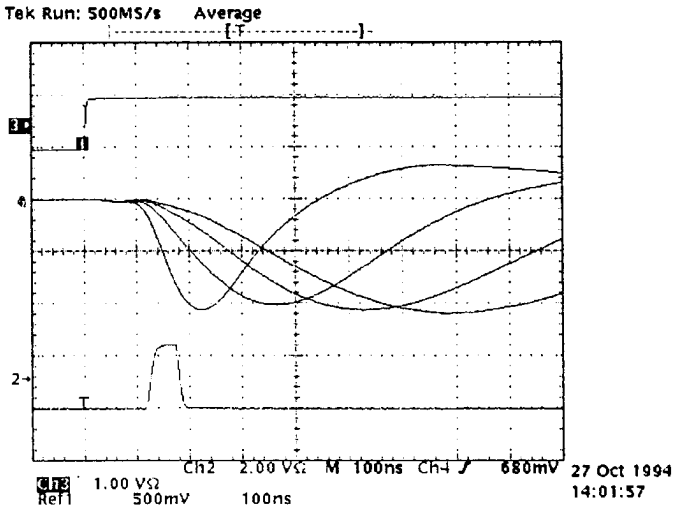

Figure 10: Upper trace: Input. Middle traces: shaper output. Lower trace: CFD output. Time scale: 100nsec/div.

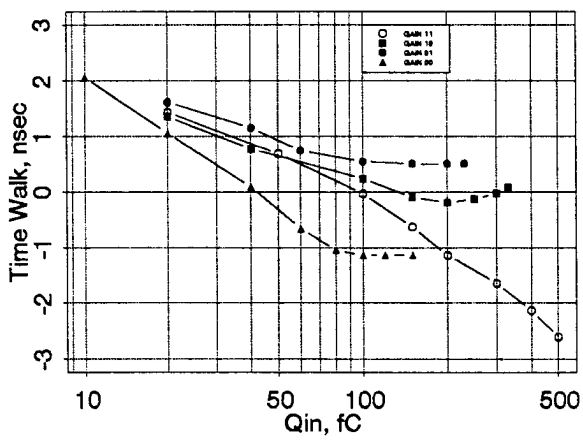

Figure 11: Time walk of the constant fraction discriminator versus input charge for four gain settings.

3. *Other Circuit Blocks*

The on-chip calibration circuit has been measured in a separate prototype chip with 3 channels. Preliminary results indicate that the capacitors match to within 0.5%.

The output track-and-hold, buffer, and multiplexer were prototyped as an 8-channel chip. Figure 13 shows the output waveform of the multiplexer with DC inputs at 200 kHz multiplexing rate. With a load capacitance of 20 pF, the multiplexer can be operated at up to 1 MHz before its accuracy is limited by slew rate effects. The combined nonlinearity of the track-and-hold, buffer, and multiplexer is below 0.7%.

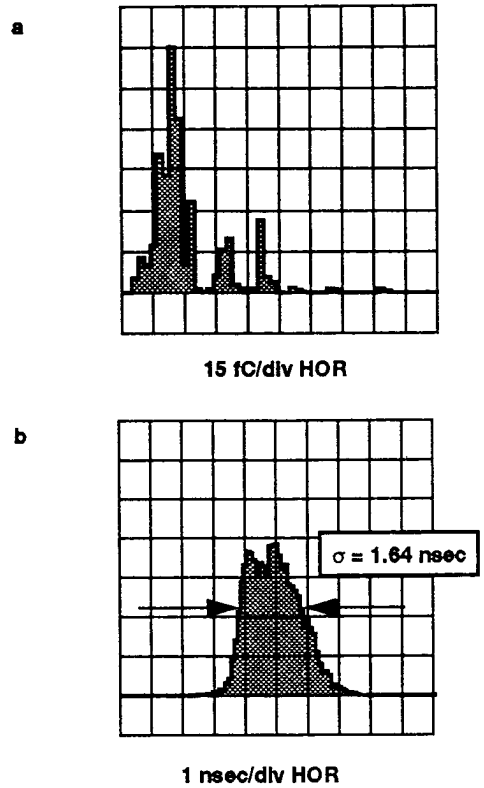

Figure 12: Constant fraction discriminator response to random pulse train. a): Amplitude spectrum at the input. b): resulting timing distribution at the CFD output. Threshold is set at 10 fC.

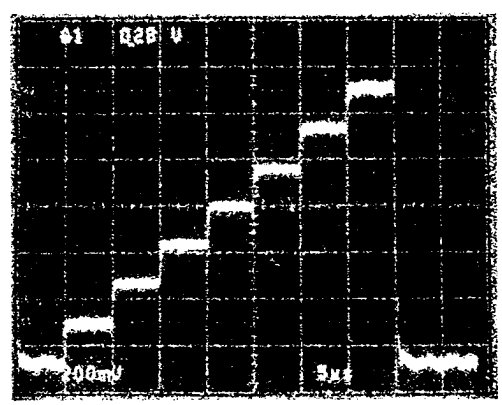

Figure 13: Output of the analog multiplexer. DC inputs, multiplexing rate 200 kHz. Vertical scale: 200mV/div. Horizontal scale: 5μs/div.

IV. CONCLUSION

A CSC readout IC has been implemented in 2μm CMOS technology which extends the capabilities of the present CSC read-

out system while putting all functions on a single chip. The chip can be used at rates up to 50kHz/strip and has noise and distortion low enough to not degrade the position resolution of the detector. An on-chip discriminator gives fast hit information with accurate timing. Properties of the IC are summarized in the table below.

CSC Front End IC	
Technology	2 um CMOS double-poly
Shaping	Bipolar, 180-550 nsec in 4 steps
Gain	4-15 mV/fC in 4 steps
Noise	620 + 8.8 e^-/pF @ 550 nsec 830 + 19 e^-/pF @ 180 nsec
Nonlinearity	0.8% to 1.5V output
Discriminator Output	5V, 50-200 nsec pulse
Discriminator Slewing	2.5 nsec, 10-500 fC
Discriminator Noise	4900 e^- @100pF
Power Consumption	50 mW/ch
Area	2.8 mm^2/chan

V. PLANS FOR FUTURE WORK

In our next iteration of this design we plan to fabricate an eight-channel chip with the blocks discussed in this article. By modifying the CFD output buffer as discussed in section III.2, simultaneous operation of the amplitude and timing channels should be possible with minimal interferance from crosstalk. We will use 1.2 μm technology which will reduce the chip area and power consumption.

VI. ACKNOWLEDGMENTS

The author gratefully acknowledges the help of A. Kandasamy who did the layout and verification of the test chips, and V. Polychronakos, V. Radeka, V. Gratchev, and V. Tcherniatine for helpful discussions and suggestions.

VII. REFERENCES

1. Gratchev, V. *et. al.*, "Position and Timing Resolution of the Interpolating Cathode Strip Chambers in a Test Beam", submitted for publication to *Nuclear Instruments and Methods B*.

2. P. O'Connor, "Monolithic Front-End IC's for Interpolating Cathode Pad and Strip Detectors for GEM", in *Proceedings of the Third International Conference on Electronics for Future Colliders*, LeCroy Corporation, Chestnut Ridge, NY, May 4-5, 1993, p. 167 - 178.

3. V. Radeka, "Low-Noise Techniques in Detectors", *Ann. Rev. Nucl. Part. Sci.* 1988, 38, p. 217-277.

4. B.T. Turko, D.C. Smith, "A Precision Timing Discriminator for High Density Detector Systems", IEEE *Trans. Nucl. Sci.*, NS-39, 1992.