Capacitive matching for MOSFET Charge-Sensitive Preamplifiers with Constant Current

\[ ENC^2 = \frac{1}{2} e_n^2 C_{in}^2 \Im_1 \]  \hspace{1cm} (1)

where

\[ C_{in} = C_{det} + C_{ox} WL \] is the total input capacitance;

\[ e_n^2 = \frac{4kT}{g_m} \] is the input voltage spectral noise density with \( a_n \approx 2/3 \) for FET;

\[ g_m = \sqrt{2\mu C_{ox}(W/L)I_d} \] MOSFET in strong inversion;
\[ = qI_d/nkT \] weak inversion;

\[ \Im_1 = \int_{-\infty}^{\infty} \left[ h'(t) \right]^2 dt \] is the series noise integral; \( h(t) \) is the impulse response.

with the current \( I_d \), length \( L \), and impulse response \( h(t) \) held constant, the optimum size for a device in strong inversion is found from:

\[
\frac{d}{dW}(ENC^2) = \frac{2kT a_n}{\sqrt{2\mu C_{ox} I_d}} \Im_1 \left\{ \frac{1}{2} \left( C_{det} + C_{ox} WL \right)^2 W^{3/2} + \frac{2(C_{det} + C_{ox} WL)C_{ox} L}{W^{1/2}} \right\} \\
= 0
\]

\[ C_{det} + C_{ox} WL = 4C_{ox} WL \]

We find

\[ C_{ox} WL = \frac{1}{3} C_{det} \] \hspace{1cm} (3)

or

\[ W_{opt} = \frac{C_{det}}{3C_{ox} L} \]

Large \( W/I_d \) ratio eventually leads to weak inversion operation. Then \( g_m \) is independent of \( W \) so any increase of \( W \) degrades the ENC. Taking this into account:

\[ W_{opt} = \min\left( \frac{C_{det}}{3C_{ox} L}, W_{wi} \right) \] where

\[ W_{wi} = \frac{2L I_d}{(3kT/q)^2 \mu C_{ox}} \] defines the boundary of weak inversion.
MOS I-V Characteristics

**Linear region** \( V_{DS} < V_{GS} - V_T \):

\[
I_D = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

(1)

**Saturation region** \( V_{DS} > V_{GS} - V_T \):

1. **Strong inversion** \( V_{GS} - V_T > \frac{3kT}{q} \):

\[
I_D = \frac{\mu C_{ox}(W/L)}{2n} (V_{GS} - V_T)^2
\]

\[
g_m \frac{I_D}{I_D} = \sqrt{\frac{\mu C_{ox}(W/L)}{2nI_D}}
\]

(2)

2. **Weak inversion** \( V_{GS} - V_T < \frac{3kT}{q} \):

\[
I_D = I_{D0} \frac{W}{L} e^{\left( \frac{qV_{GS}}{nkT} \right)}
\]

\[
g_m \frac{I_D}{I_D} = \frac{q}{nkT}
\]

- best \( g_m/I_D \)
- poor \( f_T \)

(3)

Note: \( n \) is ratio of bottom (JFET)/top (MOS) gate control:

\[
n = 1 + \frac{C_{BC}}{C_{GC}} = 1 + \frac{\sqrt{2\varepsilon qN_{SUB}}}{2C_{ox}/2(\phi_F - V_{BS})}; \text{ typically } n \sim 1.2 - 1.5
\]
Regions of operation

- weak inversion best for gain
- strong inversion best for high frequency operation

Cutoff frequency

Noise

Drain current thermal noise: \( i_n^2 = \frac{8n kT g_m}{3} \)
Flicker noise: \( v_n^2 = 4kT \frac{\rho}{W L f} \)
Input-referred noise voltage: \( 4kTR_n = v_n^2 + \frac{i_n^2}{g_m^2} \)
Equiv. input noise resistance: \( R_n = \frac{\rho}{W L f} + \frac{2}{3g_m} \)
MOS Transistor

NMOS device

Cross-section of n-well CMOS process

Charge in inversion layer controlled by gate-channel voltage
5PF CAPACITOR

5K RESISTOR

100 x 100 µm

2 µm line/space
Resistors and Capacitors in CMOS Technology

N+ DIFFUSION

POLY

WELL

"PINCHED" WELL = JFET

MOS

DOUBLE POLY
### Resistors

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<th>Component</th>
<th>Range of Values</th>
<th>Absolute Accuracy</th>
<th>Matching Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
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<tbody>
<tr>
<td>Carbon Composition</td>
<td>1 - 1G</td>
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<td>5 - 10</td>
<td>1500-5000 ppm/°C</td>
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<td>Metal Film</td>
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<td>0.1 - 1</td>
<td>25 - 100</td>
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<td>5 - 25</td>
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<td>1500</td>
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<td>1</td>
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<td>Well</td>
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<td>10,000</td>
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<td>%</td>
<td>%</td>
<td>ppm/°C</td>
<td>ppm/V</td>
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### Capacitors

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<th>Matching Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
</tr>
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<tbody>
<tr>
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<td>20</td>
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<tr>
<td>Units</td>
<td>pf, fF/μm²</td>
<td>%</td>
<td>%</td>
<td>ppm/°C</td>
<td>ppm/V</td>
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