Performance and Radiation Tolerance of the ATLAS CSC On-Chamber Electronics

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Presented At LEB2000
Krakow Poland
September 13, 2000
Outline

1. System Overview
   - Chamber Configuration
   - Signal Flow
   - Signals and Noise
   - High Rate Performance
   - Pre-Amp/Shaper
   - Sampling

2. ASMII
   - Functionality
   - Optical Links
   - Data Transmission

3. Radiation
   - Requirements
   - Component Testing
   - Test Plans

4. Summary
Signal Processing Chain

CSC Chamber     ASMI     ASMII

20M
5.4 nF
3kV

+HV

P/S

SCA

ADC

MUX

Fiber TX/RX
Signals and Noise

1. Chamber electrode Configuration
   • 4 gas gaps
   • 192 precision strips
     - Readout pitch = 5.547mm
     - Cstrip 20-50pf
   • 48 Transverse strips (no interpolation)

2. Signal Size
   • Muon generates 75 electron-ion pairs (Landau peak)
   • gas gain $\sim 10^5$
   • 12% of charge is collected by the precision cathode in 100ns
   • signal size $\sim 900,000$ e$^-$ (144 fC) $Q_c$
   • central strip of cluster receives $\sim \frac{1}{2}$ of charge $\Rightarrow 72$ fC ($Q_{c\text{,cent}}$)

3. Noise
   • Electronics noise shouldn’t degrade position resolution
   \[ \frac{\sqrt{3} \times ENC}{Q_c} \approx 33 \text{ m} \]\[ ENC \approx 0.5 \text{ fC} \approx 3100e^- \] TOTAL input referred noise
Signals and Noise

4. Signal-to-noise

\[ \text{Signal-to-noise (max. strip)} \approx \frac{Q_{\text{cent}}}{ENC} \approx \frac{72fC}{3100e} \approx 145 \]

5. Dynamic Range and Gain (for 98.5% efficiency)

\[ \frac{Q_{FS}}{Q_{\text{?}}} \approx 5 \]
\[ Q_{FS} \approx 5Q_{?} \approx 725?ENC \approx 360fC \]

6. Quantization

\[ \frac{Q_{FS}}{2^{N\text{bits}}} \approx \frac{\sqrt{12}}{ENC} \]
\[ 2^{N\text{bits}} \approx \frac{Q_{FS}}{\sqrt{12}?ENC} \approx 209 \]

\[ N\text{bits} \approx 7.7 \]
\[ N\text{bits} \approx 10 (\text{?}_{\text{Q,quant}} \approx 20\% \text{ ENC}) \text{ or } 12 (\text{?}_{\text{Q,quant}} \approx 5\% \text{ ENC}) \]

12-bits prefered to accommodate negative lobe, gain and offset variations
High Rate Performance

• Overall background rate $10^7$ Hz per chamber

• 50% charged particles, 50% neutron and ?

• Charged particle background is rejected by
  - timing window around trigger (out of time)
  - or by pattern recognition of non-projective tracks

• Neutrals can deposit high charges:
  - 50% of neutrals above $Q_{FS}$
  - 1% of neutrals above $6Q_{FS}$

• Neutrals produce short-range electrons usually confined to 1-layer

• But a neutral hit anywhere in chamber induces charge on all strips by anode-cathode crosstalk:

$$Q_{cross} \approx \frac{C_{ac}}{C_{filt}} Q_{anode} \approx 10^4 Q_{anode}$$
Pre-Amp Shaper

• Optimal pulse shaping is a compromise between noise, which degrades position resolution, and pileup which contributes to inefficiency.

• Bipolar pulse preferred in high-rate environment.

• From Monte Carlo study, peaking time should be \( \sim 100 \) ns and FW1% M < 430 ns

• Bipolar 7th-order shaper using complex poles gives same return to baseline as 12th-order CR²-RCⁿ configuration

• Pulse Waveform
Sampling Rate

- With 40 MHz sampling and only 4 samples, we can't always get the peak and both neighbors.

![40 MHz sampling graph](image)

- 20 MHz sampling/4 samples gives a wider window and doesn't degrade the resolution or efficiency.

![20 MHz sampling graph](image)
Readout Implementation

2-Bits per ADC, Single Frame Mode
(1 of 2 transmitter links shown)

Monitoring Data
From ADC [k]

DATA
From ADC [n]

Shift register

Shift register

40MHz

40MHz

RDclk = Wclk/6 = 6.67MHz
40MHz derived from G-Link Rx “strbout” signal.
Pipeline cannot accommodate higher readout rates.

6 cycles to shift out data

4x per IC,
4-IC’s service 16 ADC’s
ASMIIa Prototype
SCA Muon Mode Response

Tek Run: 5.00MS/s

Top Trace - FIFO Readout Trigger
Red - Input sin wave, 1.8MHz
Green - SCA Out+
Black - DAC response of FIFO read

Ch1
Ch2
Ch3
Ch4

1.00 V
1.00 V
1.00 V
5.00 V
1.4 V

Mode & Holdoff
Optical Data and Control Links

• Two G-Link Transmitters
  - Transmit raw data quantized to 12-bits from SCA
  - 16 bit data field
  - 40MHz frame rate

• One G-Link Receiver
  - Provides SCA control
  - Provides Calibration data and control
  - 20 bit data field
  - 40MHz frame rate
  - 14 SCA control bits
  - Provides Frame Clock for G-Link Transmitters

• ADC Outputs Serialized into G-Link data field
  - Two serial lines per ADC, 6-bits deep
  - 40MHz serial data rate
  - 8 ADC’s serialized into one G-Link Tx
Data Transmission

• Buffer data for L1 latency in SCA (~2.5us, 50-cells at 20MHz)

• Transmit 4-time samples within L1 trigger rate of 100KHz
  - Must transmit 4-samples in less than 10us
  - One time sample corresponds to reading 12 SCA channels
  - 15 SCA READ CLK cycles required for one time sample
  - 4 time samples corresponds to 60 SCA READ CLK cycles
  - SCA READ CLK >= 6.67MHz (4-samples = 9us)

• Transmit On-Chamber current and temperature
  - Digitize current sense and temperature
  - Data fused into main data stream as serial bit stream
  - Readout controlled by sparsifier

• Transmit board identification (board ID).
  - Data fused into main data stream as serial bit stream.
  - ID set by on-board switches or links.
CSC Radiation Requirements and Tolerance

• REQUIREMENTS
  - Ionizing dose of 4.4krad/yr
  - Neutron flux of $7 \times 10^{12}$ n/cm$^2$/yr
  - Converts to $1.8 \times 10^{12}$ 1-MeV equivalent n/cm$^2$/yr

• Radiation Tolerance Criteria for SEU
  - In-efficiency = 0.1%
  - In-efficiency per G-Link = $0.78 \times 10^{-6}$
  - Link down time = 1ms
  - # of chips per link = 2
  - Data dropped after recovery = 8-triggers
  - Link down probability per SEU = 100%
  - Acceptable SEU rate = 1 SEU per 43 minutes per chip
## On-Chamber Components

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDMP 1022</td>
<td>Extensive testing has been performed. Plan to conduct our own test.</td>
</tr>
<tr>
<td>HDMP 1024</td>
<td>Developing test hardware at UCI</td>
</tr>
<tr>
<td>SCA</td>
<td>Testing to be completed by LAr.</td>
</tr>
<tr>
<td>AD9042 (ADC)</td>
<td>Used on LAr FEB. Extensive testing performed by Denes at Princeton.</td>
</tr>
<tr>
<td>AD8042 (op-amp)</td>
<td>Used on LAr FEB. Ionizing survival test done by Lar.</td>
</tr>
<tr>
<td>Level Translators</td>
<td>No testing done to date.</td>
</tr>
<tr>
<td>MC10H116</td>
<td></td>
</tr>
<tr>
<td>DAC?</td>
<td>Trying to develop alternate solution for 0.5% required calibration pulse accuracy.</td>
</tr>
<tr>
<td>74ALS166</td>
<td>COTS Qualification</td>
</tr>
<tr>
<td>Pre-Amp/Shaper</td>
<td>Passed ionizing test.</td>
</tr>
<tr>
<td>ASMI/ASMII</td>
<td>Test final ASMII under Sparsifier control. Does anything unexpected happen?</td>
</tr>
</tbody>
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## COMMENTS

- Extensive testing has been performed.
- Developing test hardware at UCI.
- Testing to be completed by LAr.
- trying to develop alternate solution for 0.5% required calibration pulse accuracy.
- COTS Qualification.
Preamp Shaper Irradiation Results
0.5um CMOS HP
Preamp/Shaper Irradiation Results
0.5um CMOS HP

Gain

DC Shift

$y = -0.0654x - 4.6343$

ENC

Peaking Time
G-Link Receiver Test
Summary and the Road Ahead

1. Minimize SEU problem by moving SCA control logic off-chamber
2. Developed 24-channel prototype ASMII to verify SCA Muon Mode
3. Beam test data verified performance of Preamp/Shaper and 20MHz sampling
4. Developed VME DAQ board to support beam test of front end electronics
5. Preamp/Shaper passed Ionizing radiation test to 1Mrad
6. G-Link Receiver and Transmitter boards have been built
8. More detailed testing of SCA Muon mode required
9. Plan to develop full 192-channel ASMII within next few months
10. Beam test complete on-chamber electronics prototypes in spring of 2001
11. Evaluate cooling approach
12. Coordinate radiation test and qualification efforts with LAr and UCI