

## LOW NOISE CMOS PREAMPLIFIER-SHAPER FOR SILICON DRIFT DETECTORS\*

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### Abstract

We present a new CMOS charge sensitive amplifier (CSA) with integrated Shaper, optimized for position measurements on low capacitance Silicon Drift Detector (0.2-0.8 pF) and designed in the CMOS 1.2 $\mu$ m HP process using novel circuit techniques.

The noise sources have been minimized on a fixed power constraint, and the CSA achieves an equivalent noise charge (ENC) of 35e-rms + 58e-rms/pF at 23 $\mu$ s shaping time with a power consumption of about 3.1mW.

The circuit is continuously sensitive and requires no external adjustment. A compact MOSFET transistor with minimum added parasitic capacitances is used in the feedback network, and a novel self-adaptive bias circuit ensures stability of the value of the associated resistance (6.2M $\Omega$ ) against parametric and temperature variations.

The integrated CSA-Shaper features an accurate pole-zero cancellation scheme which cancels the non-linearity introduced by the non-linear feedback resistance.

The gain of the CSA-Shaper is 16.5mV/fC and its non-linearity is within 0.5% over 0-50fC dynamic range. The shaping time is 50ns, with an ENC of 120 e-rms.

### 1. Introduction

The Silicon Drift Detector (SDD), proposed by E. Gatti and P. Rehak in 1985 [1], couples large sensitive area with low number of read-out channels and small anode capacitance. Its features make the SDD attractive in an ever growing number of applications, like in the inner tracking system of the ALICE experiment [2].

Lot of efforts have been put so far in the development of SDDs and their front-end electronics, which has to meet several design criteria to fully exploit the potential low noise performance of the detector.

The CSA scheme is widely used at the front-end, for its conversion gain is independent on anode capacitance variations: the input charge pulse is integrated on a feedback capacitance CF, which is continuously discharged by a resistance. This can be placed in parallel to CF, and establishes a DC path which biases the anodes and sinks the detector leakage

current. Among the different technologies used for front-end circuits, the CMOS one offers the advantage of being inexpensive and readily available for full custom design [3,4]. However, several disadvantages, i.e. low transconductances of the MOSFET transistors, high flicker noise, difficulties in integrating high value resistances, call for ad-hoc design techniques [5]. In particular, noise constraints call for feedback resistances in the M $\Omega$  range, and the only practical way to cope with this requirement is by using a MOSFET transistor biased in the weak inversion region. The consequent unavoidable drawback is the strong dependence of the value of the associated drain-source resistance upon parametric process variations. Moreover, the non-linear feedback resistance worsens the linearity of the CSA conversion gain.

With the present work we propose a novel low noise CMOS CSA-Shaper circuit which addresses these issues by means of novel circuit techniques.

### 2. Core voltage amplifier

The core voltage amplifier has been implemented using a folded cascode Operational Transconductance Amplifier followed by a voltage buffer (Fig. 1).

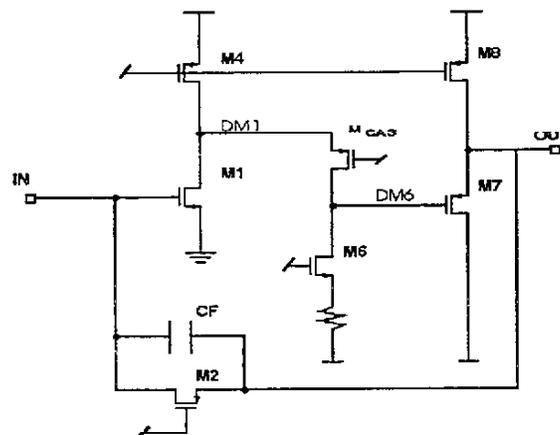


Fig.1: Charge sensitive amplifier realized as a voltage amplifier with voltage-shunt feedback.

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At the required shaping time (50ns) the series noise contributes more than the flicker one to the total ENC, thus an N-MOS transistor (M1) has been preferred at the input due to its higher transconductance [6,7]

The transconductance of M1 is equal to 3.5mS and the other secondary noise sources have been minimized.

This stage has a gain-bandwidth product of 275 MHz, and dissipates about 3.1mW. The feedback capacitor  $C_F$  is 0.1pF. With an input capacitance of 0.8pF representing the detector plus parasitic capacitances, the rise time of the CSA is 12ns.

### 3. Self-Adaptive bias circuit for the feedback transistor

The feedback transistor establishes a DC path to bias the SDD anodes and continuously discharges the feedback capacitor, thus preventing the CSA from being saturated by subsequent integration events. Noise requirements call for high feedback resistances. However, the CSA should be able to sink all the anode leakage current while keeping the electrostatic potential at the anode constant. This last requirement, important to ensure the proper collection of signal electrons on the anode array, is fulfilled if the core voltage amplifier is not saturated by leakage current, i.e. M1 (Fig.1) is biased properly. This calls for a small voltage drop along the feedback transistor, and sets an upper limit for its associated drain-source resistance. We decided to target a  $5M\Omega$  feedback resistance. High value resistances are difficult to integrate in the CMOS technology, thus we introduced the feedback MOS transistor M2 biased in the triode region. This also allows us to target a higher target resistance, as the drain-source resistance of a MOS transistor decreases as leakage current increases. In the absence of leakage current the resistance is given by:

$$R = \frac{1}{\mu C_{ox} (W/L)_2 (V_g - V_{th})_2} \quad (1)$$

where  $\mu$  is the inversion layer mobility,  $C_{ox}$  is the gate capacitance per unit area,  $W/L$  is the aspect ratio of the MOS transistor,  $V_g - V_{th}$  is the gate bias voltage at equilibrium. The relative variation of the feedback resistance is

$$\left| \frac{dR}{R} \right| = \mu C_{ox} (W/L) \cdot R \cdot |dV_{TOT}| \quad (2)$$

where  $dV_{TOT}$  represents the total variation in the control voltage of the MOSFET transistor.  $V_g$  is derived from a supply voltage, which in a well-regulated system exhibits variations of 2%. The other contributions are due to the threshold variations which can vary about

150mV from run to run. Using  $\mu=200 \text{ cm}^2/\text{Vsec}$  and  $C_{ox} = 1.7\text{fF}/\mu\text{m}^2$  and assuming the total  $dV_{TOT}$  equal to 250mV, we find  $\left| \frac{dR}{R} \right| = 43 \cdot (W/L)$  for a target value of  $R=5M\Omega$ . To keep  $R$  within 20%, we must make the aspect ratio  $W/L < 0.005$ , thus the active area would be  $200 \cdot W_{min}^2$ , and the parasitic capacitance of the device  $200 \cdot W_{min}^2 \cdot C_{ox} = 11\text{pF}$ .

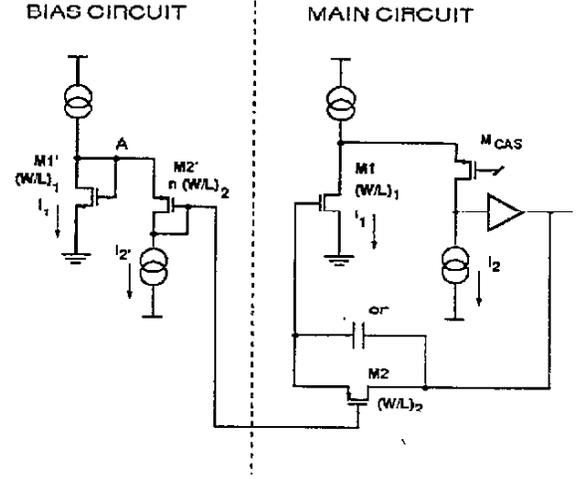


Fig.1: Self-Adaptive Bias Circuit for the Feedback MOSFET M2

Such a high capacitance would severely degrade the CSA performance, and the problem has been addressed by a self-adaptive bias circuit which allows us to use a compact device while tracking the parametric process variation and ensuring a stable value for the associated feedback resistance.

The diode connected replica M1' of M1 is biased in the same way as M1, thus the potential at node A is the same of that at the input node. In this way every threshold variation on the N-MOS devices is reproduced on the source of M2 and M2'.

Besides, M2' is created laying-out n parallel copies of M2, thus it experiences the same narrow-channel, short-channel and body effect which affects the threshold voltage of M2. By imposing the number of copies n and the current  $I_2'$  flowing into M2', the source-drain resistance of M2 is defined, which is insensitive to variations in the supply bias and threshold voltages of both N-MOS and P-MOS transistors. In other words:

$$V_{GS2} - V_{TH2} = V_{GS2'} - V_{TH2'} = \sqrt{\frac{2I_2'}{\mu \cdot C_{ox} \cdot n \cdot (W/L)_2}} \quad (3)$$

and substituting (3) in (2), the resistance is equal to:

$$R = \sqrt{\frac{n}{2I_2' \cdot \mu C_{ox} (W/L)_2}} \quad (4)$$

and the relative feedback resistance variation is equal to:

$$\left| \frac{dR}{R} \right| = \frac{1}{2} \left\{ \frac{dI_2}{I_2} + \frac{d(\mu C_{ox})}{\mu C_{ox}} \right\} \quad (5)$$

To first order, the achieved resistance is independent on threshold and power supply variations. The bias circuit controls  $I_2$  within 10%, and  $\mu C_{ox}$  is controlled to 2%. What is more important, the relative variation is now independent of the absolute value of the resistance, thus a compact, stable and high value resistance with negligible added parasitics can be introduced. In our circuit  $n=500$ ,  $I_2 = 30\mu A$ ,  $(W/L)_2 = 3/20$ , which gives a resistance of about  $1.5M\Omega$ . Due to space constraints we implemented M2' as 50 copies of a  $(W/L)_2 = 3/2$ . This produces a narrow-channel effect which increases the resistance of M2 to  $5M\Omega$ .

#### 4. Accurate Pole-Zero cancellation in the Shaper

The resistance associated with the feedback transistor M2, i.e. the pole associated with the feedback network M2-CF, changes during the discharge of Cf. Besides, the position of this pole depends also upon the value of the leakage current. Those unavoidable drawbacks worsen the CSA linearity, and we developed a variation of the classical pole-zero cancellation technique [8] to address this issue (Fig.3).

When connected to a SDD anode, the leakage current makes the CSA output positive (M2 and M3 effective source). The core voltage amplifier used in the Shaper is the same of the one used in the CSA, thus M2 and M3 are biased in the same way and exhibit the same drain source resistance variations with the leakage current and the dynamic swing of the CSA's output. In this way, the time constant associated with the parallel M3-C1 is in every moment equal to the one associated with the feedback network of the CSA, and the accurate pole-zero cancellation is carried out.

This greatly improves the linearity of the gain of the system CSA-Shaper, and allows us to build a shaper insensitive to leakage current and with high linearity over a wide dynamic range.

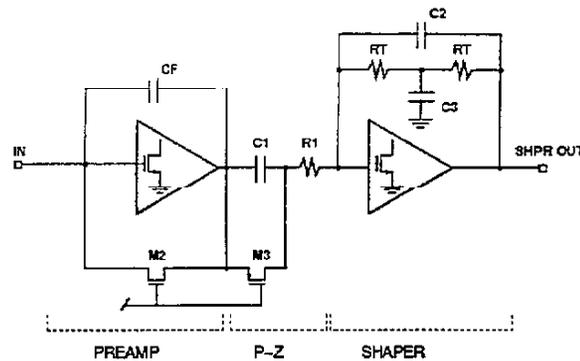


Fig.3: CSA-Shaper with pole-zero cancellation

#### 5. Shaper

The bridged T-feedback network in the second stage of Fig.3 generates two poles and one zero:

$$A_v(s) = A_0 \cdot \frac{1 - s/\omega_z}{1 + s/Q\omega_0 + s^2/\omega_0^2}$$

where  $\tau_z = -1/\omega_z = R_T C_3 / 2$ ,  $\tau_0 = -1/\omega_0 = R_T \sqrt{C_2 C_3}$  and  $Q = \sqrt{C_3 / C_2} / 2$ .

The complex poles have  $\tau_0 = 34 \text{ nsec}$  and  $Q=0.707$ , giving a good semiGaussian shape at 50ns. The Shaper dissipates 2.9mW of power.

#### 6. Experimental results

The circuit has been fabricated with double-metal, double-poly CMOS HP 1.2um process, and with minor modifications, in the Orbit 2.0um one.

The test chips include six variations for each type of circuit: in particular we included the CSA alone and the CSA-Shaper. We introduced versions with and without ESD protection structures, which are estimated to add 0.2-0.4 pF to the input capacitance. A 50fF capacitance has been introduced to test the circuit injecting charge at the input. The node Dm1 (Fig.1) has been brought to an external pad, thus it's possible to impose bias conditions on the feedback transistor M2 different than the natural one. Fig.4 shows the CSA's response to a charge pulse at various temperatures, i.e. various threshold voltages for the PMOS and NMOS transistors. By measuring the decay time of the CSA, we get an estimate of the value of the feedback resistance, which is about  $6.2M\Omega$ . The CSA's decay time, i.e. the feedback resistance, stays constant within 10% over 200mV threshold variations, thus proving the effectiveness of the self-adaptive scheme.

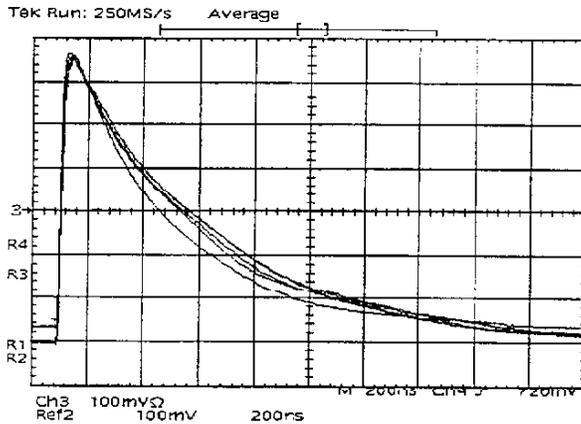


Fig.4: CSA waveform at -75, -50, -25, +25 °C.

Fig. 5 shows the CSA's output for leakage current from 0 to 200nA. The output DC level increases at leakage current increasing. Consequently, the drain-source resistance of M2 decreases.

As already pointed out, the change of the CSA's decay pole position worsens the linearity of the CSA and calls for the accurate pole-zero cancellation in the Shaper.

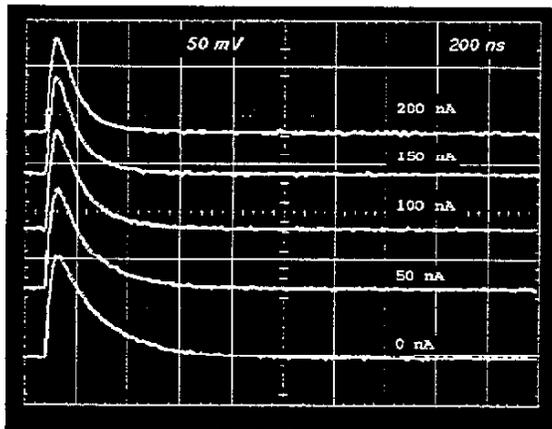


Fig. 5: CSA output for 0, 50, 100, 150, 200nA leakage current. (2.0  $\mu$ m fabrication)

The response to a charge pulse of the CSA and CSA-Shaper are respectively shown in Fig.6 at various gate voltages forced on M2 and M3 i.e., various feedback resistances. The CSA-Shaper waveform exhibits a small overshoot. Its shape keeps unchanged regardless of the position of the pole associated to the feedback network CF-M2, which is accurately cancelled by the M3-C1 network. Besides, the linearity of the CSA-Shaper has been found 0.5% over 0-50fC input charge, proving again the effectiveness of the adopted scheme.

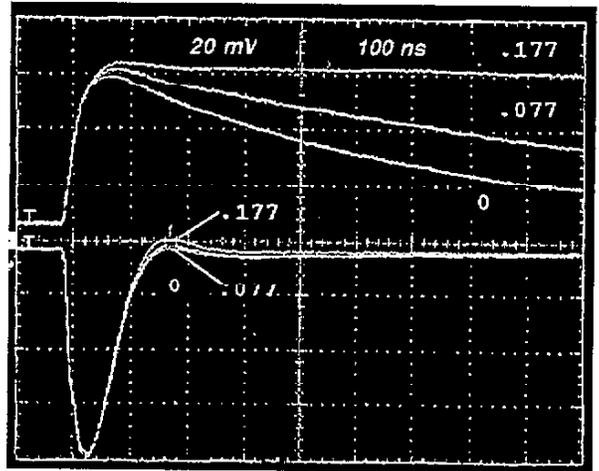


Fig.6: CSA and CSA-Shaper output waveforms at self-bias and several forced gate voltages on the feedback and pole-zero devices.

Two versions of the CSA, with and without ESD network, have been connected to an external shaper with selectable shaping time, and the measured ENC is shown in Fig.7 for two bias conditions, the self-biased condition and a higher-resistance one.

The flicker noise background is clearly visible in this last case [9], as we get rid of the parallel noise pushing the feedback resistance in the G $\Omega$  region.

Obviously, the CSA without ESD network features better noise performances than the protected one.

In the self-bias condition, the 6.3M $\Omega$  parallel noise contribution dominates the ENC at long shaping times.

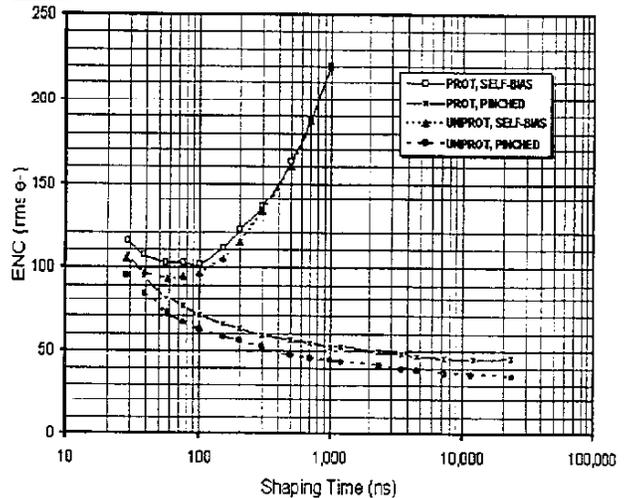


Fig.7: ENC of the CSA as a function of shaping time for two bias conditions (with and without ESD protection structures)

The circuit has been coupled to a Si detector with Cd=1.37pF and the spectrum of a AM241 source has

been taken with the CSA coupled to an external 1 $\mu$ s shaper (Fig.8) with the feedback device pinched off. The ENC is 148 e-rms, and the estimated 0.3pF capacitance due to 2 bond wires and 1cm PC board traces, gives a noise slope of 58e/pF.

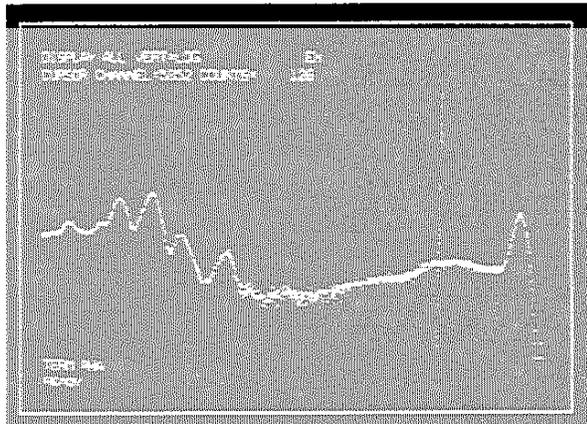


Fig. 8: Spectrum of AM241 with CSA connected to an external Shaper and the feedback device pinched off. ENC=180 e rms at  $t_s=2\mu$ s.

The integrated CSA-Shaper has been coupled to the Si photodiode: Fig.9 shows an ionizing event from AM241 in self-biased condition at +15 °C. The AM241 spectrum has been taken (Fig.9). At room temperature,  $t_s=50$ ns,  $C_d=1.37$ pF, ENC=255 e-rms, with a noise slope of 120 e rms + 107 e rms/pF. The higher ENC is due to the increased series noise contribution at the shorter shaping time (50ns). At  $T=-75^\circ\text{C}$  with the feedback device pinched off, the reduced series noise makes the ENC equal to 180 e-rms.

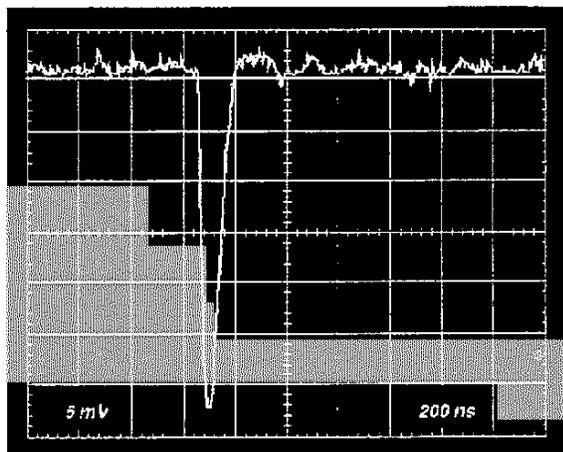


Fig.9: Ionizing event from AM241 with integrated CSA-Shaper in self-biased condition at +15 °C.

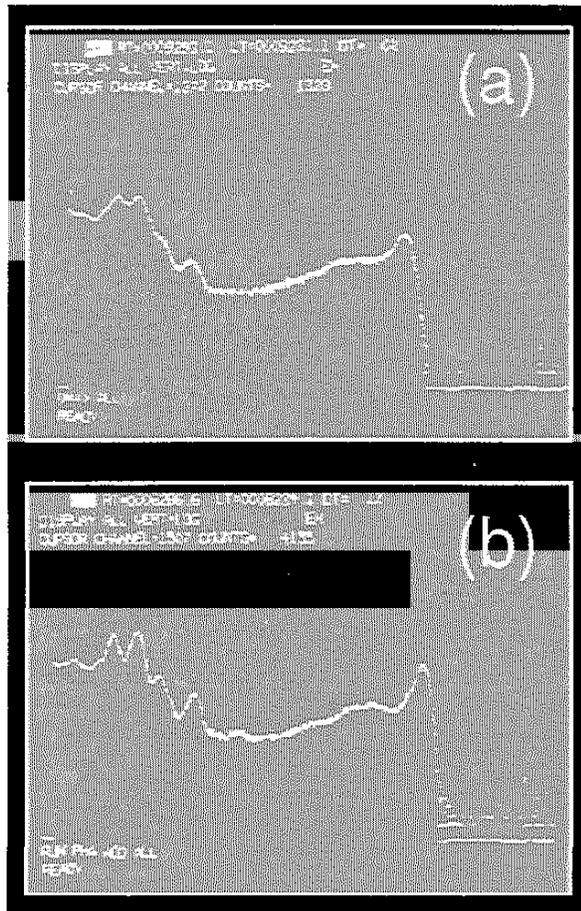


Fig. 10: Spectrum of AM241 with integrated CSA-Shaper. (a) Self-biased condition, room temperature. (b) Feedback device pinched off,  $T=-75^\circ\text{C}$ .

## 7. Conclusion

A novel low noise CMOS CSA-Shaper, optimized for position measurements on SDD has been proposed and fabricated with double-metal, double-poly IIP 1.2 $\mu$ m process. Its key features include: low noise, high linearity, continuously sensitive, no external components or critical adjustment required. The performance of the CSA-Shaper is summarised in Tab.I.

Technology	1.2 $\mu$ m nwell CMOS
Gain	16.5 mV/fC
Shaping	50 ns unipolar
Noise	120 + 107 e/pF
Effective feedback R	6.3 M $\Omega$
Maximum detector leakage	1.5 $\mu$ A
Linearity	< 0.5% to 50 fC Qin
Power Dissipation	6.1 mW/channel

Table I - Performance Summary of CMOS CSA-Shaper

## 8. Acknowledgments

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