Low-Noise CMOS Preamplifier-Shaper for Silicon Drift Detectors

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Abstract

We have designed a 16-channel preamplifier-shaper for particle tracking using silicon drift detectors (SDD). The preamplifier, which is optimized for a detector capacitance of 0.2 - 0.8 pF, uses two new circuit techniques to achieve a low noise (ENC 120 e^- + 62 e^-/pF), high linearity (< 0.5% to 50 fC), and good tolerance to process variations and temperature and power supply fluctuations. The circuit is continuously sensitive, has no digital signals on chip, and requires no external components or critical adjustments. The peaking time of the shaper is 50 nsec and the power dissipation, including an off-chip driver, is 6.5 mW/channel. The circuit is fabricated in 1.2μm CMOS and can accomodate detector leakage currents of up to 1.5 uA.

Although the circuit was developed for use with particle tracking detectors, these techniques are also well-suited for the design of lower-noise preamplifiers for high-resolution X-ray spectroscopy systems.

I. Introduction

Silicon drift detectors [1] are well-suited for 2-D tracking in a high multiplicity environment because of their large sensitive area for charge collection combined with low anode capacitance. To fully exploit the features of the SDD, the front-end electronics has to meet several design criteria. Lots of efforts have been put so far in the development of various circuits implemented in different technologies [2-4].

The CSA scheme is widely used at the front-end, for its the conversion gain is independent of anode capacitance variations: the input charge pulse is integrated on a feedback capacitance which is continuously discharged by a resistance Rf. This DC path biases the anodes and sinks the leakage current Ileak.

Among the different technologies used for front-end circuits, CMOS offers the advantage of being inexpensive and readily available for full custom design. However, several disadvantages, i.e. low transconductances of the MOSFET transistors, higher flicker noise, difficulties in integrating high value resistances, call for ad-hoc design techniques [5]. In particular, noise constraints call for a feedback resistance in the Megaohm range. This requirement can be satisfied in CMOS technology by using a MOSFET resistor biased in the triode region. The consequent unavoidable drawbacks are the strong dependence of the associated non-linear drain-source resistance on parametric process variations and the worsening of the CSA linearity.

With the present work we describe a novel low noise CMOS CSA-Shaper-Driver circuit [6] which addresses these issues by means of novel circuit techniques, and its integration into a 16-channel monolithic circuit.

II. Circuit Design

A. Core voltage amplifier:

The core voltage amplifier has been implemented using a folded cascode Operational Transconductance Amplifier (OTA) followed by a voltage buffer (Fig. 1).

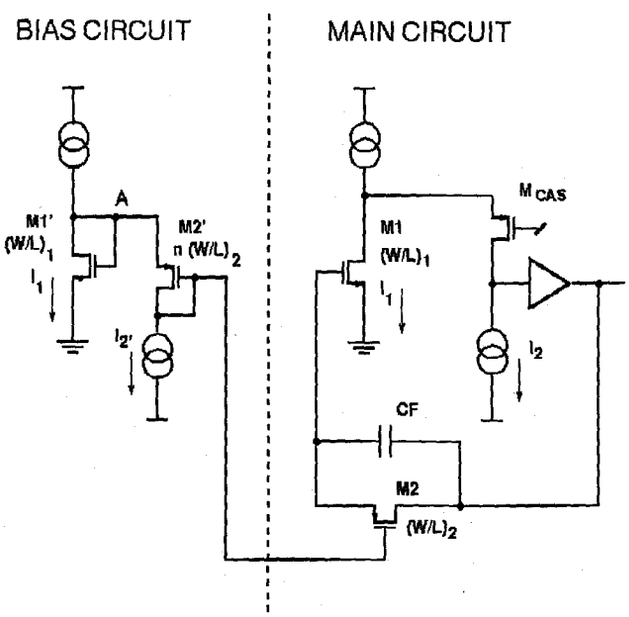

Fig.1: Folded cascode (main circuit) and self-adaptive bias circuit

At the required shaping time (50ns) the series noise contribution to the ENC is higher than the flicker one, thus an N-MOS transistor (M1) is preferred at the input due to its higher transconductance.

The transconductance of M1 is equal to 3.5 mS and the other secondary noise sources have been minimized.

This stage has a gain-bandwidth product of 275 MHz and the feedback capacitor CF is 0.1pF. With an input capacitance of 0.8pF representing the detector plus parasitic capacitances, the rise time of the CSA is 12 nsec.

B. Self-Adaptive bias circuit for the feedback transistor

The trade-off between low noise requirements (high resistance) and the capability of the CSA to sink all the anode leakage current (low resistance), place the feedback resistance in the Megaohm range. The unavoidable use of a MOS transistor (M2) biased in the triode region, allows us to target a higher resistance (5MΩ) for M2, as its drain-source resistance decreas-

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es as leakage current increases.

In the absence of leakage current the resistance is given by:

$$R = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{gs} - V_T)} \quad (1)$$

where μ is the inversion layer mobility, C_{ox} is the gate capacitance per unit area, W/L is the aspect ratio of the MOS transistor, V_{gs} is the gate-source bias voltage at equilibrium. The relative variation of the feedback resistance is:

$$\left|\frac{dR}{R}\right| = \mu C_{ox}\frac{W}{L} \cdot R \cdot |dV_{TOT}| \quad (2)$$

where dV_{TOT} represents the total variation in the control voltage of the MOSFET transistor, mainly due to the spread of the PMOS and NMOS threshold voltages from run to run (200mV). To keep R reasonably stable we must make the aspect ratio W/L very small, introducing a high parasitic capacitance which would severely degrade the CSA performances. The problem has been addressed biasing the feedback MOSFET with an adaptive self-bias circuit (Fig.1) which tracks the parametric process variation ensuring a stable value for the feedback resistance.

The diode connected replica M1' of M1 is biased in the same way as M1, thus the potential at node A is the same of that at the input node. In this way every threshold variation on the N-MOS devices is reproduced identically on the source of M2 and M2'.

M2' is created by laying-out n parallel copies of M2, thus it experiences the same narrow-channel, short-channel and body effect on the threshold voltage as M2. By imposing the number of copies n and the current I2' flowing into M2', the source-drain resistance of M2 is defined, which is insensitive to variation in the supply bias and threshold voltages of both N-MOS and P-MOS transistors. In other words:

$$V_{GS2} - V_{TH2} = V_{GS2'} - V_{TH2'} = \sqrt{\frac{2I_{2'}}{\mu C_{ox} \cdot n \cdot \left(\frac{W}{L}\right)_2}} \quad (3)$$

and substituting (3) in (1), the resistance is equal to:

$$R = \sqrt{\frac{n}{2I_{2'} \cdot \mu C_{ox} \cdot \left(\frac{W}{L}\right)_2}} \quad (4)$$

C. Accurate Pole-Zero cancellation in the Shaper

The resistance associated with the feedback transistor M2, i.e. the pole associated with the feedback network M2-CF, changes during the discharge of CF. Besides, the position of this pole depends also upon the value of the leakage current. Those unavoidable drawbacks worsen the CSA linearity, and we developed a variation of the classical pole-zero cancellation technique to address this issue (Fig.2).

When connected to a SDD anode, the leakage current makes the CSA output positive (M2 and M2' effective source). The core voltage amplifier used in the shaper is the same as the one used in the CSA, thus M2 and M2' are biased in the same way and exhibit the same drain-source resistance variation with leakage current and the dynamic swing of the CSA's output. In this way, the time constant of the parallel combination M3-C1 is at every moment equal to the decay pole of the feedback network of the CSA (M2-CF), and the accurate pole-zero cancellation is obtained.

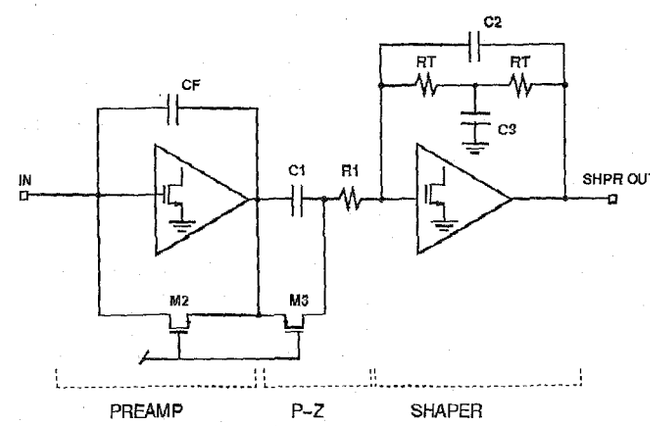

Fig.2: Pole-Zero cancellation scheme

The shaper generates two poles, giving a good semi-Gaussian shape at 50 nsec.

D. Variable-gain Output Stage

To drive off-chip capacitive loads up to 50 pF, an AC-coupled output stage with 4 digitally-selectable gain ranges is incorporated. The driving stage is a complementary Class AB follower to minimize the static power consumption.

To enable sensing of the leakage current of the detector, this stage can be configured as a low-frequency DC gain stage. Another switch re-biases the output follower at higher current, which allows loads up to 250 pF to be driven.

III. Experimental Results

The circuit has been fabricated through MOSIS in a double-metal, nwell CMOS 1.2μm process with linear MOS capacitor.

On a test chip, we fabricated circuits having the preamplifier output available for testing. These chips enabled us to

verify the correct functioning of the self-adaptive bias circuit.

By measuring the decay time of the CSA, we get an estimate of the value of the feedback resistance, which is about 6.2MΩ, 20% higher then the simulated one. Fig.3 shows the CSA's decay at various environment temperature, i.e. various threshold voltages.

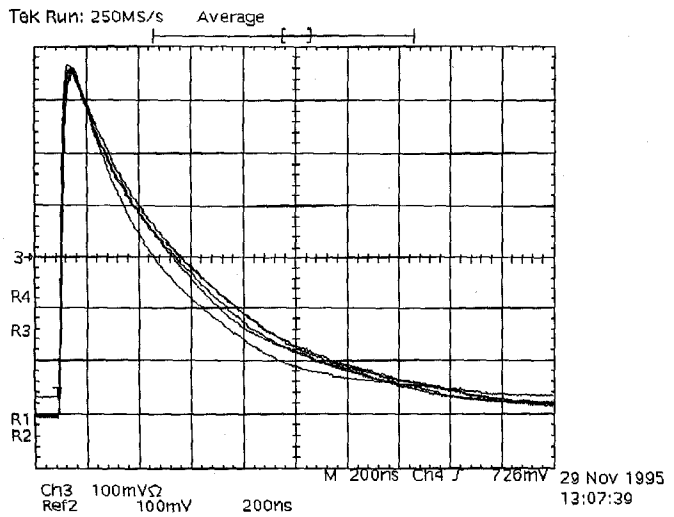

Fig.3: CSA response to a charge pulse at various temperature T= (-75, -50, -25, 25) °C

The CSA's decay time, i.e. the feedback resistance, stays constant within 10% over 200mV threshold variations, thus proving the effectiveness of the self-adaptive scheme. The response to a charge pulse of the CSA and CSA-Shaper are respectively shown in Fig.4 at various bias conditions of M2, i.e., various feedback resistance. The CSA-Shaper response to a charge pulse exhibits a small overshoot, and the output waveform remains unchanged regardless of the position of the pole associated with the feedback network CF-M2. Besides, the linearity of the CSA-Shaper has been found to be 0.3% over 0-50fC input charge, again proving the effectiveness of the adopted scheme.

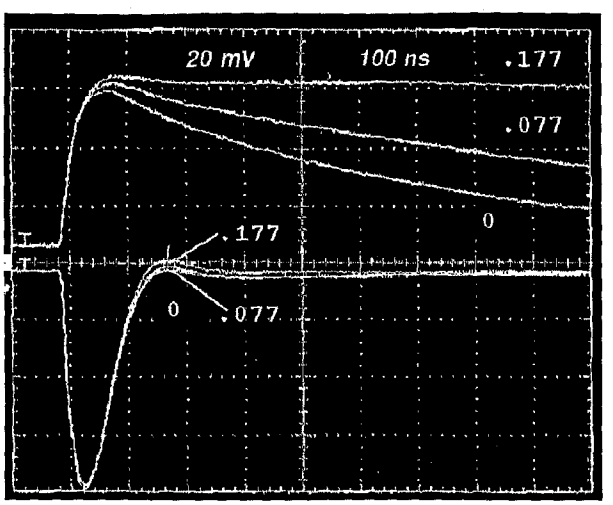

Fig.4: CSA and CSA-Shaper response to a charge pulse at various feedback resistance values

Two versions of the CSA, with and without ESD network, have been connected to an external shaper with selectable shaping time, and the measured ENC is shown in Fig.5 for two bias conditions, the self-biased condition and a higher-resistance one.

The flicker noise background is clearly visible in this last case, as we get rid of the parallel noise by biasing the feedback resistance into the Gigaohm region.

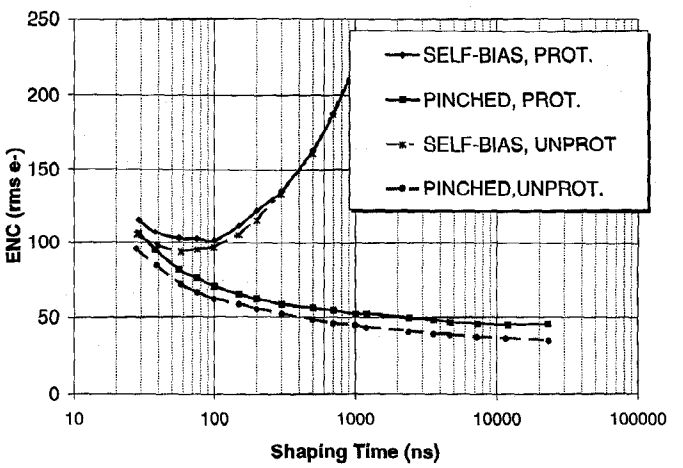

Fig.5: ENC vs. shaping time of CSA

In the self-bias condition, the parallel noise contribution dominates the ENC at long shaping times.

The CSA-Shaper has been coupled to a Si detector with Cd=1.3pF and the spectrum of a ^{241}Am source has been taken. The ENC is equal to 255 rms e^- at room temperature (Fig.6a). When cooled down at -75°C (Fig.6b), the ENC is equal to 180 e^- rms, due to the reduced series noise.

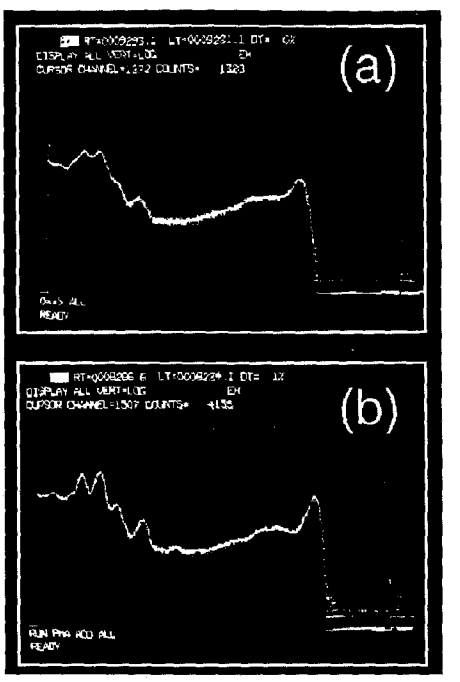

Fig.6: ^{241}Am spectrum taken with CSA-Shaper. (a) room temperature, (b) -75 °C

Fig. 7 shows the CSA-Shaper-Driver's output vs. input charge. The overall gain is selectable as 22, 33, 39, or 91 mV/fC. Nonlinearity is better than 0.5% on the low gain ranges, up to 50 fC Qin.

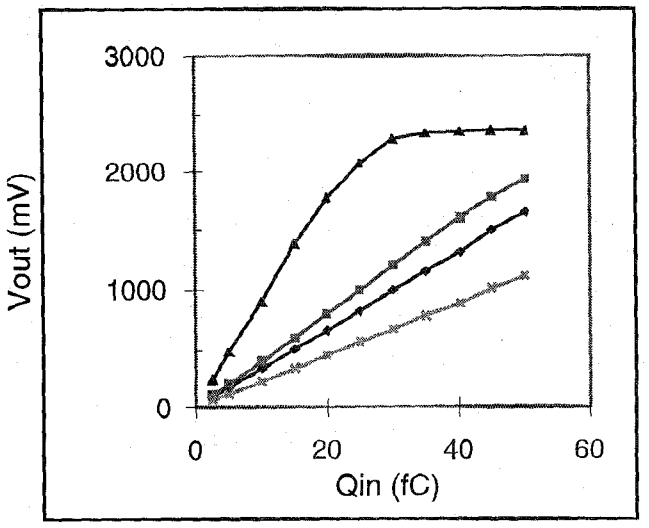

Fig. 7: Output of CSA-shaper-driver vs. input charge for the 4 gain ranges.

In an effort to measure the effect of ESD protection network capacitance on noise, three types of input protection were used. On channels 1-6 and 11-16, an ESD-protection cell from a vendor library was used with the input series resistor removed. Channels 9-10 had the same network with the sizes of the protection devices reduced to 30% of their original values. On channels 7-8, no protection was used.

Fig. 8 shows the resulting noise (average of 5 chips.) The influence of the protection network capacitance can be clearly seen. From the data we can estimate the capacitance of the protection network as roughly 0.25 pF.

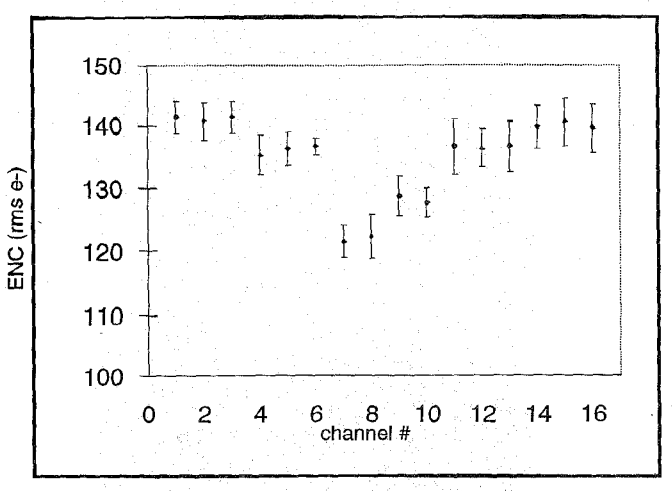

Fig. 8: Noise vs. channel (average of 5 chips.) Chan. 7-8 have no protection. Chan 9-10 have reduced protection.

Over 5 chips from the same run, the gain exhibited a +/- 0.6% variation.

Crosstalk was also studied. For a charge of 20 fC injected into one channel, adjacent channel crosstalk was in the range of 0.7 - 0.9%. Non-neighboring channels had 0.2 - 0.4% crosstalk.

Table 1 summarizes the performance of the circuit.

TABLE 1

Technology	1.2 um CMOS
Shaping	50 nsec unipolar
Gain	Variable (30,30,40, 90 mV/fC)
Noise	120 e^- + 62 e^-/pF
Maximum detector leakage	1.5 uA
Linearity	0.5% to 50 fC
Power dissipation	6.5 mW/channel

IV. Conclusion

A novel low noise CMOS CSA-Shaper, optimized for position measurements on SDD has been proposed and fabricated with double-metal, double-poly HP 1.2μm process. Its key features include, low noise, high linearity, continuously sensitive, no external components or critical adjustment required. Future work will extend these concepts to lower-noise circuits.

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VI. References

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