

CMOS Preamplifier with High Linearity and Ultra Low Noise for X-Ray Spectroscopy

P. O'Connor*, G. Gramegna[†], P. Rehak*, F. Corsi[†], C. Marzocca[†]

* Brookhaven National Laboratory, Upton, NY 11973 USA

[†]Politecnico di Bari, Dipartimento di Elettrotecnica ed Elettronica, via E. Orabona 4, 70125 Bari, Italy

Abstract

We report here an ultra low noise charge sensitive monolithic CMOS amplifier (CSA) suitable for small anode capacitance (200fF), low leakage current solid state detectors. The CSA is continuously sensitive, the charge from the input node being drained by a feedback transistor Mf biased as a resistor with effective values in the GΩ range. This very high value was achieved by a novel scheme which tracks threshold variations, and power supply and temperature fluctuations. A good linearity of the CSA conversion gain is achieved (<0.1% up to 1.8fC input charge) by inserting a voltage divider between the output of the CSA and the source of Mf.

The equivalent noise charge (ENC) of the CSA is equal to the theoretical lower limit imposed by the flicker noise. The circuit has been fabricated in two different CMOS technologies. With no detector connected, we measure a room-temperature ENC of $9 e^-$ rms at 12 μsec shaping time. When coupled to a cooled detector a FWHM of 111 eV is obtained at 2.4 μsec shaping, corresponding to an ENC of $13 e^-$ rms.

This is the best reported energy resolution ever obtained with a CMOS preamplifier.

I. INTRODUCTION

A large number of applications require extremely low noise detection systems, based on small capacitance and low leakage current detectors [1,2]. The charge sensitive amplifier (CSA) is widely used at the front-end, as its conversion gain is independent of anode capacitance variations (see Fig.1). The charge resulting from an ionizing event is collected at the anode and transferred onto a feedback capacitor Cf. The capacitor has to be discharged to avoid the saturation of the CSA by a charge delivered by events and detector leakage current. This DC feedback path is realized in different ways depending on the technology used to fabricate the CSA.

Among the available technologies, CMOS offers the advantage of being inexpensive and readily available for prototyping. On the other hand, it has some disadvantages i.e. the higher flicker noise compared to other technologies, and the difficulty of integrating large value resistances. For the considered low noise application the DC stabilization of the amplifier is the most critical aspect of the design.

Various approaches have been proposed so far. A pulsed reset [11] can be used for systems with a small number of channels, at the cost of increased system complexity. Other

continuously sensitive CMOS CSA for low capacitance detectors rely on a differential transconductance schemes [2],[10]. These have several drawbacks. First, the tail current of the transconductor must be adjusted to accommodate the maximum expected leakage current. This penalizes low-leakage channels, where the parallel noise of the feedback circuit will be greater than the shot noise due to the detector. Secondly, the effective feedback transconductance varies with leakage current, causing a shift in the frequency of the feedback pole which in turn effects the gain. The same effect occurs with large signal currents, giving such circuits poor linearity. Finally, this type of feedback element contains many transistors. This leads to increased capacitance at the input node (hence more series noise), increased layout area, and a complex feedback loop which can be difficult to stabilize.

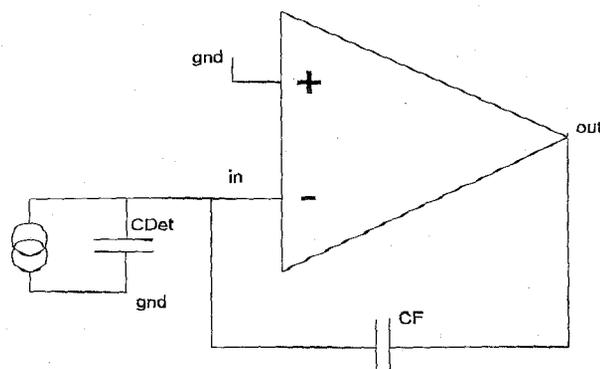


Fig.1: Charge Sensitive Amplifier (CSA) based on a core voltage amplifier with shunt feedback

A practical way to establish the DC feedback in a continuously sensitive CSA is by using a transistor Mf biased in the triode region in parallel to Cf. This DC feedback scheme can accommodate a large leakage current since increasing I_{leak} reduces the effective resistance and keeps the CSA from becoming saturated [5].

The parallel noise associated with the drain-source resistance R_{ds} of Mf doesn't contribute to the parallel noise if $R_{ds} \gg 50mV/I_{leak}$. For ultra low noise applications I_{leak} can be 1 - 10pA, and the only practical way to achieve the required 5 - 50GΩ resistance is by biasing Mf close to the weak inversion region. The drawback is the extreme sensitivity of the associated R_{ds} to even small variations in the biasing conditions, i.e. the potential at the input transistor of the

CSA, the threshold of M_f , the potential at the output node of the CSA.

Consequently two issues need to be addressed: i) how to bias M_f to achieve the $G\Omega$ region for its effective resistance and how to stabilize its resistance against parametric process variation during chip production, in particular the threshold variations which can reach $\pm 100\text{mV}$ from chip to chip; ii) how to improve the linearity of a system with a non-linear element inserted in the feedback loop. The worsening of the linearity is due to the change of the decay time during the transient, and the dependence of its value upon the input charge.

We addressed both issues by means of novel circuit techniques. M_f is biased in or near weak inversion by using a variation of our previously reported scheme for producing a high-value DC feedback resistance in a CSA using MOSFET adaptive matching techniques [8]. Here we implemented the self-adaptive scheme with a P-channel input device where a minimum size P-channel feedback transistor is biased close to weak inversion to achieve a resistance three orders of magnitude ($G\Omega$ region) larger than the one achieved in [8] with a N-channel input device.

The sufficiently large feedback resistance of our schemes allowed us to design a continuously sensitive high linearity CMOS CSA for low anode capacitance, low leakage current detector with equivalent noise charge (ENC) equal to the theoretical lower limit imposed by flicker noise. The circuit was fabricated in two different foundries: i) HP $1.2\mu\text{m}$ and ii) AMS $1.2\mu\text{m}$ process in order to compare the flicker noise behavior of the two processes.

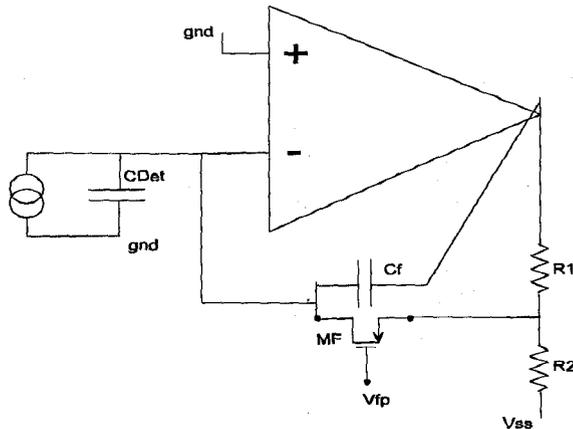


Fig.2: T-Network with minimum size MOSFET transistor M_f

II. CIRCUIT DESIGN

A. T-Network in the DC path

Noise constraints require a sufficiently large feedback resistor, thus the feedback transistor M_f (see Fig.2) is biased close to the weak inversion region, where R_{ds} is strongly affected by biasing condition variations. The non-linear R_{ds}

changes during the decay time, and its mean value depends upon the amplitude of the charge pulse.

In our case of $C_f=15\text{fF}$ and $Q_{in}=0.75\text{fC}$ the CSA output swings 50mV which, when applied to the gate-source voltage of M_f corresponds to a variation of almost a factor of 4 in the feedback resistance. This affects the conversion gain, as a charge pulse is integrated with a finite rise time on the feedback C_f , and discharged with a decay time which is a function of the pulse amplitude.

The peak amplitude is affected by the ratio of the pulse rise time to the decay time, that is, by the relative position of the two poles in the preamplifier transfer function. The minimal effect of the decay time on the pulse amplitude is achieved when the poles are far apart.

To improve the linearity we introduced a voltage divider between the output of the CSA and the source of M_f (Fig. 2.) The CSA output voltage swing as a response to an input charge is attenuated three times at the source of M_f . The decreased V_{gs} change during the dynamic output swing decreases the R_{ds} variations. Moreover, the decay time of the impulse response takes three times longer than a feedback network without the attenuator. The linearity of the CSA gain benefits from the multiplied decay time, i.e. the increased ratio between the two poles. The increased decay time is an advantage when an external shaper is used. With typical values of $R_{ds}=3\text{G}\Omega$ and $C_f=15\text{fF}$ we achieve a decay constant of $140\mu\text{s}$. If the shaping time is $4\mu\text{s}$, then the decay of the pulse from the preamplifier is only 3% and any imperfect tail cancellation due to the dependence of the decay time on the amplitude influences the linearity only in the second order.

B. Self-Adaptive Bias Circuit for M_f

The feedback resistance contributes negligible parallel noise if:

$$4kT/R < 2qI_L \quad (1)$$

With leakage current $I_L=1\text{pA} - 100\text{pA}$ this sets R in the range

$$0.5\text{ G}\Omega < R < 50\text{ G}\Omega \quad (2)$$

We used a $3 \times 3\ \mu\text{m}$ p-channel MOS transistor M_f as the feedback resistor. It adds only negligible parasitic capacitance to the input node and in parallel to the feedback capacitance. M_f works in the near-subthreshold region where its associated resistance is exponentially sensitive to its biasing conditions.

The new self bias scheme is an extension on the scheme reported in [8]. There a CMOS CSA with N-channel input device, matched to 0.8pF input capacitance, has been developed for a particle tracking system. In that application,

the peaking time was 50 nsec., and parallel noise and leakage current considerations dictated the choice of a feedback resistance of 6 MΩ, achieved with a W/L=3/20 MOS device biased in the triode strong inversion region.

Now the problem is similar, but the scheme reported in [8] must be modified for use with a P-channel input device. Moreover, the requirements are more challenging: noise considerations call for an associated feedback resistance three orders of magnitude larger (GΩ region) and we are forced to use a minimum size MOSFET device with negligible parasitic capacitances added to the input node. This sets Mf in the subthreshold region, where Rds is extremely sensitive to the biasing condition of Mf.

The solution is to apply the self-adaptive scheme to a P-channel input device with improved capability to track threshold variations in P and N-channel transistors. The circuit is shown in Fig.3, and our goal is to keep:

$$V_{G,Mf} - V_{S,Mf} - V_{T,Mf} = \text{const} \quad (3)$$

even when $V_{GS,Mf}$ is only a few times kT/q below threshold, as is necessary for large R with small W/L. Note that $V_{S,Mf}$ is determined mainly by the threshold of PMOS device M1, whose fluctuations are only partially correlated with $V_{T,Mf}$ of Mf. The third term in (1), $V_{T,Mf}$, is influenced by the body effect and by the narrow-channel effect [5]:

$$V_{T,Mf} = V_T(V_{BS,Mf}, W_{Mf}) \quad (4)$$

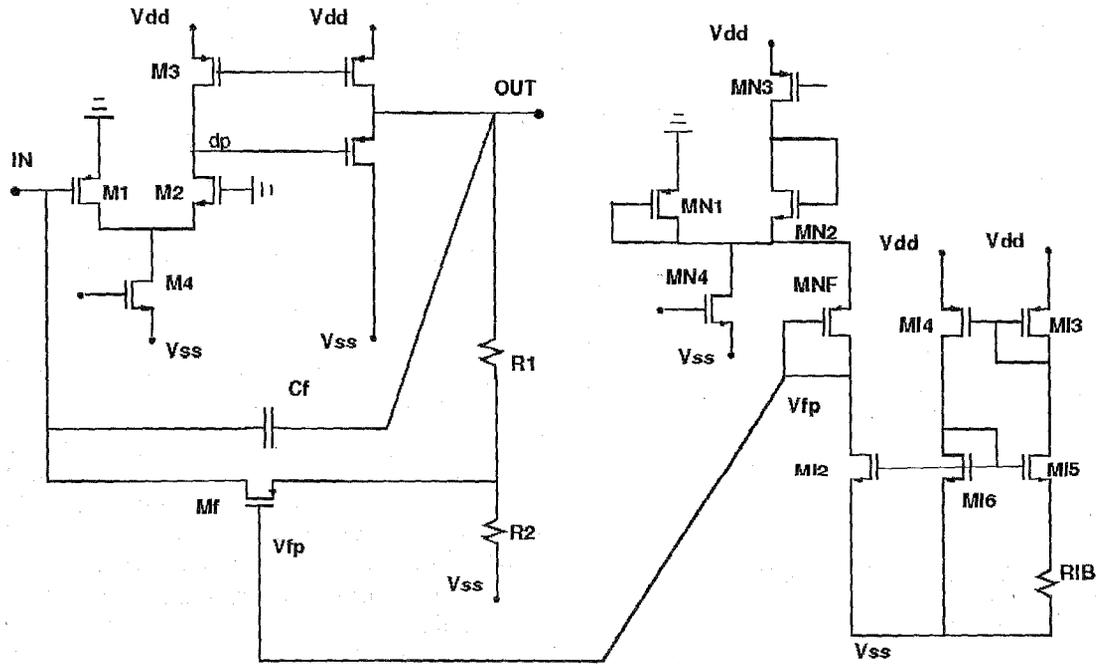


Fig.3: Core voltage amplifier (left hand side of picture) and self adaptive bias scheme (right hand side)

The gate voltage $V_{G,Mf}$ tracks the variations in V_{T1} and $V_{T,Mf}$. a diode-connected replica MN1 of M1 is biased at the same current density so that the voltage at the drain of MN1 tracks its threshold ($V_{G,MN1} = V_{G,M1}$). Moreover, the required gate-to-source voltage of the feedback device is generated by passing a current $I_{d,MNF}$ through diode MNF. MNF is a scaled copy of Mf:

$$(W/L)_{MNF} = n (W/L)_{Mf} \quad (5)$$

created by laying out n parallel copies of Mf. Since MNF has the same V_{BS} and width as Mf, it experiences the same body and narrow-channel effects. It results that $V_{GS,Mf} = V_{GS,MNF}$.

Note that the maximum achievable feedback resistance in Mf is determined by its V_{gs} , which is controlled by the V_{gs} of replica transistor MNF and the scaling ration n . In this circuit we set $n=180$ and we use a low-current source (MI2-MI6, RIB in Fig. 3) to set $I_{d,MNF}=12nA$

In addition to compensating for threshold voltage variations, this circuit is also immune to power supply fluctuations and noise since the critical node voltages are referenced only to ground and to transistor thresholds. The residual power supply coupling will be determined by the quality of the current sources.

Of course, the self-bias circuitry need only be placed once for a multi-channel chip, with the gate voltage V_{fp} routed to many preamplifier channels.

When detector leakage current is present, the output node (right-hand side of Mf in Fig. 3) moves positive and becomes Mf's effective source. This causes a reduction of the static feedback resistance. This reduction is desired because it extends the range of the allowable leakage current from the detector. Clearly a higher value of the detector leakage current degrades the energy resolution.

The node Vfp (gate of Mf) has been brought to an external pad, and it's possible to force on the gate bias conditions different than the natural one. This feature was used to obtain the best possible noise performance, albeit defeating the self-adaptive bias scheme.

C. Core Voltage Amplifier

The CSA consists of a core voltage amplifier with shunted feedback capacitance Cf. The lower limit for Cf, which has been chosen here equal to 15fC, is set by the undesired, non-linear, parasitic drain-source capacitance associated with the minimum size feedback device Mf. The core voltage amplifier used in the CSA is a classical folded cascode OTA followed by a voltage buffer (Fig.3).

A large feedback resistance realized by our technique and the absence of strict speed requirements typical of X-Ray spectroscopy applications allows us to use long shaping time. In this condition the series noise can be made sufficiently low that it doesn't contribute significantly to the ENC. The achievable ENC is limited by the flicker (1/f) noise. A PMOS input stage transistor was chosen to benefit from its lower flicker noise in spite of its higher series noise at otherwise identical conditions. The capacitive matching was also implemented for the flicker noise, that is, we have $C_{gt}=C_{det}$.

To compare the flicker noise performance of two foundries, we fabricated the prototype using the HP 1.2 μ m and AMS 1.2 μ m process. Designs for different foundries are identical but for the aspect ratio of the input transistor. We designed the HP preamp to match a C_{det} of 200 fF, while the AMS version has an input capacitance matching $C_{det} = 130$ fF. The input devices are biased at about 1mA. The feedback transistors are biased to give an expected RF (in simulation) of 0.30 and 0.83 G Ω for the HP and AMS circuits respectively. The AMS chip includes one CSA with full input electrostatic discharge (ESD) protection and one without.

The most important secondary noise sources in the CSA are the current sources M3 and M4, whose noise contribution have been minimized with respect to the input transistor M1.

The open-loop voltage gain of the preamplifier is

$$A_v(s) = \frac{g_{m1}R_0}{(1+s\tau_1)(1+s\tau_2)} \cdot \frac{R_{o1}}{(R_{o1}+R_{icas})} \quad (6)$$

and the two poles are given by:

$$\tau_1 = R_0C_0, \quad (7)$$

$$\tau_2 = R_{icas}C_1 \quad (8)$$

where g_{m1} is the transconductance of M1. R_{o1} is the output resistance of M1 in parallel with the output resistance of M4, R_0 and C_0 are the effective resistance and capacitance seen from node dp to ground, and C_1 is the effective capacitance at the drain of M1. R_{icas} , the input resistance of the cascode transistor M2, is inversely proportional to g_{m2} . This stage has a gain of about 1300, a gain-bandwidth product of 250 MHz, and dissipates about 11 mW. With an input capacitance of 0.2pF representing the detector plus parasitics, the rise time to a charge impulse is < 40 nsec.

III. EXPERIMENTAL RESULTS

A. Linearity of the CSA conversion gain

We measured the peak output voltage of the AMS preamplifier (no detector connected) using the on-chip injection capacitor and a multi channel analyzer. In Fig.4 the CSA gain vs. input charge is reported. It was found to be linear to better than 0.1% up to an input charge of 1.8 fC.

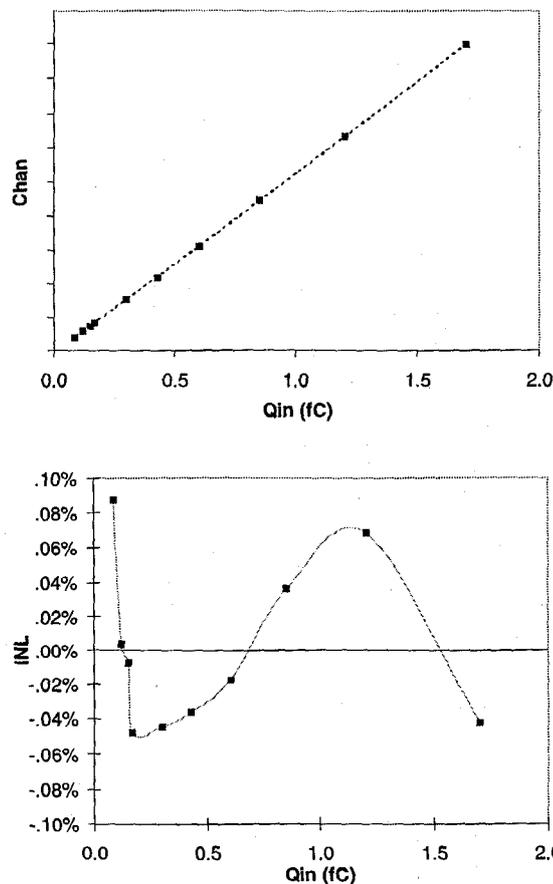


Fig.4: Conversion gain and integral nonlinearity of the CSA vs. input charge.

B. Self-adaptive bias circuit

We measured the equivalent resistance of the feedback device by measuring the fall time of the CSA output response to a charge impulse. In the self-biased condition RF was about 280 MΩ and about 1.8 GΩ for the HP the AMS device respectively.

In Fig.5 the CSA response to a charge pulse is shown at different temperature (AMS version). The temperature variation produces a threshold variation of 200 mV in both P and N channel devices. The change of the RF is less than 20% when changing the temperature by 100° C. Without threshold tracking, the effective RF would be expected to change more than 2 orders of magnitude over this range. Said another way, our self-bias circuit must track the threshold voltage changes to within 16mV. Second-order effects, such as hole mobility and Cf capacitance change with temperature, may also contribute.

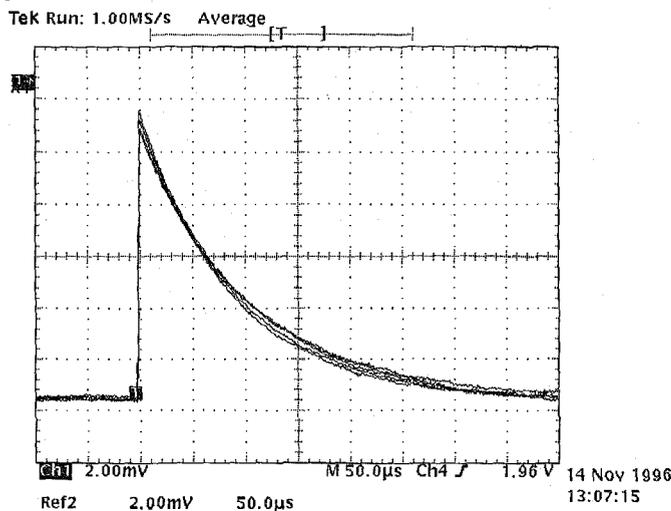


Fig. 5: Response of the CSA to a charge pulse at different temperatures (-75,-50,-25,0,25)°C. The higher resistance corresponds to the higher temperature.

C. Noise - CSA with no detector connected

For these measurements, the preamps were mounted on an FR-4 test board but not bonded to any detector. The input parasitic capacitance due to the on-chip wiring and bond pad were estimated as 240fF and 310fF for the AMS and HP circuits, respectively.

The ENC vs. shaping time of the CSA was measured at different temperatures with an external shaping amplifier. The results are shown in Fig. 6 for the AMS version. The upper group of curves is for the preamp in its self-biased condition. The lower data set is obtained after optimizing the bias voltage VFP for each temperature. Solid lines are a fit of the data to

$$ENC^2 = A + B \cdot T_s + C/T_s, \tag{9}$$

from which we can find the three noise parameters Rs, Rp, and KFP, the series and parallel white noise equivalent resistances and the 1/f noise coefficient respectively.

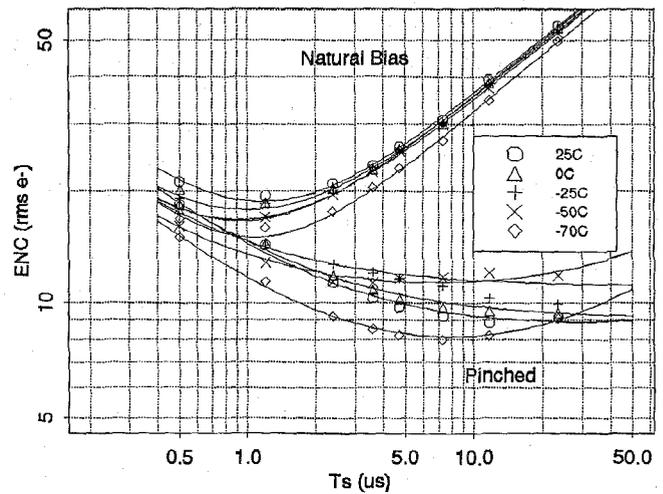


Fig. 6: ENC vs. shaping time for the AMS CSA at 5 temperatures. Feedback device self-biased (upper group) and high-RF bias (lower curves.) Preamp not connected to detector.

These are plotted as a function of temperature for the HP and AMS processes in Fig. 7.

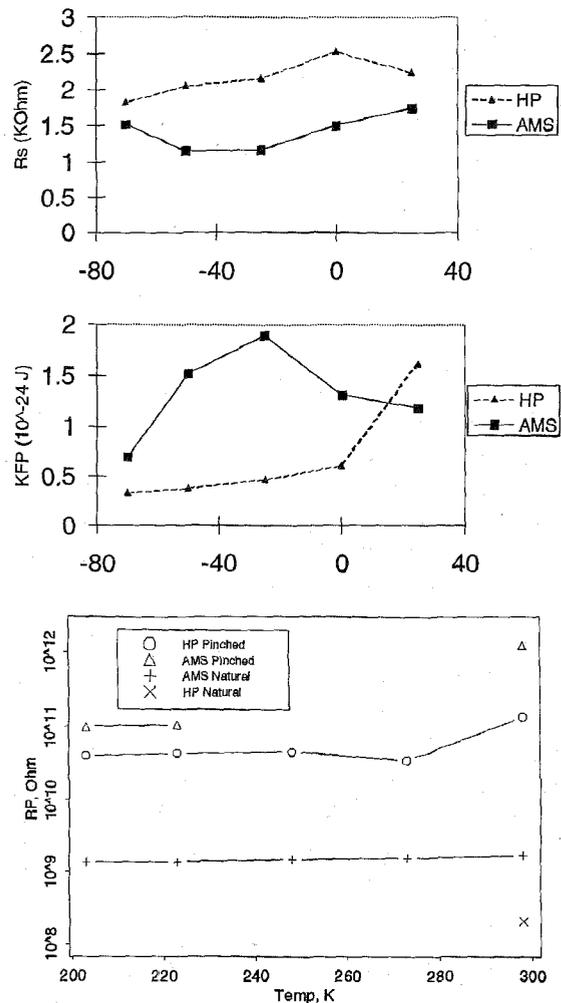


Fig. 7: Noise parameters Rs, Rp, and KFP for HP and AMS preamps extracted from the data of Fig. 6.

Fig. 8 shows room temperature noise-vs.-shaping time curves for the HP and AMS preamps in the natural and high-RF bias conditions. The HP circuit has higher series and parallel noise due to its higher input capacitance and lower RF than the AMS version.

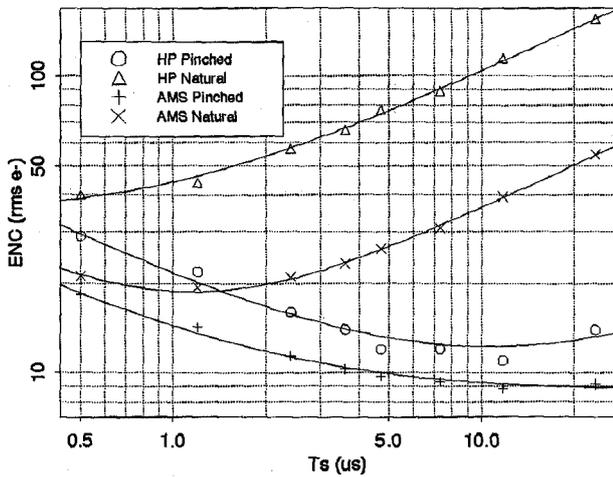


Fig. 8: ENC vs. shaping time of the HP and AMS versions in the self biased condition and with Mf at high resistance.

The values of the equivalent parallel noise resistance for the AMS preamp are summarized in Table 1 at different temperatures, and are in a good agreement with the values measured from the decay time.

Table 1

Equivalent feedback resistance of AMS premp determined by two methods

T (°C)	R parallel noise (GΩ)	R decay time (GΩ)
25	1.66	1.81
-70	1.35	1.52

D. Noise - CSA connected to SDD detector.

The preamplifier input was bonded to an anode of a silicon drift detector (SDD). The anode capacitance was about 0.1 pF. The set-up used is shown in Fig. 9. The chip carrier is close to the center of the picture, the circular SDD is slightly to the left and partially screened by PC board carrying the detector. The SDD is almost 3cm in diameter, however, only its central part was biased to be active to limit the leakage current flowing into the anode. A very long (1.5cm) bond connection from the central anode of the SDD to the input of the CSA was used. We estimated that this connection added about 0.14pF to the input capacitance.

The response of the CSA and the response of the CSA connected to an external shaper (3.6us shaping time) to an X-Ray from Mn is shown in Fig. 10. We also recorded the spectra of ^{55}Fe and ^{241}Am sources. These are shown in Fig. 11 and Fig. 12, respectively.

For these measurements, the feedback device was pinched off by an external control voltage (the self-adaptive bias

circuit was not used). The measurements were performed at -70°C to eliminate any noticeable contribution to the noise from the detector leakage current. In this conditions, the FWHM of the system is 111eV, which is an improvement of almost a factor of 2 over the best previously reported resolution of a Si detector coupled to a CMOS circuit [2].

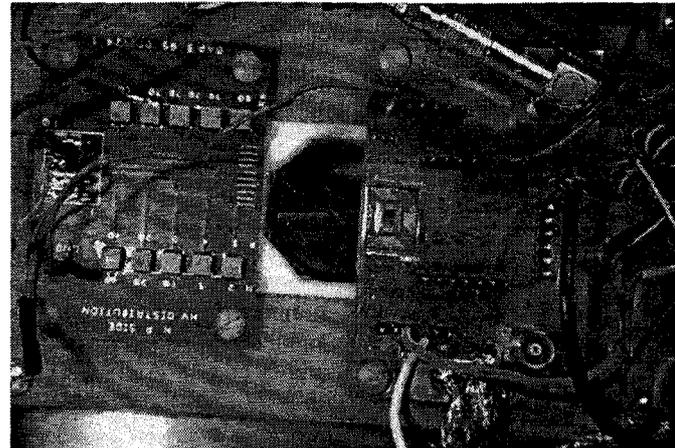


Fig. 9: Experimental set-up. The CSA is connected with 1.5cm bonding connection to the central anode of the circular SDD.

This noise performance was obtained with a pseudo-gaussian shaping form at a shaping time long enough and the leakage current low enough that practically the only contribution to the noise was the flicker 1/f noise. It is possible to use an optimal filter for the series 1/f noise according to the reference [12]. The practical realization of this optimal filter with a digital signal processing system is described in reference [13]. An improvement of 18% was achieved. We estimate that with a filter designed to optimize the 1/f noise the preamplifier with a detector connected can reach the noise performance of 11 electrons r.m.s.

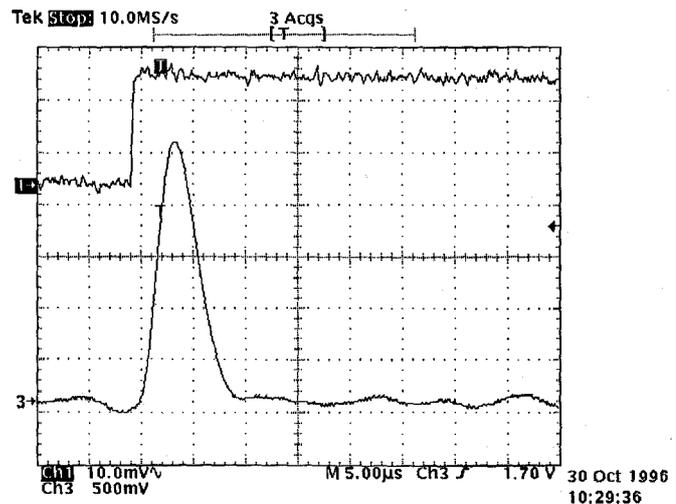


Fig. 10: Event from ^{55}Fe : the upper waveform is the CSA response, the bottom one is the CSA connected to an external shaper ($t_s=2\mu\text{m}$).

The noise performance of the detector preamplifier combination was studied also at -20°C , a temperature which can be reached by a simple Peltier cooler. The dependence of ENC on the shaping time was studied. From a curve similar to one shown on Fig. 6 the three main noise sources were identified. The leakage current of the detector was about 15pA ; if we use the equivalent series noise resistance of $2\text{k}\Omega$ as reported in Fig. 7 the total capacitance of the input node from the series noise contribution is 0.6pF . The constant contribution of the flicker noise is 13 electrons r.m.s.

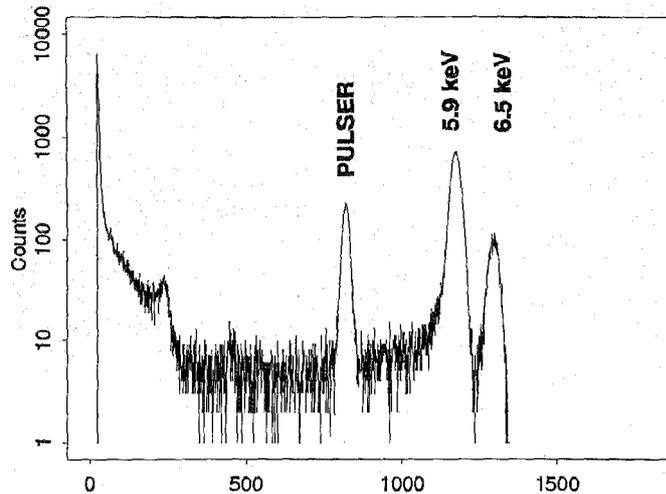


Figure 11: ^{55}Fe spectrum of the AMS preamplifier at -70°C . FWHM of the pulser peak is 111eV (13e^- rms.)

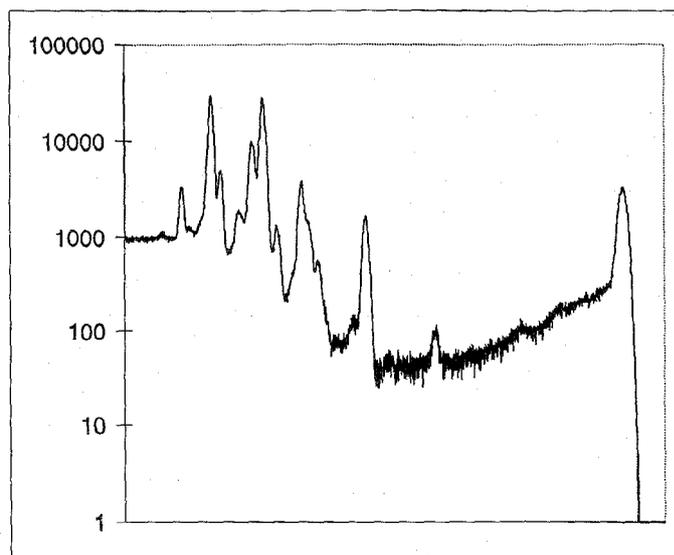


Fig. 12: ^{241}Am spectrum measured with the HP preamplifier at -70°C .

There are three different approaches to the front end read out electronics for X-Ray spectroscopy with silicon drift detectors offering the smallest detector capacitance. The first approach is the integration of the first transistor into the detector itself. [14]. This approach gave the lowest noise performance up to now. [15] This technology, however, has its own limitation. The transistor has to be placed on the

surface of the detector increasing the usually otherwise negligible capacitance of the anode. The transistor is produced with all constraints dictated by the production of the highest quality silicon drift detectors. The best up to date transistor is a Single Sided Gate n-channel JFET with the channel length about $5\mu\text{m}$.

The second, CMOS approach of this paper with the p-channel MOS transistor is relatively new. MOS transistors used to be avoided as the first transistors of a low noise application for their large $1/f$ noise. The use of a p-channel transistor makes this excess noise almost tolerable. The low mobility of holes at the silicon-silicon dioxide interface by a factor of six relative to the mobility of electrons in the bulk of n-type silicon of the first approach is compensated by much shorter channel length available in the CMOS technology.

The third approach is to use a traditional discrete n-channel JFET as a first transistor. Recently MOXTEK [16] introduced fast JFETs with the gate capacitance down to 0.5pF . The test of the X-Ray systems is still in progress.

The final noise performance of all 3 approaches is limited by the $1/f$ noise. The origin of this noise may be very different in 3 different first transistors. Given this uncertainty it is difficult to predict which approach will finally lead to the best performance.

IV. CONCLUSIONS

A high linearity, ultra low noise CSA for X-Ray spectroscopy has been fabricated in two technologies by using novel circuit techniques. The CSA is continuously sensitive, and requires no external components or adjustments to be operated. In its self-biased condition, the AMS version has $1.8\text{G}\Omega$ feedback resistance, the HP one $280\text{M}\Omega$. The linearity of the system ($<0.1\%$ up to 1.8fC input charge) has been significantly improved by using a T-network. The absence of strict speed requirement, and the huge feedback resistance featured by our CSA allows us to shape at long shaping times.

At room temperature and with the feedback device pinched off, the ENC of the CSA alone is 9e^- rms. With a cooled SDD detector ($T=-75^{\circ}\text{C}$), the electronic FWHM is equal to 111eV ($\text{ENC}=13\text{e}^-$ rms).

These results are the best noise performances ever reported with a CMOS CSA.

V. ACKNOWLEDGMENTS

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