

Advanced Readout ASICs for Multielement CZT Detectors

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ABSTRACT

A generation of high performance front-end and read-out ASICs customized for highly segmented CdZnTe sensors is presented. The ASICs, developed in a multi-year effort at Brookhaven National Laboratory, are targeted to a wide range of applications including medical, safeguards/security, industrial, research, and spectroscopy.

The front-end multichannel ASICs provide high accuracy low noise preamplification and filtering of signals, with versions for small and large area CdZnTe elements. They implement a high order unipolar or bipolar shaper, an innovative low noise continuous reset system with self-adapting capability to the wide range of detector leakage currents, a new system for stabilizing the output baseline and high output driving capability. The general-purpose versions include programmable gain and peaking time. The read-out multichannel ASICs provide fully data driven high accuracy amplitude and time measurements, multiplexing and time domain derandomization of the shaped pulses. They implement a fast arbitration scheme and an array of innovative two-phase offset-free rail-to-rail analog peak detectors for buffering and absorption of input rate fluctuations, thus greatly relaxing the rate requirement on the external ADC. Pulse amplitude, hit timing, pulse risetime, and channel address per processed pulse are available at the output in correspondence of an external readout request.

Prototype chips have been fabricated in 0.5 and 0.35 μm CMOS and tested. Design concepts and experimental results are discussed.

Keywords: CMOS, preamplifier, low-noise, CZT, ASIC, shaper, peak detector, derandomizer

1. INTRODUCTION

Use of CMOS ASICs for front-end amplifiers in particle and radiation detectors began in the late 1980's with circuits developed for high-energy physics (HEP) particle tracking with silicon strip detectors¹⁻⁴. Although these chips were made in 3 μm technology, they achieved widespread acceptance by enabling dense, high channel count systems to be constructed at reasonable cost. Work on CMOS readout ASICs started at Brookhaven National Laboratory in 1991. The BNL effort focused initially on multiwire proportional chamber readout, followed in 1995 by work with silicon drift detectors. These applications present challenges to the ASIC design which are significantly different from those in Si strip readout in HEP:

- a wide detector capacitance range from 0.1 pF – 200 pF;
- the need to work at high signal-to-noise ratios of 200:1 or better for good position interpolation and energy resolution;
- the need to work with random pulses from X-ray sources.

The techniques and insights acquired in the development of these new ASICs are also helpful in the readout of other radiation sensors like CdZnTe (CZT). Since 1997 there has been a collaborative research program in ASICs for CZT between BNL's Instrumentation Division and researchers at eV Products and at the BNL National Synchrotron Light Source. The sections that follow describe the ASICs that have been developed for CZT under this collaboration.

2. AMPLIFIER ASICS

The goal of the CZT amplifier development program has been to produce multichannel preamplifier/shaper ASICs having performance characteristics (noise, linearity, stability) adequate for spectroscopic applications, while reducing the cost, area, and power dissipation by 1 or 2 orders of magnitude compared to previous hybrid and discrete implementations. The most challenging aspects of high performance charge amplifier design in CMOS are: correct dimensioning and biasing of the input MOSFET for minimum noise, a DC-coupled preamplifier reset circuit with good compliance, achieving a well-controlled pulse shape and stable baseline, high power supply rejection and low temperature coefficient. The subsections that follow detail the circuit techniques used to achieve these results.

Fig. 1 is a simplified schematic of a single ASIC channel, showing the major blocks.

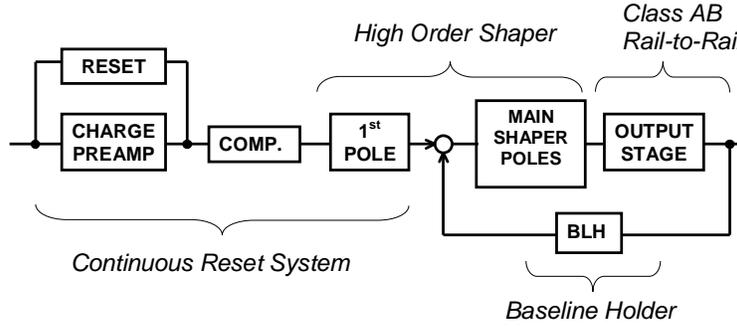


Fig. 1: Channel simplified schematic

2.1 Low-noise, capacitively matched preamplifier

CZT applications have expanded and now include soft X-ray to multi-MeV energies, and element sizes from about 0.1 – 20 mm². As a consequence, detector capacitance can vary over a wide range. The noise of the front-end preamplifier (expressed as equivalent input noise charge, ENC) is a function of the detector capacitance, shaping time, leakage current, and allowed power dissipation in the electronics:

$$ENC^2 = \left[A_1 \frac{1}{\tau_p} \frac{4kT}{g_m} + A_3 \frac{K_F}{C_G} \right] (C_G + C_D)^2 + A_2 \tau_p 2q(I_L + I_{RST}) \quad (1)$$

where A_1 - A_3 are coefficients related to the pulse shaping filter, τ_p is the pulse peaking time, C_D , C_G are the detector and MOSFET capacitance respectively, I_L is the detector leakage current, and K_F is the 1/f noise coefficient. C_D and I_D are set by the detector, and τ_p is determined by the rate expected in the application. The transconductance of the input MOSFET, g_m , is constrained by the allowed power dissipation P_d ($g_m \sim P_d^{1/2}$), a limit which is partially compensated by the reduction in minimum channel length L and supply voltage V_{DD} in scaled CMOS technologies. To each value of detector capacitance C_D and power dissipation P_d there corresponds a value of C_G (i.e. of the channel width W) which minimizes the first term of Eq. (1) ⁵. If no limit is imposed on the drain current I_D , the optimum condition leads to $C_G = C_D$ (and then $ENC \propto C_D^{1/2}$). If a limit is imposed on the drain current I_D , as in most practical cases, the optimum condition leads to $C_G = C_D/3$ ($ENC \propto C_D^{3/4}$) if the FET operates above threshold (strong inversion for a MOSFET), and to $C_G \ll C_D/3$ ($ENC \propto C_D$) if the FET operates below threshold (weak and moderate inversion for a MOSFET). From Fig. 2 one sees that the optimum MOSFET capacitance C_G reaches values as low as $0.01C_D$, as C_D increases and I_D decreases. Concerning the second term of Eq. (1), the negligible dependence of K_F on the operating point leads to the optimum condition $C_G = C_D$. The optimum C_G which minimizes both the first and the second term of Eq. (1) is the result of a compromise which takes into account both the thermal and the 1/f noise contributions from the input FET for a given peaking time τ_p . Mathematical models were developed to find the optimum transistor size under the constraints of available power and

peaking time. These models consider series, parallel, and 1/f noise, excess noise due to short-gate effects, transconductance behavior under strong, moderate, and weak inversion, mobility reduction, and parasitic effects of capacitance and dielectric loss.

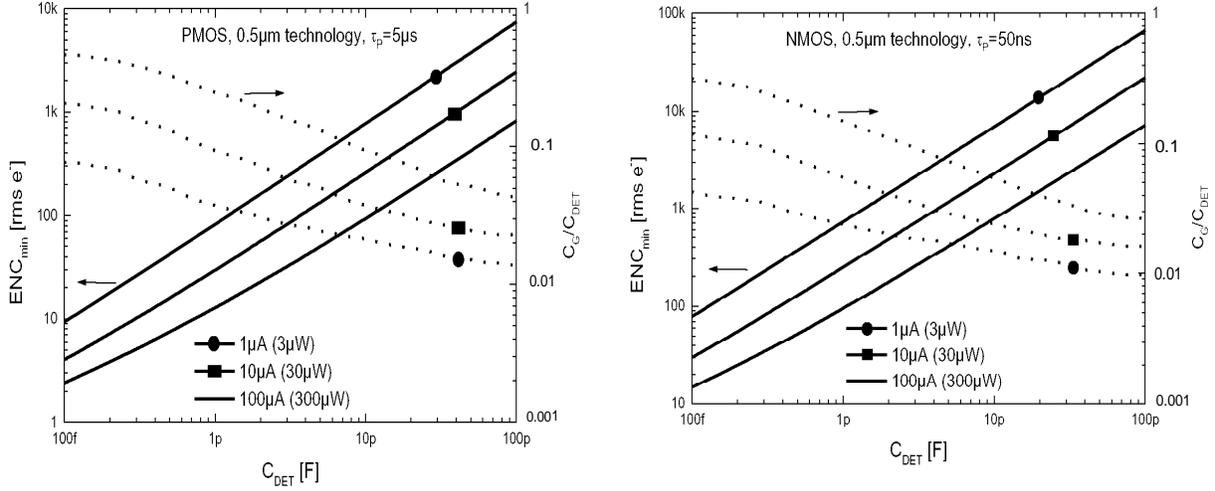


Fig. 2. Dependence of the minimum achievable ENC on the detector capacitance C_{DET} for different values of I_D (i.e. power dissipated by the input line) for a commercial 0.5 μm CMOS technology and corresponding optimum ratio C_G/C_{DET} . The cases of the PMOS (a) for $\tau_p = 5 \mu\text{s}$ and of the NMOS (b) for $\tau_p = 50 \text{ ns}$ are compared ($I_L=0$ in both cases).

2.2 Continuous reset system

The low-frequency feedback of a CMOS ASIC preamplifier presents a significant design challenge. It is required to stabilize the preamplifier's operating point and to discharge the feedback capacitance while contributing negligibly to noise and nonlinearity, and it must be insensitive to process, temperature, and power supply variation. In the case of detectors which are *dc-coupled* to the integrated front-end electronics, the reset system must also supply the detector leakage current, which is subject to large variation and drift due to thermal effects, degradation and parameter spread. As shown in Eq. (1), the reset system contributes an equivalent parallel noise current I_{RST} which adds quadratically to the detector leakage current. The classical solution based on the use of a simple resistor R_F in parallel to the feedback capacitance is usually impossible to implement in monolithic technology, since R_F must have a value in the $10^7 \Omega$ range (noise $4kT/R_F$ to be compared to $2qI_L$). Several solutions to the reset problem based on active devices have been consequently developed. The most common techniques are

- MOSFET switch;
- single MOSFET in feedback with gate bias adjusted to produce high effective resistance;
- low-frequency feedback transconductance.

The MOSFET switch attains very low noise since its effective resistance is nearly infinite in the OFF state. The user must supply a periodic reset pulse at sufficiently high rate to keep the amplifier from saturating. The pixel with the highest leakage current will determine the reset rate, and all other pixels will have to be reset at an unnecessarily high rate. The charge amplifier is prone to oscillation when the switch is in the ON state, and charge injected through the reset line can corrupt the output for several microseconds after reset.

In the case of the single MOS transistor, there must be a method to bias the feedback transistor into a very high-resistance state. To compensate for process and temperature-induced threshold shifts, the gate voltage is usually left for the user to adjust. Also, the MOS transistor nonlinearity is detrimental to the accuracy of the amplifier.

The third approach uses a low-bandwidth differential pair in feedback around the preamplifier which sets the output voltage to V_{REF} . The low-frequency pole at g_m/C_f is nonlinear and difficult to compensate. This circuit must be designed to source the worst-case maximum leakage current, which adds unnecessary parallel noise to the less-leaky channels.

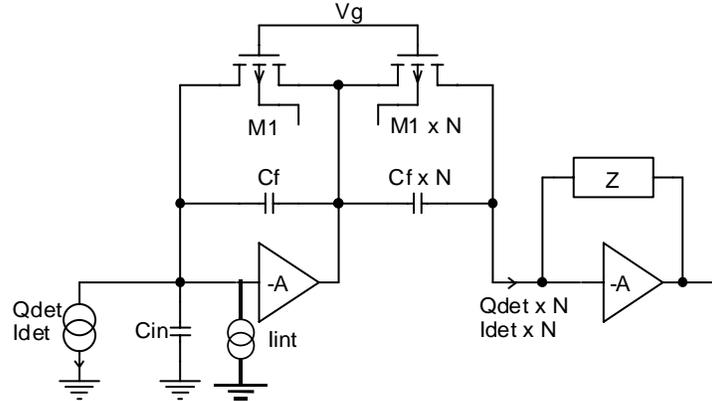


Fig. 3: Compensated reset system which self-adapts to the leakage current

The technique used in the present work is based on a monolithic version of the classical pole-zero cancellation circuit, as shown in Fig. 3⁶. In this circuit, the DC feedback is provided by a long-channel PMOS M1. M1 is biased into the saturation region by the detector leakage current and appropriate choice of the gate voltage (note that in this case the gate voltage is not critical and may be pre-set to a fixed potential since small on-chip current source $I_{int} \sim 10$ pA ensures that the transistor is always turned on). In analogy to the classical pole-zero compensation circuit, the zero formed by the compensation devices (M1 x N) and (Cf x N) exactly cancels the feedback pole due to M1, Cf. Excellent cancellation is achieved because the circuit relies only on good matching of the feedback and compensation MOSFETs. Note that since the two transistors' gates and drains are tied together, and their sources are tied to virtual grounds at similar DC potential, the pole-zero cancellation is effective even in the presence of large leakage and/or signal currents. Therefore the linearity of the system is preserved even though the time constant C_f/g_{m1} varies strongly with I_{leak} and Q_{sig} . As long as M1 is in saturation and in strong inversion, it contributes only thermal noise due to its effective resistance $1/g_{m1}$, which is always less than the shot noise of the detector leakage current. Overall, the circuit behaves as a charge or current amplifier with gain N. It is possible to construct a two-stage compensation circuit to achieve higher values of N. Fig. 4 shows the nonlinearity and pulse shape stability that result from the compensated reset system.

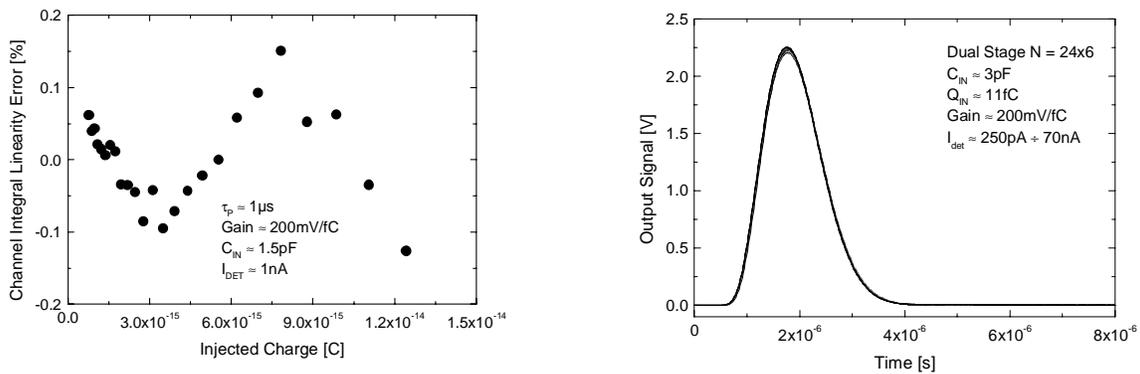


Fig. 4: Compensated reset system. (a) nonlinearity (b) pulse shape stability up to 70 nA.

2.3 High order shaping

Many monolithic amplifiers have low-order g_m -C filters to provide the pulse shaping. Although these filters are very power efficient, the most stable and controlled pulse shapes can only be obtained using feedback amplifiers with passive

components to determine the pole location. Our CZT amplifiers use high-order, complex-pole, active-RC filters to provide stable pulse shapes with the best combination of noise and rate-handling capability. Fig. 5 illustrates the benefits of high-order complex pole filters. In Fig. 5 three filters are compared. All three filters have equal 0.1% - 0.1% widths, and thus the same rate capability. The second-order filter is highly asymmetric and therefore has a high ratio of width to peaking time; accordingly it will have the highest series noise. The fifth-order filter made with 5 coincident real poles has a longer peaking time for the same width. The best ratio of width to τ_p is with the fifth order complex-pole filter, where the pole locations are determined using the Gaussian approximation method of Ohkawa⁷. The lower peak curvature of the 5th order complex shape is also beneficial for reducing ballistic deficit as commonly encountered in CZT detectors.

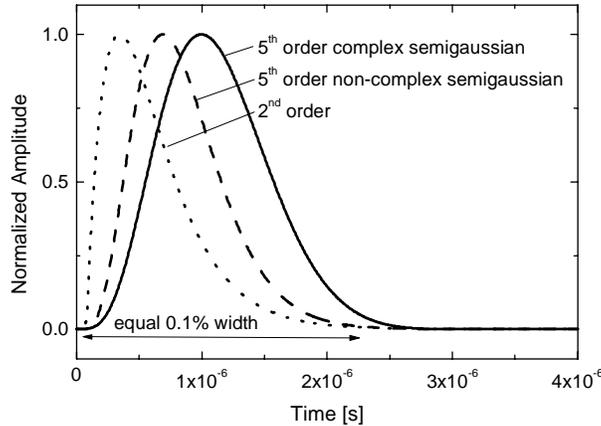


Fig. 5: Comparison of pulse shapes for 2nd order and 5th order filters with real or complex poles. All pulse shapes have the same full width at 0.1% maximum. The 5th order complex shaper has the best ratio of width to peaking time, leading to minimum series noise at equal rate.

2.4 Baseline holder

Amplifiers with unipolar shaping will experience baseline shifts due to rate fluctuations. For this reason, a baseline holder circuit based on a slew-rate limited nonlinearity was implemented⁸. A differential stage compares the output to a desired VREF and the output is low-pass filtered and fed back to the shaper input to stabilize the baseline. Large signal excursions are clipped by a slew-rate limited stage between the diff amp and the low-pass filter. Fig. 6 shows the effectiveness of the baseline holder.

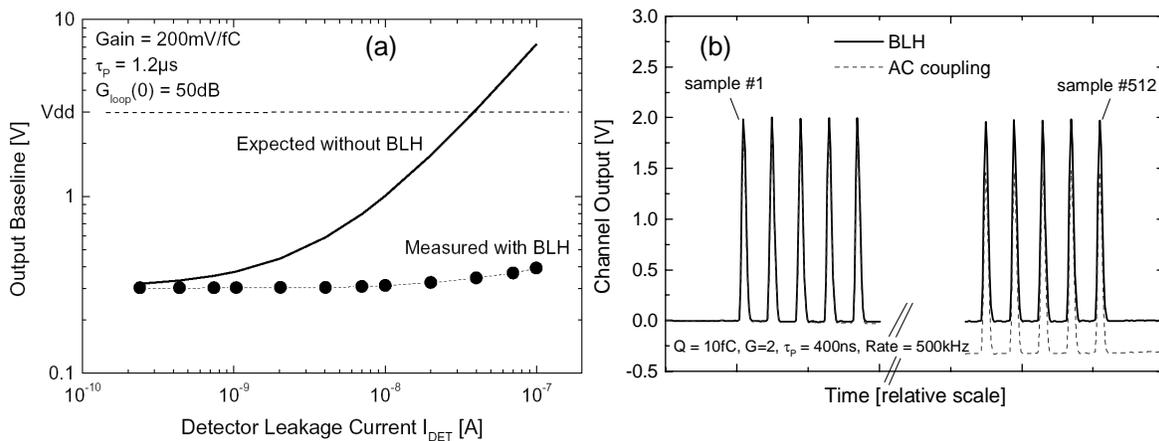


Fig. 6: Baseline holder action. (a) Stabilization of the baseline at DC. Solid curve is expected response without baseline holder: amplifier output saturates at 30 nA leakage. Points are measured with BLH. (b) Stabilization of the transient baseline in response to 512-pulse burst. Solid curves: pulse response of AC-coupled system. After 512 pulses, the baseline has drifted down ~ 300 mV. Dotted curve: same pulse sequence with baseline holder active. Baseline shift is negligible.

2.5 Practical amplifier considerations

Spectroscopy amplifiers need a high level of stability on time scale of several hours to acquire spectra from weak sources. The gain and offset should be insensitive to variations in input capacitance, output load impedance, temperature, supply voltage, count rate, and leakage current. Also, matching of amplifier gain and offset from channel to channel and from chip to chip is important in multichannel systems. As already discussed, the compensated reset system and the baseline holder give high immunity to leakage current variations. Other techniques that contribute to robust circuit operation are:

- all quiescent operating points set by threshold-referenced bias circuits which have high PSRR and adapt to process variation of threshold voltage;
- proper layout of differential pair transistors in the baseline holder and output driver to minimize mismatch;
- ability to put bias circuits of many chips in parallel to minimize chip-to-chip variation.

Table 1 shows the sensitivity of the CZT amplifiers to leakage current, supply voltage, temperature, rate, input capacitance, and output load impedance.

Table 1: Measured gain and baseline sensitivity for CZT amplifier ASICs

	I_{leak}	Supply	Temperature	Rate (to $5/\tau_p$)	C_{in}	Z_{load}
Gain	$< 0.1\%/nA$	$<.001\%/V$	$-0.04\%/^{\circ}C$	$< 0.1\%$	$<0.1\%/pF$	No slew-rate limit
Baseline	$< 0.3mV/nA$	$<30 \mu V/V$	$75 \mu V/^{\circ}C$	$< 8 mV$	-	$Z_{out} \sim 150 \Omega$

The ASICs provide several other features to enhance usability. In most ASICs gain and peaking time are programmable, and there are on-chip calibration capacitors and switches to enable easy calibration on a channel-by-channel basis.

Figure 7 shows the insensitivity of the output pulse shape to leakage and temperature. Figure 8 shows the gain and peak-time programmability.

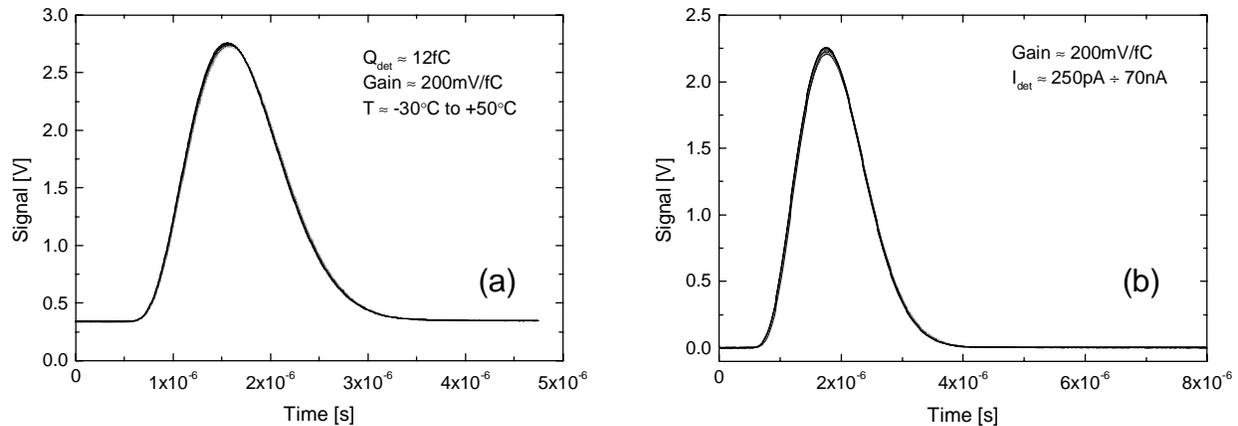


Figure 7: Amplifier output pulse shape vs: (a) temperature -30° - $+50^{\circ}C$ and (b) leakage current $250 pA - 70 nA$.

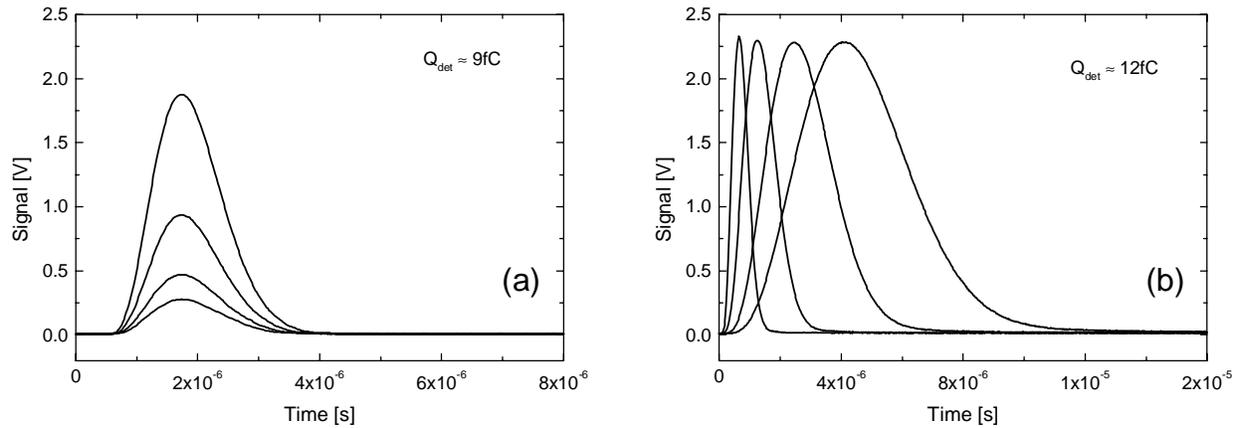


Fig. 8: Gain (a) and peaking time (b) programmability.

2.7 CZT amplifier family

As of early 2002, four amplifiers have been developed for a range of CZT applications. They differ in channel count, shaping time, and pulse shape⁹. Table 2 gives the specifications of the four amplifiers. All circuits have NMOS input transistors, PMOS feedback transistors, and compensated reset systems. CMOS technology is 0.5 micron triple-metal with linear MOS capacitor. A single power supply of 3.3V is used in all chips. Output baseline is +0.3V (adjustable to 0V on some circuits) and maximum linear signal swing is 3V. They operate with negative input current (leakage and signal current flow away from the preamplifier) and have positive-going output polarity. They each have programmable calibration capacitance and can source up to 100 nA of detector leakage current.

Table 2: CZT ASIC family developed at BNL

ASIC	Optimized detector capacitance [pF]	Channels / chip	Peaking time [μ s]	Gain [mV/fC]	Power dissipation [mW/ch]	ENC [r.m.s. e ⁻]
General Purpose	3	16	0.6, 1.2, 2, 4	30, 50 100, 200	18	30 + 20 /pF
Medium speed	3	4	0.4	200	18	29 + 27 /pF
High speed bipolar	3	8	0.2	240	18	42 + 44 /pF
High capacitance	12	8	0.6, 1.2, 2, 4	30, 50, 100, 200	35	57 + 10 /pF

A layout drawing of the general-purpose ASIC is shown in Fig. 9. Fig. 10 shows spectra taken with CZT detectors and the general-purpose ASIC.



Fig. 9: Layout of the 16-channel general purpose CZT preamplifier/shaper ASIC. Die size is 5.1 x 3.7 mm.

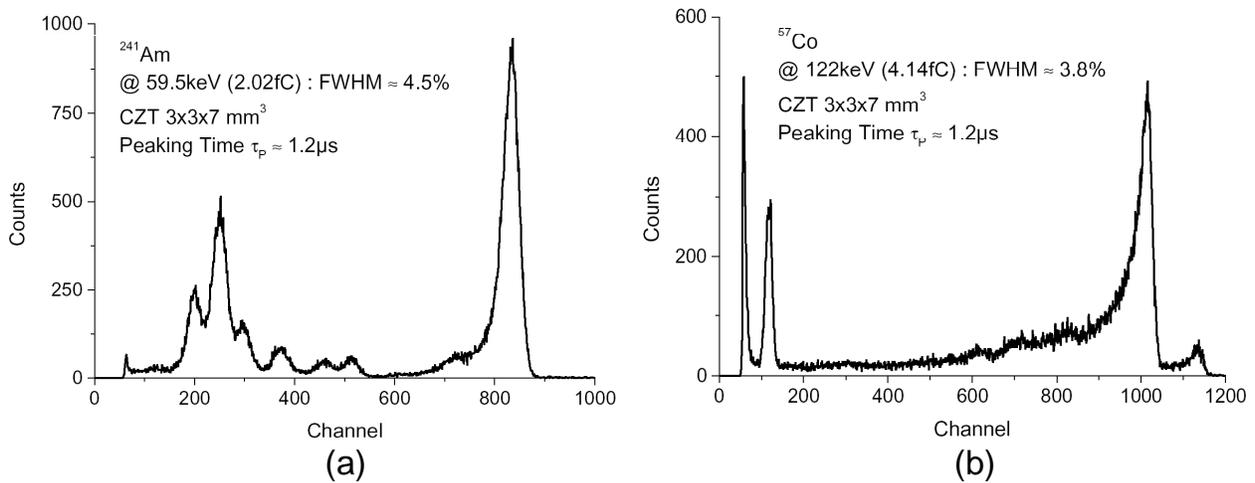


Fig. 10: Spectra taken with CZT detectors and the general-purpose ASIC. (a) ²⁴¹Am; (b) ⁵⁷Co.

2.8 Applications

Fig. 11 shows two medical applications which use the general-purpose amplifier ASICs. Fig. 11 (a) shows a prototype gamma-camera array built by eV Products. It consists of 96 CZT crystals with 32 pixels each. The 3072 signals are individually read out via 192 ASICs plus discrete logic and multiplexing to produce a serial data stream of 12-bit pixel address and 12-bit energy for each event detected by the CZT array. This array had an average FWHM of ~3.8% at 122KeV. A total of 3035 channels passed all specifications. 33 channels had high FWHM (>8%), 3 channels had low photopeak efficiency and 1 channel was electrically dead.

Fig. 11(b) shows a handheld gamma camera containing a large (34 x 34 x 5 mm) single CZT detector with 256 pixels. Readout is provided by 16 general purpose ASICs, with on-board signal processing to calculate the number of counts per pixel in a region of interest in a given time period. The system is capable of about 4.8M events/s. FWHM at 122 keV is typically 4.0%.

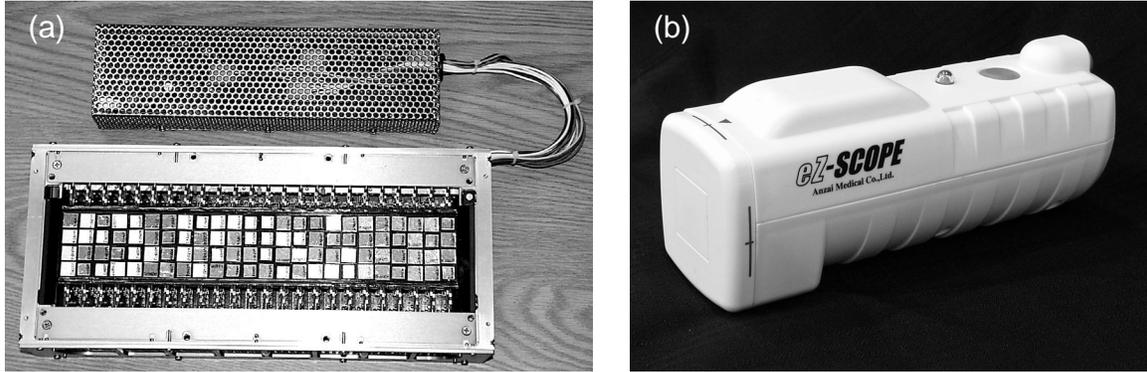


Fig. 11 Medical imaging applications using ASIC readout: (a) prototype gamma camera detector array with 3072 CZT pixels read out with 192 general purpose ASICs; (b) handheld gamma camera.

3. SAMPLING, MULTIPLEXING, AND DERANDOMIZING ASICS

Monolithic techniques can dramatically reduce the size and cost of the front-end amplifiers, enabling systems with very high channel counts to be envisioned. However, in the overall system the cost of the sampling and digitizing electronics may become dominant. The high bandwidth analog interconnects from the front-end amplifiers to the sampling and digitizing electronics can also be very costly. For all but the most cost-insensitive applications, it is essential to concentrate the analog signals near to the front ends before performing the analog-to-digital conversion. Existing approaches to sample and digitize data in high-channel-count systems are inefficient and are not optimized for applications with random pulses.

Common techniques include sample/hold or analog pipelines followed by analog multiplexing. The drawbacks are the requirement of an external trigger to define the time of occurrence of the event, the lack of sparsification, and the low speed of analog multiplexing (10 MHz max. for high accuracy systems), whereby higher multiplexing ratios lead to longer readout times. In the case of the sample/hold, deadtime during readout also limits the efficiency of data collection. The minimum requirements for a fast, efficient multiplexing readout for random pulses are:

- self-triggered sampling system with independent per-channel triggers having negligible time walk;
- sparse readout which eliminates multiplexer and digitizer cycles by detecting and skipping unoccupied channels;
- buffer “memory” (analog storage for 4 – 8 events) for derandomization.

A block diagram illustrating the idealized functionality of such a readout is shown in Figure 12. In operation, such an ASIC would function as an analog FIFO in which random pulses arrive on many input channels. A single output port provides sparsified, derandomized data consisting of peak amplitude, time, and channel address for each pulse. The on-chip logic provides an interface between the asynchronous input streams and a continuously-clocked, synchronous digitizer and data acquisition system.

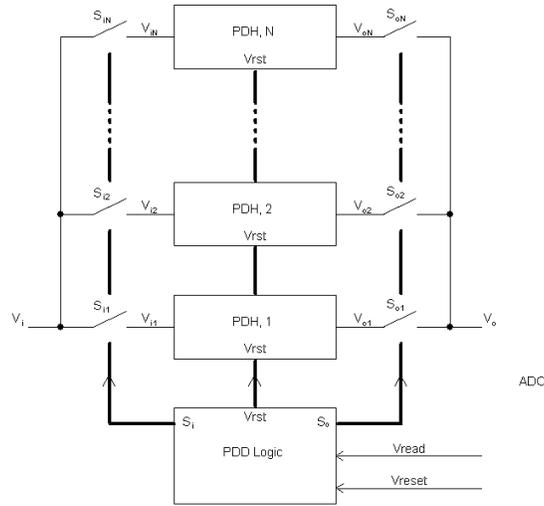


Fig. 13: Simplified schematic of the PDD for storing and derandomizing up to N samples

While one PDH is being read out, another can accept input pulses. By choosing a large enough buffer size N, we can eliminate nearly all dead time while clocking the ADC at the average event rate. The PDD1 ASIC is a realization of the circuit in Fig. 13 with $N=2$.

To test the PDD1 with realistic signals the test system shown in Fig. 14(a) was constructed. A linear array of 32 CdZnTe (CZT) detectors on 3.5 mm pitch was exposed to ^{241}Am X-rays. Two 16-channel preamplifier/shaper ASICs produced unipolar, $1.2 \mu\text{s}$ τ_p pulses which were fed into the SSM ASIC described in subsection 3.1. The SSM routes above-threshold inputs to the PDD input along with the 5-bit address of the selected channel. The PDD generates a short pulse (PK_FND) whenever a new peak is detected. In response to a READ request from the data acquisition system (pulser), the next peak sample is presented to the 12-bit ADC. A logic analyzer captures the digital PEAK and corresponding channel ADDRESS. After a fixed delay the pulser RESETs the PDD that was read out, making it available to process the next input pulse. The system shown in Fig. 14(a) consumes only about 0.8 mW per channel (excluding the pre-amp/shaper) and can fit into a PC board less than 15 cm on a side. Fig. 14(b) shows the waveforms PDD_IN, PK_FND, PDD_OUT, and READ for a typical acquisition. Note that the input pulses (and PK_FND signals) occur randomly, while the READ process is synchronous. The READ rate, 200 kHz in this example, is matched to the average input rate. Whenever a new READ is issued, PDD_OUT changes. It can be seen, for example, that the PDD detected and stored the third pulse before the second pulse was read out, demonstrating correct derandomization. Note that it would be difficult or impossible to capture the pulse train shown in Fig. 14(b) with either the track-and-hold or switched capacitor analog memory architectures, because they lack sparsification and self-triggering.

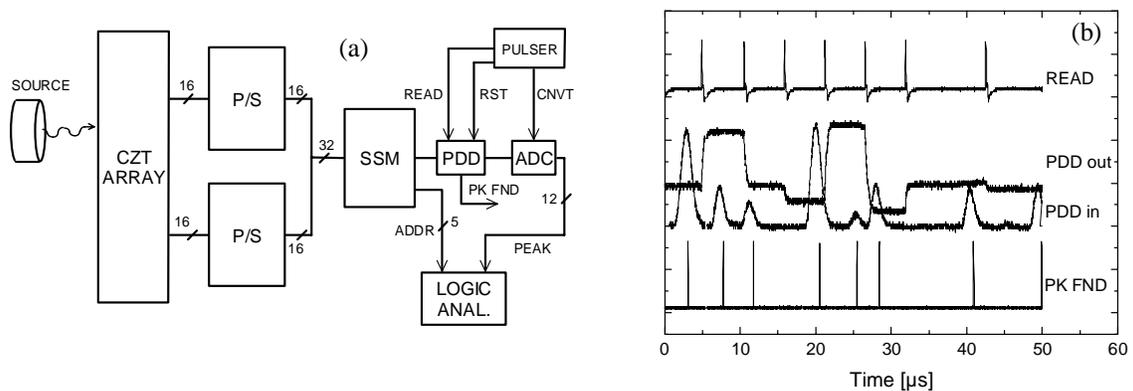


Fig. 14: (a) test setup block diagram; (b) waveforms at the input and outputs of the PDD1 ASIC.

3.3 Amplitude and Time Measurement ASIC with Analog Derandomization

A new sampling and derandomizing ASIC (PDD2) has been developed with five significant advancements over the SSM/PDD1 combination:

- single-chip implementation of the sampling, buffering, and derandomizing functions;
- improved peak detector capable of operating with fast pulses (to 50 ns peaking time);
- buffer memory cells increased from N=2 to N=8;
- 32:1 multiplexer of SSM replaced with 32:8 crosspoint switch and improved arbitration logic which reduces downtime per pulse to less than 3 ns;
- dual-mode time to amplitude converter (TAC) associated with each PD to provide timing information.

A simplified schematic that illustrates the architecture is shown in Figure 15. The ASIC consists of:

- inputs for 32 shaped, positive unipolar pulses with minimum peaking time of 50 ns;
- 32 comparators with common threshold;
- array of 8 offset-free, two-phase peak detectors with associated TACs;
- 32-to-8 crosspoint switch that can route any input channel to any PD/TAC;
- fast, nonblocking arbitration logic to control the crosspoint switch;
- output multiplexer and sequencing logic to control the readout of the PD/TACs

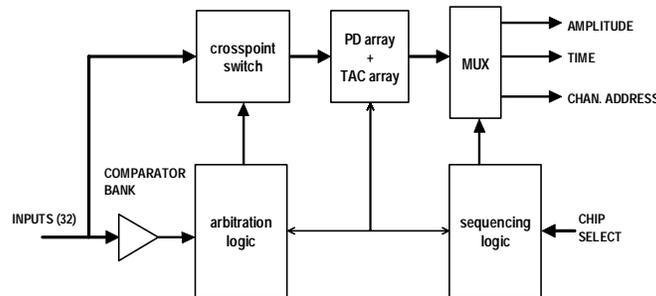


Fig. 15: Block diagram of the Amplitude and Time measurement ASIC showing the routing of the input signals to the PD/ TAC arrays.

The 32 comparators monitor the inputs for activity. When an input goes above threshold, the arbitration logic sets up a connection between that channel and the next available peak detector. The connection is maintained until the peak is found. Then the peak amplitude is stored on the PD hold capacitor until the external ADC becomes available to digitize that sample. At that time the sequencing logic presents the amplitude and time (analog) samples from the PD/TAC to the ADC along with the address of the channel where the hit occurred. Incoming pulses are not blocked as long as there is at least one PD free. The arbitration logic is based on a fast wired-or and can discriminate between comparator events from different channels occurring about 3 ns apart and prioritizes for events within 3 ns.

The TAC has a programmable measurement mode. In “risetime” mode it measures the time from the comparator firing until a peak is detected. In “time of occurrence” mode, the TAC is started when the peak is detected and stopped when the readout sequencer presents the peak sample to the output. The TAC can also be used to reject pulses based on a timing constraint. For example, this method can be used for risetime discrimination or for timing out pulses after a fixed delay. The elements of the PD/TAC array are available to any input channel; thus, resources can be allocated to highly active channels as necessary. Traditional FIFO control lines (FULL, EMPTY, DATA VALID, READ CLOCK) are available for operating the ASIC in continuously clocked, polled, interrupt-driven, or token-passing mode. In addition, an SPI compatible interface allows serial configuration of TAC gain and mode, arbitration locking, channel exclusion, powerdown, and analog monitor functions.

We performed Monte Carlo simulations of the performance of a 32-channel ASIC to be fabricated in 0.35 μm DP-4M CMOS during summer 2002. Fig. 16(a) shows the blocking probability as a function of the output/input rate ratio for 4 and 8 peak detectors. Fig. 16(b) shows blocking probability as a function of input rate for 50ns pulses at two output/input rate ratios. For readout rate of twice the pulse rate, the efficiency is excellent up to rates in excess of 1 MHz/channel.

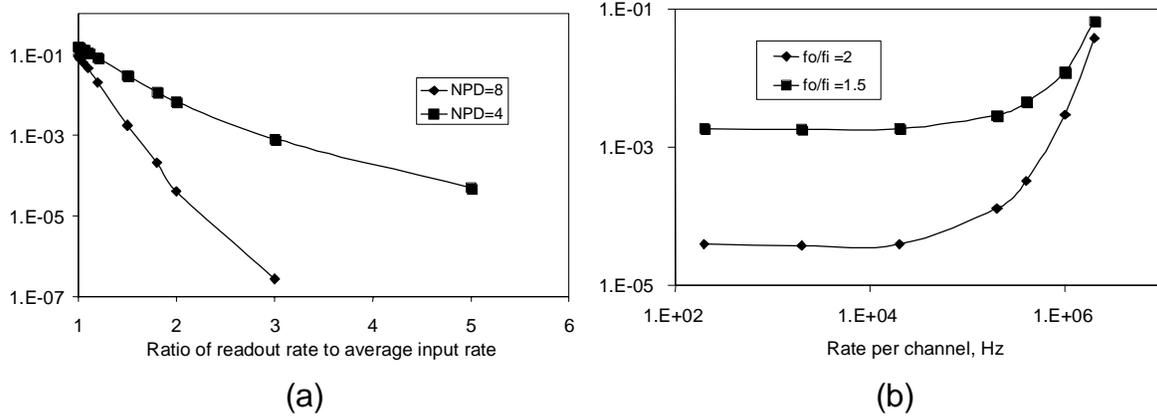


Fig. 16. Blocking probability of the PDD2 ASIC (a) as function of the ratio of readout rate to average input rate; (b) as a function of input rate.

Fig. 17 shows a 40 μs portion of a BSIM3v3.1 SPICE simulation of the circuit with pulses on 16 inputs. To simulate the signals expected in a spectroscopy experiment, the arrival times of the pulses are Poisson distributed with a mean rate of 100 kHz per channel. Amplitudes of the pulses are random, and peaking times of 50ns to 1 μs are used. The circuit responds to read requests by outputting the peak sample from each channel that was hit. Address and time of occurrence of the corresponding hit are also output.

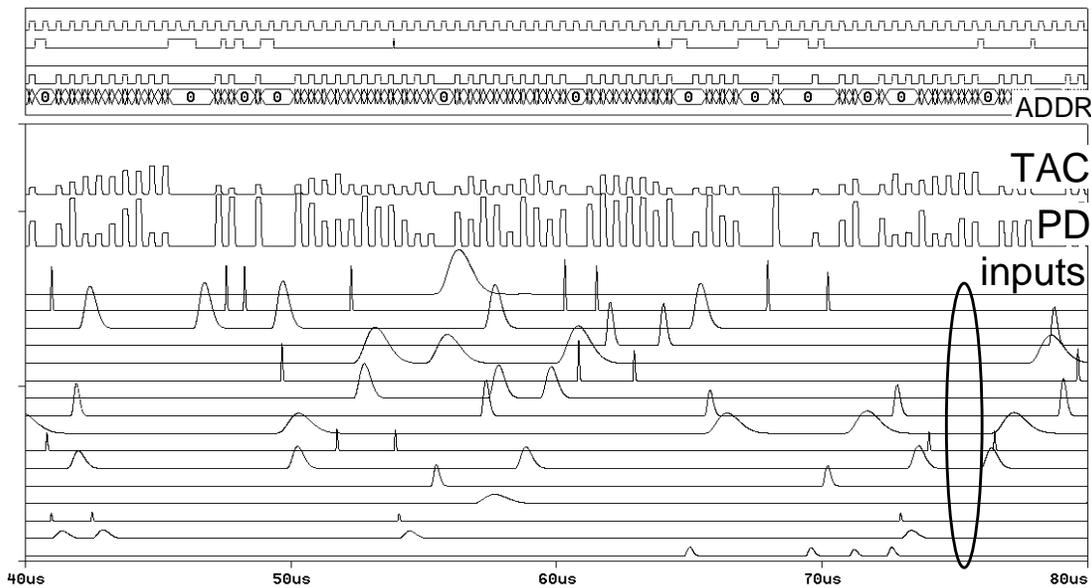


Fig. 17. Simulation of the PDD2 ASIC with 16 active inputs. Upper traces are the readout clock, EMPTY, FULL, DATA VALID, and address output. Lower traces are the input pulses and PD/TAC outputs.

4. SUMMARY

A family of ASICs for accurate and efficient readout of CZT detectors has been developed. The amplifier ASICs use new techniques of capacitance matching, compensated continuous preamplifier reset, high-order shaping, baseline holder, and full self-biasing for improved accuracy and stability. The sampling, derandomizing, and multiplexing PDD2 ASIC uses a new self-triggered, sparsifying architecture based on an innovative two-phase peak detector to enable the readout of 32 channels (amplitude and time) at up to 1 Mcps per channel with a single ADC at more than 99% efficiency. Using a combination of the amplifier and PDD2 ASICs with commercial ADCs, a complete multichannel pulse height/time measurement system with 10-bit/5 ns accuracy can be constructed with a power dissipation less than 25 mW/channel and an ASIC cost of less than \$5/channel.

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