

Amplitude and time measurement ASIC with analog derandomization¹

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Abstract

A versatile 32-channel ASIC has been developed for accurate processing of high-rate pulse signals from highly segmented detectors. In contrast to conventional approaches, this circuit affords a dramatic reduction in data volume through the use of analog techniques (precision peak detectors and time-to-amplitude converters) together with fast arbitration and sequencing logic to concentrate the data before digitization. In operation the circuit functions like a data-driven analog first-in, first-out (FIFO) memory between the preamplifiers and the ADC. Peak amplitudes of pulses arriving at any one of the 32 inputs are sampled, stored, and queued for readout and digitization through a single output port. Hit timing, pulse risetime, and channel address are also available at the output.

Prototype chips have been fabricated in 0.35 micron CMOS and tested. Amplitude accuracy of the peak detect and hold circuit is 0.2% (absolute) and 0.04% (nonlinearity) for signals within 0.3V of either supply rail. Time walk is below 5 ns, droop rate is 250 mV/s, and power consumption is less than 2 mW/channel at pulse rates up to 500 kHz per channel. © 2001 Elsevier Science. All rights reserved

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1. Introduction

There is a trend in state-of-the-art radiation detectors towards highly segmented electrodes with massively parallel readout. This move to high channel count systems has been stimulated by the development of monolithic circuits that have dramatically reduced the per-channel cost of the front-end electronics. However, the existing approaches to collect and record the data generated by these front-ends are complex and inefficient, and the cost saving at the system level is incommensurate with the advantage provided by monolithic integration. Tradeoffs between cost, complexity, accuracy, and data bandwidth are common.

The most flexible approach to data collection is to digitize the signals immediately after the preamplifier and antialiasing filter and to perform all subsequent operations (pedestal/gain correction, peak extraction, sparsification, and buffering) in the digital domain. This method requires a high rate ADC for each channel, generates a huge volume of digital data, and is generally too expensive for large systems. The alternative is to concentrate the data in analog form in front of the ADC. Common techniques include sample/hold or analog pipelines followed by analog multiplexing. The drawbacks are the requirement of an external trigger to define the time of occurrence of the event, the lack of sparsification, and the low speed of analog multiplexing. In the case of the sample/hold,

deadtime during readout also limits the efficiency of data collection.

We have developed a multichannel readout ASIC that samples, sparsifies, and buffers pulse signals without the need of an external trigger. It has been developed for spectroscopy applications with randomly occurring pulses but can also be used with interpolating position-sensing detectors. The sampling and buffering are accomplished using fast and accurate peak detector (PD) circuits in conjunction with time-to-amplitude converters (TAC) to provide pulse amplitude and timing information.

2. ASIC architecture

A simplified schematic that illustrates the architecture is shown in Figure 1. The ASIC consists of:

- inputs for 32 shaped, positive unipolar pulses with minimum peaking time of 50 ns;
- 32 comparators with common threshold;
- array of 8 offset-free, two-phase peak detectors [1] with associated TACs;
- 32-to-8 crosspoint switch that can route any input channel to any PD/TAC;
- fast, nonblocking arbitration logic to control the crosspoint switch;
- output multiplexer and sequencing logic to control the readout of the PD/TACs

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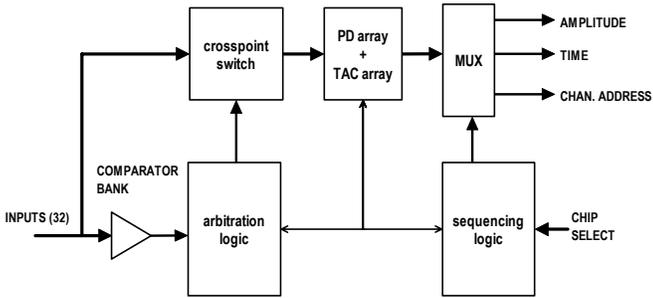


Fig. 1: Block diagram of the Amplitude and Time measurement ASIC showing the routing of the input signals to the PD/ TAC arrays.

The 32 comparators monitor the inputs for activity. When an input goes above threshold, the arbitration logic sets up a connection between that channel and the next available peak detector. The connection is maintained until the peak is found. Then the peak amplitude is stored on the PD hold capacitor until the external ADC becomes available to digitize that sample. At that time the sequencing logic presents the amplitude and time (analog) samples from the PD/TAC to the ADC along with the address of the channel where the hit occurred. Incoming pulses are not blocked as long as there is at least one PD free.

The elements of the PD/TAC array are available to any input channel; thus, resources can be allocated to highly active channels as necessary.

Traditional FIFO control lines (FULL, EMPTY, DATA VALID, READ CLOCK) are available for operating the ASIC in continuously clocked, polled, interrupt-driven, or token-passing mode. In addition, an SPI compatible interface allows serial configuration of TAC gain and mode, arbitration locking, channel exclusion, powerdown, and analog monitor functions.

3. Circuit design

3.1. Peak detector

The main building block of the system is a novel two-phase peak detector (PD) that circumvents the major sources of error of conventional configurations [1]. An analysis of the limitations of the classical CMOS PD was given in [2]. Summarizing, the two-phase approach eliminates the errors caused by amplifier offset by re-configuring the amplifier as a unity-gain follower of the voltage on the hold capacitor, while also providing strong drive capability. By canceling amplifier offset, the two-phase PD can also be designed for rail-to-rail sensing and driving. Switching between tracking and holding phases is automatic and provides a time marker with characteristics similar to that of a zero-crossing discriminator.

In the present design, the speed and accuracy of the two-phase PD were improved to allow it to process pulses with peaking times down to 50 ns. A comparison of the absolute

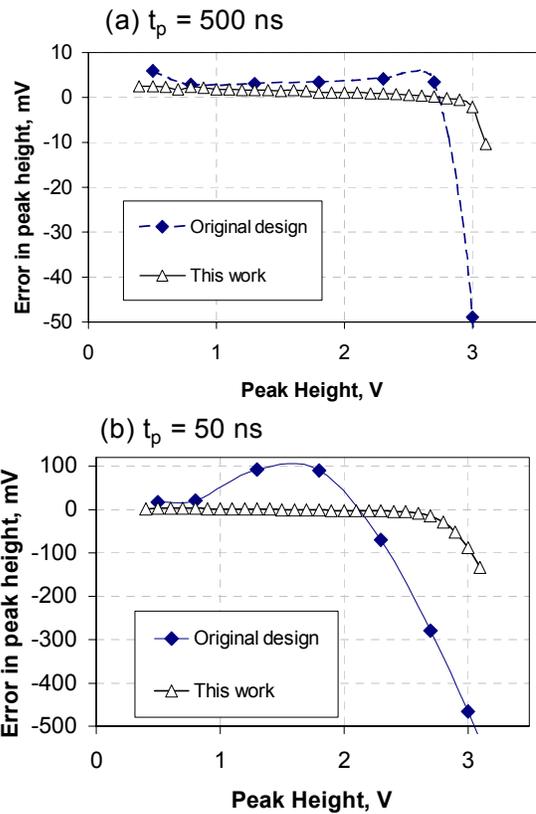


Fig. 2: Pulse height accuracy for original and new PD designs (simulated). (a) Peaking time = 500 ns; (b) peaking time = 50 ns

error in peak height for the original [1] and new designs is shown in Figure 2

3.2. Time-to-amplitude converter

Two time-to-amplitude converters (TACs) are associated with each PD. The TAC is based on a capacitor charged by a constant current source. Full scale can be varied from 0.5 to 64 μ s by means of an on-board DAC. The main TAC has two programmable measurement modes: in “risetime” mode it measures the time from comparator firing until a peak is detected, while in “time of occurrence” mode the TAC is started when a peak is detected and stopped by the readout request, allowing measurement of the hit time relative to a (known) system clock.

The secondary TAC is a time-out control, which resets the PD after a known delay. This feature prevents PDs from being locked out of the arbitration pool in case of an anomalous comparator firing. It can also be used to reject pulses based on a risetime constraint, or as a latency delay in systems with a delayed global trigger.

Time measurement accuracy of the TAC was simulated for a train of random pulses of varying width and amplitude. The linearity and residuals are shown in Figure 3.

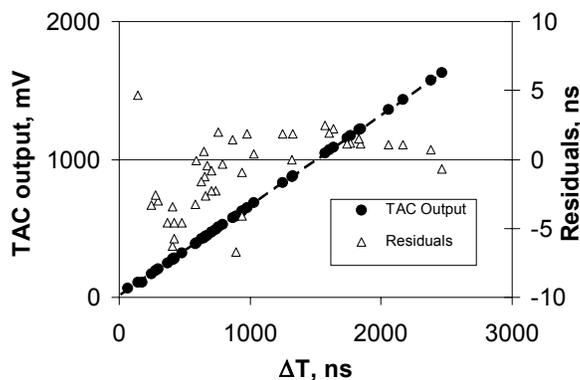


Fig. 3: Linearity of the TAC in occurrence time mode (simulated).

3.3. Arbitration logic

The arbitration logic and crosspoint switch are arrayed in a matrix of 32 rows and 8 columns. Arbitration logic is asynchronous and responds to three types of event: comparator firing, peak_found signal from the PD, and read_request from the external data acquisition system (DAQ). A fast wired-OR allows the logic to discriminate between comparator events from different channels occurring about 3 ns apart. If events arrive within 3 ns, priority is given to the lower-numbered channel and the events on the higher-numbered channels are rejected. The impact of this preferential treatment of the low-numbered channels is a small bias in favor of the lower-numbered channels. However, the bias amounts to less than 0.04% at the highest expected count rate.

In response to a read_request the amplitude, time, and channel address are presented to the DAQ in the same sequence that they were recorded.

The chip will be fabricated during summer 2002 in a 0.35 μm DP-4M CMOS process. Power consumption is expected to be less than 2 mW/channel.

4. Simulation

We performed 500000-event Monte Carlo simulations of the ASIC with randomly arriving pulses of 50 ns peaking time to determine efficiency. The inefficiency (fraction of events blocked) was recorded as a function of the ratio of the readout rate to the average input event rate. Figure 4(a) shows the blocking probability for 4- and 8-PD arrays. In Fig. 4(b) the inefficiency is given for an 8-PD array as a function of input rate, when the read_request frequency was fixed at 1.5 and 2.0 times the average event rate. For 8 peak detectors, the efficiency is excellent up to rates in excess of 1 MHz/channel. The inefficiency rises at high rates when the peaking time becomes an appreciable fraction of the average inter-arrival time.

Fig. 5 shows a 40 μs portion of a full transistor-level (BSIM3v3.1) SPICE simulation of the circuit with pulses on 16 inputs. To simulate the signals expected in a spectroscopy

experiment, the arrival times of the pulses are Poisson distributed with a mean rate of 100 kHz per channel. Amplitudes of the pulses are random, and peaking times of 50ns to 1 μs are used. The circuit responds to read requests by outputting the peak sample from each channel that was hit. Address and time of the corresponding hit are also output.

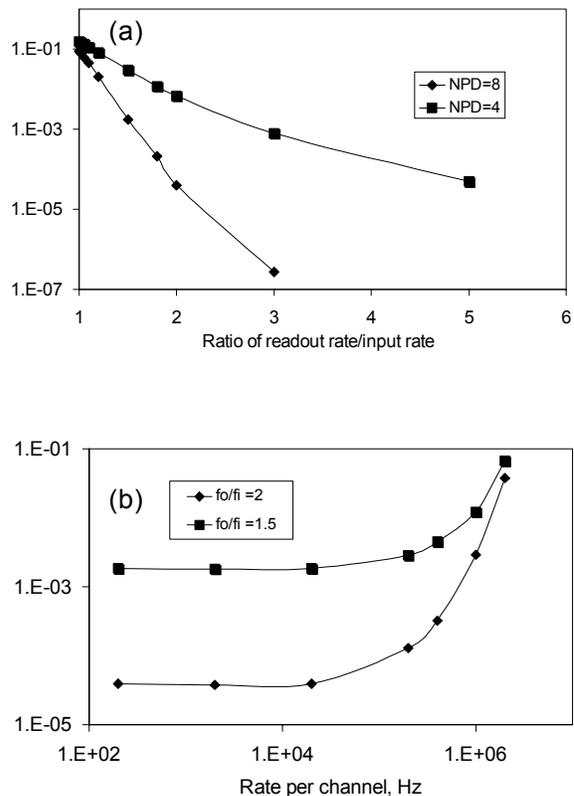


Figure 4. (a) Inefficiency as a function of the ratio of readout rate to average input rate. (b) Inefficiency as a function of average input pulse rate, for two ratios of readout rate to input rate.

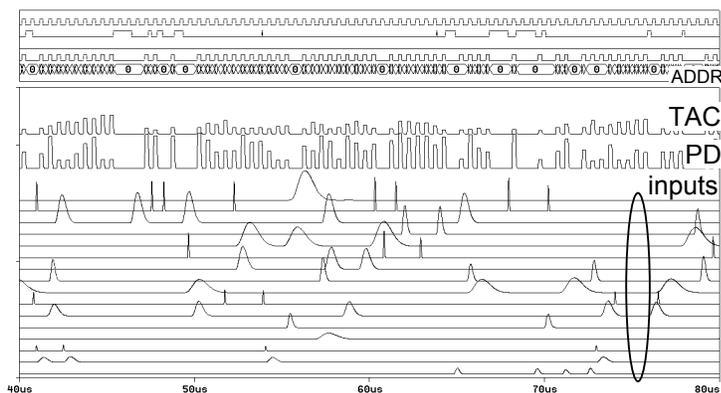


Figure 5. Simulation of the ASIC with 16 active inputs. Upper traces are the readout clock, EMPTY, FULL, DATA VALID, and address output. Lower traces are the input pulses and PD/TAC outputs.

5. Comparison with conventional readouts

Let us contrast the efficiency of the peak-detect/derandomizer (PDD) with the alternative approaches to multichannel data acquisition.

5.1. Direct digitization

Direct digitization with free-running ADCs [3,4] (waveform recording) is impractical in systems with high channel count because of the cost and power dissipation of the ADCs and the huge volume of data generated. If a trigger is available, the length of the waveform record can be reduced; but a means must be found to adjust the timing of the trigger to capture the peak of the pulse.

5.2. Sample-and-hold with analog multiplexing

The most common data-concentrating readout, the sample and hold with analog multiplexing (SH/AM) [5,6] suffers from long deadtime since it can only buffer one event. Amplifier settling time limits the maximum rate of an analog multiplexer, and so there is a design tradeoff between accuracy, multiplexing ratio, and deadtime. The other inefficiency in the SH/AM stems from the need to read out unoccupied channels, i.e. there is no sparsification until after the analog multiplexer. For a 32-channel chip with 10 MHz multiplexing, the maximum input event rate for 99% efficiency is less than 1.5 kHz per channel. Because the readout is unsparsified, 97% (31/32) of the digitized data must be eliminated in a fast digital processor.

5.3. Analog pipeline memory

Analog pipeline memory with analog multiplexing (AP/AM) [7-9] can increase the rate capability compared with the SH/AM approach by providing on-chip buffering, but the control logic to allow simultaneous read and write of the pipeline is complex. This architecture does not overcome the bottleneck of the analog multiplexer, which limits the rate. For the same channel count and analog multiplexing speed, the AP/AM can handle event rates about 6-8 times higher than the SH/AM if sufficient buffer cells are provided. Post-multiplexing data sparsification is still needed.

Inherently, neither the SH/AM nor the AP/AM circuitry generates its own sampling trigger. The SH/AM must get a HOLD strobe from either on- or off-chip, and timing errors in the strobe introduce inaccuracy in the pulse amplitude measurement because the peak is not sampled precisely. In the AP/AM the usual approach is to sample continuously, read out several samples, and interpolate the peak. This can improve accuracy at the expense of high-bandwidth sampling and more digitization.

5.4. Single peak detector per channel

In this form of readout, there is a single peak detector per channel followed by an analog multiplexer [10]. Unlike in the SH/AM, this architecture is self-triggered and provision may be made for sparse readout [11,12]. The main performance

constraint, however, is deadtime due to the lack of a derandomizing buffer as in the SH/AM. Therefore this architecture is limited to low-rate applications. Also, it requires high power consumption because the number of PDs equals the number of analog channels.

5.5. Peak detector/derandomizer

The PDD ASIC described here can operate at rates up to 300 kHz per channel with 99% efficiency. This rate capability is faster than the SH/AM and AP/AM of similar channel count by a factor of about 200 and 30 times respectively. The increased efficiency is a result of three factors:

- the shared 8-event, on-chip derandomizing buffer;
- self-sparsification which reduces the number of samples to be read out by a factor of 32; and
- reduction of the multiplexing ratio by a factor of 4, i.e. 32 channels are read out by multiplexing the outputs of 8 PD cells.

In addition, the chip generates accurate timing information without the need for an external trigger.

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