Microelectronics for Future RHIC Detectors

RHIC Detector Workshop – Nov. 13-14, 2001
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BNL
Outline

• Survey of present RHIC experiments

• Microelectronics Trends 1991 – 2001
  – CMOS scaling
  – Advances in packaging, PCB, assembly technology

• Power and Interconnect
Custom monolithic front ends

- Can be efficiently mass-produced with excellent economy of scale:
  - E.g., maskset + 10 wafers ~ $300K, 1000 chips/wafer
  - Additional wafer ~ $5K
  - Incremental cost < $10/chip
  - Chip may have 16 – 128 channels
- Can be located close to dense detector electrode arrays
  - pixels, micropattern & segmented cathode designs
- Can combine functions on single chip, replacing PCB/hybrid/cable connections with lower cost on-chip connection
- Can reduce power*
Advantages of monolithic realization

Improvement over hybrid + rack-based system:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>X 200</td>
</tr>
<tr>
<td>Power</td>
<td>X 10³</td>
</tr>
<tr>
<td>Volume</td>
<td>X 2*10⁶</td>
</tr>
</tbody>
</table>

Monolithic also adds functionality:

- cal. pulse distribution
- sample/hold
- multiplexing
Microelectronics in RHIC 2001

- **STAR**
  - TPC
    - CMOS 1.2 μm P/S, SCA, packaged
  - SVT
    - Bipolar P/S, CMOS 1.2 mm SCA, 240-channel ceramic hybrid

- **PHENIX**
  - MVD
    - 1.2 μm CMOS P/S, AMU/ADC, ceramic MCM
  - EMCAL
    - 1.2 μm CMOS integrator/VGA/TAC/sum, AMU/ADC, packaged
  - Pad chamber
    - 1.2 μm CMOS P/S/D, 1.0 μm CMOS DMU, packaged
Microelectronics in RHIC 2001 (con’t)

• PHENIX con’t.
  – Drift Chamber
    • Bipolar A/S/D, 0.8 µm CMOS TDC, packaged
  – Time Expansion Chamber
    • 1.2 µm CMOS P/S, FADC, 1.0 µm DMU packaged
  – RICH
    • 1.2 µm CMOS integrator/TAC, AMU/ADC, packaged
  – Muon tracker
    • 1.2 µm CMOS P/S, AMU/ADC packaged

• PHOBOS
  – Si pad
    • 1.2 µm CMOS (VA-HDR1 from IDE), chip-on-board
TEC Front-End Card

PHENIX TEC Front End PCB
BNL Instrumentation Div. 1998

INPUT CONNECTORS x 4

OUTPUT CONNECTORS x 2

ID Bits
RS-422 Tx

Octal Preamplifier Shaper (IC31A) 8

Octal Preamplifier Shaper (IC31A) 8

Octal Preamplifier Shaper (IC31A) 8

PWR
Power Regulators

PLD, DAC & Calibration

Fully Differential Line Drivers 16

Fully Differential Line Drivers 16

Fully Differential Line Drivers 16

PHENIX TEC Front End PCB
BNL Instrumentation Div. 1998

INPUT CONNECTORS AND GEOMETRICAL ADDRESS

ESD PROTECTION

DIFFERENTIAL LINE DRIVER (64 SIGNALS)

POWER CONDITIONING

RS-422 INTERFACE

DIGITAL CONTROL AND CALIBRATION
SVT Preamp/Shaper

Die Layout

Output Waveform
SVT 240-channel multi-chip module

Microelectronics in RHIC 2001 – Summary

• Monolithics are used to read out all detector types:
  – Semiconductor
  – Gas avalanche
  – Scintillator/PMT

• About 0.5M channels instrumented with monolithic electronics

• About 17 custom chips have been developed

• Designs done by national laboratories (13), university groups (2), industry (3)
Custom Monolithics – technology options

- **Standard CMOS**
  - Highest integration density
  - Suitable for most analog designs (low voltage issues for deep submicron)
  - Best for combining analog and digital
  - Widely available
  - Short life cycle (2 years/generation)

- **Bipolar**
  - Workhorse of “old” analog
  - Limited vendor availability
  - Speed/power advantage over CMOS (diminishing)
  - Low integration density

- **BiCMOS**
  - Complex process, expensive

- **SiGe**
  - Increasing use driven by RF circuits
  - Interesting for high frequency work

- **Silicon on insulator (SOI)**
  - Modest speed advantage for digital
  - Drawbacks for analog
  - Rad-hard

- **GaAs**
  - Digital, RF only
CMOS layout examples

Analog

Digital
CMOS Scaling

- Driven by digital VLSI circuit needs
- Goals: in each generation:
  - 2X increase in density
  - 1.5X increase in speed
  - Control short-channel effects, threshold fluctuation
  - < 1 failure in $10^7$ hours
# CMOS Technology Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>85</th>
<th>88</th>
<th>91</th>
<th>94</th>
<th>97</th>
<th>00</th>
<th>02</th>
<th>04</th>
<th>07</th>
<th>10</th>
<th>13</th>
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<tbody>
<tr>
<td>Min. feature size [µm]</td>
<td>2</td>
<td>1.5</td>
<td>1.0</td>
<td>0.7</td>
<td>0.5</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.10</td>
<td>0.07</td>
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<tr>
<td>Gate oxide [nm]</td>
<td>44</td>
<td>33</td>
<td>22</td>
<td>16</td>
<td>11</td>
<td>7.7</td>
<td>5.5</td>
<td>4.0</td>
<td>2.9</td>
<td>2.2</td>
<td>1.6</td>
</tr>
<tr>
<td>Power supply [V]</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5/3.3</td>
<td>3.3</td>
<td>2.5</td>
<td>1.8</td>
<td>1.2</td>
<td>1</td>
<td>.7</td>
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<tr>
<td>Threshold voltage [V]</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
<td>0.45</td>
<td>0.4</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
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</table>
IBM Cu-11 Process (Blue Logic)

- $L_{eff} = 0.08 \, \mu m$, $L_{cham} = 0.11 \, \mu m$
- Up to 40 million wireable gates
- Trench capacitor embedded DRAM with up to 16 M\text{b} per macro
- Dense high-performance, compatible SRAMs
- Power supply: 1.2 V with 1.5 V option
- I/O power supply: 3.3 V (dual oxide option)/
  2.5 V (dual oxide option)/ 1.8 V/1.5 V
- Power dissipation of 0.009 \mu W/MHz/gate
- Gate delays of 27 picoseconds (2-input NAND gate)
- Seven levels of copper for global routing
- Low-k dielectric for high performance and reduced power and noise
- HyperBGA (flip chip): 2577 total leads
Technology features for low-noise analog circuits

- High $g_m/C_{gs}$ ratio ($f_T$)
- Low $\gamma$ ($\gamma = g_m \times R_n$)
- Low 1/f noise
- High input impedance device
- High $g_m/g_d$
- Controllable sub-nA current sources
- High-quality floating capacitor
- Good switch device
- Excellent AC isolation
- High supply voltage
- ESD-tolerant
- Radiation-tolerant

Color key:
- improvement with scaling
- no improvement expected
- degradation with scaling
Noise and power vs. scaling

4 detector scenarios for scaling study

<table>
<thead>
<tr>
<th>System</th>
<th>$C_{det}$</th>
<th>$t_s$</th>
<th>$P$</th>
<th>$L_{min}$</th>
<th>Detector</th>
<th>Typical Application</th>
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<tr>
<td>a</td>
<td>30</td>
<td>75</td>
<td>10</td>
<td>0.001</td>
<td>Wire Chamber</td>
<td>Tracking, Imaging</td>
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<tr>
<td>b</td>
<td>15</td>
<td>25</td>
<td>0.2</td>
<td>10</td>
<td>Si Strip</td>
<td>Tracking</td>
</tr>
<tr>
<td>c</td>
<td>0.3</td>
<td>25</td>
<td>0.02</td>
<td>1</td>
<td>Si Pixel</td>
<td>Tracking</td>
</tr>
<tr>
<td>d</td>
<td>3</td>
<td>2500 – 500*</td>
<td>10</td>
<td>0.01</td>
<td>Semiconductor</td>
<td>Spectroscopy</td>
</tr>
</tbody>
</table>

UNITS: pF, ns, mW, nA

Noise vs. scaling (power held constant)

Power vs. scaling (noise held constant)
Dynamic range vs. scaling
Gate tunneling current

- Gate current expected to increase 100 – 200 x per generation below 0.18 \( \mu \)m.
- \( J_{ox} \approx 100 \text{ A/cm}^2 \) projected for \( L_{min} = 0.1 \) \( \mu \)m generation with nitrided \( \text{SiO}_2 \).
- Considered tolerable for digital circuits (total gate area per chip \( \approx 0.1 \text{ cm}^2 \)).
- Typical CSA input FET would have \( I_G \approx 1 - 10 \) \( \mu \)A; \( ENC_p \approx 2000 - 7000 \) rms e- at 1 \( \mu \)sec.

SiO\(_2\) gate leakage current (Lo et al., Electron Dev. Letters 1997)
Monolithics in scaled CMOS

- **Analog:**
  - Noise limits not changing significantly
  - Power can be reduced
  - Design effort required for high dynamic-range systems
  - Increased integration density, but not as much as digital
- **Digital:**
  - Big increase in integration density
  - Reduction in power
  - Big increase in clock frequency
  - Need to manage design complexity
- **Analog/digital co-existence**
  - Simulation capability limited
  - Anticipate the need to iterate
Power

Example: CMS Tracker

- Total # channels: 75,500 FE chips x 128 = ~10M
- Power/FE: 2.3 mW/channel
- Pwr/ch data TX: ~0.6 mW/channel
- Supply: 2.5 V and 1.25 V, $P_{tot} = ~30$ kW
- Total FE currents: $IDD_{125}: \sim 7.5$ kA, $IDD_{250}: \sim 6.5$ kA
- Remote supplies
- # of service cables: 1,800
- Power in the cables: > 75 kW
- Cross section of power cables and cooling pipes directly proportional to power dissipated!
Interconnect: Technology

• Significant advances in packaging, PCB, assembly technology
  – Thin- and fine-pitch leaded SMT components; BGAs; chip-scale packages; packages with low thermal resistance
  – Flip-chip and chip-on-board assembly
  – Microvias, thin-core laminates, flex for high density integration (HDI)
  – Passive component miniaturization, arrays
Cellular telephone handset trends

• **1991 cell phone**
  - ¼ pound
  - 12V battery
  - 700 components
  - 8 hrs assembly time
  - $600

• **2001 cell phone**
  - 2 oz.
  - 3V battery
  - 4 –5 modular components + passives integrated in substrate
  - 15 minute assembly time
  - < $150 or free

![Graph showing trends in cell phone weight over time.](image)

*Figure 4 - Capacitors Ranging from 1206, 0805, 0603, 0402 and 0201*

![Image of a wrist camera.](image)

This is the world's first WRIST CAMERA. It features 1 MB of memory to hold up to 100 images.
Standard packages of 2001

National microSMD
1.41 x 1.67 x 0.85mm body size (8L)
“Silicon Dust”

Amkor thin BGA

Stacked chip-scale package
Interconnect issues in monolithic front ends

- Detector $\rightarrow$ preamplifier
  - Lowest possible capacitance
  - Ease of assembly
  - Diagnostics
  - Repair/rewire
- Front end $\rightarrow$ ADC
  - Efficient use of expensive “analog” interconnect
- ADC $\rightarrow$ off-detector processing
  - Efficient use of bandwidth for cost/power control
- System-level power distribution
Detector-preamplifier connection can’t be designed after-the-fact!
Cost of interconnect

Relative Interconnect Cost

Distance From Chip Center (m)

- Analog
- Digital

IC, PKG, Box, PCB, Network
Summary

• RHIC detector upgrade programs can take advantage of a decade of progress in microelectronics.

• Up-front attention to power and interconnect issues is essential (avoid cable/connector/cooling problems after installation):
  – Look for opportunities to save power at all levels:
    • Technology
    • Circuit topology
    • Architecture
    • Algorithms
    • Data compression
  – For matrix-type detectors, design readout plane together with FEE
  – Maximize the use of on-chip interconnect
    • Don’t transfer analog data from chip-to-chip
    • Zero-suppress on-detector
    • Make efficient use of data transmission channel off-detector