Advanced Readout ASICs for Multi-Element CdZnTe Sensors

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Outline

• **Front-end ASICs**
  • input MOSFET optimization
  • self-adaptive continuous reset of the preamplifier
  • high order shaping
  • output baseline stabilizer (BLH)
  • summary of the first generation

• **Data-concentration ASICs**
  • two-phase peak detector
  • derandomization process
  • the 32-channel prototype
    • high reliability
    • high stability
    • ease of use (plug & play)
    • spectroscopic quality
    • data concentration optimization
The BNL-eV cooperation

• Started in September 1997

• First 4 channel front-end ASIC prototype available in April 1999

• As of Jun 2002:
  • four front-end ASICs completed (three in production)
    • number of channels (4 - 16)
    • gain (30 - 240 mV/fC, settable)
    • speed (unipolar/bipolar shaping, 0.2 - 4 µs peaking time, settable)
    • input MOSFET (matching 3 or 12 pF input capacitance)
  • one 32-channels arbitration - multiplexing mixed-signal ASIC completed
  • one 32-channels arbitration - peak detection - derandomizing - multiplexing mixed-signal ASIC prototype under development (in fabrication)
Preamplification and processing of signals from CZT

- high reliability
- ease of use
- spectroscopic quality
- data concentration optimization

CZT pixel
charge preamplifier
reset
high-order shaper
baseline stabilizer
amplitude and timing extractor
back-end processing & data concentration
to external ADC
Input MOSFET optimization

\[ ENC^2 = A_1 \tau_p \left( \frac{C_p + C_i + C_g}{g_m} \right)^2 + A_2 A_f \left( C_p + C_i + C_g \right)^2 + \frac{A_3}{\tau_p} \left( I_p + I_{rst} \right) \]

\( g_m, C_g, A_f \), are functions of input MOSFET width \( W \) and power \( P \)
Input MOSFET optimization

\[ C_g \approx \left( C_{ox}L + C_{ov} \right) \cdot W \]

\[ A_f \approx K_f / \left( C_{ox}L \cdot W \right) \]
Input MOSFET optimization

Technology
- 0.50µm
- 0.35µm
- 0.25µm
- 0.18µm

n-channel MOSFET, $\tau_P = 1\mu s$, $C_p + C_i = 3pF$

ENC [rms e] vs Power $P$ [W]

$C_g / (C_p + C_i)$ vs Power $P$ [W]
Input MOSFET optimization

- Power $P$
  - $100\mu W$
  - $1\text{mW}$
  - $10\text{mW}$

- FWHM
  - $\text{FWHM}_{\text{CzT}}$ [eV]

- $C_g / (C_p + C_i)$

- n-channel MOSFET, 0.5µm technology, $\tau_p = 1\mu s$
Input MOSFET optimization

g_m and r_o are functions of Vds
Continuous reset of the preamplifier

- L/W>>1, strong inversion, saturation
- $V_{gr}$
- $\frac{1}{N} \times I_p$
- $\frac{1}{N} \times Q$
- $\frac{1}{N} \times M_f$
- $\frac{1}{N} \times C_f$

- Current gain equal to $N$
- Fully linear
- **Self-adapts** to leakage current
- Minimum noise contribution

1st stage of shaper
Continuous reset of the preamplifier

\[
\frac{2kT}{R_s} \frac{1}{N^2} \equiv q \cdot I_{eq} \quad \text{Rs} \approx 100k\Omega \rightarrow I_{eq} \approx 1nA
\]

Rs \approx 100kO \rightarrow I_{eq} \approx 25pA
Continuous reset of the preamplifier

Channel integral linearity error [%] vs Injected charge [fC]

- $\tau_p = 1\mu s$
- Gain $= 200\text{mV/fC}$
- $C_{\text{load}} = 200\text{pF}$
- $C_p + C_i = 1.5\text{pF}$
- $I_p = 1\text{nA}$

Output vs pixel leakage current

- $C_p + C_i = 3\text{pF}$
- $Q = 11\text{fC}$
- Gain $= 200\text{mV/fC}$
- $I_p = 250\text{pA} \div 70\text{nA}$
High order shaping

\[ \text{ENC}^2 = \alpha A_W \tau_W \left( \frac{C_p + C_i + C_g}{g_m} \right)^2 + \ldots \]

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<thead>
<tr>
<th>$5^{\text{th}} \text{ cpx}$</th>
<th>1</th>
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</thead>
<tbody>
<tr>
<td>$5^{\text{th}}$</td>
<td>1.24</td>
</tr>
<tr>
<td>$2^{\text{nd}}$</td>
<td>2.64</td>
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</table>
Output baseline stabilizer

- High-order shaper
- Low-frequency low-pass filter
- x100
- Differentiator
- Vref
Output baseline stabilizer

Transfer function

Performance at high rate

Channel Gain [Ω]

Frequency [Hz]

Channel Output [V]

Time [s]

Transfer function performance at high rate

peaking time = 400ns, rate = 20kHz - 500kHz
First generation of front-end ASICs

other features

- plug & play
- per-channel test capacitor
- programmable gain
- programmable peaking time
- high output drive capability
- high stability vs temperature

\[ C_p+C_i \approx 1.5\text{pF} \]
\[ Q \approx 12\text{fC} \]
\[ \text{Gain} = 200\text{mV/fC} \]
\[ T \approx -30\text{°C} \text{ to } +50\text{°C} \]
The first generation of front-end ASICs

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</thead>
<tbody>
<tr>
<td>General purpose</td>
<td>3</td>
<td>16</td>
<td>0.6, 1.2, 2.0, 4.0</td>
<td>30, 50, 100, 200</td>
<td>18</td>
<td>30+20/pF</td>
<td>LFOV Gamma Camera SFOV Gamma Camera Nuclear Safeguards</td>
</tr>
<tr>
<td>Medium speed</td>
<td>3</td>
<td>4</td>
<td>0.4</td>
<td>200</td>
<td>18</td>
<td>29+27/pF</td>
<td>Down Hole Well Logging X-Ray Diffraction Gauges</td>
</tr>
<tr>
<td>High speed bipolar</td>
<td>3</td>
<td>8</td>
<td>0.2</td>
<td>240</td>
<td>18</td>
<td>42+44/pF</td>
<td>Bone Densitometry Pulse Mode CT Industrial X-Ray</td>
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<tr>
<td>High capacitance</td>
<td>12</td>
<td>8</td>
<td>0.6, 1.2, 2.0, 4.0</td>
<td>30, 50, 100, 200</td>
<td>35</td>
<td>57+10/pF</td>
<td>Industrial Strip Detectors Backscatter Gauges Large Area Detector</td>
</tr>
</tbody>
</table>

Technology: 0.5µm CMOS SP3M
CZT – ASIC spectra measurements

**241Am spectrum**

- FWHM $\approx 4.5\%$ at 59.5keV
- CZT 3x3x7 mm$^3$
- Peaking Time $\tau_p \approx 1.2\mu$s

**57Co spectrum**

- FWHM $\approx 3.8\%$ at 122keV
- CZT 3x3x7 mm$^3$
- Peaking Time $\tau_p \approx 1.2\mu$s
CZT – ASIC spectra measurements

$^{241}$Am spectrum

- detector thickness 3mm
- detector bias -600V
- resolution 4.3% at 59keV
- gain 200mV/fC
- peaking time 1.2µs

$^{57}$Co spectrum

- detector thickness 3mm
- detector bias -600V
- resolution 3.5% at 122keV, 21.8% at 14keV
- gain 200mV/fC
- peaking time 1.2µs
CZT – ASIC applications

**Solstice Gamma camera**

- 96 CZT crystals
- 3072 pixels
- 196 front-end ASICs
- 1.3M events/second
- average FWHM 3.8% at 122keV

**eZ-SCOPE hand held Gamma camera**

- 1 CZT crystal
- 256 pixels
- 16 front-end ASICs
- 4.8M events/second
- average FWHM 4.0% at 122keV
CZT – ASIC applications

Bone Densitometry – GE Lunar Detector

- 16 CZT crystals
- 16 pixels 3 x 7 x 3 mm³
- 2 front-end ASICs
- DEXA (Dual Energy X-ray Absorptiometry)
- ASICs replaced 17 circuit boards (over 500 components) and improved performances
Pulse amplitude extraction: classical CMOS configurations

**Sample/hold**

- Timing signal needed
- Switch charge injection
- Poor drive capability
- Deadtime until readout
- Power dissipation

**Peak detect/hold (PDH)**

- Accuracy impaired by op-amp offsets and CMRR
- Poor drive capability
- Deadtime until readout
- Self-triggered
- Timing signal
The two-phase PDH concept

**Write phase**
- behaves like classical configuration

**Read phase**
- op-amp re-used as buffer
- **offset** and CMMR **errors canceled**
- enables **rail-to-rail** sensing
- good **drive capability**
- **self-switching** (peak found)
Two-phase PDH: offset cancellation

chip 1 – negative offset

chip 2 – positive offset
Two-phase PDH: performance

<table>
<thead>
<tr>
<th>Parameter:</th>
<th>Value: PDDv1 (PDDv2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 um CMOS DP4M</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3V</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>0.3 - 3.0 V</td>
</tr>
<tr>
<td>Minimum peaking time</td>
<td>500 (50) ns</td>
</tr>
<tr>
<td>Absolute accuracy</td>
<td>&lt; 0.20%</td>
</tr>
<tr>
<td>Linearity</td>
<td>&lt; 0.05%</td>
</tr>
<tr>
<td>Droop rate</td>
<td>250 mV/s</td>
</tr>
<tr>
<td>Timing accuracy</td>
<td>5 ns</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>3.5 (2.0) mW/ch</td>
</tr>
</tbody>
</table>

![Graph showing absolute accuracy of PDDv1](image)

PDDv1: absolute accuracy
Derandomization with N two-phase PDHs (PDD)

-measured derandomization
(M=16, N = 2)

-ADC

-M front-end channels

-N two-phase PDH

-output MUX

-arbitration logic & crosspoint switch
Derandomization efficiency vs N

The larger is $N$, the lower can be the $fo/fi$ ratio.

$fo/fi = \text{ADC rate} / \text{average input rate}$

$\tau_p = 50\text{ns}$, $fi = 3.2\text{MHz}$

The larger is $N$, the lower can be the $fo/fi$ ratio.
Derandomization efficiency and TAC linearity

**Blocking Probability**

- $\text{fo/fi} = 2$
- $\text{fo/fi} = 1.5$

**TAC Linearity**

- TAC output, mV
- Residuals, ns

Rate per channel, Hz

- $1 \times 10^2$
- $1 \times 10^4$
- $1 \times 10^6$
32-channels PDD ASIC

- One-chip solution
- $N_{\text{CHAN}} = 32$, $N_{\text{PD}} = 8$
- Dual-mode TAC
  - risetime
  - time of occurrence
- Amplitude, address, timing outputs
- 50 ns minimum pulsewidth
- $t_{\text{ARB}} \sim 5$ ns
- Rate capability $\sim 10$ MHz
- SPI interface:
  - serial configuration of TAC gain and mode
  - arbitration locking
  - channel exclusion
  - powerdown
  - analog monitor
  - Digital convenience outputs (used for configuring companion amplifier chip)
- FIFO-like control and readout interface
32-channels PDD ASIC: layout

- Size: 3.2 x 3.2 mm²
- Power: 2mW / channel
- Technology: 0.35µm CMOS DP4M
Summary

• A generation of high-performance **front-end ASICs** has been developed
  • advanced circuit solutions
  • high reliability, stability, ease of use
  • produced in large quantity
  • implemented in products commercialized by eV

• A generation of **data concentration ASICs** is being developed
  • based on a high-performance peak detector of novel concept
  • self-triggering, multiplexing, derandomizing, sparsifying
  • providing amplitude, timing and address information per event
  • a 32-channels, 8 PDs, 10MHz prototype is in fabrication