# Monolithic CMOS Detectors for Tracking and the Sticky Photo-Gate

Wieman
RNC
LBNL
9-Feb-2005

# Things to cover

- Brief report on the STAR Heavy Flavor Tracker program, an inner vertex detector to use monolithic CMOS pixel detectors
- Some work on a photo-gate, an attempted improvement on the CMOS pixels

# Cover page from proposal just submited to STAR managment

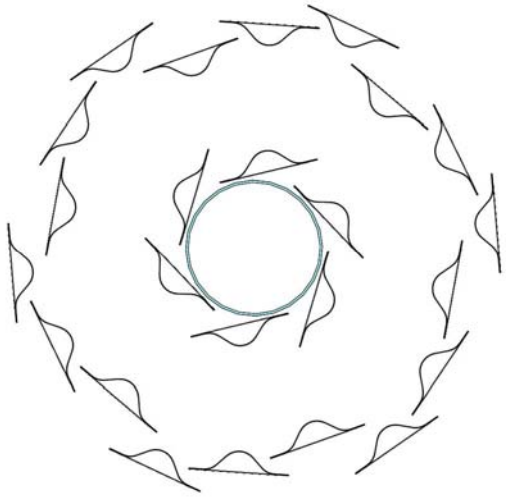
**A Heavy Flavor Tracker for STAR**

Z. Xu
Brookhaven National Laboratory, Upton, New York 11973
Y. Chen, S. Kleinfelder, A. Koohi, S. Li
University of California, Irvine, California
H. Huang, A. Tai
University of California, Los Angeles, California 90095
V. Kushpil, M. Sumbera
Nuclear Physics Institute AS CR, 250 68 Rez/Prague, Czech Republic
C. Colledani, W. Dulinski, A. Himmi, C. Hu, A. Shabetai, M. Szelezniak, I. Valin, M. Winter
Institut de Recherches Subatomique, Strasbourg, France
M. Miller, B. Surrow, G. Van Nieuwenhuizen
Massachusetts Institute of Technology, Cambridge, MA 02139
F. Bieser, R. Gareus, L. Greiner, F. Lesser, H.S. Matis, M. Oldenburg, H.G. Ritter, L. Pierpoint, F. Retiere, A. Rose, K. Schweda, E. Sichtermann, J.H. Thomas, H. Wieman, E. Yamamoto
Lawrence Berkeley National Laboratory, Berkeley, California 94720
I. Kotov
Ohio State University, Columbus, Ohio 43210

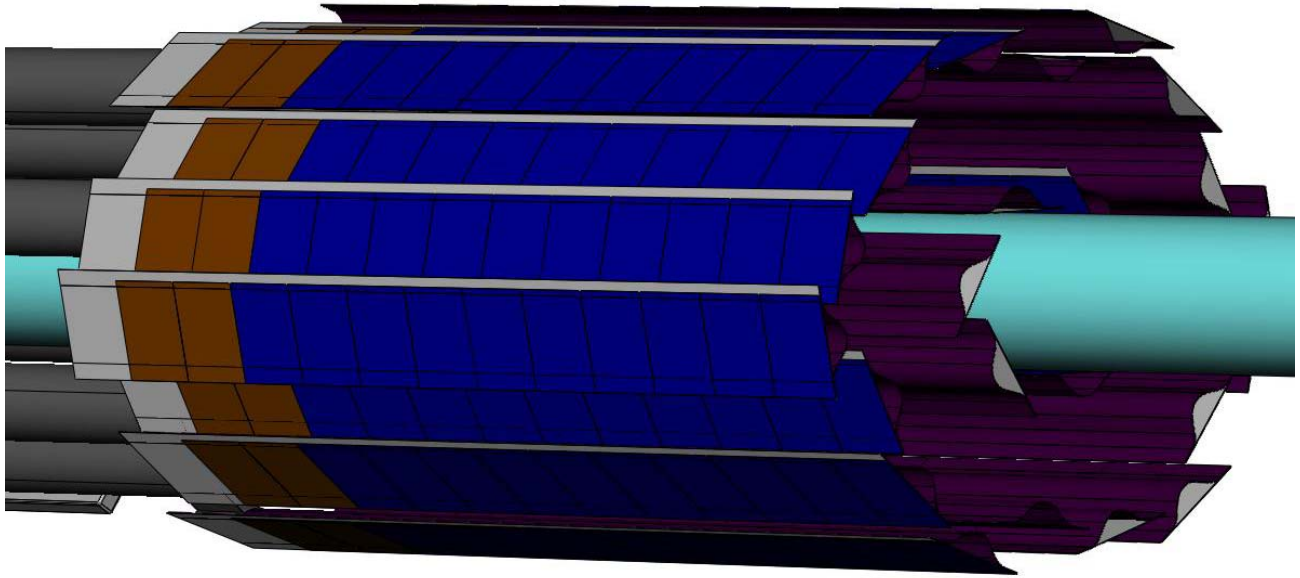
(The contributing authors to this proposal, listed above, gratefully acknowledge the support of their funding agencies.)

# STAR Micro Vertex Detector

- Two layers
  - 1.5 cm radius
  - 4.5 cm radius
- 24 ladders
  - 2 cm X 20 cm each
  - < 0.3% $X_0$
  - ~ 100 Mega Pixels



**Purpose:**
**Greatly improve D meson capability in STAR**



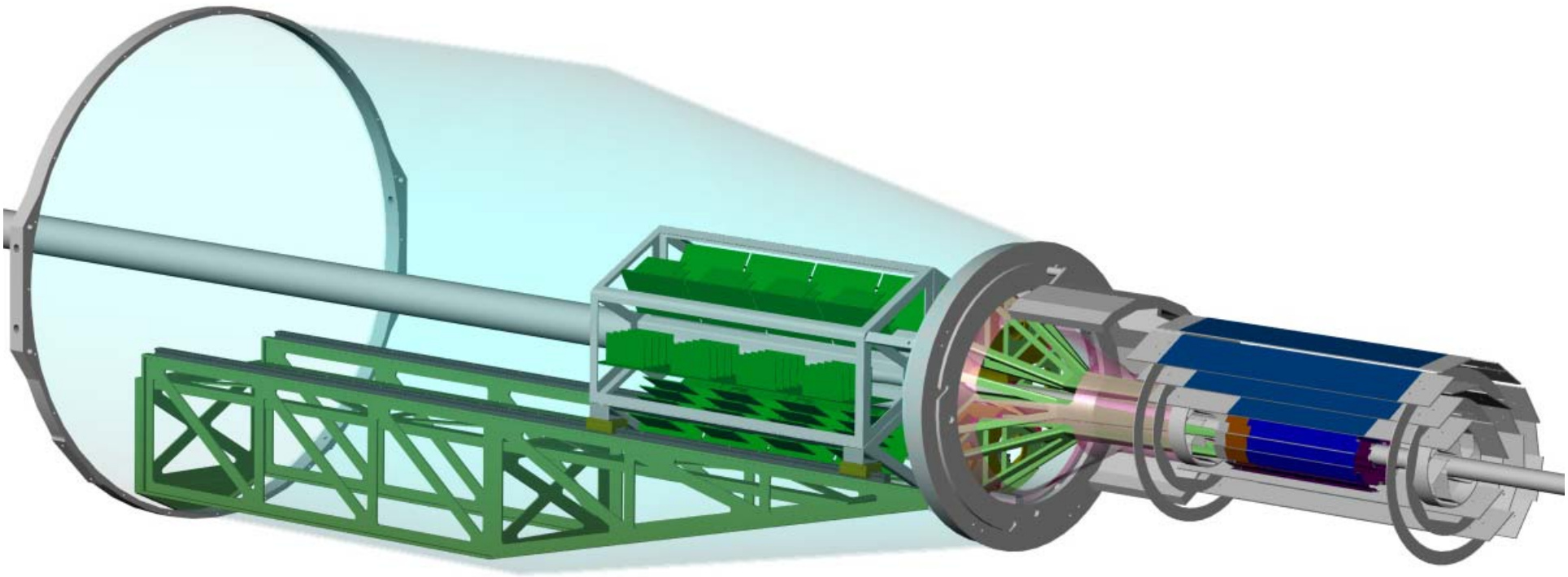
# Selected Detector Parameters and Specifications

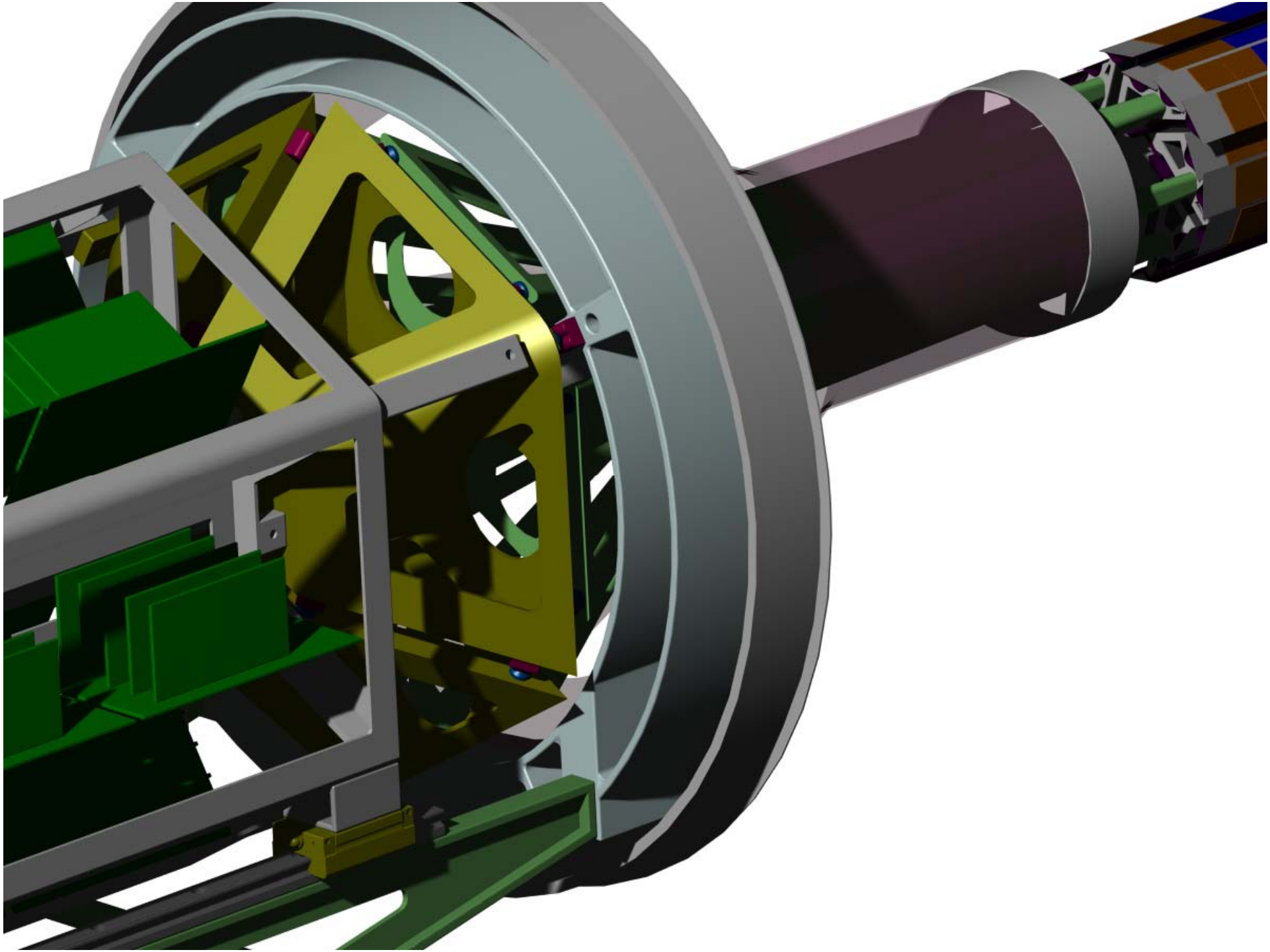
| | |
|---|---|
| Min I efficiency | 98% |
| Accidental rate | < 100 /cm$^2$ |
| Position resolution | < 10 $\mu$m |
| Number of pixels | 98,304,00 |
| Pixel dimension | 30 $\mu$m $\times$ 30 $\mu$m |
| Detector chip active area | 19.2 mm $\times$ 19.2 mm |
| Detector chip pixel array | 640 $\times$ 640 |
| Number of ladders | 24 |
| Ladder active area | 192 mm $\times$ 19.2 mm |
| Number of barrels | 2 |
| Inner barrel (6 ladders) | r = 1.5 cm |
| Outer barrel (18 ladders) | r = 4.5 cm |

# Selected Detector Parameters and Specifications

| | |
|---|---|
| Frame read time | 4 ms |
| Pixel read rate, after zero suppression | 63 MHz |
| Ladder % $X_0$ | 0.26% |
| Cooling | Room temperature air, 1 m/s |
| Power | 100 mW/cm$^2$ |
| | |

# Conceptual mechanical design

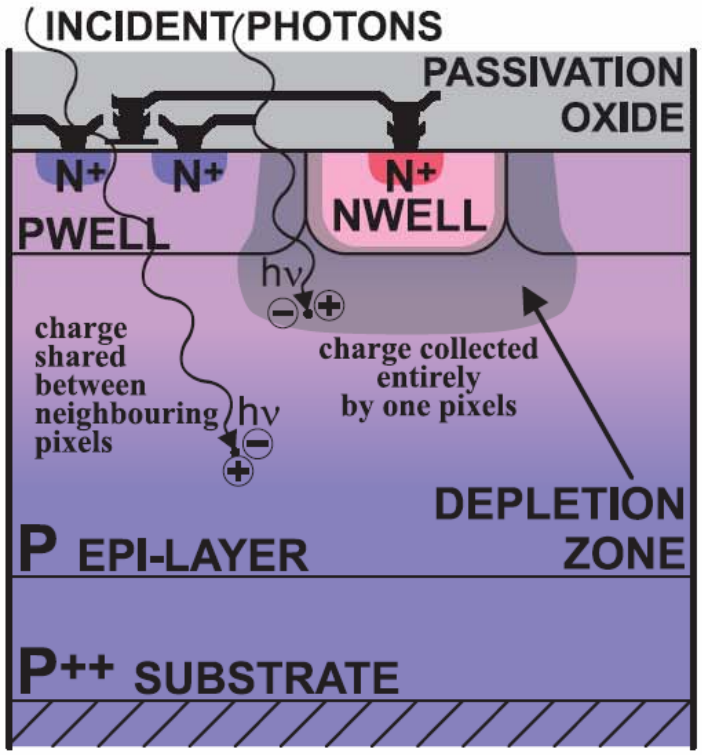




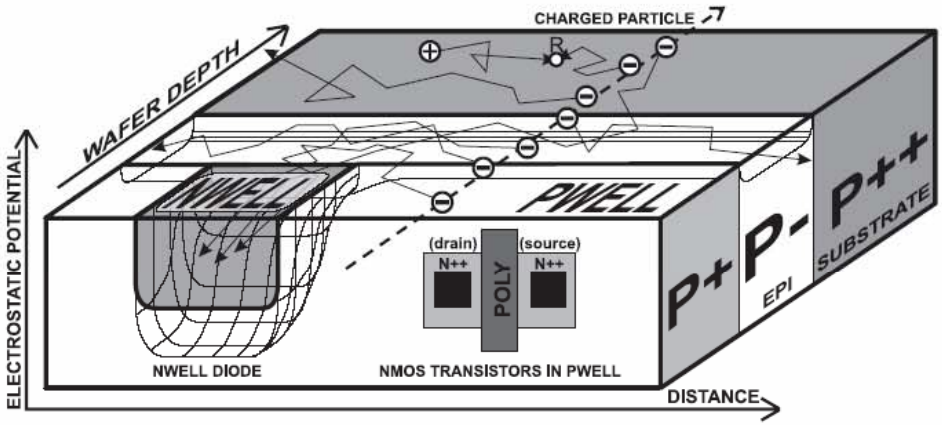
Grzegorz DEPTUCH
deptuch@lepsi.in2p3.fr

# ☑ Operation Principle of CMOS Sensors for Particle Detection

- In visible light CMOS cameras, moderately doped epitaxial layer provides long minority carrier lifetime ...




- Charge generated in non-depleted region collected through thermal diffusion (or it recombines…) ...

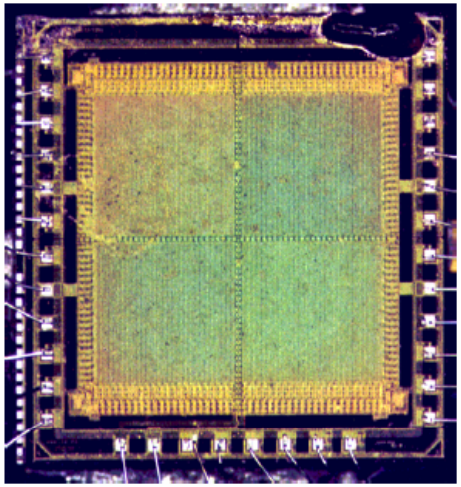



- Potential barriers at layer interfaces confine the charge - improving collection efficiency ...
- Active volume underneath the readout electronics ⇨ **100% fill factor**; charge collected by deep n-well/p-epi diode.

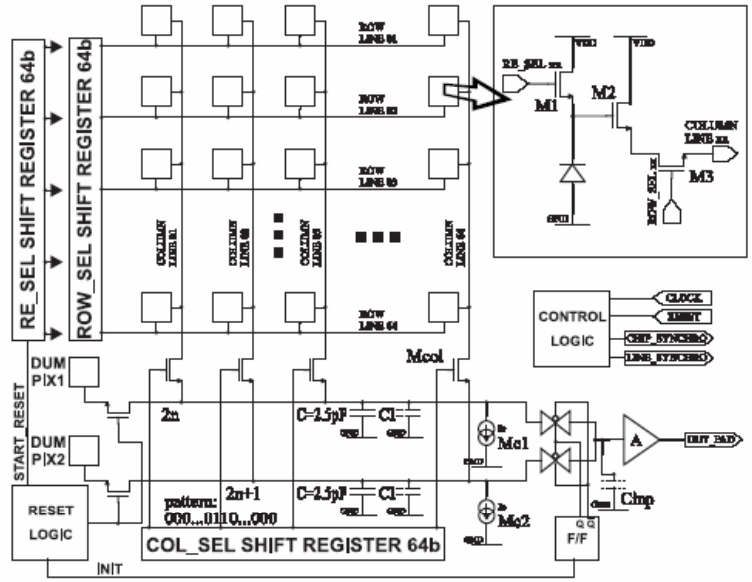
Grzegorz DEPTUCH
deptuch@lepsi.in2p3.fr

# ☑ First Prototypes - Summary of Performances

## MIMOSA I
die size 3.6 × 4.2 mm²

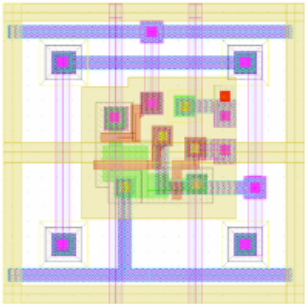


Device internal architecture
e.g. MIMOSA II

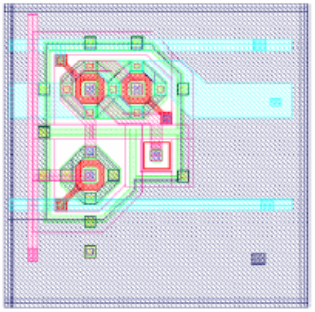



## Examples of pixel layouts

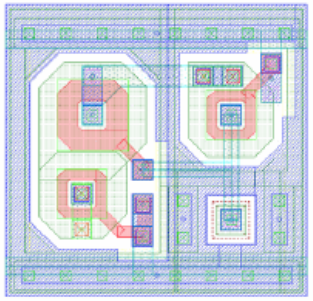
M I: 20× 20 µm²



M II: 20× 20 µm²



M III: 8× 8 µm²

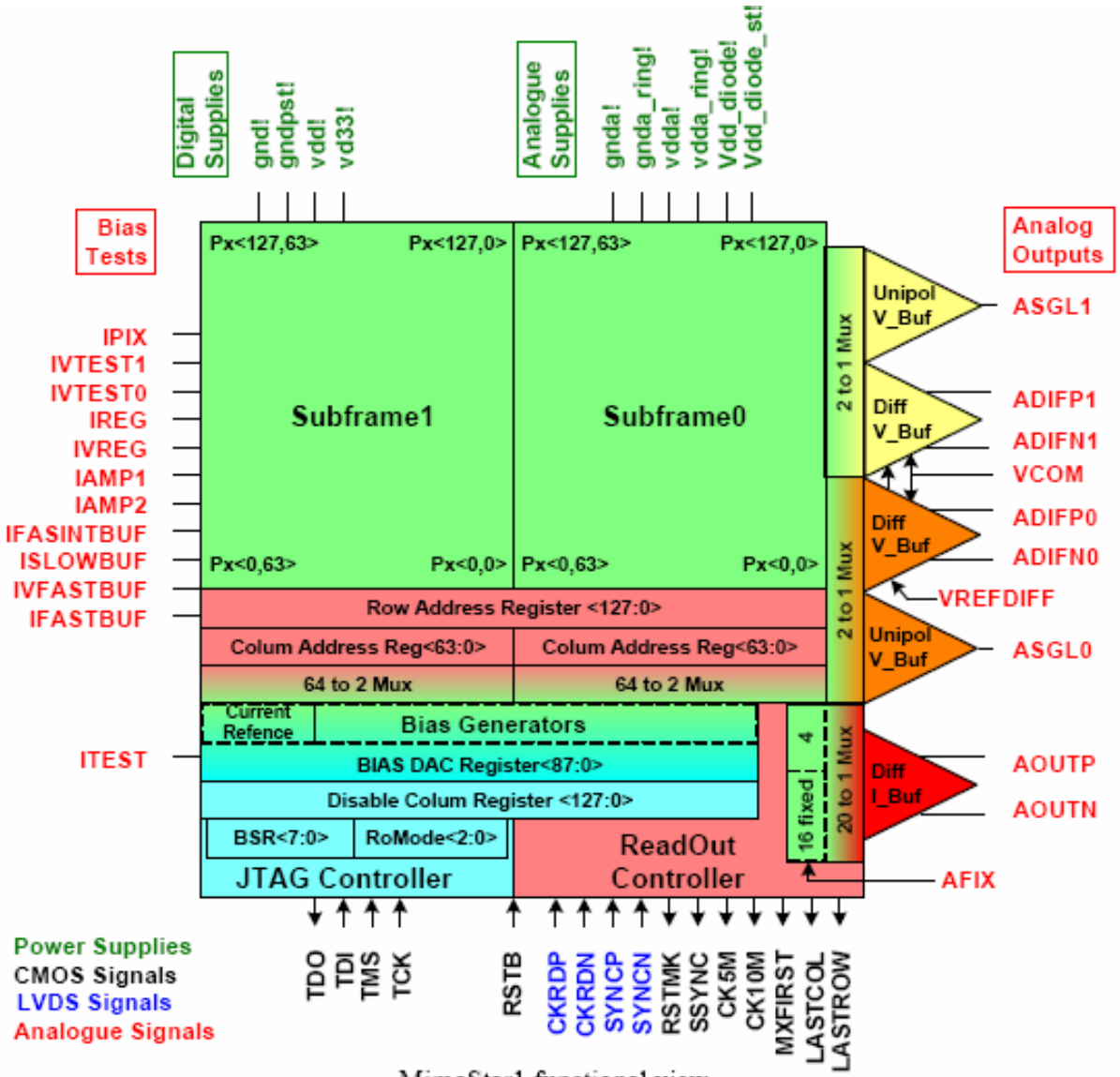


| Prototype, Process | Epitaxial layer, Pixel pitch | Chip configuration | Sensitive diode element | Peculiar features |
|---|---|---|---|---|
| MI ’99, 0.6 µm | ~14 µm, 20 µm | 4×64×64 pixels square layout | n-well/p-epi 3.1×3.1 µm² | thick epitaxial layer, 1 and 4 diodes / pixel<br>serial analogue readout $f_{clk}$<5MHz |
| MII ’00, 0.35 µm | ~4 µm, 20 µm | 6×64×64 pixels square and staggered layouts | n-well/p-epi 1.7×1.7 µm² | 1 and 2 diode / pixel<br>structures for irradiation tests<br>serial analogue readout $f_{clk}$<25MHz |
| MIII ’01, 0.25 µm | ~2 µm, 8 µm | 2×128×128 pixels staggered layout | n-well/p-epi 1.0×1.0 µm² | thin epitaxial layer, 1 diode / pixel<br>varied size of SF transistor<br>structures for irradiation tests<br>serial analogue readout $f_{clk}$<40MHz |
| MIV ’01, 0.35 µm | $p^-$-type substrate, 20 µm | 4×64×64 pixels square layout | n-well/p-sub 2.0×2.0 µm² | no epitaxial layer, 1 and 3 diodes pixels<br>current mode pixel (photoFET)<br>auto-reverse-polarised diodes<br>serial analogue readout $f_{clk}$<40MHz |

# MimoStar1
# User Manual

MimoStar1 User Manual v1.0

C. Colledani, G. Deptuch, H. Himmi, Ch. Hu, I.Valin
Institut de Recherches Subatomiques
Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux
IN2P3-CNRS / ULP Strasbourg – France

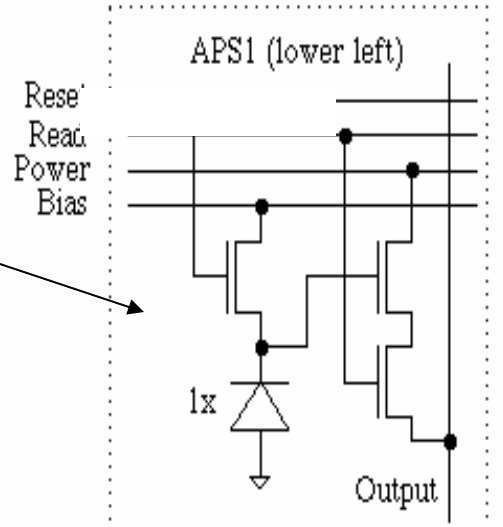


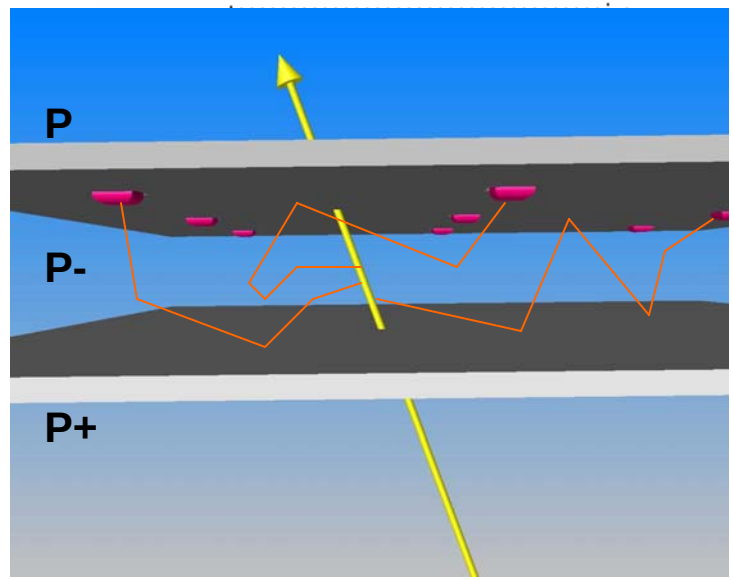

MimoStar1 functional view

Does not correspond to the floorplan; neither for the core, neither for the pad ring

# Photo gate purpose – to address standard pixel limitations

- With the standard CMOS pixel array off chip CDS is required to remove fixed pattern noise and KTC reset noise
- In the standard CMOS pixel array the signal is spread over multiple diodes
  - Penalty in signal to noise
- Potential advantages of photo-gate
  - Use like CCD – read voltage, transfer charge – read voltage again and take difference. Gives on chip CDS
  - Increase signal by reducing signal spreading to adjacent pixels. The photo gate permits large geometry without adding capacitance to the sense node.



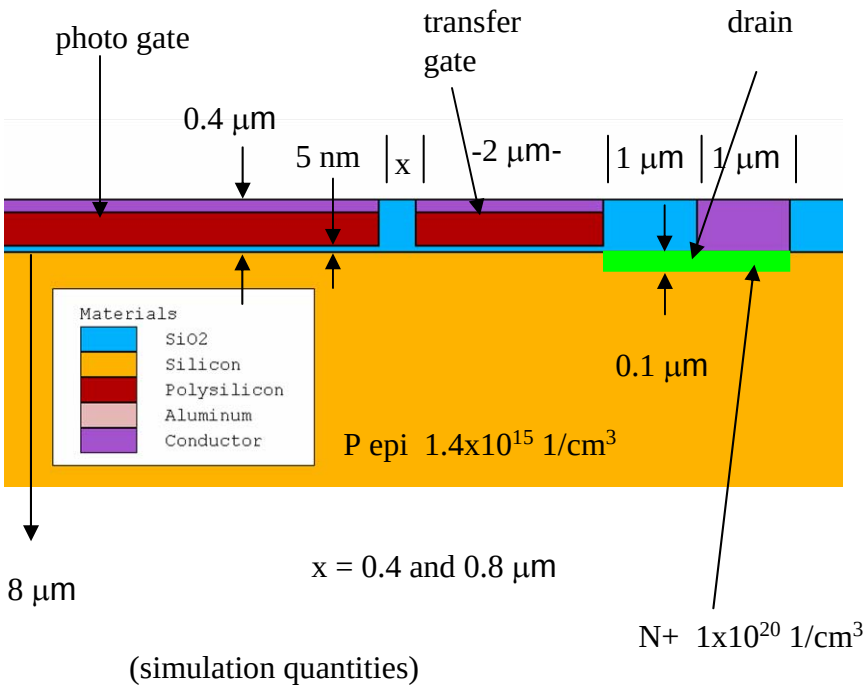




Standard diode geometry

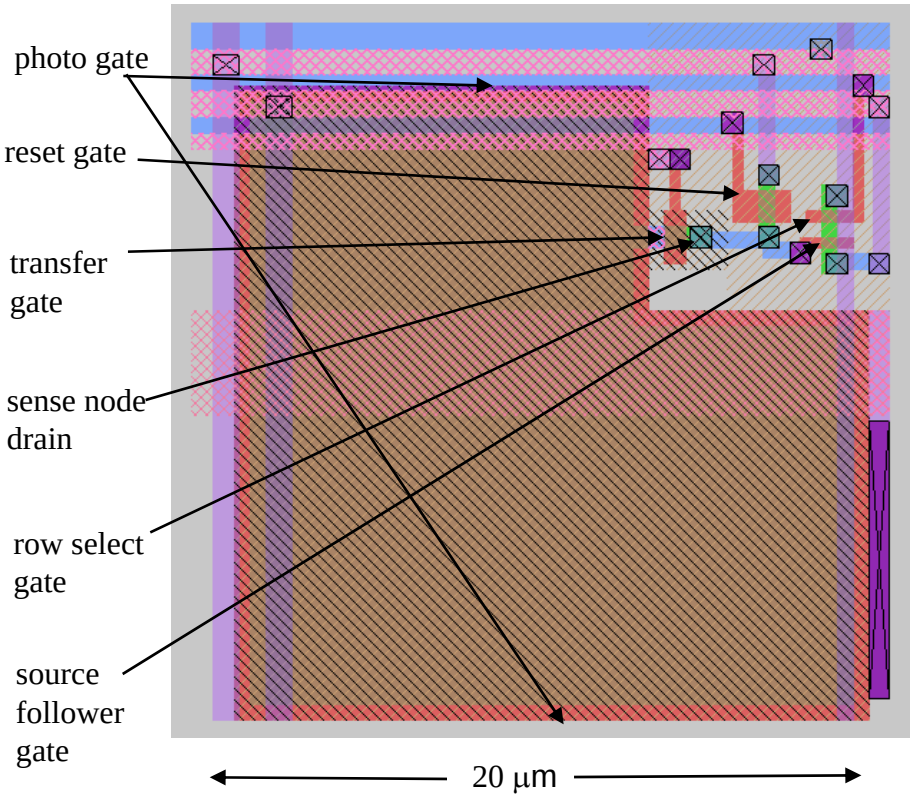
# Photo-gate geometry

**Chip designed and built by**
**Stuart Kleinfelder and Yandong Chen**
**UC Irvine**

- Large photo-gate to collect large fraction of the charge on a single pixel, directly on the p- epi layer
- Small transfer gate also directly on p- epi layer
- Small drain (minimum capacitance) connected to source follower gate (sense node)

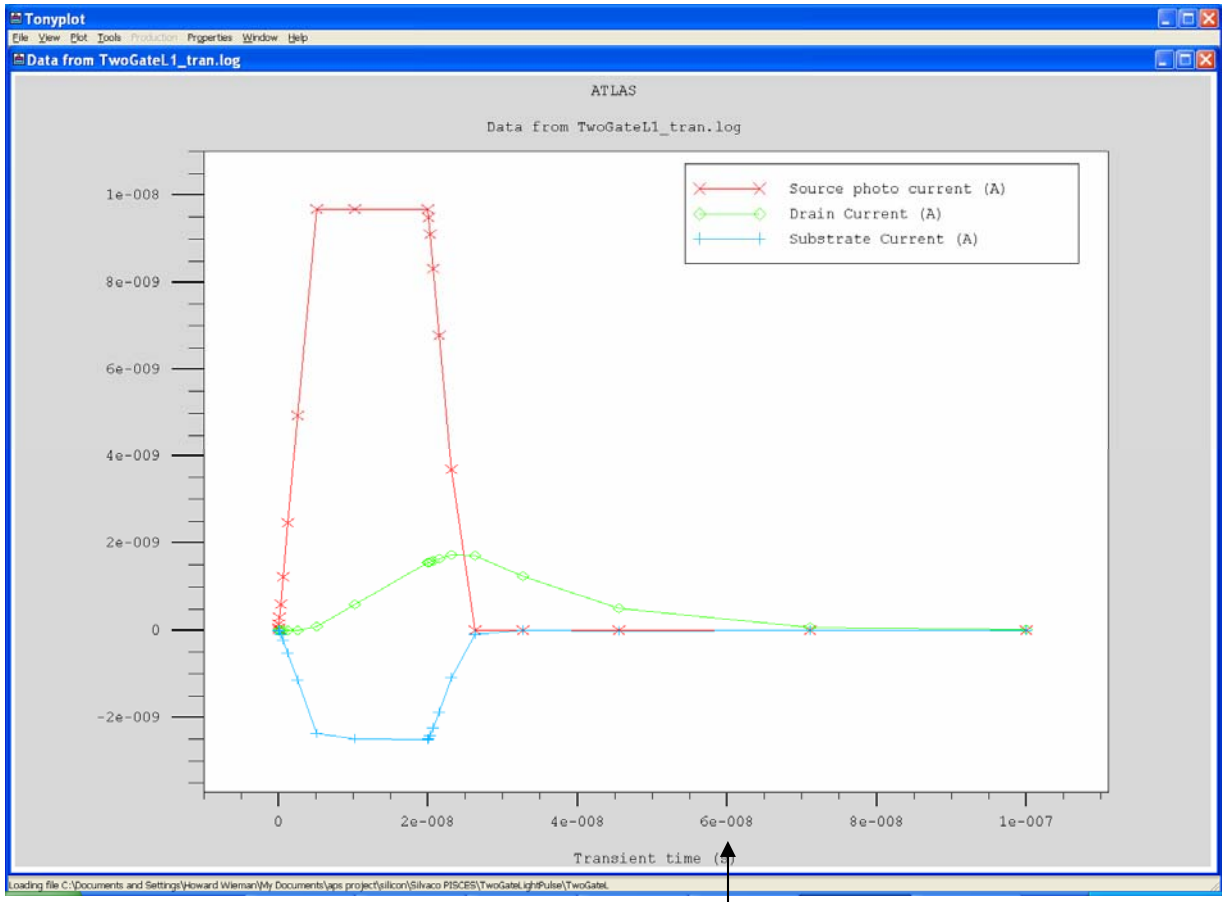



(simulation quantities)



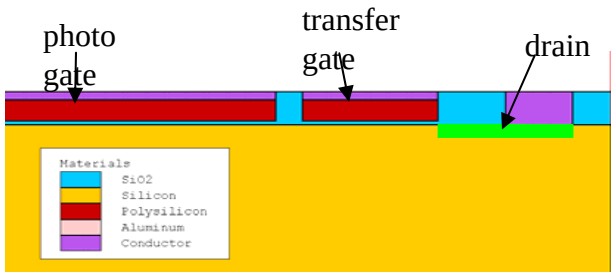
# Drain current after light injection

- Nano amp drain current
- Rapid electron transfer - complete in 60 ns




60 ns

**Light injection**

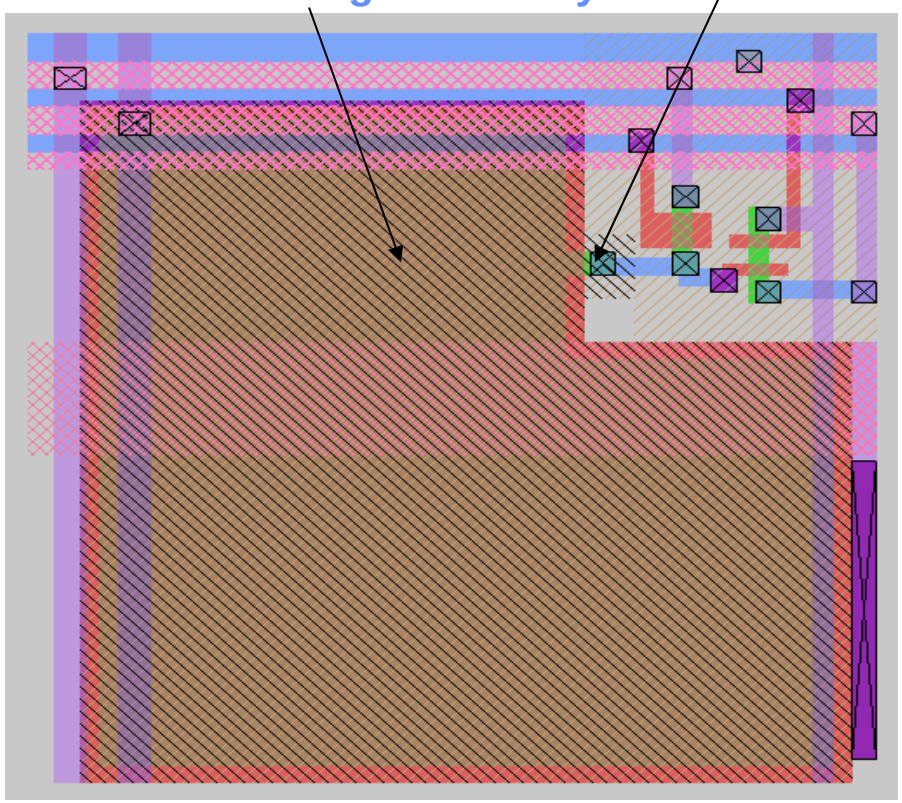



**Simulation using SILVACO ATLAS running on laptop. Service through eecad, only a few 10s of dollars to run. About to change to per day cost of ~$170**

**Relied on Zhang Li and Wei Chen to get started**

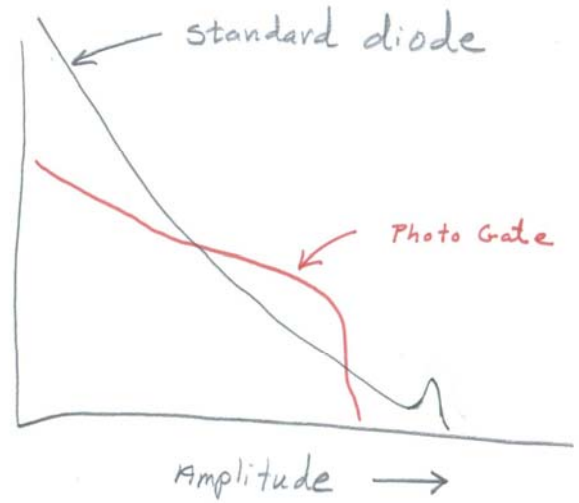
# First silicon tests

Photo-gate directly to sense node drain



DC bias:
V photo-gate 0.6 V
V drain 2.4 V

Accumulated histogram of output signal for Fe55 X-ray test after CDS correction



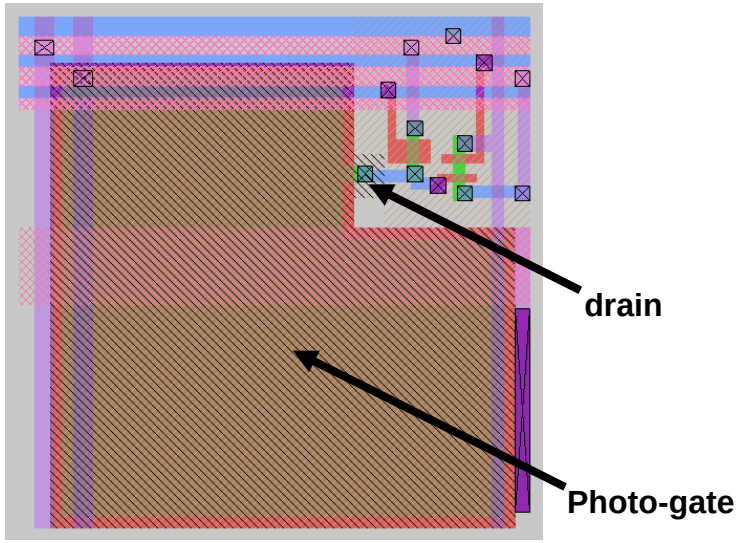

**Issues:**

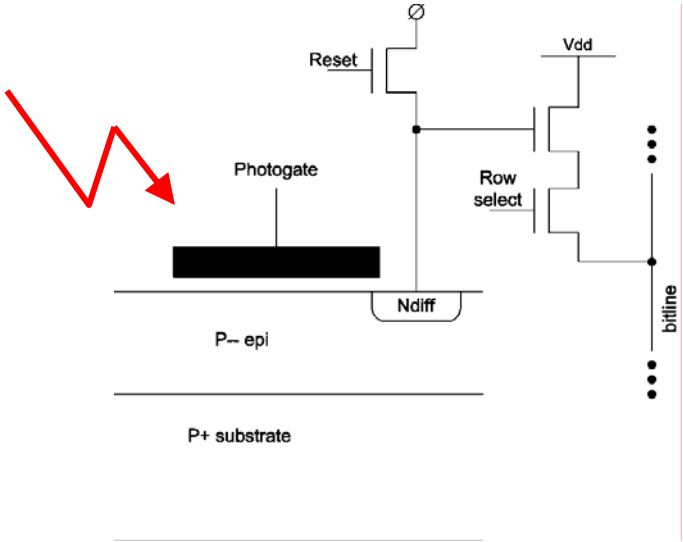
- Signal spreading
- Reduced gain

# Photo-gate LED test

- Used a single pixel in sector 5 (simple structure with photo-gate and small drain on the edge)
  - Photo-gate voltage 1 volt
  - Drain voltage set by full reset voltage
- Test sequence
  - Reset all pixels
  - Clock row and column shift registers to select a single pixel
  - Inject 2 red LED pulses
  - Observe output voltage with oscilloscope throughout sequence
- Also did same test with sector 1 ( the standard diode) for comparison

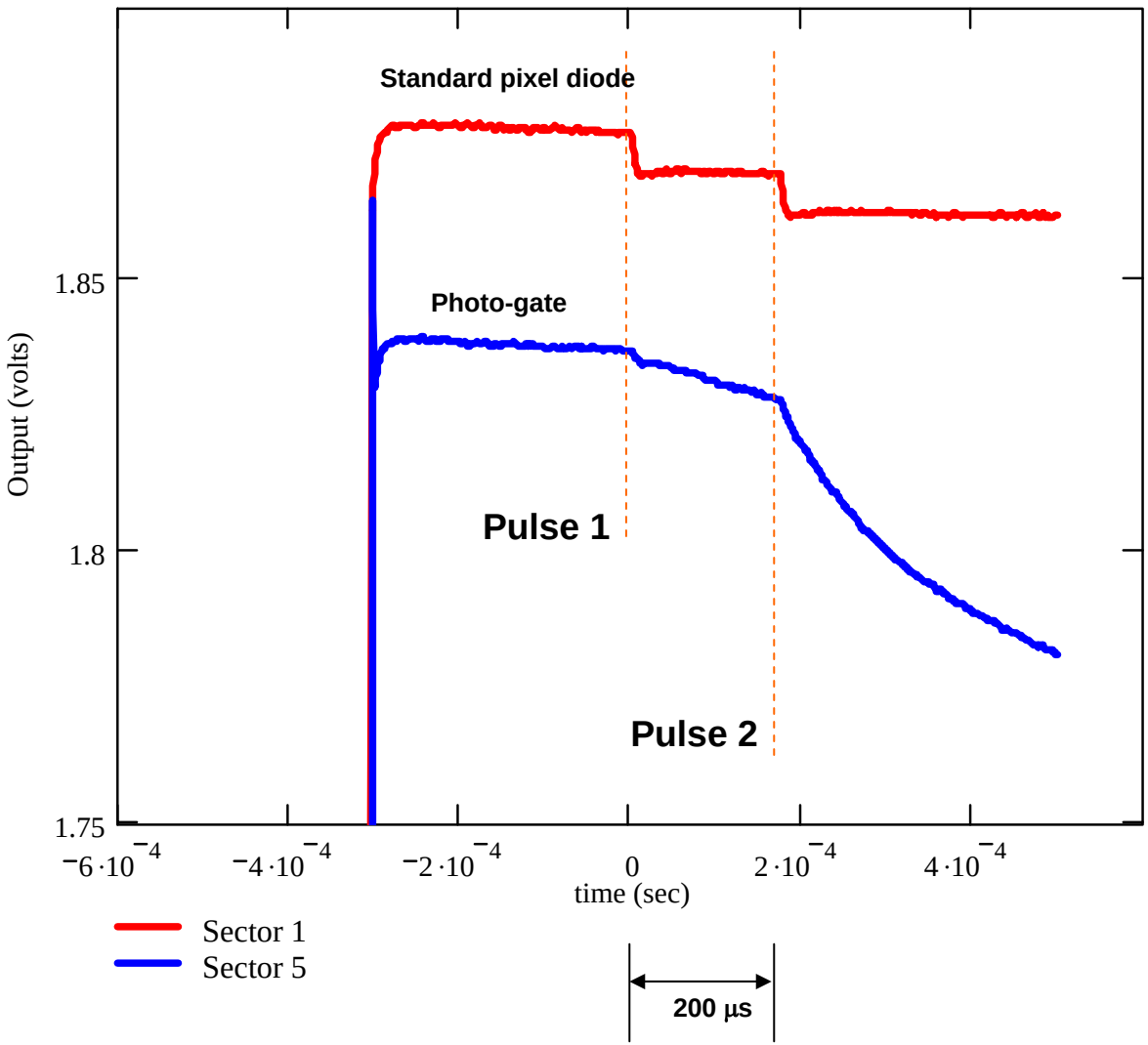
**Sector 5**



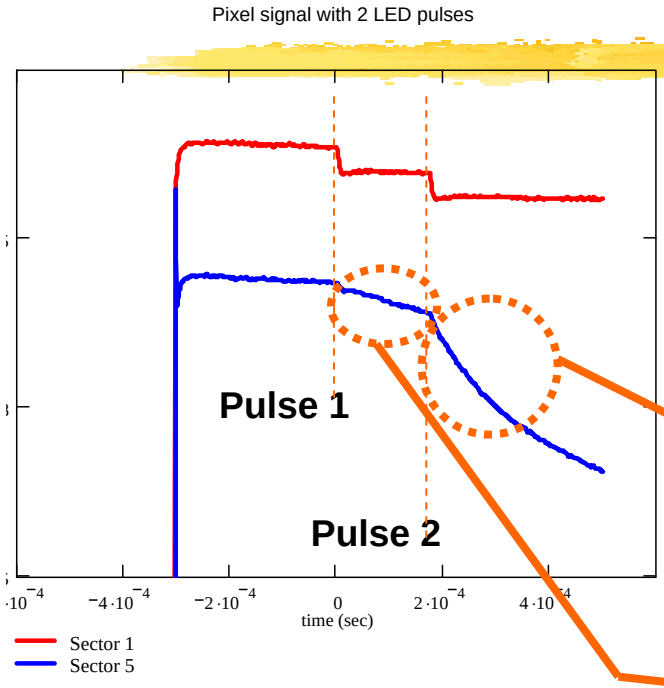
# Measured output voltage

Pixel signal with 2 LED pulses




- Features to note
  - Both sectors exposed to same LED pulses, but light attenuated for sector 1
  - Sector 5 response to 1st LED pulse much smaller than to 2nd
  - Sector 5 leakage current ramp increases after 1st LED pulse
  - Response difference for the two pulses in sector 5 is directly related to gate, since sector 1 shows that readout structures are not affected differently by the two pulses
  - Reducing the pulse separation did not change effect

# Photo-gate time response to two pulses the same, only amplitude difference




**Adjust amplitude and overlay**

Signal fits:

$$-\left[1-\exp\left(-\frac{t}{\tau}\right)\right]$$

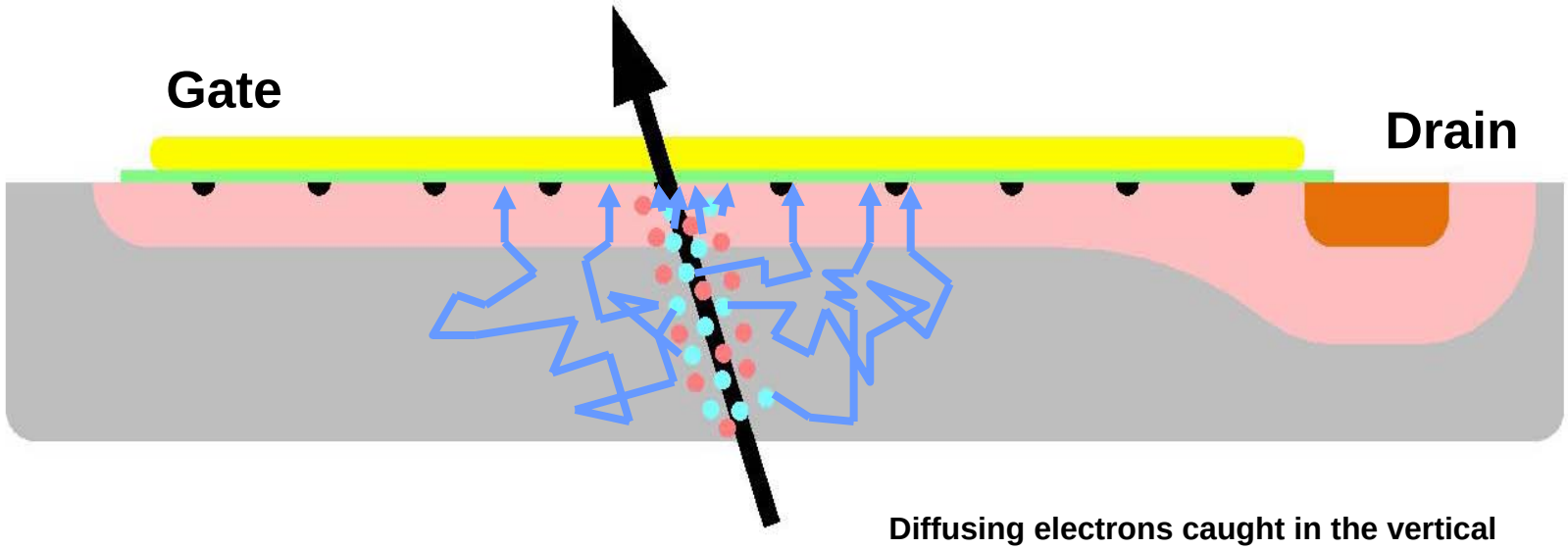
+ plus leakage slope

$$\tau = 204\ \mu s$$

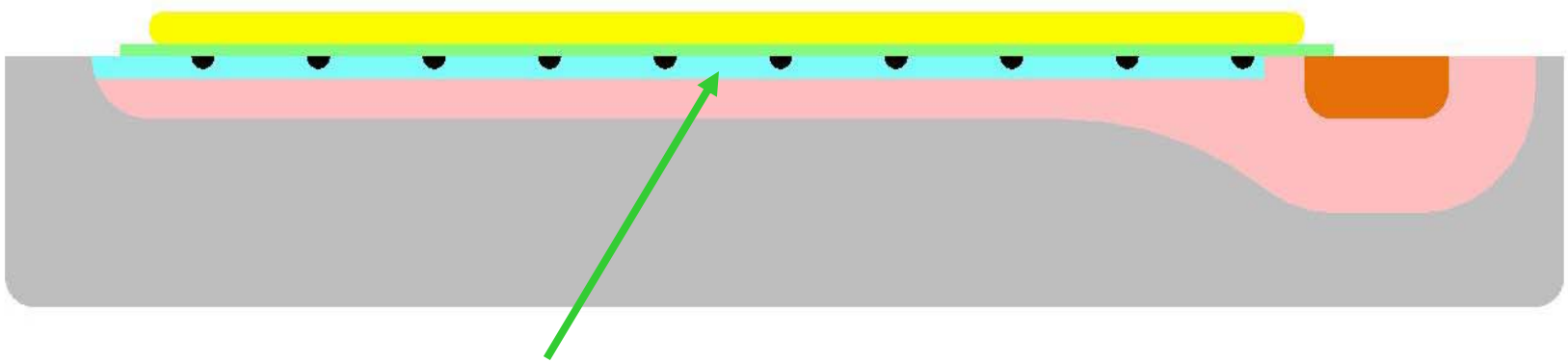
# Photo-gate

- Test chip
  - Measured charge transfer (200 μs)
- Can surface states explain the delay, calculate expectations
  - The transfer process
  - Rate of direct transfer, diffusion from gate to drain
  - Rate of surface state population
    - Determine density of electrons at $SiO^2$ – Si surface
  - Time for surface state decay back to conduction band
    - Can this account for delay

# First step of electron collection

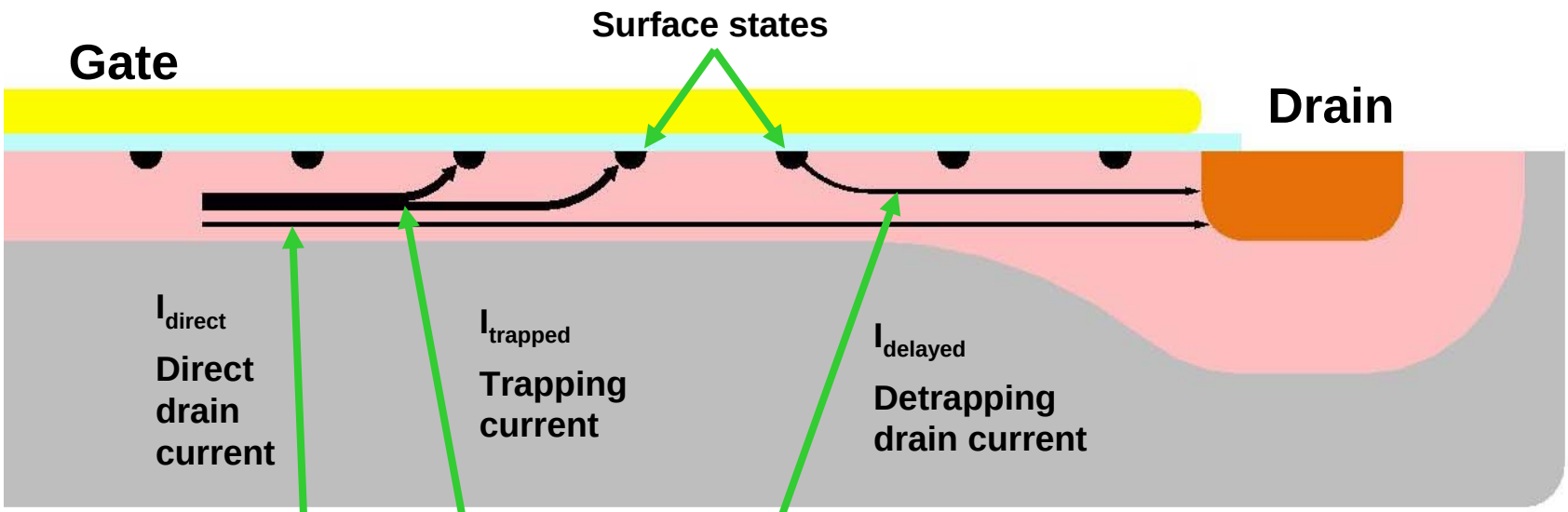



Diffusing electrons caught in the vertical space charge field under the gate



Electrons distribute along the surface

# Next step – getting to the drain



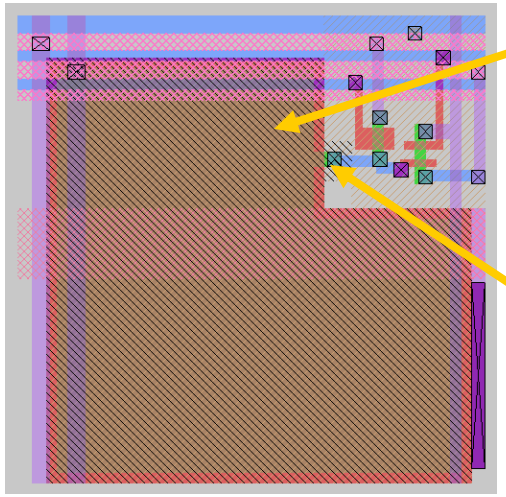

$$\frac{d}{dt}N_e(t) = -N_e(t)\cdot\alpha - N_e(t)\cdot\beta + \int_0^t N_e(t_p)\cdot S(t,t_p)\,dt_p$$

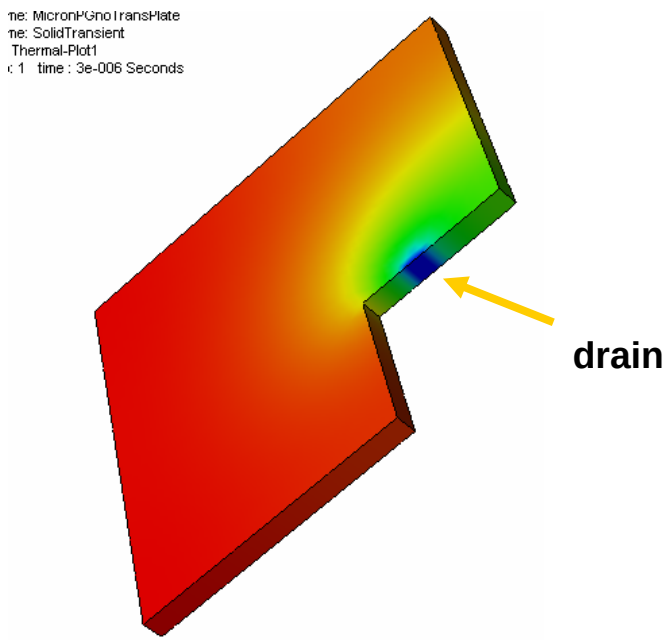
$N_e(t)$ **The number of electrons under the gate**

**Don't need to solve equation to check for delay**

**Determine if $I_{direct} << I_{trapped}$ and $I_{delayed}$ is small then signal collection is slow, more electrons spend time bound in surface states**

# Simple diffusion transfer of electrons from gate to drain




## Diffusion equation in 1D

$$\frac{d}{dt}n = D_n \cdot \frac{d^2}{dx^2}n$$

| | |
|---|---|
| $n$ | electron density |
| $D_n$ | electron diffusion constant in silicon |

**Solve with COSMOS FEA (~3D) – thermal transient solution, analogous diffusion equation**

**Start with uniform temperature and a heat sink at the drain**

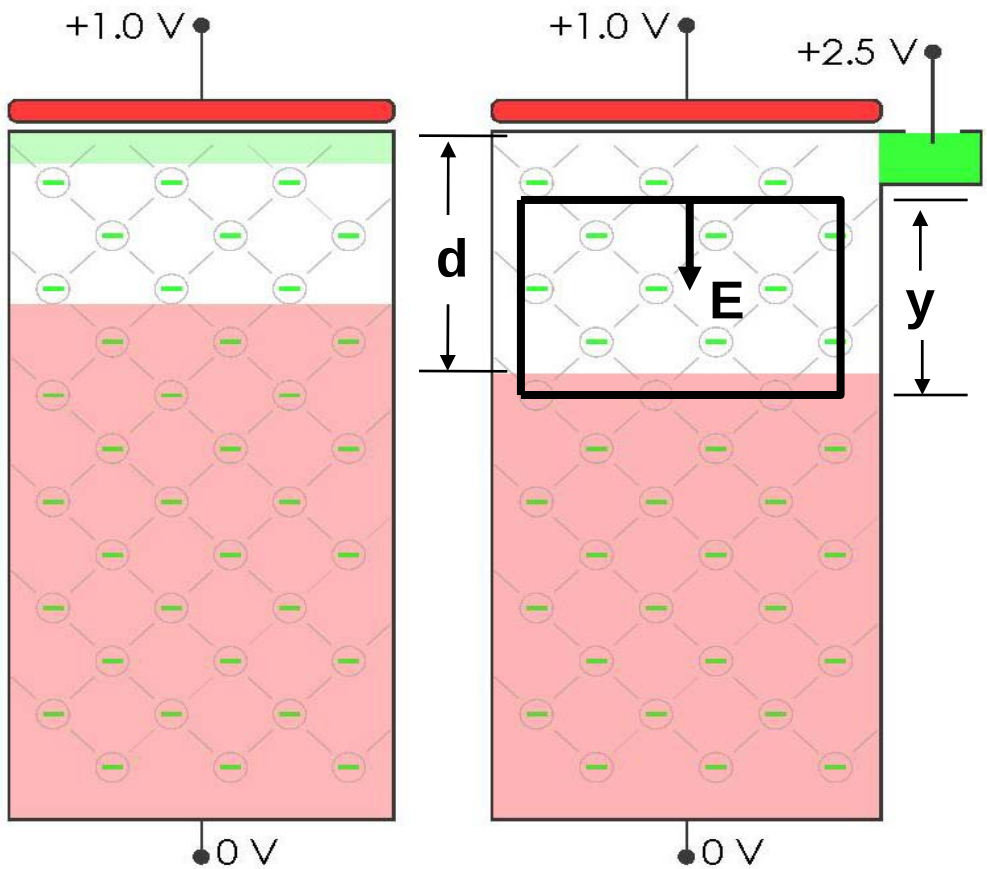
**Convert to electron diffusion**

**Result:**

$$N(t) = N_0 \cdot \exp\left(\frac{-t}{\tau_n}\right)$$ total electrons under gate

$\tau_n$ **= 120 ns**

# Silicon electric field under the gate




p- epi

p- epi with n type drain

$$\int \vec{E}\,d\vec{s} = \frac{1}{\varepsilon_s}\cdot\int q\,dv$$

**Using Gaussian pill box**

$$|E(y)| = y\cdot N_A\cdot qe\cdot\frac{1}{\varepsilon_s}$$

$$N_A = 1.4\times 10^{15}\,\frac{1}{cm^3}$$ acceptor density

$$V(y) = \int_0^y E(y)\,dy = \frac{1}{2}\cdot y^2\cdot N_A\cdot\frac{qe}{\varepsilon_s}$$

$$d = \sqrt{\frac{2\cdot v_s\cdot\varepsilon_s}{N_A\cdot qe}} = 1\mu m$$

$v_s$ **= ~ 1.0 V since no inversion charge, ignoring work function differences**

# Density of electrons at the surface left by LED

electron density distribution under the gate

$$D_n \cdot \frac{d}{dy} n + E(y) \cdot n \cdot \mu_n = 0$$

The static electron density n(y) set by condition that diffusion and drift cancel

use Einstein relation $D_n = \left( \frac{k_b \cdot T}{qe} \right) \cdot \mu_n$

Debye length $L_D = \sqrt{\frac{k_b \cdot T \cdot \varepsilon_s}{N_A \cdot qe^2}}$ = 110 nm

**1/e distance = 12 nm**

depletion depth $d = \sqrt{\frac{2 \cdot v_s \cdot \varepsilon_s}{N_A \cdot qe}}$ = 960 nm

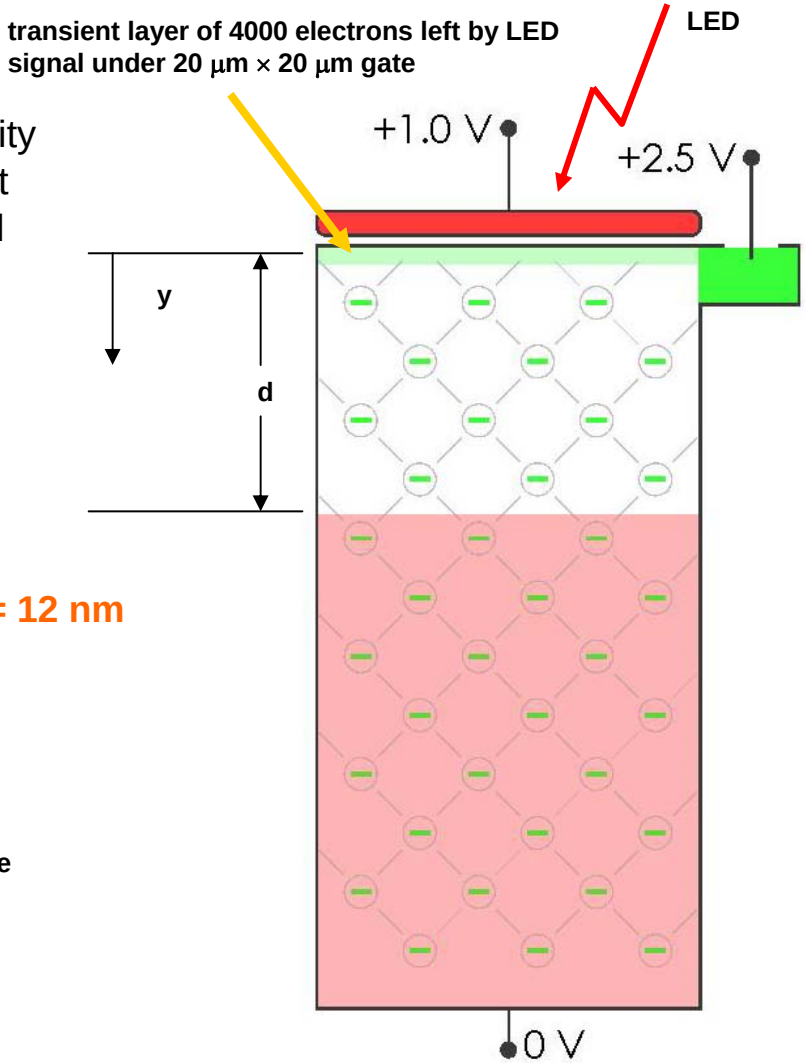
$$n(y) = n_s \cdot \exp\left( \frac{-d \cdot y}{L_D^2} \right)$$

solution

**Integrate over volume under gate to get $n_s$**

$$n_s = \frac{d \cdot Ntotal}{L_D^2 \cdot A_g}$$

$$n_s = 8 \times 10^{14} \frac{1}{cm^3}$$



# Rate of capture into surface states

$$\frac{d}{dt}N_e = -v_{th}\cdot\sigma_n\cdot N_{st}\cdot A_g\cdot n_s$$

rate of loss of electrons into surface states, see Zhang Li and H. Kramer

$v_{th}$ electron thermal velocity

$\sigma_n$ surface state capture cross section

$N_{st}$ surface state density, from Sze

**Measured by C vs freq, see Sze**

**Use number of empty traps**

$A_g$ area of the capture surface

$n_s$ electron density at the surface (from last page)

$$\frac{d}{dt}N_e = \frac{-N_e}{\tau_{st}}$$

**capture** **direct diffusion**

$$\tau_{st} = 75\text{ ns} < \tau_n = 120\text{ ns}$$

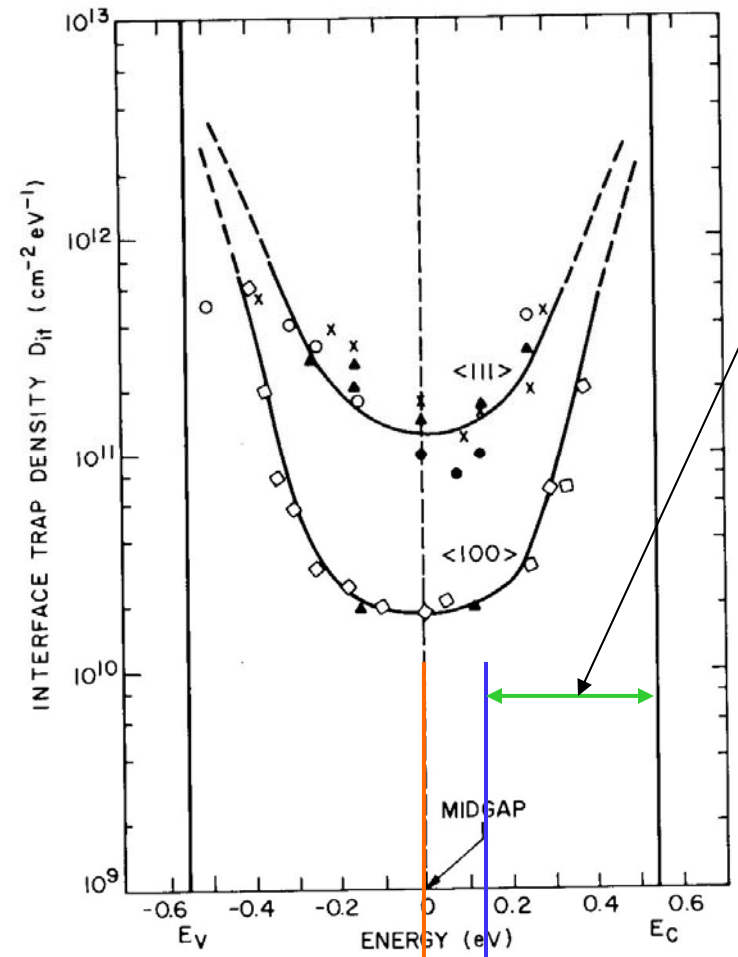
$$\tau_{st} = \frac{L_D^2}{d\cdot v_{th}\cdot\sigma_n\cdot N_{st}} = 75\text{ns}$$

time constant for capture

**Capture to surface states faster than direct diffusion to drain therefore surface states will affect transfer rate**

# Energy window for contributing traps – how many traps

Sze




$$\tau_{sd} := \frac{1}{v_{th} \cdot \sigma_n \cdot N_c \cdot \exp\left(\frac{-\Delta E}{k_b \cdot T}\right)}$$

**Decay time constant back to the conduction band, Zhang Li paper**

$\Delta E$ trap energy separation from the conduction band

$v_{th}$ thermal electron velocity

$\sigma_n$ cross section

$N_c$ Effective density of conduction band states

$$N_{st} = 2.6 \times 10^{9} \frac{1}{cm^2}$$

$$N_{st} \cdot A_g = 1 \times 10^{4}$$

**Number of contributing traps**

**Traps already filled**

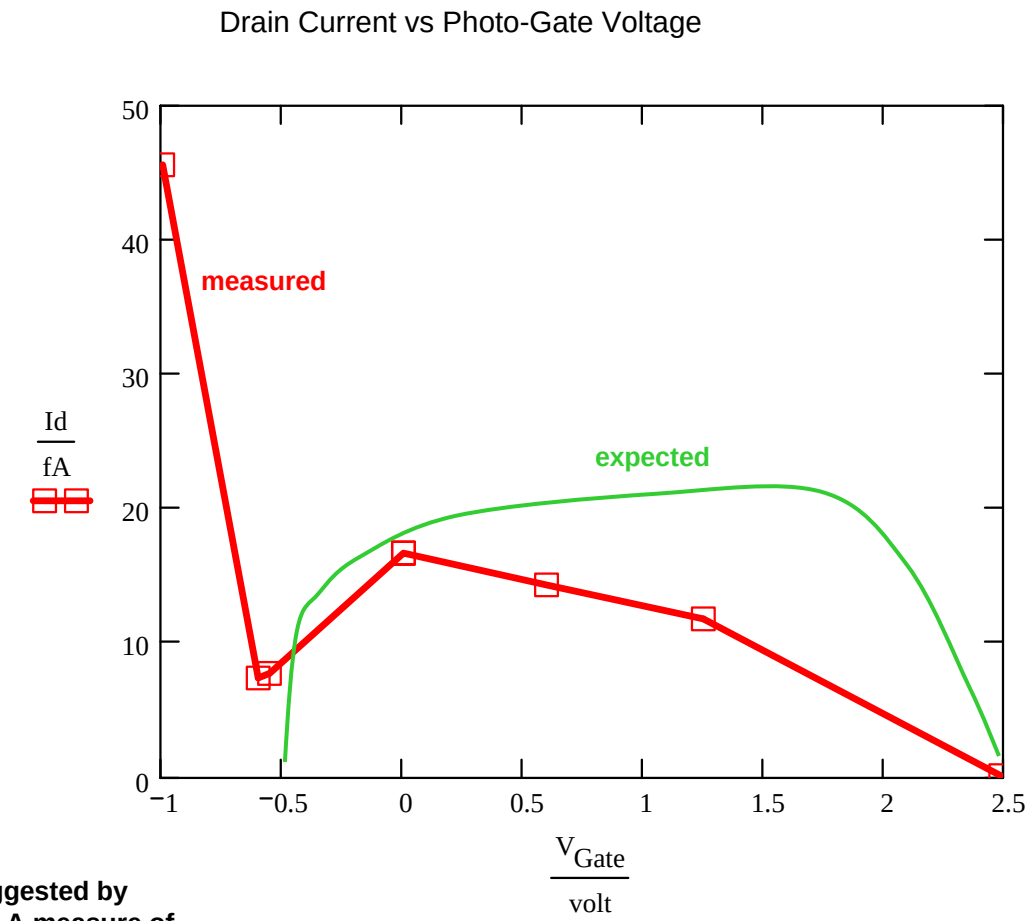
**Less than 100 μs decay time**

**More than 15 ms decay time**

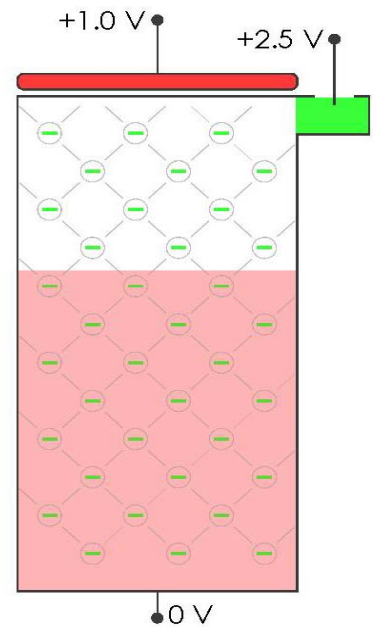
# Number of empty traps is reasonable

- 10000 - The number of empty traps from the Sze plot which were empty and had a lifetime of more than 100 $\mu$s
  - A plausible number for the trapping time ( 75 ns )
  - A plausible number for saturation with the estimated 4000 photo generated electrons

# Leakage Current measured as a function of gate voltage




**The Read Shockley Hall leakage current from surface states should be large when depleted and should diminish when space charge is neutralized.**




**As suggested by Pavel. A measure of leakage current as a function gate voltage down below depletion voltage**

**Expected region where no longer depleted, but still a puzzle**

**Same as a gated diode**

# Density of surface states from leakage current

$$U_s = N_{stI} \cdot v_{th} \cdot \sigma_n \cdot \frac{n_i}{2}$$

Reed Shockley Hall recombination rate per unit area for fully depleted

**not in thermal equilibrium**

$$I_{leak} = 13fA$$

**Measured leak**

$$N_{stI} = 2 \cdot \frac{I_{leak}}{v_{th} \cdot \sigma_n \cdot n_i \cdot qe \cdot A_g}$$

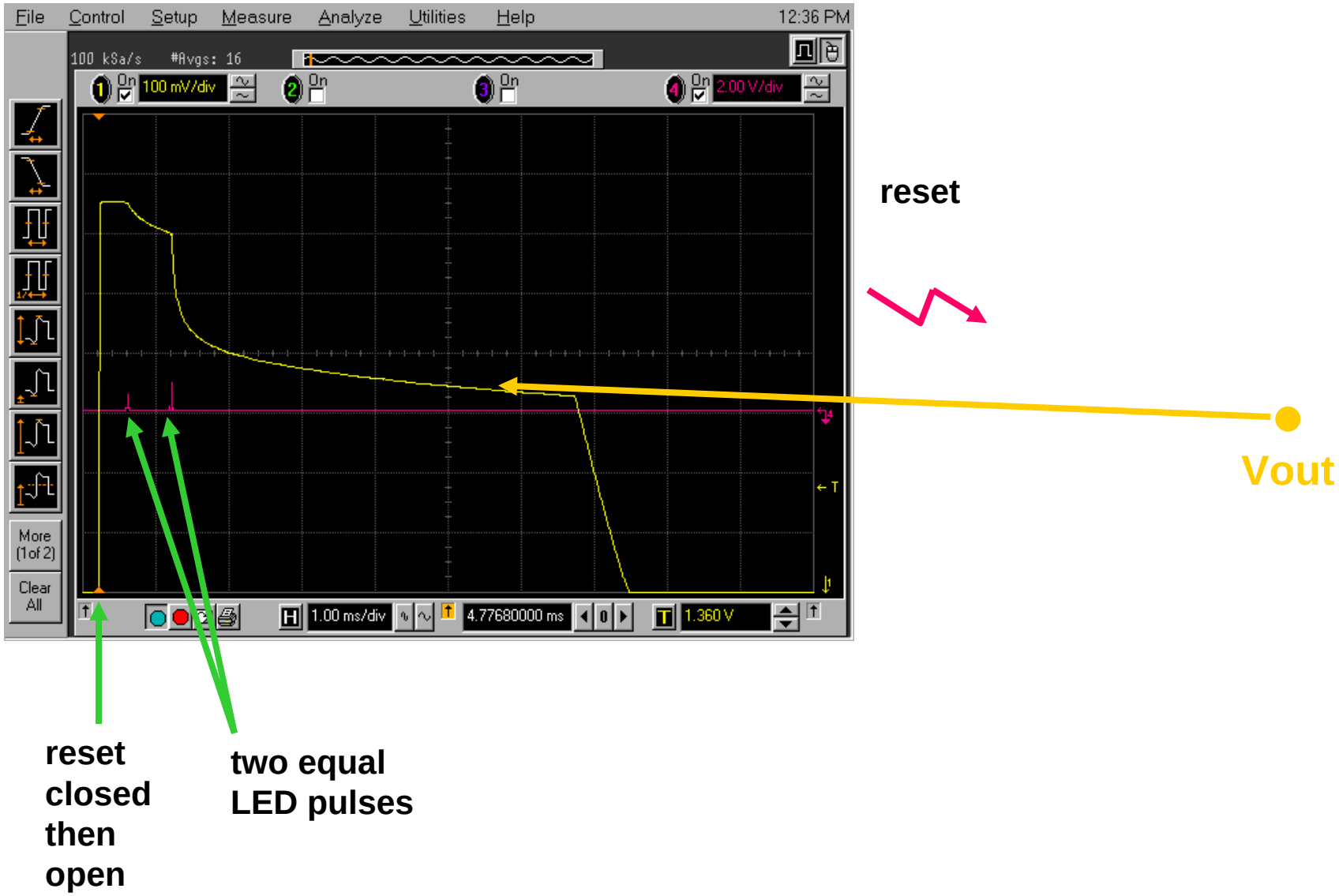
$$N_{stI} = 4.2 \times 10^8 \frac{1}{cm^2}$$

**16% of the Sze value used for trap capture time**

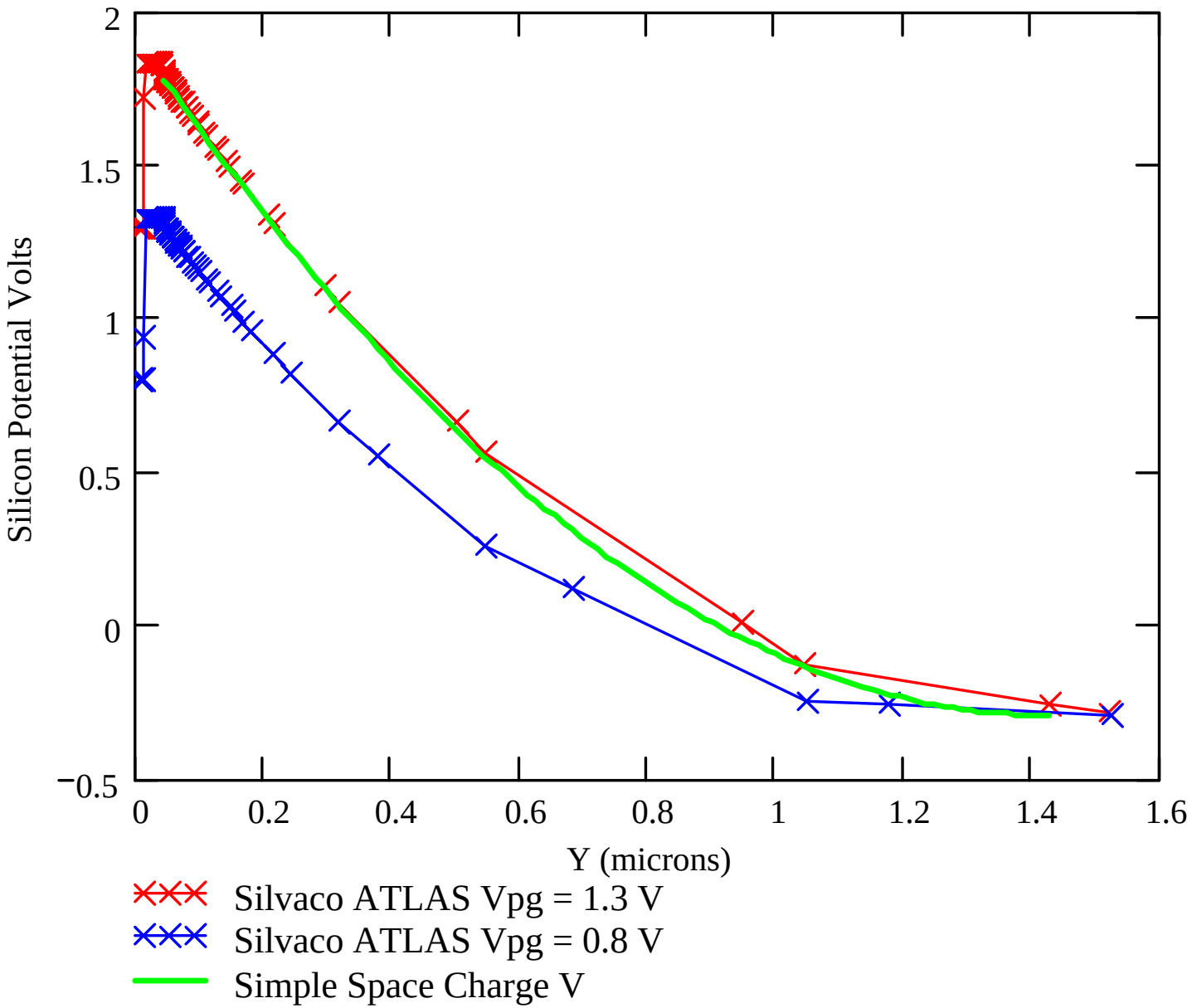
# Concluding remarks

- Some questions remain, but surface traps could explain photo-gate behavior
  - They provide delay on right order
  - They seem to have right number to see saturation effects
  - They are consistent with observed leakage current
- Another significant problem is the large leakage current, 10 times larger than pixel diode
- Note, both Turchetta and Janesick tell me they have tried and failed to make a working photo-gate in standard CMOS. Janesick saw the same type of delayed signal
- Janesick has made photo-gates work using a special process from Jazz Semiconductor with buried channel -- big bucks
- Will there eventually be a photo process that available to us with buried channel?

# Evidence for saturated traps using 2 equal LED pulses?



# Silvaco ATLAS compared to simple space Carge potential



# Recombination rate at surface

**= 0 if in thermal equilibrium**

$$U_s = N_{st} \cdot v_{th} \cdot \sigma \cdot \frac{\left(p_s \cdot n_s - n_i^2\right)}{p_s + n_s + 2 \cdot n_i \cdot \cosh\left(\frac{E_{st} - E_i}{k_b \cdot T}\right)}$$

surface recombination rate per unit area

$$n_s = 8 \times 10^{14} \frac{1}{cm^3}$$

from LED pulse

$$p_s = 4 \times 10^{3} \frac{1}{cm^3}$$

or less (SILVACO ATLAS)

$$n_i = 1.45 \times 10^{10} \frac{1}{cm^3}$$

intrinsic denstiy

so $\quad p_s \cdot n_s - n_i^2 = -n_i^2$

**Totally depleted even with LED pulse**
**Large leakage current no recombination**