An Amplitude and Time Measurement ASIC with Analog Derandomization

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Instrumentation Division Seminar

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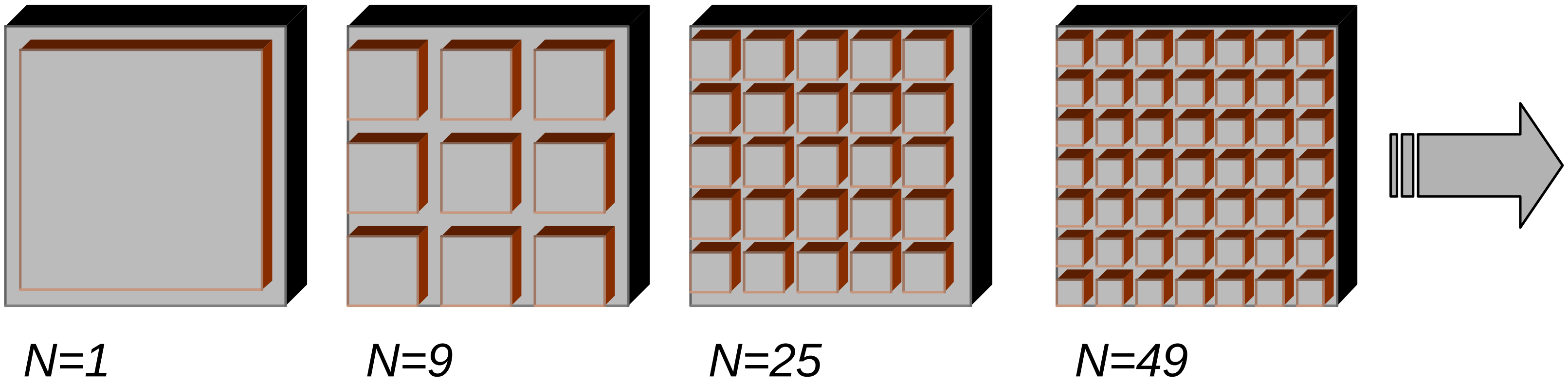
BROOKHAVEN
NATIONAL LABORATORY
Instrumentation Division

Highly segmented detectors



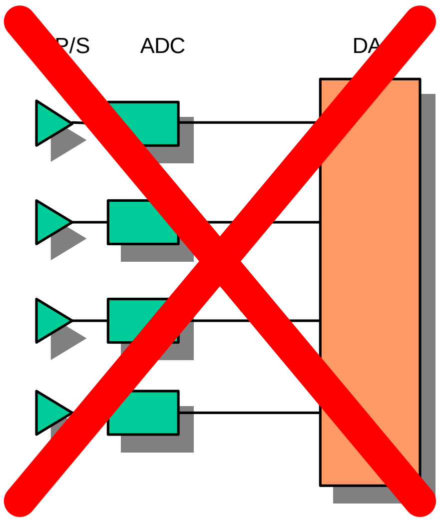
Benefits:

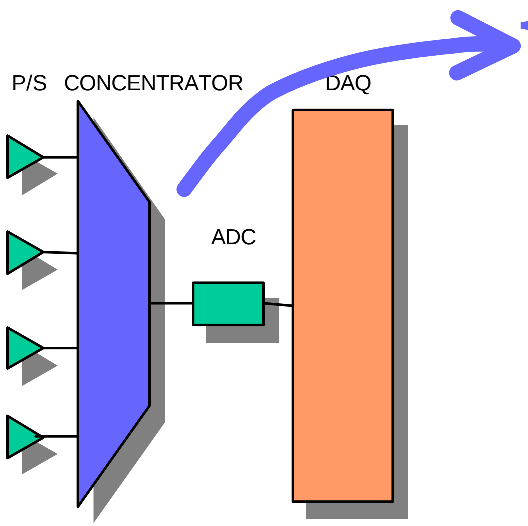
- Position Resolution
  - pixel pitch ~ $1/\sqrt{N}$
- Energy resolution:
  - C_{DET} ~ $1/N$
  - I_{DARK} ~ $1/N$
  - pulse shaping time ~ N
- Rate capability
  - pileup ~ $1/N$
- "Small pixel" effect
  - improve energy resolution in detectors with poor hole transport

Drawbacks:

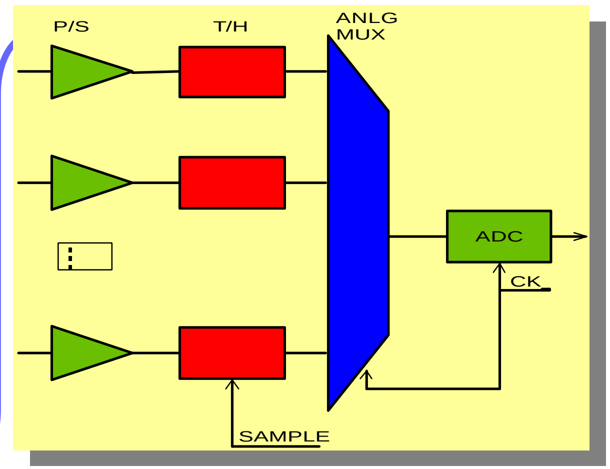
- Interconnect density
  - density ~ N
- Electronics channel count
  - cost ~ N
  - power ~ N

Data-concentrating architectures



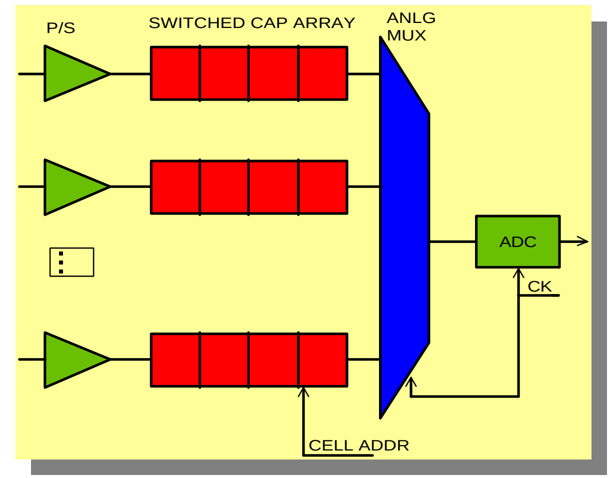


Track-and-Hold + Analog Multiplex



- unbuffered => deadtime
- long readout time
- needs accurate trigger

Analog Memory + Analog Multiplex

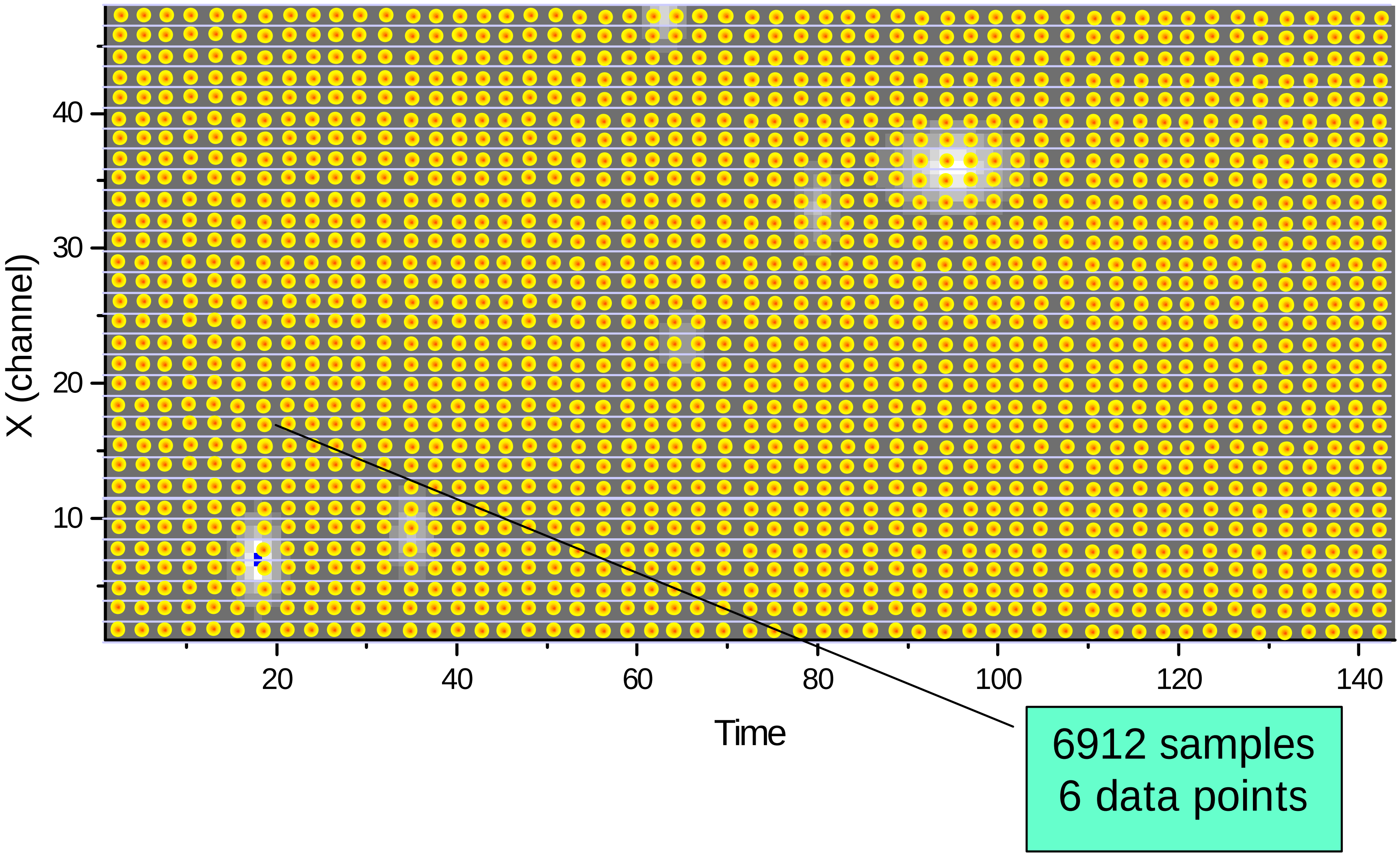


- can be deadtimeless
- complex control
- long readout time
- needs trigger + multiple samples

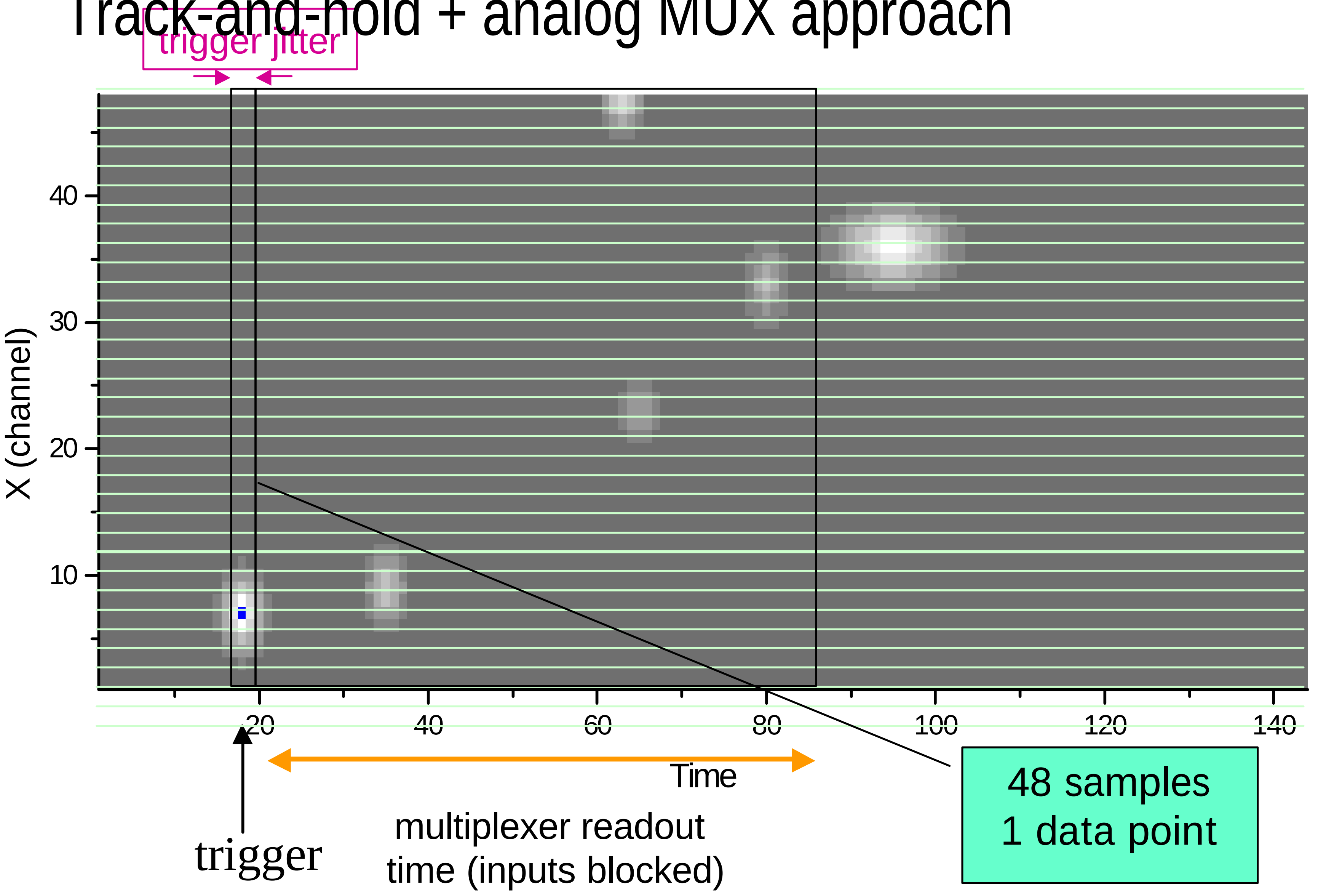
Both:

- **buy high integration at the price of efficiency**
- **problems in untriggered systems**

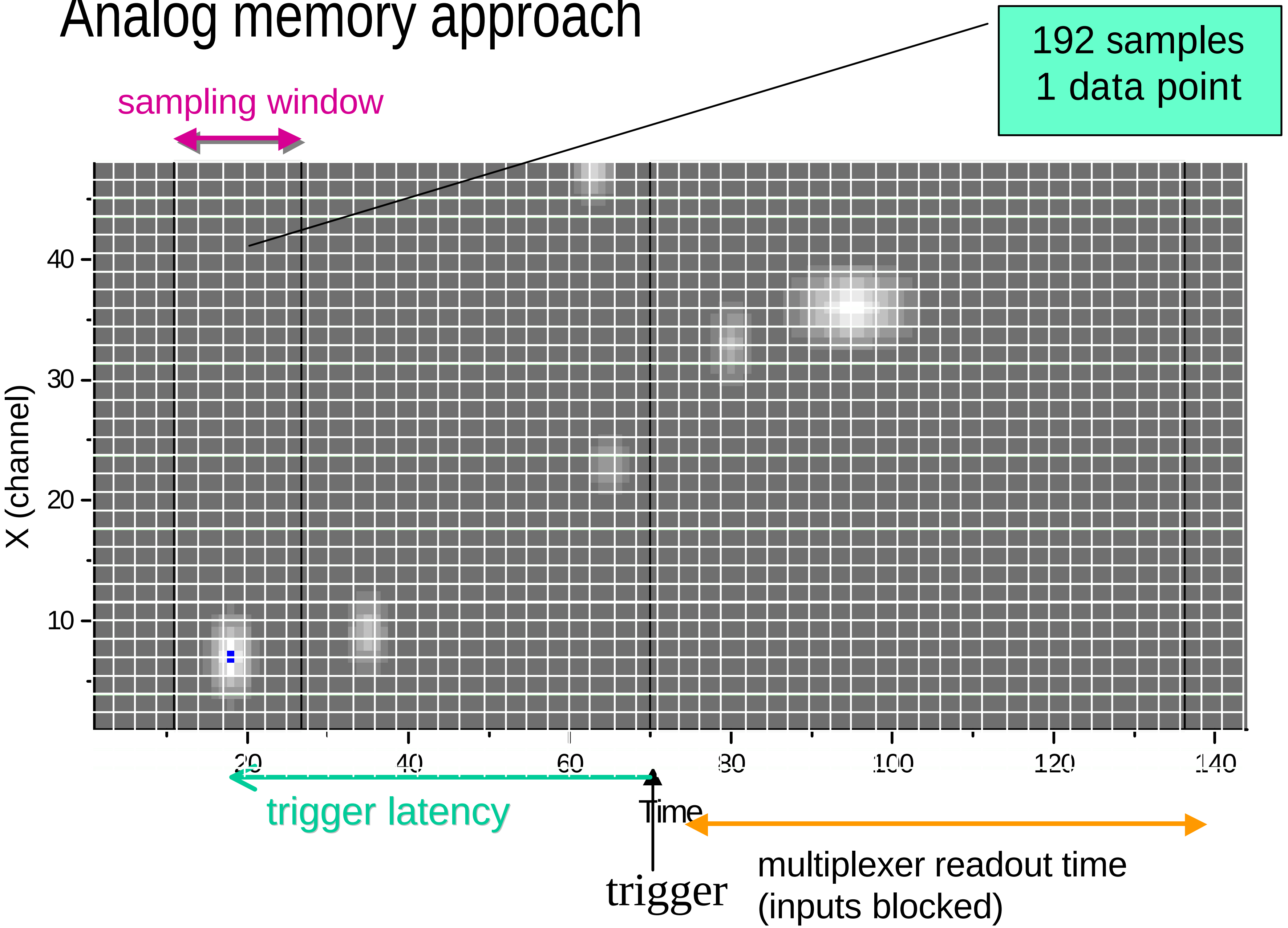
Flash ADC approach



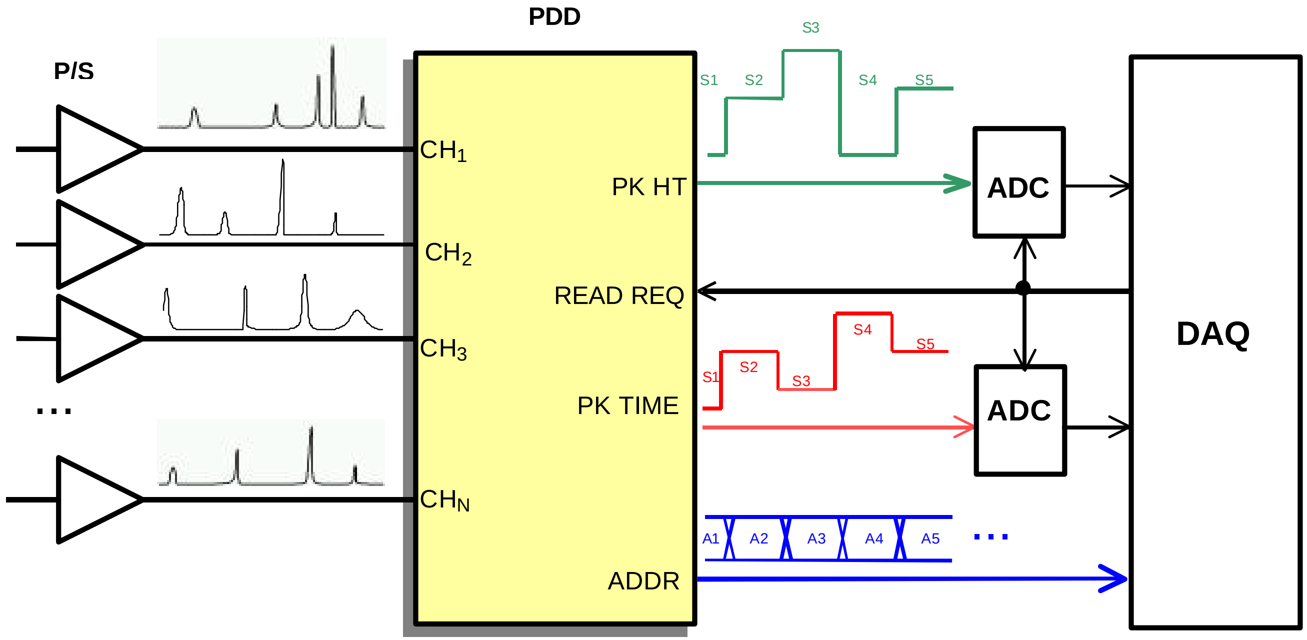
Track-and-hold + analog MUX approach



Analog memory approach



Efficient analog data concentration ASIC (analog FIFO)

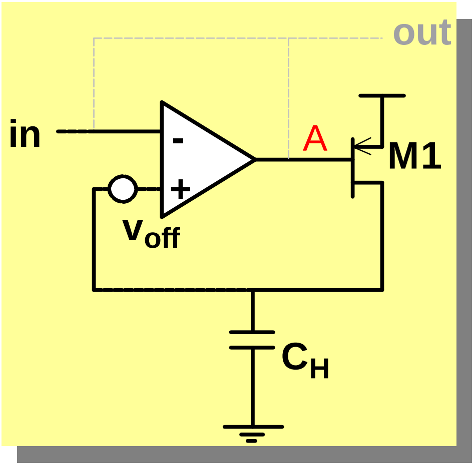


- Self-triggered sampling system
  - independent per-channel triggers
  - negligible time walk
- Sparse readout
  - skip unoccupied channels
- Buffer “memory”
  - analog storage for 4 – 8 events
- NO
  - external trigger
  - sample/hold
  - timing controls

Improved CMOS PD Using Two-Phase Configuration

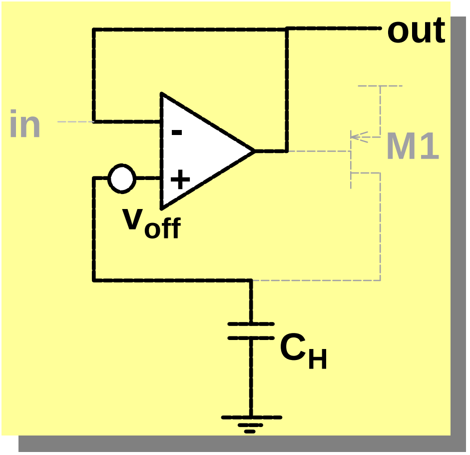
Write phase

- conventional peak detector
- M1: unidirectional current source
- voltage on C_H includes op-amp errors (offset, CMRR)



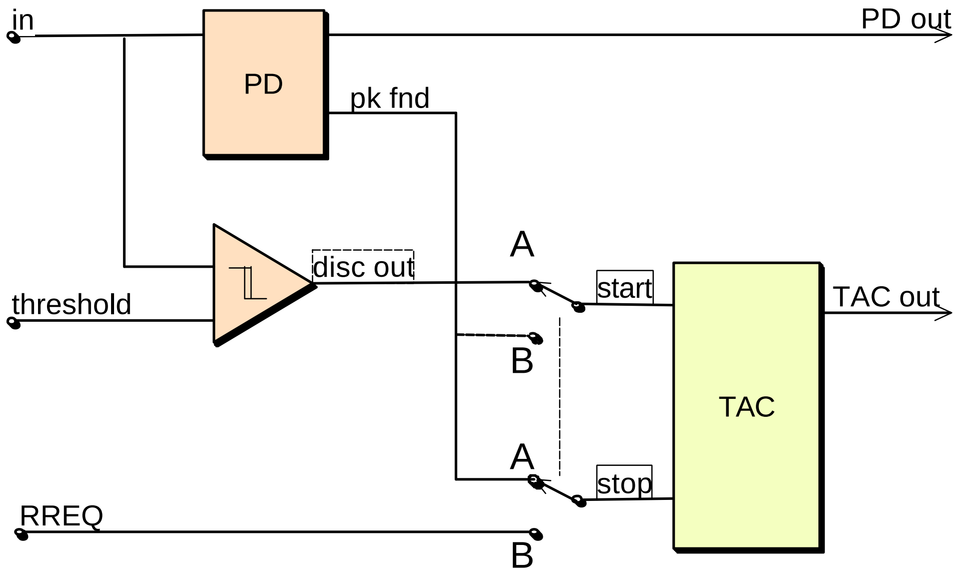
Read phase

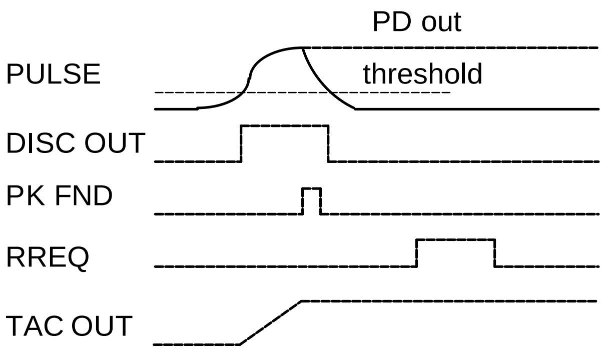
- same op-amp re-used as unity-gain buffer
- same CM voltage
- ***op-amp errors cancel***
- enables rail-to-rail sensing
- provides good drive capability



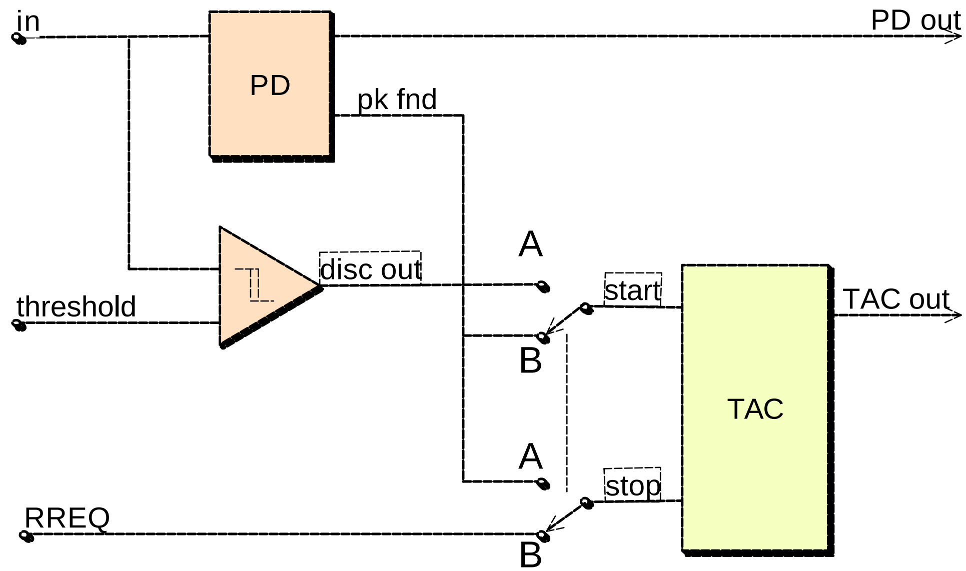
U.S. Pat. 6,512,399

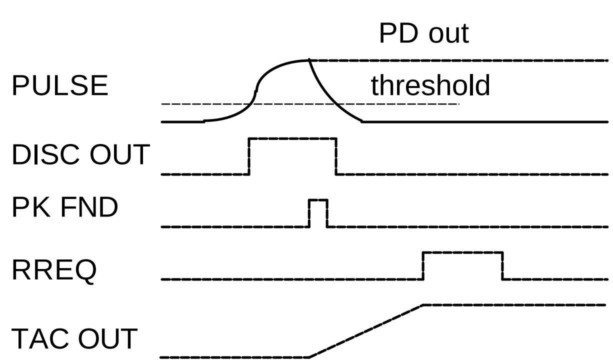
Time Detector – risetime mode





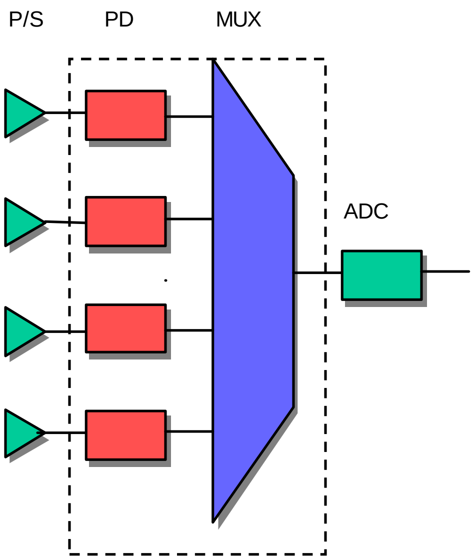
Time Detector – time of occurrence mode



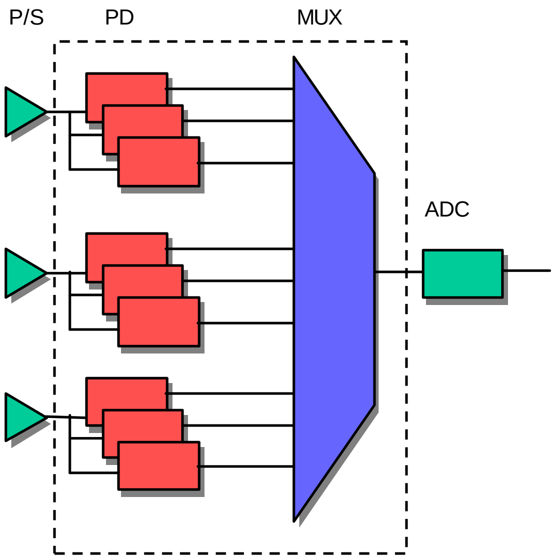


Derandomizing architectures

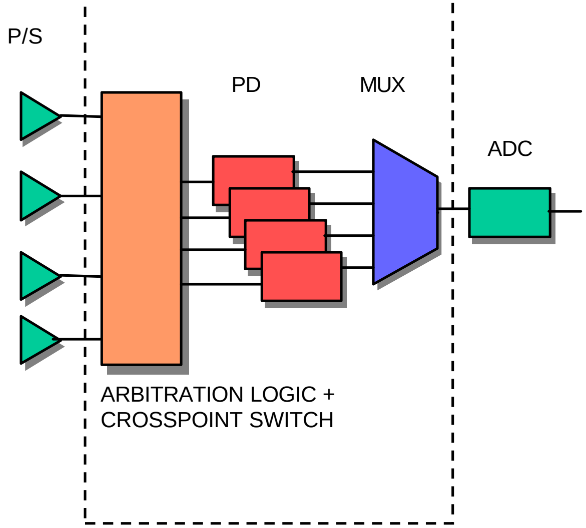
One PD per channel



Multiple PDs per channel



Multiple PDs shared by all channels

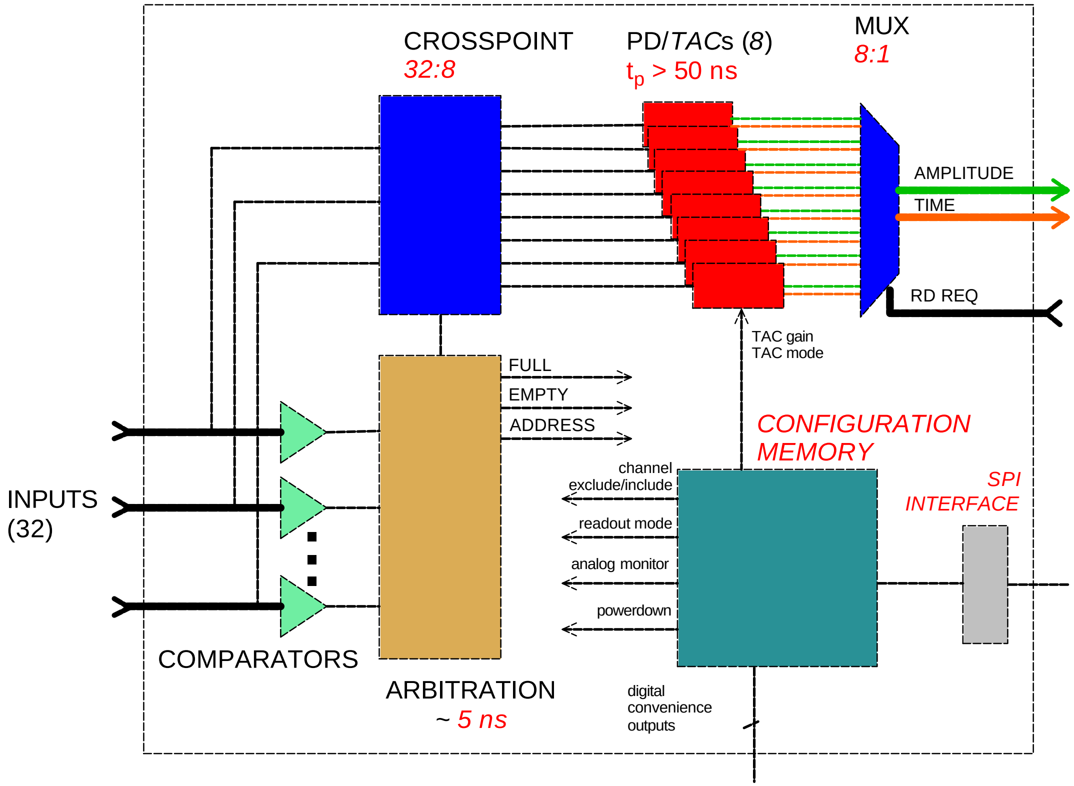


- self-triggering
- unbuffered -> deadtime
- long readout time

- self-triggering
- buffered
- long readout time
- high power dissipation
  ($N_{PD} > N_{CHAN}$)

- self-triggering
- buffered
- reduced readout time
- reduced power dissipation
  ($N_{PD} < N_{CHAN}$)

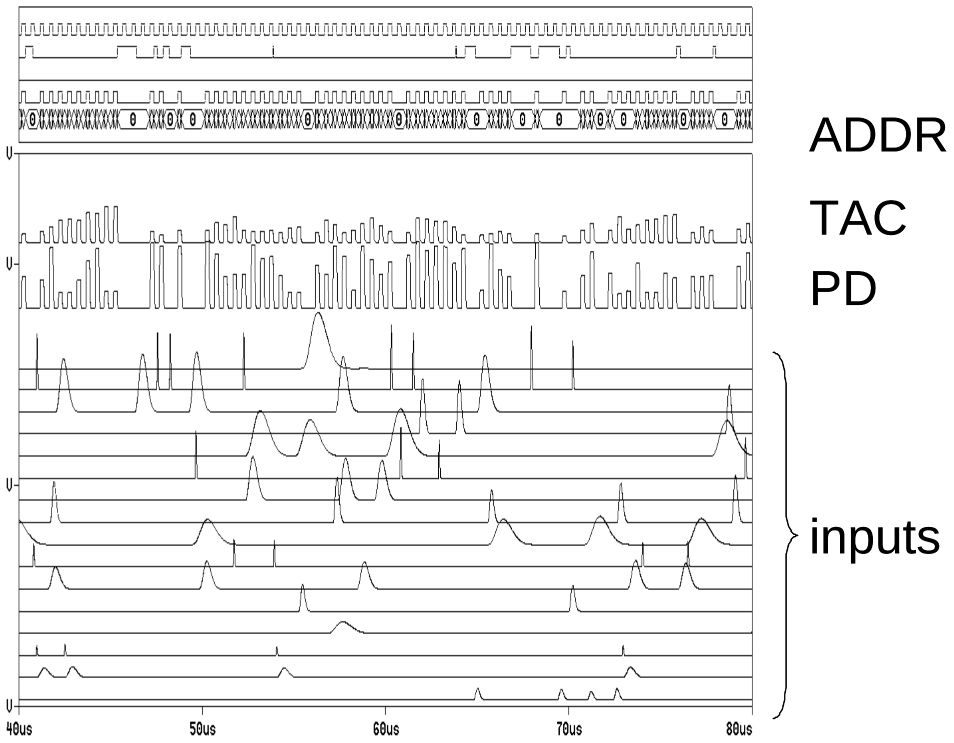
Block diagram



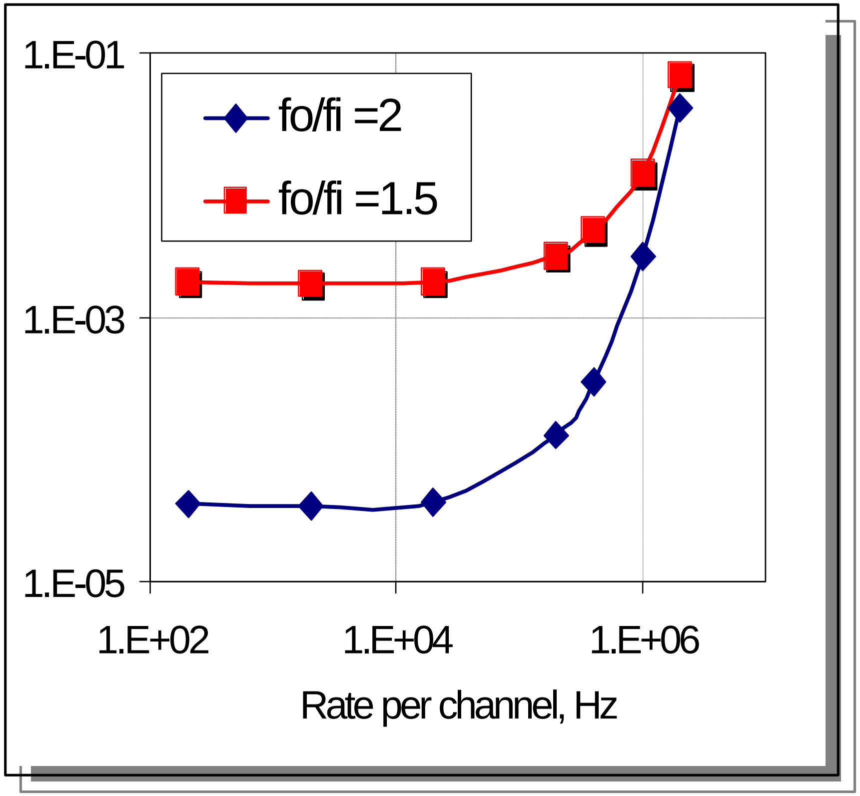
- One-chip solution
- $N_{CHAN} = 32$, $N_{PD} = 8$
- Dual-mode TAC
  - risetime
  - time of occurrence
- Amplitude, address, time outputs
- 50 ns minimum pulsewidth
- $t_{ARB} \sim 5$ ns
- Rate capability ~ 10 MHz
- SPI interface:
  - serial configuration of TAC gain and mode
  - arbitration locking
  - channel exclusion
  - powerdown
  - analog monitor
  - Digital convenience outputs (used for configuring companion amplifier chip)
- FIFO-like control and readout interface

Simulations

Simulation with random inputs



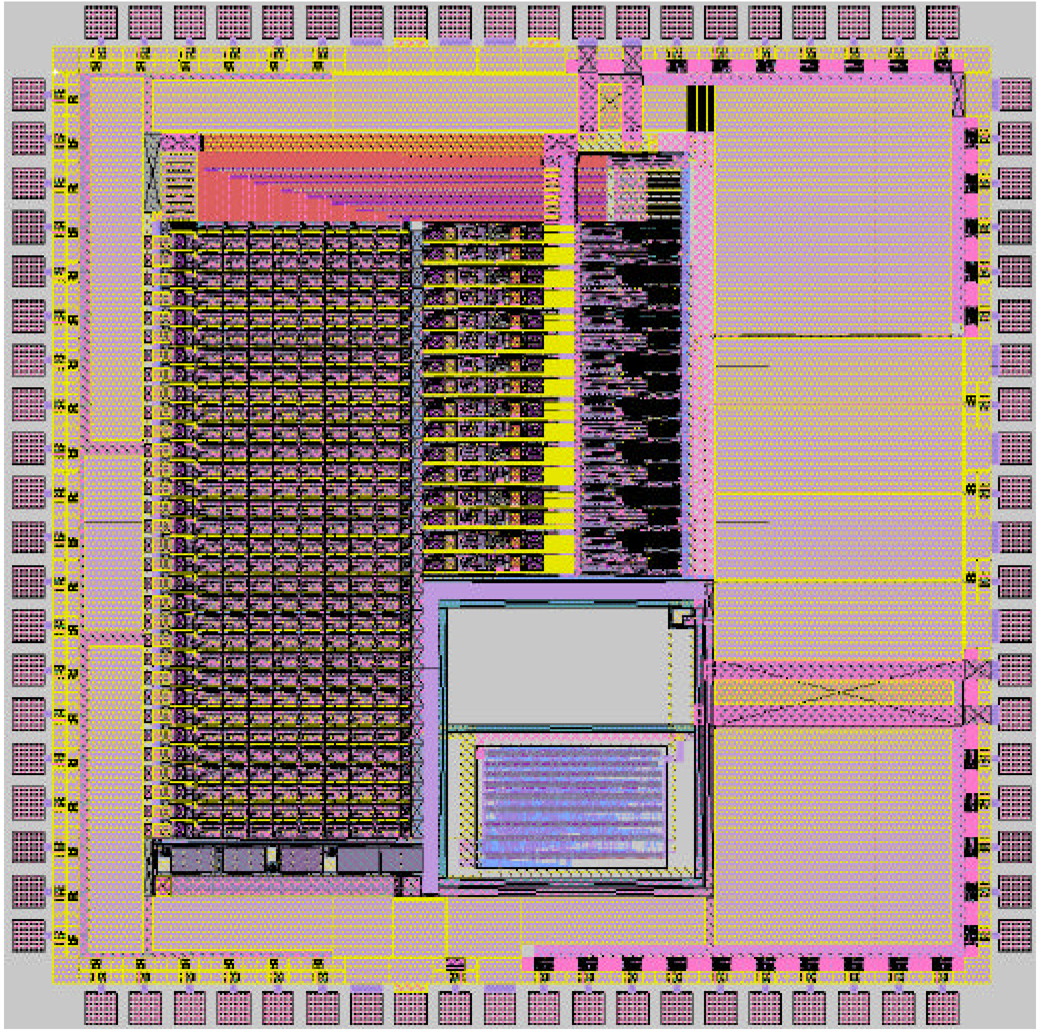
Inefficiency vs. Input Rate



- 1.6 Mcps input rate (16 channels)
- 2 MHz output clock
- Poisson distribution of event times
- Variation of pulsewidth, amplitude

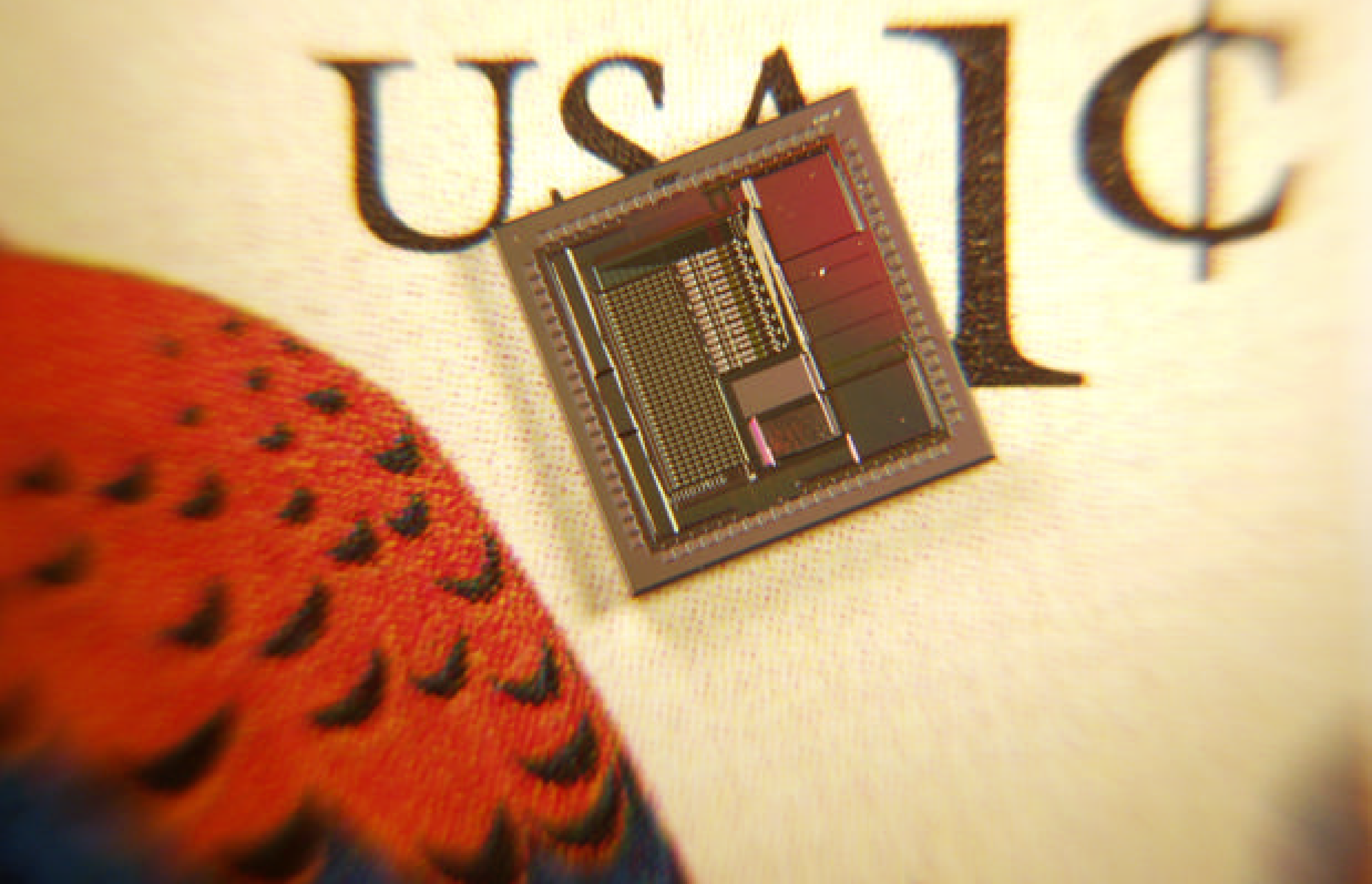
Blocking probability as a function of average input pulse rate, for two ratios of readout rate to input rate (Monte Carlo simulation).

Layout

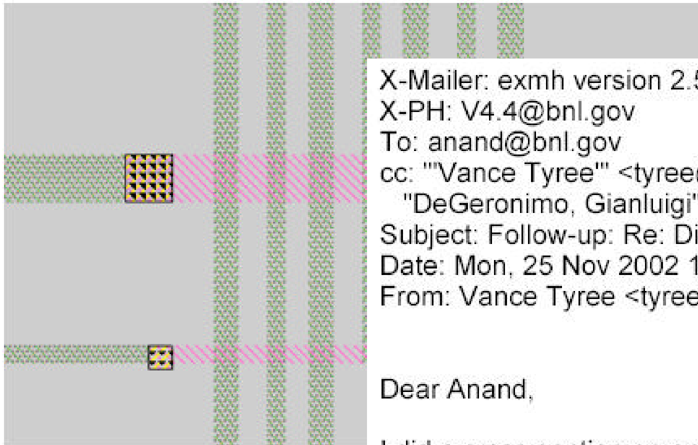


size : 3.2 x 3.2 mm²
power : 2mW / channel
technology: 0.35µm CMOS
DP4M

Die photo



Metallization problems suspected with this run



MAGIC coordinates : (10[illegible]

- Top horizontal M4 line width is 8λ (1.6[illegible]
- Bottom horizontal M4 line width is 3λ ([illegible]
- Spacing between M4 via and vertical [illegible]
- Vertical lines: size 4λ, 3λ, 4λ, 3λ, 4λ, 3[illegible]

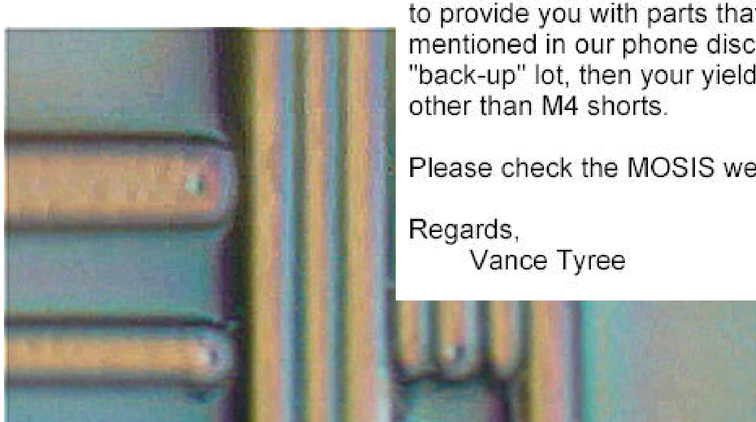
X-Mailer: exmh version 2.5 07/13/2001 with nmh-1.0.4
X-PH: V4.4@bnl.gov
To: anand@bnl.gov
cc: '"Vance Tyree"' <tyree@mosis.org>, "O'Connor, Paul" <poc@bnl.gov>,
"DeGeronimo, Gianluigi" <degeronimo@bnl.gov>, tyree@ISI.EDU
Subject: Follow-up: Re: Die Photographs for Design 65031
Date: Mon, 25 Nov 2002 13:58:39 -0800
From: Vance Tyree <tyree@ISI.EDU>

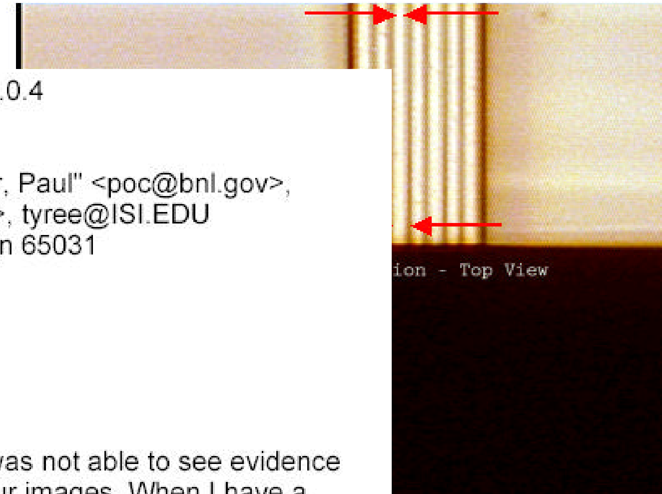
Dear Anand,

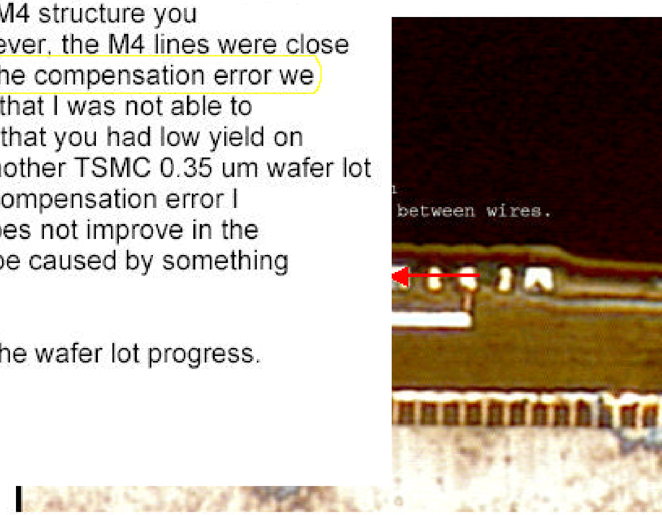
I did a cross section on one of the 65031 die and was not able to see evidence of shorts between the M4 lines you indicated in your images. When I have a little more time, I will cross section further into the M4 structure you indicated looking for evidence of shorted M4. However, the M4 lines were close enough together to be a potential yield issue with the compensation error we found in the mask preparation on that lot. The fact that I was not able to confirm shorted M4 lines does not change the fact that you had low yield on lot T26C. Your chip has already been placed on another TSMC 0.35 um wafer lot to provide you with parts that do not have the M4 compensation error I mentioned in our phone discussion. If your yield does not improve in the "back-up" lot, then your yield problem will have to be caused by something other than M4 shorts.

Please check the MOSIS web page for details on the wafer lot progress.

Regards,
Vance Tyree

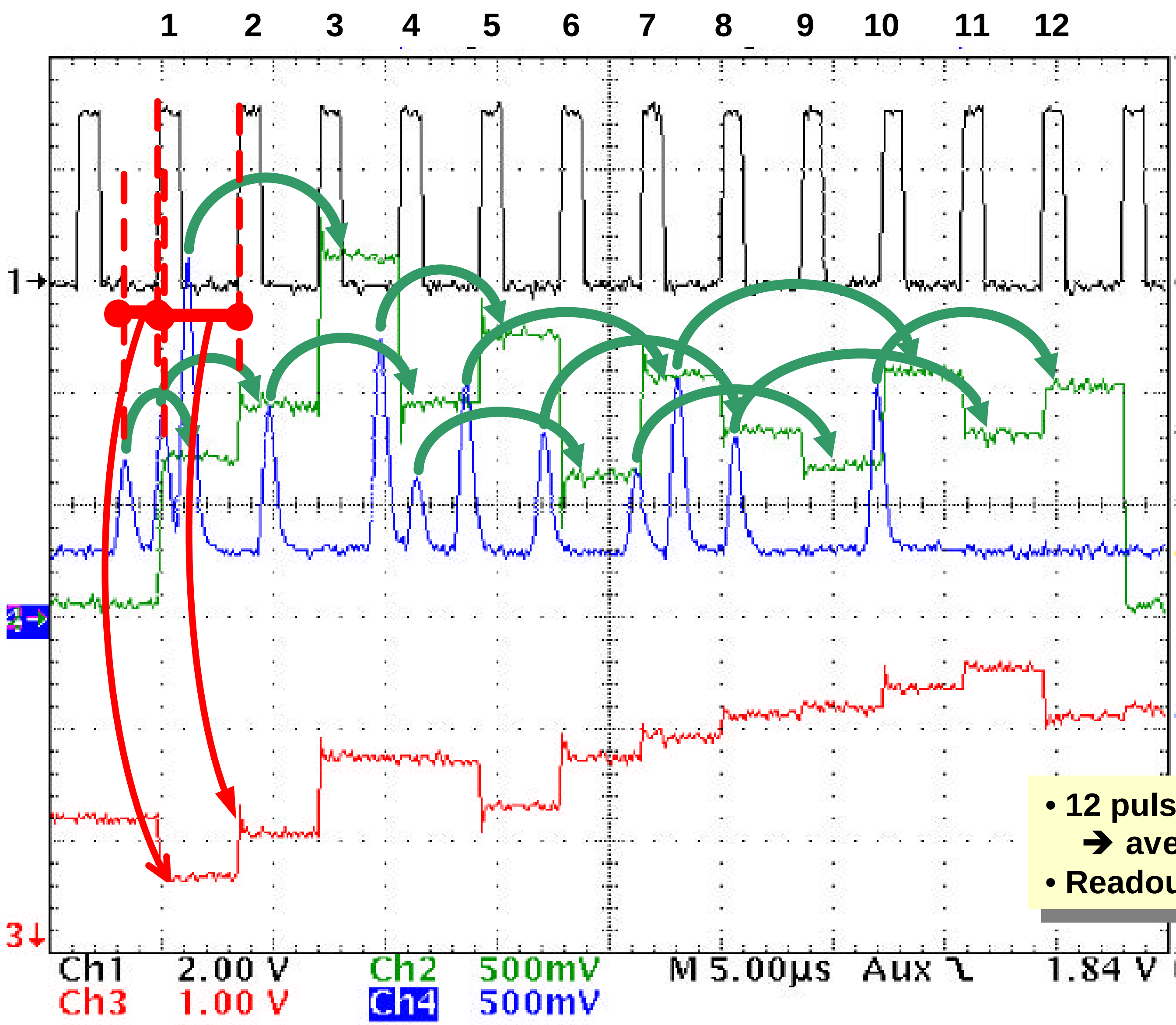






Spacing from layout is 4λ (0.8μm).
Size of left line from layout is 3λ (0.6μm).
Size of right line from layout is 4λ (0.8μm).

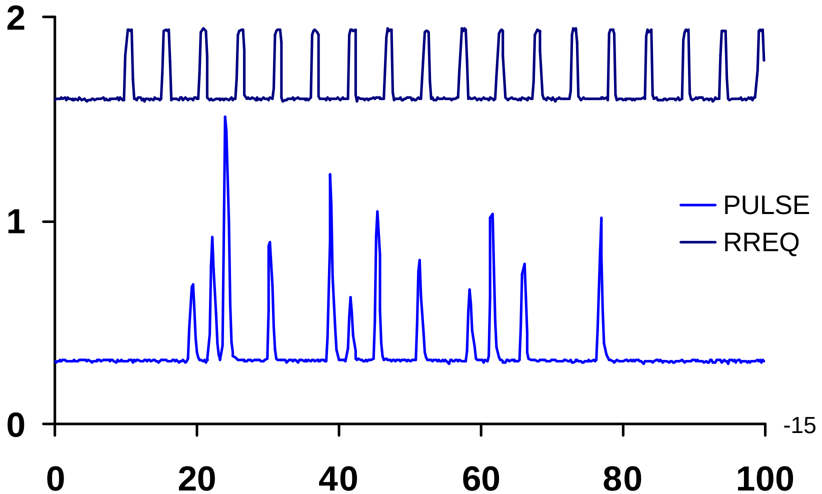
Sampling and derandomization



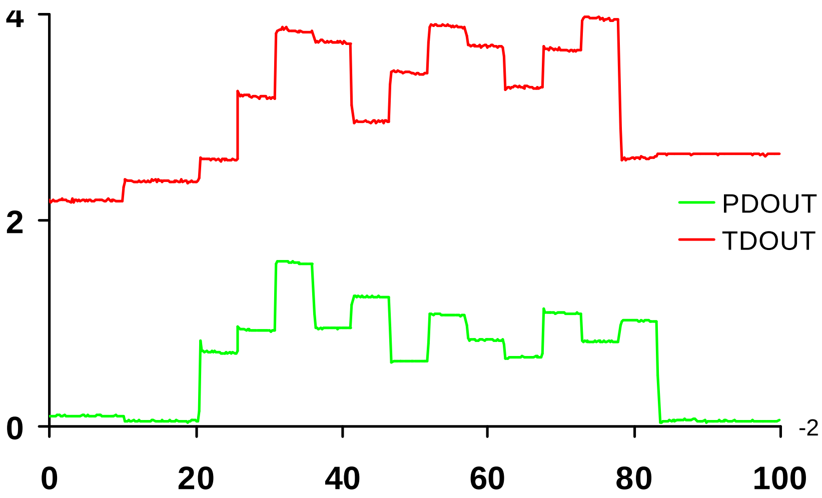
Black – Read Request
Blue – pulse input
Green – PD output
Red – TD output, occurrence time mode

- 12 pulses in 35 ms
  ➔ average rate 340 kHz
- Readout rate 275 kHz

Reconstruction of peak height and time

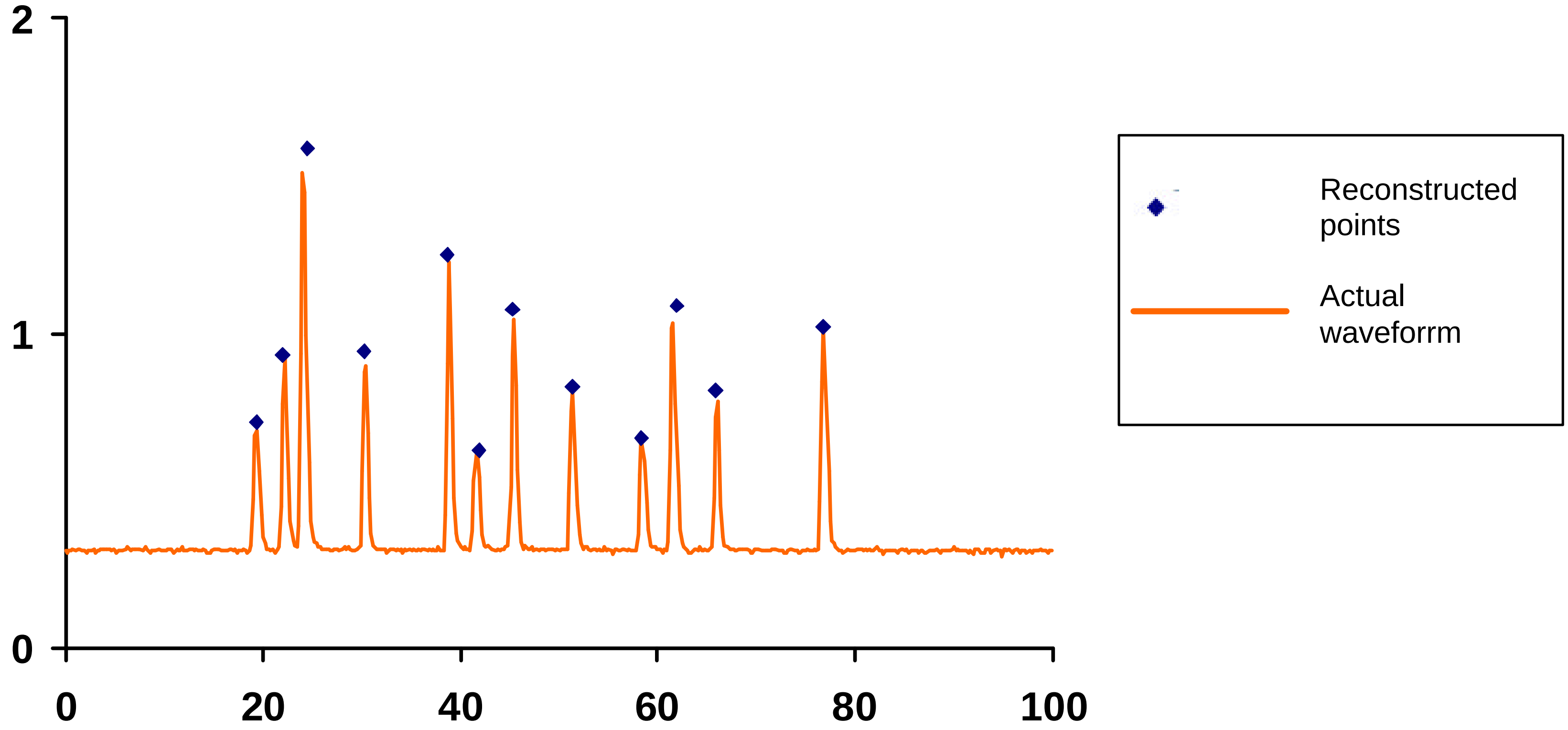


ASIC Inputs



ASIC Outputs

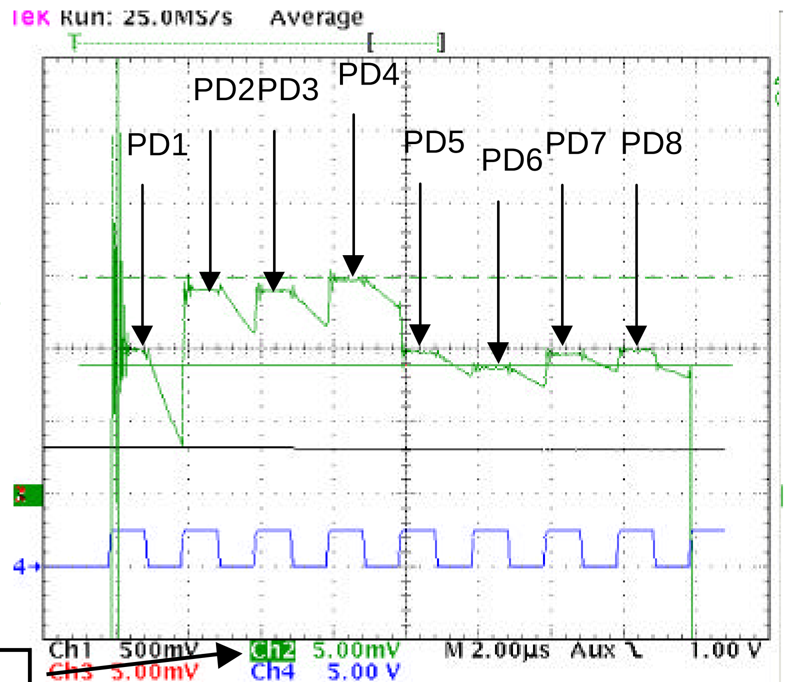
Reconstruction of peak height and time



Peak detector accuracy

PDOUT

RREQ



NOTE 5 mV/div

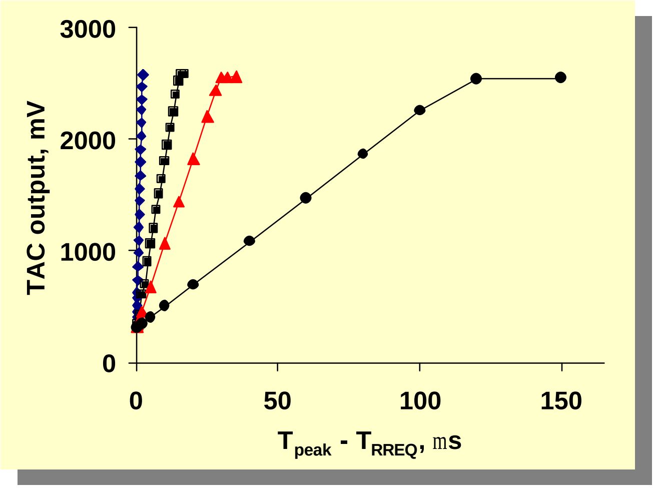
Pulse	Peak Ht. (mV)	PDOUT (mV)	Error* (mV)
1	949.9	948.2	-1.7
2	954.1	948.6	-5.5
3	954.1	948.7	-5.4
4	954.9	948.9	-6
5	950.0	948.8	-1.2
6	948.8	949.0	0.2
7	949.5	949.3	-0.2
8	950.0	949.1	-0.9

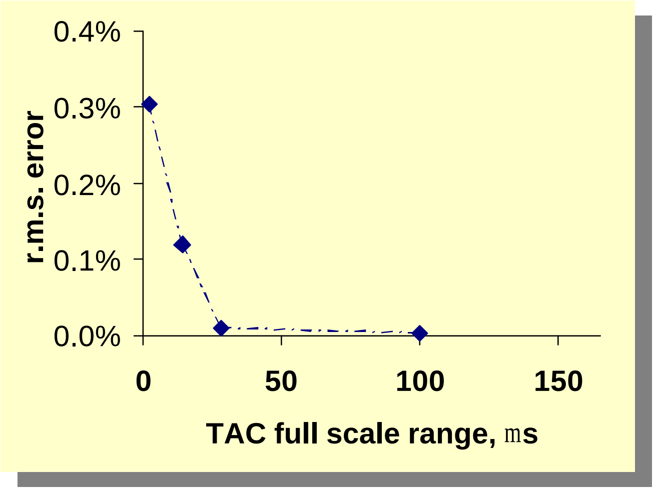
Uniformity:
2.59 mV r.m.s.

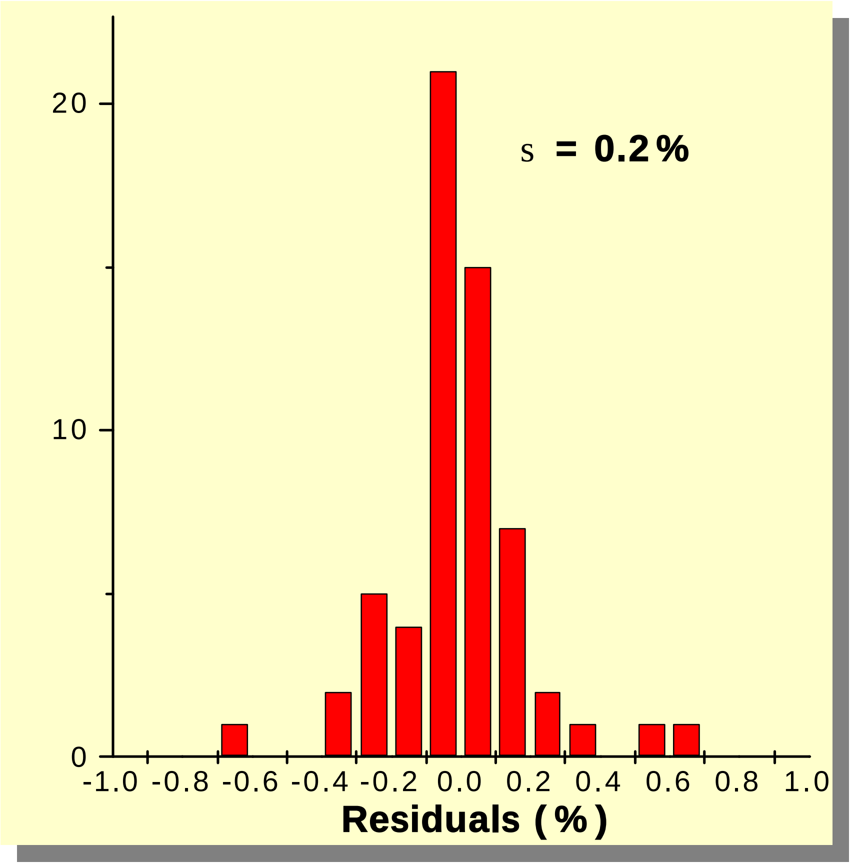
8 “identical” pulses into CH1. RREQ burst follows after ~ 5 µs.
Peak height. PDOUT measured on TDS784 scope, Ch.1 and 2.
*Absolute accuracy results so far don’t consider op-amp, scope offsets.

TAC results

Occurrence time mode

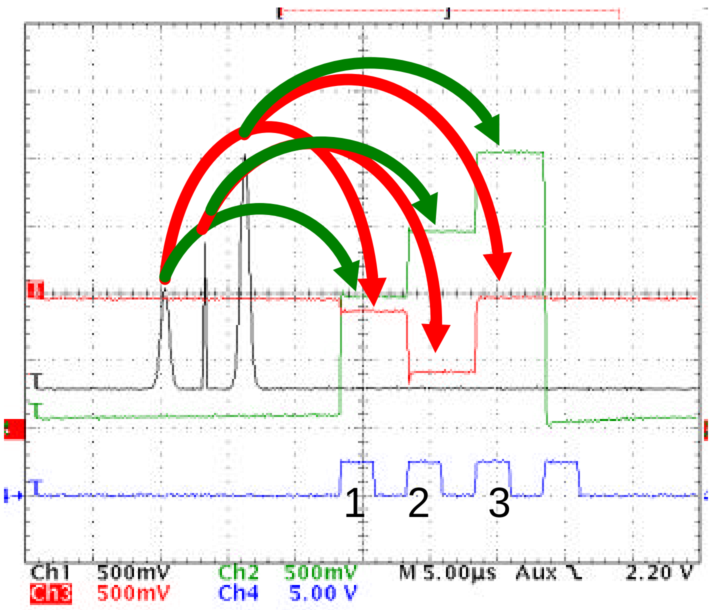






TAC results

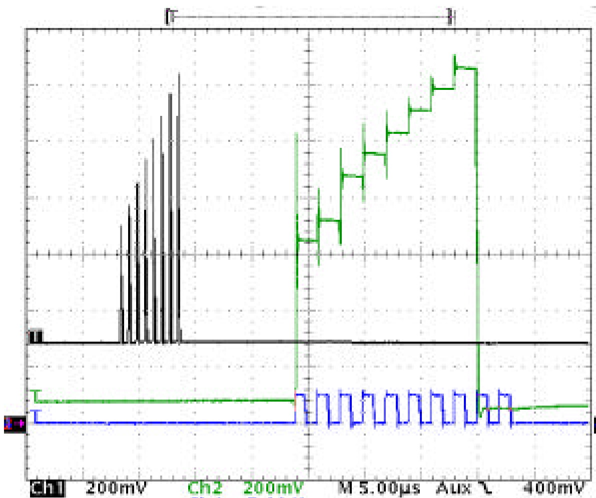
Risetime mode



Black – pulse input
Blue – READ REQUEST
Green – PD output
Red – TAC output, risetime mode

High rate capability

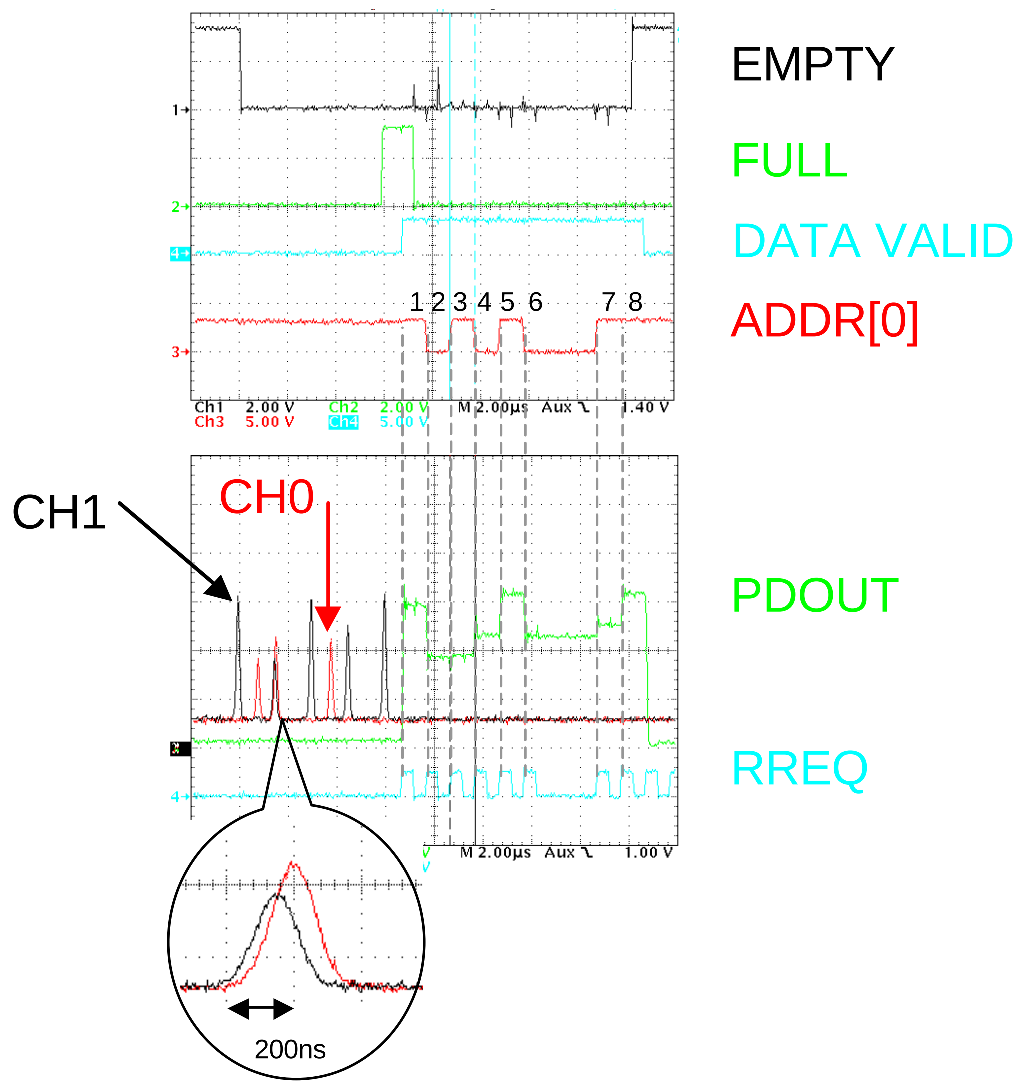
Fast pulses, high rate



Black – pulse input
Blue – Read Request
Green – PD output

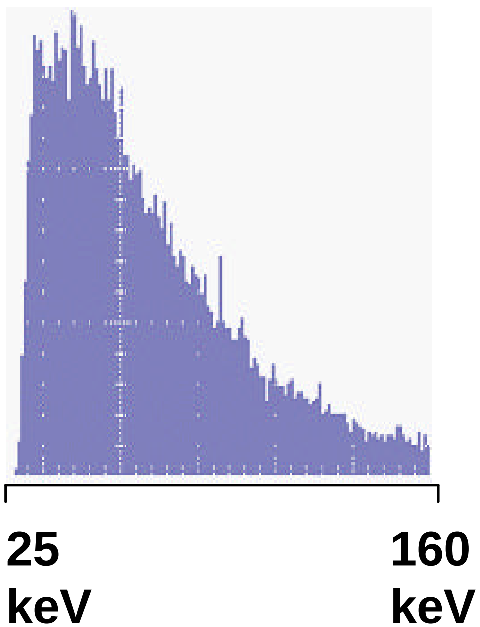
- Input pulses:
  - 30 ns peaking time
  - 1.6 MHz rate
- Readout rate 500 kHz

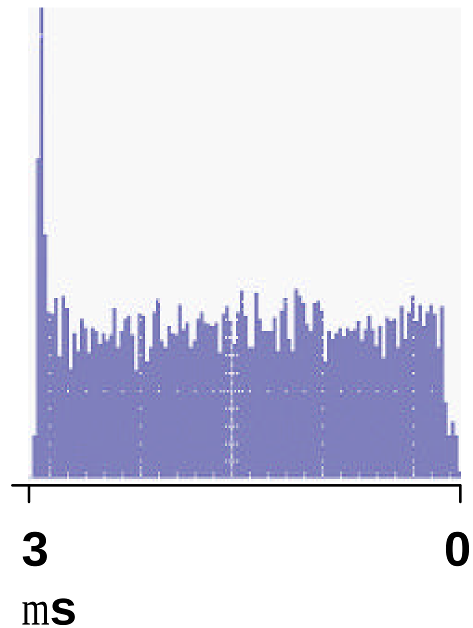
Fast channel-channel arbitration

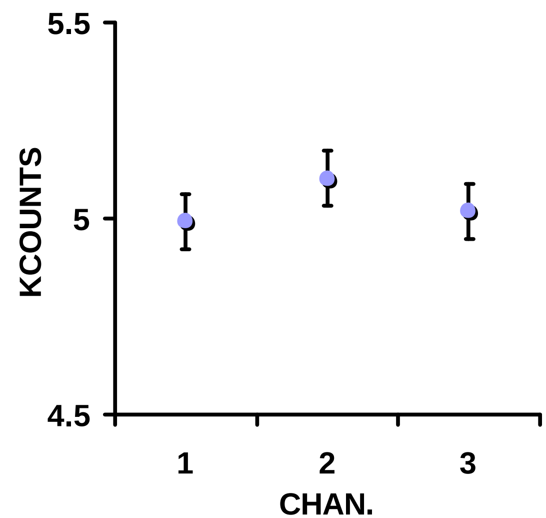


First results with CdZnTe detectors

Peak amplitude	Time wrt RREQ	Address



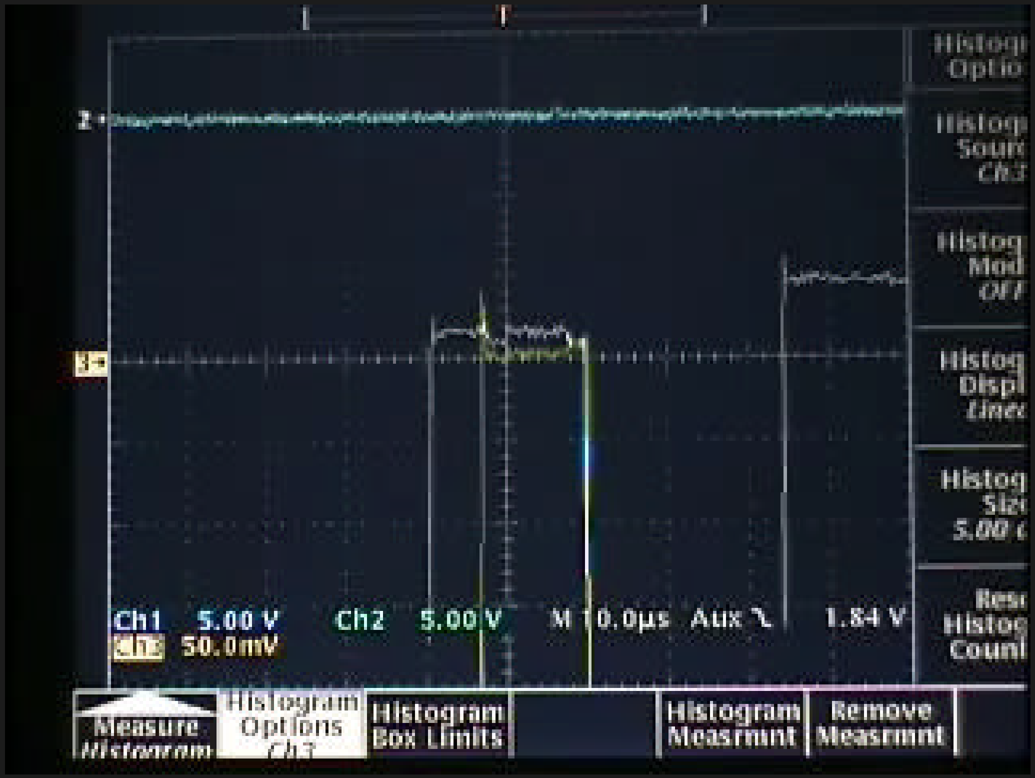




f_{RREQ} = 250 kHz
Peaking time 500ns
Cosmic ray source, rate ~ 1 Hz

Peak height, amplitude spectrum, address

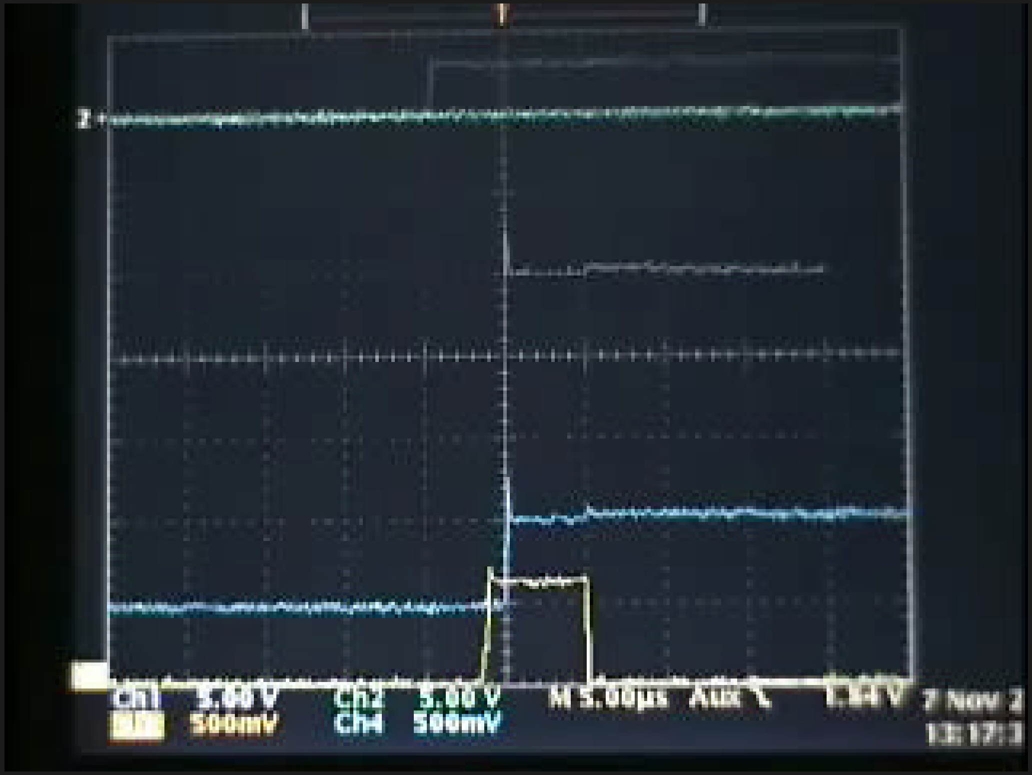
HISTOGRAM



ADDR[1:0]

PD OUT

Peak height, time, address

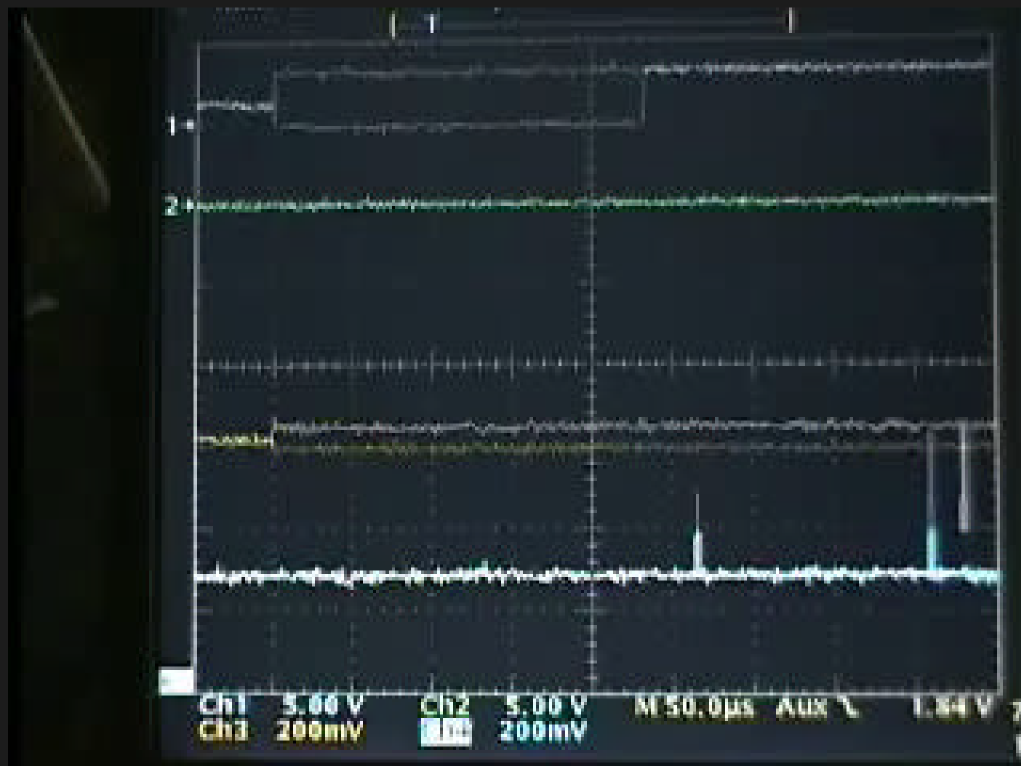


ADDR[1:0]

TDOUT

PD OUT

f_{RREQ} sweep



FULL

EMPTY

PD OUT

PULSE IN

Summary

- New architecture for efficient readout of multichannel detectors
  - *Self-triggered and self-sparsifying*
  - *High efficiency at high concentration ratio*
  - *Rate capability improvement over present architectures*
- Based on new 2-phase peak detector combined with dual-mode TAC
  - *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
  - *Low power (2 mW per channel)*
- Experimental 32-channel chip demonstrated
  - *Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel*
  - *Crosspoint switch and 8-event buffer for high efficiency*
  - *Simultaneous amplitude, time, and address measurement*

BACKUPS

Summary

- New architecture for efficient readout of multichannel detectors
    - *Self-triggered and self-sparsifying*
    - *High efficiency at high concentration ratio*
- Based on new 2-phase peak detector combined with dual-mode TAC
    - *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
    - *Low power (2 mW)*
- Peak detector – derandomizer (PDD-1) with 2-event buffer demonstrated:

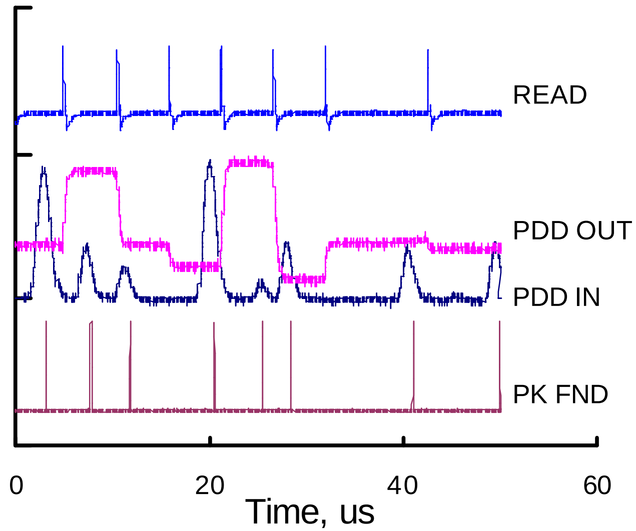
- Peak detector array shared by all channels
- $N_{CHAN} = 32$, $N_{PD} = 8$
- Dual-mode TAC using timing signal from PDs can measure:
  - risetime
  - time of occurrence
- Amplitude, time, channel address outputs
- 50 ns minimum pulsewidth
- $t_{ARB} \sim 5$ ns
- Rate capability ~ 10 MHz
- FIFO-like control and readout interface
- A prototype having $N_{PD}=2$ has been studied experimentally (PDD1)

Comparison of readout architectures

Architecture	Max. rate	No. digitizations per pulse	Example: N_{CH}=32, f_{mux}=5 MHz, N_{SAMP}=3, 1-e = 99%	
			R_{max}	N_{dig}
Track/Hold + Mux	$\frac{f_{MUX} \cdot F(e,1)}{N_{CH}}$	N_{CH}	23 kHz	32
Analog pipeline + Mux	$\frac{f_{MUX} \cdot F(e,N_{BUF})}{N_{CH} \cdot N_{SAMP}}$	$N_{CH} \cdot N_{SAMP}$	52 kHz	96
PDD-2	$f_{MUX} \cdot F(e,N_{PD})$	1.2 ~ 2	3.3 MHz	1

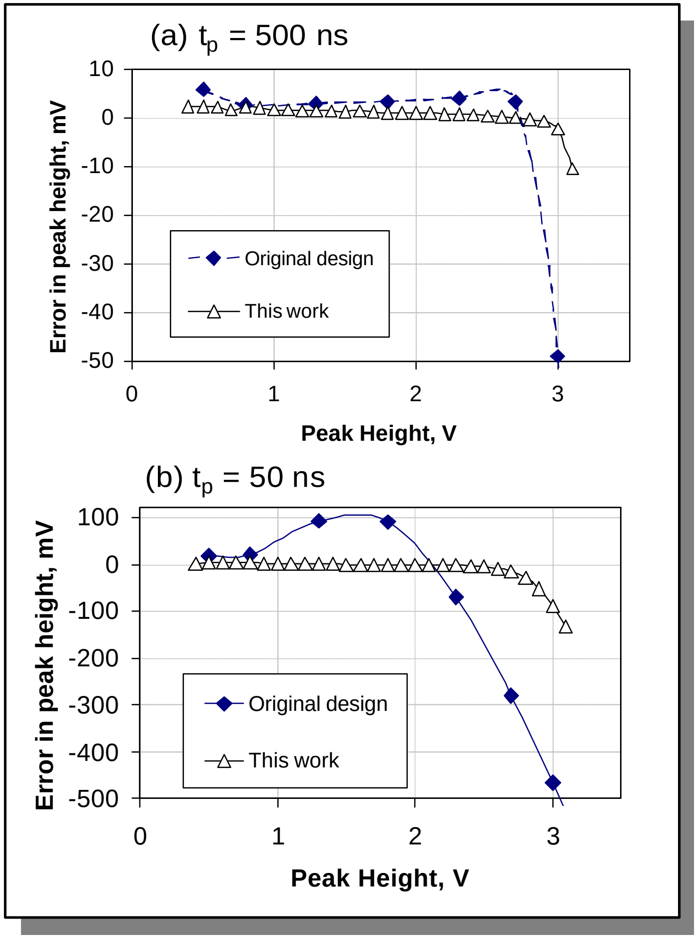
f_{MUX}	Analog multiplexer rate
N_{CH}	No. of channels/chip
N_{BUF}	No. of buffer cells in pipeline
N_{PD}	No. of peak detectors in PDD
N_{SAMP}	No. of pipeline samples read out per pulse
$F(e,N)$	Poisson factor to get inefficiency ε given N buffer locations: For ε = 1%, F(ε,1) ~ 0.15, F(ε,8) ~ 1

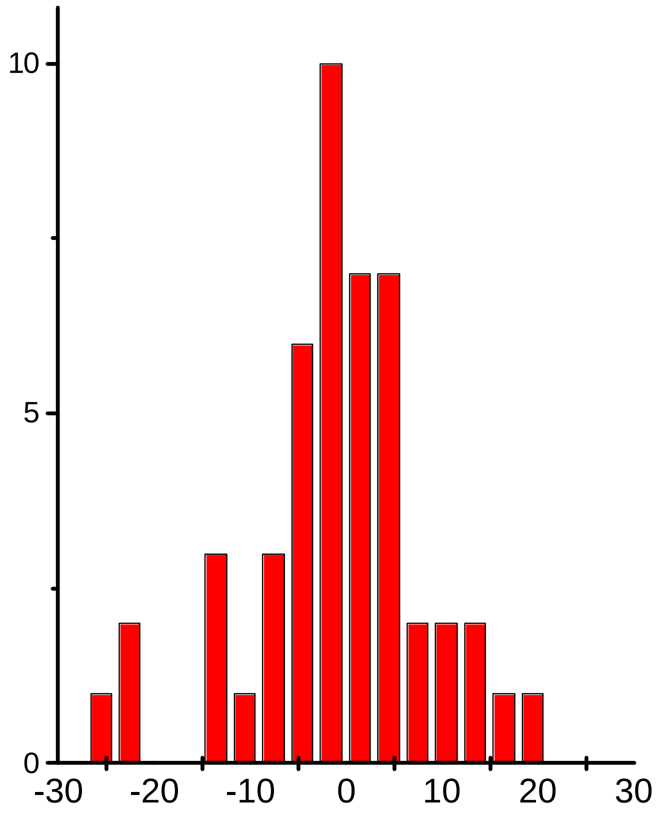
Waveforms



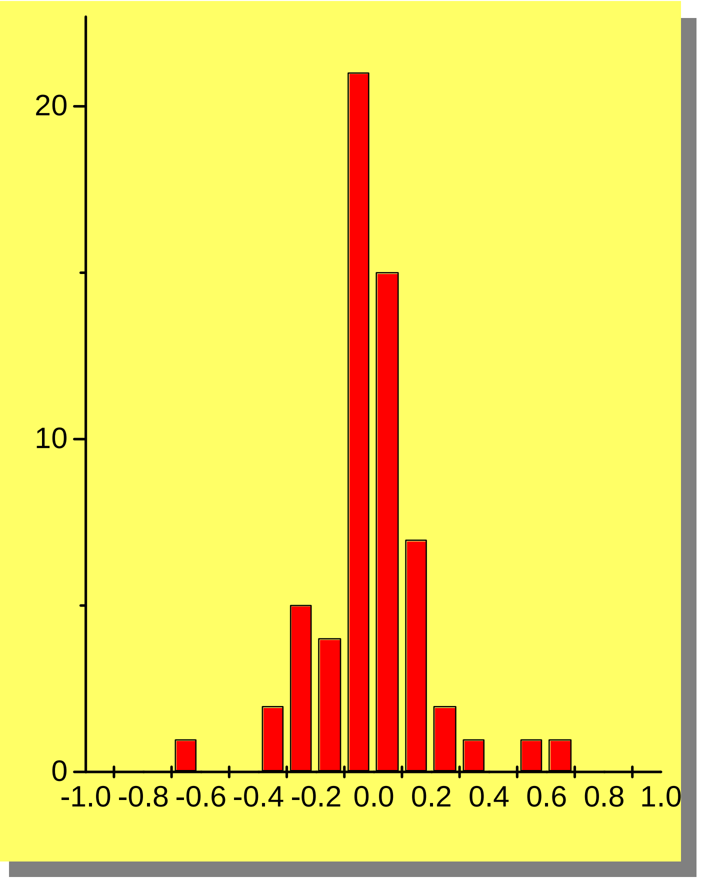
Parameter:	Value: PDD-1 (PDD-2)
Technology	0.35 um CMOS DP4M
Supply voltage	3.3V
Input voltage range	0.3 - 3.0 V
Minimum pulse width	500 (50) ns
Absolute accuracy	0.20%
Linearity	0.05%
Droop rate	250 mV/s
Timing accuracy	5 ns
Power dissipation	3.5 (2.0) mW/chan

Amplitude Accuracy

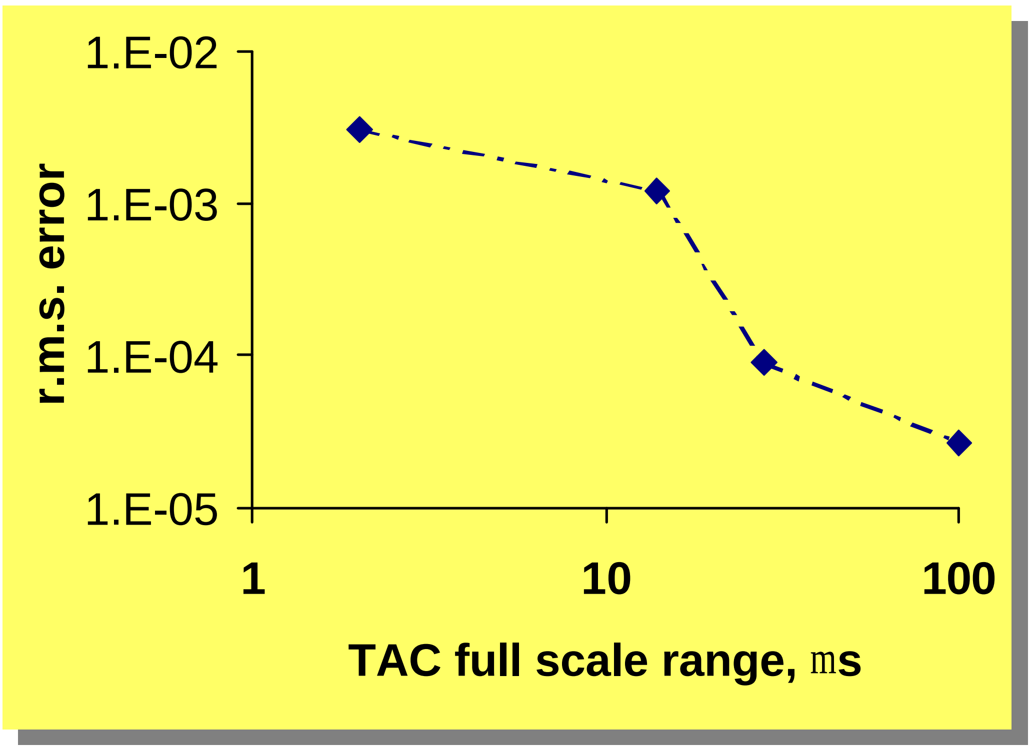




10
5
0
-30
-20
-10
0
10
20
30



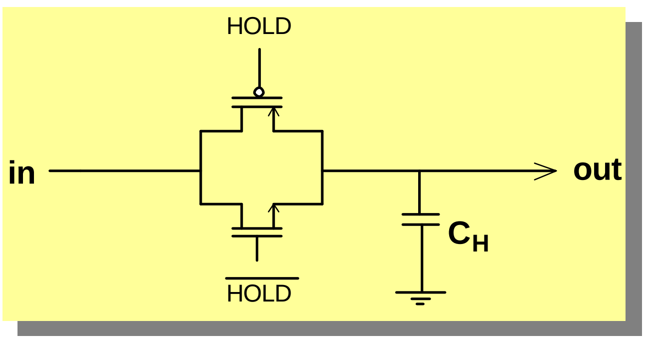
20
10
0
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0



1.E-02
1.E-03
1.E-04
1.E-05
r.m.s. error
1
10
100
TAC full scale range, ms

Candidate sampling/memory cells in CMOS

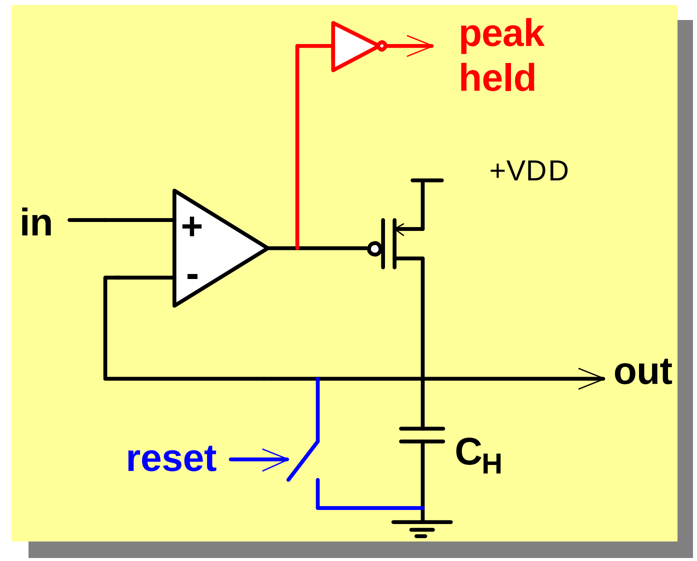
Sample/hold using switched capacitor



- small
- low-power

- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

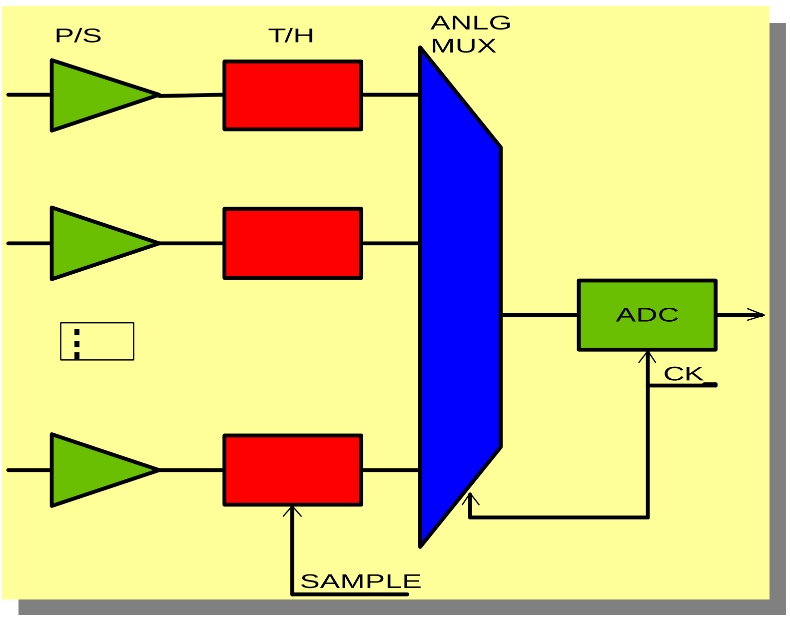
Peak Detector (PD)

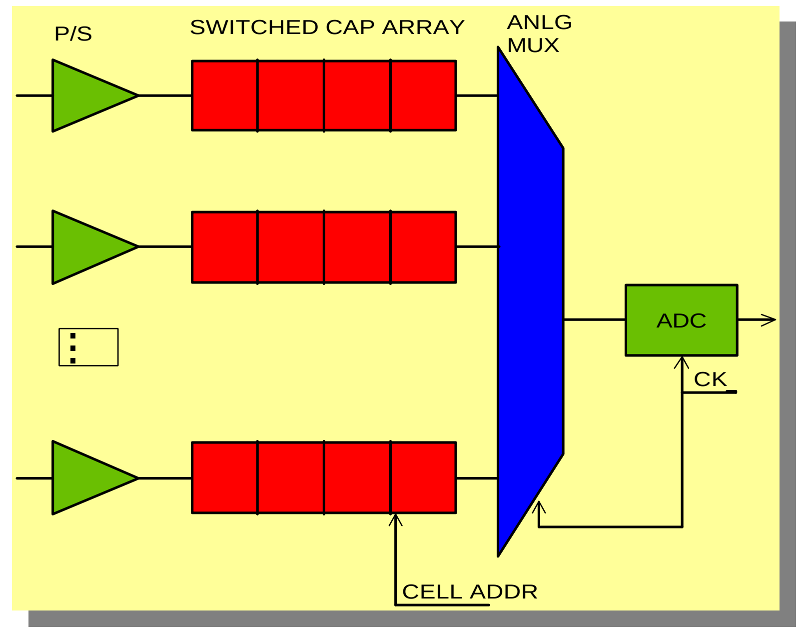


- self-triggered
- timing output
- feedback loop

- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate

Conventional Architectures Based on Switched-Capacitor Sampling





Both these conventional techniques require a trigger to identify the hit time. After sampling the pulse, all channels are sent sequentially to the multiplexer. This approach can provide high integration density (e.g., 128 channels per chip) but only at the expense of long readout time.