An Amplitude and Time Measurement ASIC with Analog Derandomization

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Highly segmented detectors

**Benefits:**
- **Position Resolution**
  - pixel pitch $\sim \frac{1}{\sqrt{N}}$
- **Energy resolution:**
  - $C_{DET} \sim \frac{1}{N}$
  - $I_{DARK} \sim \frac{1}{N}$
  - pulse shaping time $\sim N$
- **Rate capability**
  - pileup $\sim \frac{1}{N}$
- **“Small pixel” effect**
  - improve energy resolution in detectors with poor hole transport

**Drawbacks:**
- **Interconnect density**
  - density $\sim N$
- **Electronics channel count**
  - cost $\sim N$
  - power $\sim N$
**Data-concentrating architectures**

- **Track-and-Hold + Analog Multiplex**
  - Unbuffered => deadtime
  - Long readout time
  - Needs accurate trigger

- **Analog Memory + Analog Multiplex**
  - Can be deadtimeless
  - Complex control
  - Long readout time
  - Needs trigger + multiple samples

**Both:**
- Buy high integration at the price of efficiency
- Problems in untriggered systems
Flash ADC approach

6912 samples
6 data points
Track-and-hold + analog MUX approach

- Trigger jitter
- Time (inputs blocked)
- Multiplexer readout

48 samples
1 data point
Analog memory approach

- Sampling window
- Trigger latency
- Multiplexer readout time (inputs blocked)
- 192 samples
- 1 data point
Efficient analog data concentration ASIC (analog FIFO)

- Self-triggered sampling system
  - independent per-channel triggers
  - negligible time walk
- Sparse readout
  - skip unoccupied channels
- Buffer “memory”
  - analog storage for 4 – 8 events

- NO
  - external trigger
  - sample/hold
  - timing controls
Improved CMOS PD Using Two-Phase Configuration

**Write phase**
- conventional peak detector
- M1: unidirectional current source
- voltage on C_H includes op-amp errors (offset, CMRR)

**Read phase**
- same op-amp re-used as unity-gain buffer
- same CM voltage
  - *op-amp errors cancel*
- enables rail-to-rail sensing
- provides good drive capability

U.S. Pat. 6,512,399
Time Detector – risetime mode
Time Detector – time of occurrence mode

**Diagram Description:**
- **PD** (Peak Finder): Outputs pk fnd.
- **TAC** (Time to Amplitude Converter): Inputs start and stop, Outputs TAC out.
- **Threshold Comparator**: Outputs disc out.
- **Input (in)** feeds into PD.
- **Output (PD out)** is connected to TAC.
- **RREQ** (Request) connects to TAC.

**Waves Diagram:**
- **PULSE**
- **DISC OUT**
- **PK FND**
- **RREQ**
- **TAC OUT**
Derandomizing architectures

One PD per channel
- self-triggering
- unbuffered -> deadtime
- long readout time

Multiple PDs per channel
- self-triggering
- buffered
- long readout time
- high power dissipation ($N_{PD} > N_{CHAN}$)

Multiple PDs shared by all channels
- self-triggering
- buffered
- reduced readout time
- reduced power dissipation ($N_{PD} < N_{CHAN}$)
• One-chip solution
• \( N_{\text{CHAN}} = 32, \ N_{\text{PD}} = 8 \)
• Dual-mode TAC
  – risetime
  – time of occurrence
• Amplitude, address, time outputs
• 50 ns minimum pulsewidth
• \( t_{\text{ARB}} \sim 5 \text{ ns} \)
• Rate capability \( \sim 10 \text{ MHz} \)
• SPI interface:
  – serial configuration of TAC gain and mode
  – arbitration locking
  – channel exclusion
  – powerdown
  – analog monitor
  – Digital convenience outputs (used for configuring companion amplifier chip)
• FIFO-like control and readout interface
Simulations

Simulation with random inputs

- 1.6 Mcps input rate (16 channels)
- 2 MHz output clock
- Poisson distribution of event times
- Variation of pulsewidth, amplitude

Inefficiency vs. Input Rate

Blocking probability as a function of average input pulse rate, for two ratios of readout rate to input rate (Monte Carlo simulation).
Layout

size: 3.2 x 3.2 mm²
power: 2mW / channel
technology: 0.35µm CMOS DP4M
Die photo
Metallization problems suspected with this run

Dear Anand,

I did a cross section on one of the 65031 die and was not able to see evidence of shorts between the M4 lines you indicated in your images. When I have a little more time, I will cross section further into the M4 structure you indicated looking for evidence of shorted M4. However, the M4 lines were close enough together to be a potential yield issue with the compensation error we found in the mask preparation on that lot. The fact that I was not able to confirm shorted M4 lines does not change the fact that you had low yield on lot T26C. Your chip has already been placed on another TSMC 0.35 um wafer lot to provide you with parts that do not have the M4 compensation error I mentioned in our phone discussion. If your yield does not improve in the “back-up” lot, then your yield problem will have to be caused by something other than M4 shorts.

Please check the MOSIS web page for details on the wafer lot progress.

Regards,

Vance Tyree

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X-Mailer: axmh version 2.5 07/13/2001 with nmh-1.0.4
X-PH: V4.4@bnl.gov
To: anand@bnl.gov
cc: "Vance Tyree" <tyree@mosis.org>, "O'Connor, Paul" <pc@bnl.gov>, "DeGeronimo, Gianluigi" <degeronimo@bnl.gov>, tyree@ISI.EDU
Subject: Follow-up: Re: Die Photographs for Design 65031
Date: Mon, 25 Nov 2002 13:58:39 -0800
From: Vance Tyree <tyree@ISI.EDU>
Sampling and derandomization

Black – Read Request
Blue – pulse input
Green – PD output
Red – TD output, occurrence time mode

• 12 pulses in 35 $\mu$s
  ➔ average rate 340 kHz
• Readout rate 275 kHz
Reconstruction of peak height and time

ASIC Inputs

ASIC Outputs
Reconstruction of peak height and time

![Graph showing the reconstruction of peak height and time with reconstructed points and actual waveform.]
Peak detector accuracy

8 “identical” pulses into CH1. RREQ burst follows after ~ 5 µs.
Peak height. PDOUT measured on TDS784 scope, Ch.1 and 2.
*Absolute accuracy results so far don’t consider op-amp, scope offsets.

Uniformity:
2.59 mV r.m.s.

<table>
<thead>
<tr>
<th>Pulse</th>
<th>Peak Ht. (mV)</th>
<th>PDOUT (mV)</th>
<th>Error* (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>949.9</td>
<td>948.2</td>
<td>-1.7</td>
</tr>
<tr>
<td>2</td>
<td>954.1</td>
<td>948.6</td>
<td>-5.5</td>
</tr>
<tr>
<td>3</td>
<td>954.1</td>
<td>948.7</td>
<td>-5.4</td>
</tr>
<tr>
<td>4</td>
<td>954.9</td>
<td>948.9</td>
<td>-6</td>
</tr>
<tr>
<td>5</td>
<td>950.0</td>
<td>948.8</td>
<td>-1.2</td>
</tr>
<tr>
<td>6</td>
<td>948.8</td>
<td>949.0</td>
<td>0.2</td>
</tr>
<tr>
<td>7</td>
<td>949.5</td>
<td>949.3</td>
<td>-0.2</td>
</tr>
<tr>
<td>8</td>
<td>950.0</td>
<td>949.1</td>
<td>-0.9</td>
</tr>
</tbody>
</table>

NOTE 5

mV/div

Uniformity:
2.59 mV r.m.s.
TAC results

Occurrence time mode

\[
\begin{align*}
\text{TAC full scale range, } \mu\text{s} & \quad 0 & \quad 50 & \quad 100 & \quad 150 \\
\text{TAC output, mV} & \quad 0 & \quad 500 & \quad 1000 & \quad 1500 & \quad 2000 & \quad 2500 & \quad 3000 \\
\text{r.m.s. error} & \quad 0 & \quad 0.1 & \quad 0.2 & \quad 0.3 & \quad 0.4 & \quad 0.5 & \quad 0.6 & \quad 0.7 & \quad 0.8 & \quad 0.9 & \quad 1.0
\end{align*}
\]

\[
\begin{align*}
\text{T}_\text{peak} - \text{T}_\text{RREQ}, \mu\text{s} & \quad 0 & \quad 50 & \quad 100 & \quad 150 & \quad 200 & \quad 250 & \quad 300 \\
\text{TAC output, mV} & \quad 0 & \quad 500 & \quad 1000 & \quad 1500 & \quad 2000 & \quad 2500 & \quad 3000
\end{align*}
\]

\[
\sigma = 0.2\%
\]
TAC results

Risetime mode

Black – pulse input
Blue – READ REQUEST
Green – PD output
Red – TAC output, risetime mode
High rate capability

Fast pulses, high rate

Input pulses:
- 30 ns peaking time
- 1.6 MHz rate
- Readout rate 500 kHz

Black – pulse input
Blue – Read Request
Green – PD output

Fast channel-channel arbitration

EMPTY
FULL
DATA VALID
ADDR[0]
PDOUT
RREQ

CH1

CH0

200ns
First results with CdZnTe detectors

<table>
<thead>
<tr>
<th>Peak amplitude</th>
<th>Time wrt RREQ</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 keV</td>
<td>3 μs</td>
<td>0</td>
</tr>
<tr>
<td>160 keV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$f_{RREQ} = 250$ kHz
Peaking time 500ns
Cosmic ray source, rate ~ 1 Hz
Peak height, amplitude spectrum, address

ADD[1:0]

PD OUT

HISTOGRAM
Peak height, time, address
\( f_{RREQ} \) sweep

- FULL
- EMPTY
- PD OUT
- PULSE IN
Summary

• New architecture for efficient readout of multichannel detectors
  • Self-triggered and self-sparsifying
  • High efficiency at high concentration ratio
  • Rate capability improvement over present architectures

• Based on new 2-phase peak detector combined with dual-mode TAC
  • High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)
  • Low power (2 mW per channel)

• Experimental 32-channel chip demonstrated
  • Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel
  • Crosspoint switch and 8-event buffer for high efficiency
  • Simultaneous amplitude, time, and address measurement
BACKUPS
Summary

• New architecture for efficient readout of multichannel detectors
  • Self-triggered and self-sparsifying
  • High efficiency at high concentration ratio

• Based on new 2-phase peak detector combined with dual-mode TAC
  • High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)
  • Low power (2 mW)

• Peak detector – derandomizer (PDD-1) with 2-event buffer demonstrated:
• Peak detector array shared by all channels
• \(N_{CHAN} = 32, N_{PD} = 8\)
• Dual-mode TAC using timing signal from PDs can measure:
  - risetime
  - time of occurrence
• Amplitude, time, channel address outputs
• 50 ns minimum pulsewidth
• \(t_{ARB} \sim 5\) ns
• Rate capability \(\sim 10\) MHz
• FIFO-like control and readout interface
• A prototype having \(N_{PD}=2\) has been studied experimentally (PDD1)
## Comparison of readout architectures

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Max. rate</th>
<th>No. digitizations per pulse</th>
<th>Example: $N_{CH}=32$, $f_{mux}=5$ MHz, $N_{SAMP}=3$, $1-\varepsilon = 99%$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Track/Hold + Mux</td>
<td>$f_{MUX} \cdot F(\varepsilon,1)$ (\frac{1}{N_{CH}})</td>
<td>$N_{CH}$</td>
<td>$R_{\text{max}}$ = 23 kHz, $N_{dig} = 32$</td>
</tr>
<tr>
<td>Analog pipeline + Mux</td>
<td>$f_{MUX} \cdot F(\varepsilon,N_{BUF})$ (\frac{1}{N_{CH} \cdot N_{SAMP}})</td>
<td>$N_{CH} \cdot N_{SAMP}$</td>
<td>$R_{\text{max}}$ = 52 kHz, $N_{dig} = 96$</td>
</tr>
<tr>
<td>PDD-2</td>
<td>$f_{MUX} \cdot F(\varepsilon,N_{PD})$</td>
<td>1.2 to 2</td>
<td>$R_{\text{max}}$ = 3.3 MHz, $N_{dig} = 1$</td>
</tr>
</tbody>
</table>

- $f_{MUX}$: Analog multiplexer rate
- $N_{CH}$: No. of channels/chip
- $N_{BUF}$: No. of buffer cells in pipeline
- $N_{PD}$: No. of peak detectors in PDD
- $N_{SAMP}$: No. of pipeline samples read out per pulse
- $F(\varepsilon, N)$: Poisson factor to get inefficiency $\varepsilon$ given $N$ buffer locations:
  - For $\varepsilon = 1\%$, $F(\varepsilon,1) \approx 0.15$, $F(\varepsilon,8) \approx 1$
Parameter: Value: PDD-1 (PDD-2)
Technology 0.35 um CMOS DP4M
Supply voltage 3.3V
Input voltage range 0.3 - 3.0 V
Minimum pulse width 500 (50) ns
Absolute accuracy 0.20%
Linearity 0.05%
Droop rate 250 mV/s
Timing accuracy 5 ns
Power dissipation 3.5 (2.0) mW/chan
Candidate sampling/memory cells in CMOS

Sample/hold using switched capacitor

- small
- low-power
- timing of hold signal: needs CFD for walk-free operation
- switch charge injection
- poor drive capability: needs output amp

Peak Detector (PD)

- self-triggered
- timing output
- feedback loop
- deadtime until readout reset
- poor drive capability
- accuracy impaired by opamp offsets, CMRR, slew rate
Conventional Architectures Based on Switched-Capacitor Sampling

Both these conventional techniques require a trigger to identify the hit time. After sampling the pulse, all channels are sent sequentially to the multiplexer. This approach can provide high integration density (e.g., 128 channels per chip) but only at the expense of long readout time.