120 degree Neutron Detector installed at LANSCE
Detector Charge Collection

Upper cathode wires configured into readout nodes with resistive charge division in same manner as lower cathode

To analog shaping amplifiers, pulse stretcher and sequential switching into centroid finding filter
Detector Charge Collection

15 readout taps per segment

17 readout taps per segment
ADC outputs for Y-axis channels with neutron hit centered between preamps
ADC outputs for X-axis channels with neutron hit directly over preamp

Charge amplitude

Channel #
Detector Electronics

• Provide X,Y position for the center of charge in under 4 uS.

• Provide a set of software tools for calibrating electronics and displaying data.

• Interface to the Los Alamos LANSCE-12 data collection system.
Complete Electronics Chain for 1 Segment

Preamp | Shaper | ADC | Node Selector | Centroid Finding
-------|--------|-----|--------------|-----------------
Upper Cathode

Shaper & Disc. | Prog. Delay | Neutron Energy Selection
Anode

Lower Cathode

Neutron Beam Chopper

Y-Position

2-D Histogram

E₁ E₂ E₃ E₄ E₅
Position Encoding Across Boundaries
Position Encoding Across Boundaries Implementation
Preamp Driver Motherboard
VME Motherboard
Digital Daughterboard Block Diagram

- Digital Daughterboard Block Diagram
- ADC data
- Data / Address Bus
- Altera APEX 20K FPGA
- SRAM 128k * 24
- Data / Address Bus
- Motorolla 56301 DSP
- SPI Interface
- Anode I/O
- 128k * 24 SRAM
- 2M * 8 FLASH
- Data/Cmd Requests
- Position Data
Digital Daughterboard
Steps to Calculate the Center of Charge

• Read 17 x-axis ADC’s, 15 y-axis ADC’s, 3 neighbor x-axis ADC’s
• For each channel
  – Offset Correction (subtraction)
  – Gain Correction (multiplication)
• Search for channel with the maximum charge
• Calculate center of charge
• Add Result to Histogram
• Send Result to Los Alamos Acquisition System
Center of Charge Equation

\[
\left( \frac{c - a}{a + b + c} + \text{node#}_{\text{max}} \right) \times \text{bins/node}
\]
Altera APEX 20K FPGA

- **Embedded System blocks**
  - Dual-Port RAM, FIFO, RAM, ROM, FIFO
  - RAM sizes up to 440 kbits.

- **Support for various I/O standards**
  - LVTTL, LVCMOS, LVDS, LVPECL, GTL+
  - Up to 808 user I/O pins

- **Signal Tap logic analysis**

- **Density up to 1.5 million gates**

- **On chip PLL  1x-160x multiplication**

- **0.15µm, 6 layer (all copper-20KC) process**
FPGA Block Diagram

1 x-position ADC's from detector n-1

15 x-position ADC's

2 x-position ADC's from detector n+1

Read X Dimension ADC's → Offset Table → Offset Correction → Gain Table → Gain Correction → Find Node with Maximum Charge → Compute:

Numerator: (c - a) & Denominator: (a + b + c)

Compute:

Numerator: (c - a) & Denominator: (a + b + c)
Motorola DSP56301 Digital Signal Processor

- 100 MIPS Performance @ 100Mhz
- On-chip program and data memory
- On-chip SRAM and SDRAM controllers
- Two High Speed Synchronous Serial Ports
- RS-232 Interface
- 40 Programmable GPIO pins
- On Chip debug port
DSP Software Flowchart

1. Reset
   - Initialize
      - Neutron event
        - Yes: Read FPGA
          - Re-arm FPGA
            - Calculate Centroids
              - Update Histogram
                - Send result to Readout Board
        - No: Process Request
          - Request from PC
            - Yes: Reset
            - No: Neutron event

This flowchart represents the process flow for DSP software, starting with a reset event. It involves initializing, checking for neutron events, reading from an FPGA, re-arming the FPGA, calculating centroids, updating histograms, and sending results to a readout board.
Some Supported Request types

- **Histogram**
  - Dump x,y position histogram
  - Dump Anode Histogram
  - Dump Cathode Sum Histograms
  - Clear histograms

- **Dump ADC Data (Diagnostic)**
  - Raw Data
  - Offset corrected
  - Offset & Gain corrected

- **Calibration**
  - Offset Calibration
  - Gain Calibration
  - Dump Current calibration values

- **Status**
  - Event rate, Anode trigger levels, gain settings, software & firmware versions.
Readout Board

- Interface to CHARM “twinkle” box
- Interface to PC via National Instruments DIO32-HS Digital I/O module
- Interface to Los Alamos LANSCE-12 data acquisition system

Processed x,y positions feed in here
Neutron Detector Electronics Control & Display Page

Clicking on the links below will start a labview virtual instrument (VI) on the host machine. Once the VI has loaded you can right-click on the panel to take control. Due to current licensing limitations, only one client can view these controls at a time...

Status & Control
- View Detector Settings
- Change Detector Settings

Histogramming
- View 1 segment histogram
- View 2 segment histogram
- View 3 segment histogram

Diagnostics
- Display all ADC outputs

Calibration
- Calibrate

Advanced
- View Arse and Histograms
- View Arse and Sum Histograms
Labview Status vi
Labview Control vi
Read ADC outputs vi
Display 2 Segment vi
Display Anode Histogram vi

ND120 Anode Histogram

Main Anode

charge level
Display Cathode Sum vi
Calibration

ND120: Calibration

Procedure
1. Terminate high voltage.
2. Disable boundary Anode. Noise use Control V.
3. Turn on power. Noise, move switch from ext to high.
4. Do Offset Calibration
   a. Disconnect cathode pulser
   b. Select Function to Offset Calibration
   c. Cycle through each detector segment.
5. Do Gain Calibration
   a. Reconnect cathode pulser
   b. Select cathode pulser voltage 0 V to 0.3 V
   c. Select Function to Gain Calibration
   d. Cycle through each detector segment.
6. View Offset & Gain Results. (optional)
7. Turn off power. Noise, move switch from high to ext.
8. Enable Boundary Anode. Noise use Control V.
9. Turn back on high voltage.
An X-ray Transmission Image of a Copper Mask
(5.9keV x-rays, 0.1pC anode charge, Ar/C0₂ 20%)