Superconductor Microelectronics for Detector Readout

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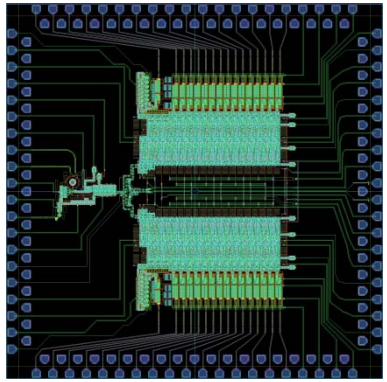
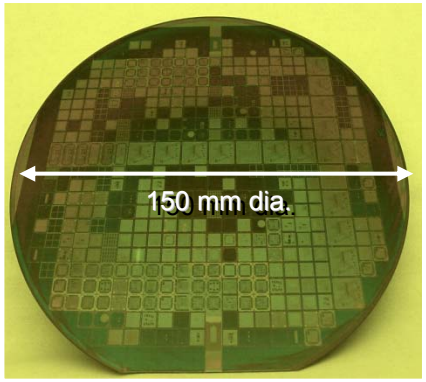
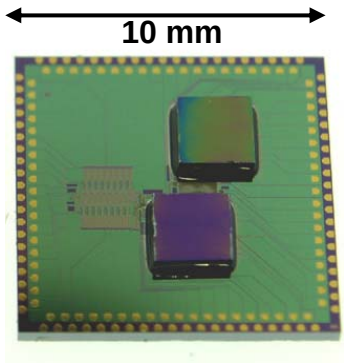
HYPRES

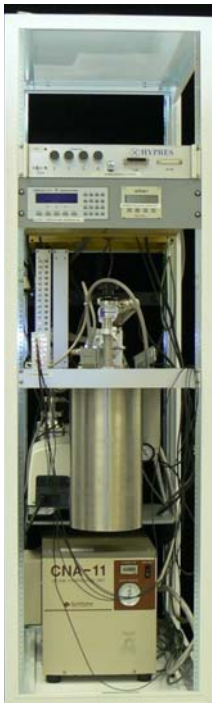
A Complete Superconductor Electronics Company

- Integrated Circuit Design (Cadence-based suites)
- Integrated Circuit Fabrication (All-thin-film process)
- Multi-Chip Module Integration
- Cryopackaging and Interface Electronics
- Final Assembly and Test



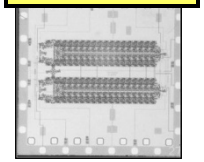




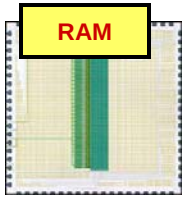


HYPRES: A Brief History

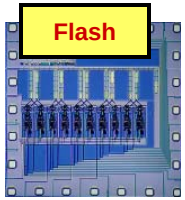
PSP-1000: 70-GHz Sampling Oscilloscope



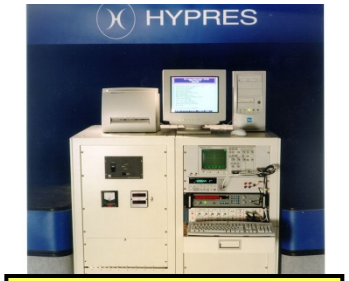
FFT Element



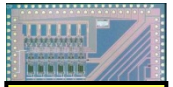
RAM



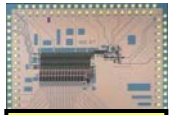
Flash



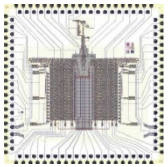
Primary Voltage Standard

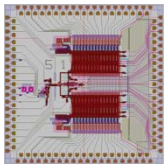


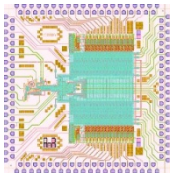
Transient Digitizer



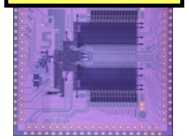
ADC+DDF







ADR



1983 — 1989 — 1995 — 2000 — 2008

The Beginning

- Nb/AlOx/Nb JJ Fab
- Innovative 'spray' cooling of chip
- System Integration
- Award-winning Product
- No demand

New Ideas

- RSFQ
- Ultrafast Digital Logic Circuits
- Analog-to-digital converters: Flash and Oversampled delta modulator
- No clear goal

Consolidation

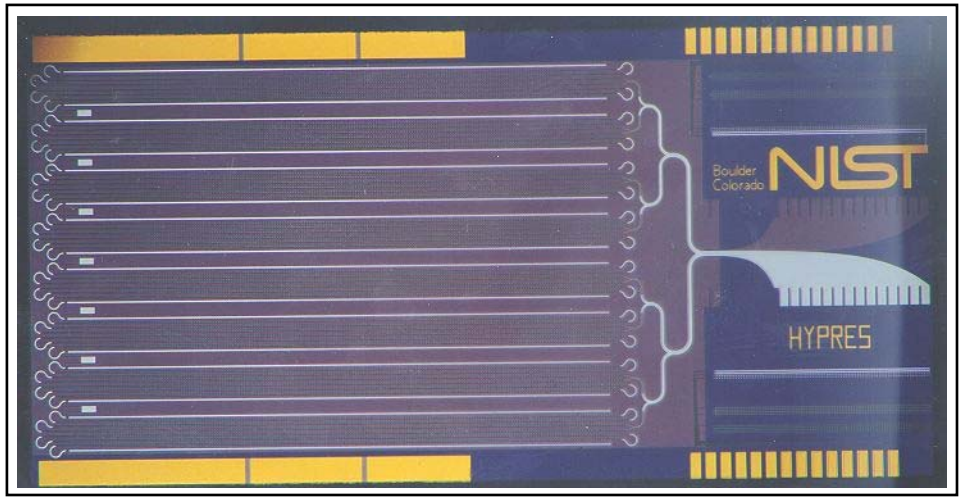
- COTS Cryocooler Cryopackaging
- Variety of Digital and Mixed-Signal ICs Demonstrations
- Primary Voltage Standard Product
- No pull from small instrumentation Market

Focused Growth

- Digital-RF
- System Integration Infrastructure
- All Digital Receivers (ADR) and Transmitters
- Military RF Market
- Commercial Wireless Communication Market

Commercial Product

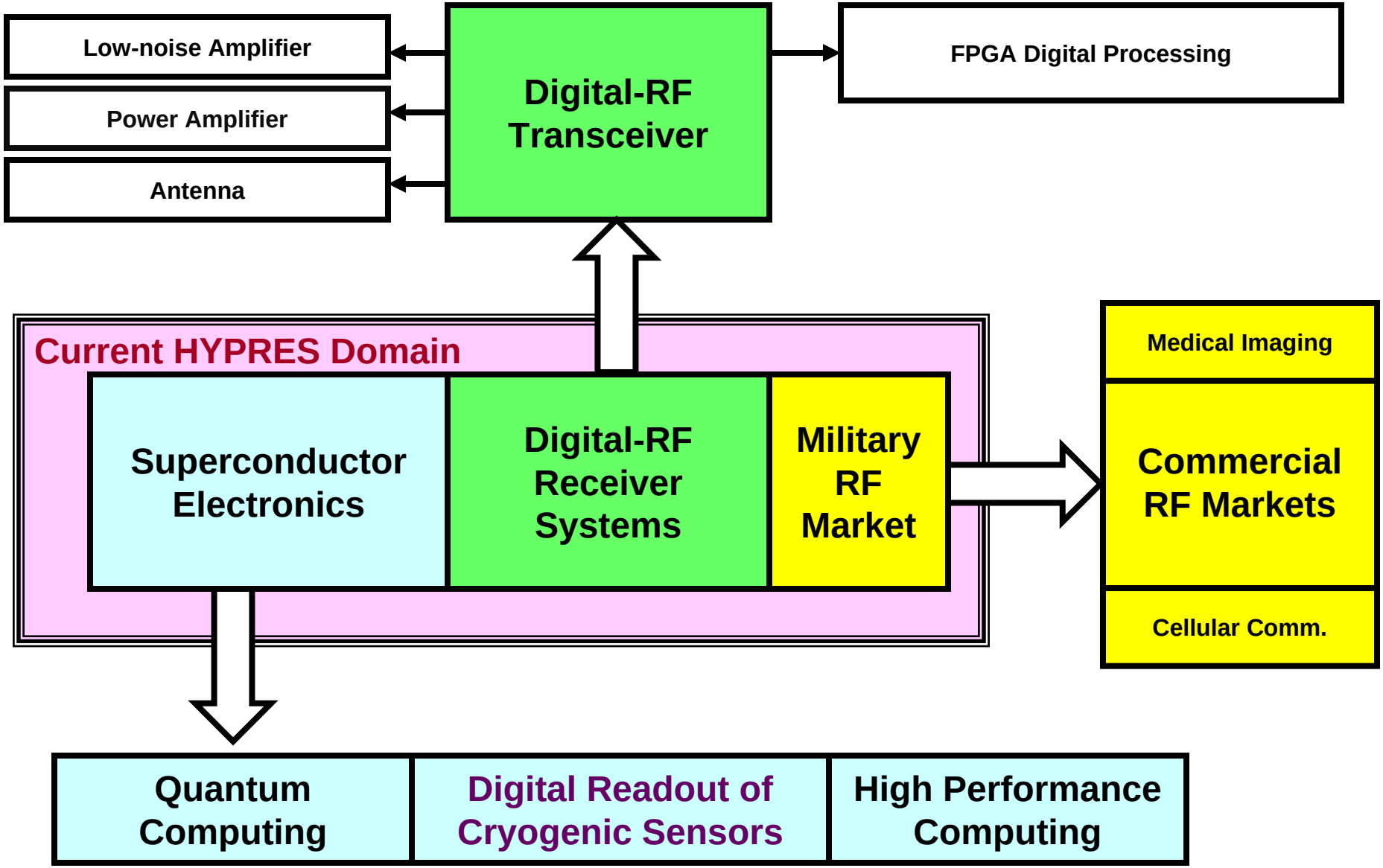
Commercial Primary Voltage Standard for Metrology



1cm x 2 cm 10 Volt Chip with
5ppb accuracy
(23,000 Josephson junctions)

Cryocooled Voltage Standard System

Expansion Strategy



Unique Features of Digital Superconductor Technology

- **Ultra-High digital logic speed**

  Single Flux Quantum (SFQ) logic is the world's fastest
  (Devices ~10 to 100X faster than semiconductor, demonstrated at **>750 Gbps**)

- **Ultra-Low power dissipation**

  10,000X lower than semiconductor technology
  (Switching energy ~ **2×10^{-19} J**, **5×10^{3} $k_B T\ln 2$** @4K, Power dissipation for large scale IC ~ **1 mW**)

- **Fundamental linearity using magnetic flux quantization**

  Conversion between analog and digital domains through flux quantum (Φ_0 = h/2e) is independent of circuit parameters ⇒ **High-SFDR ADC and DAC**

- **Extremely low noise**

  Receiver System Noise Temperature T_S ~ T_A
  (Thermal noise contribution is essentially negligible)

- **Ideal interconnects**

  Low-impedance superconductor interconnects have negligible loss, dispersion and crosstalk ⇒ **speed-of-light transmission in LSI circuits, no RC delay**

- **High radiation hardness**

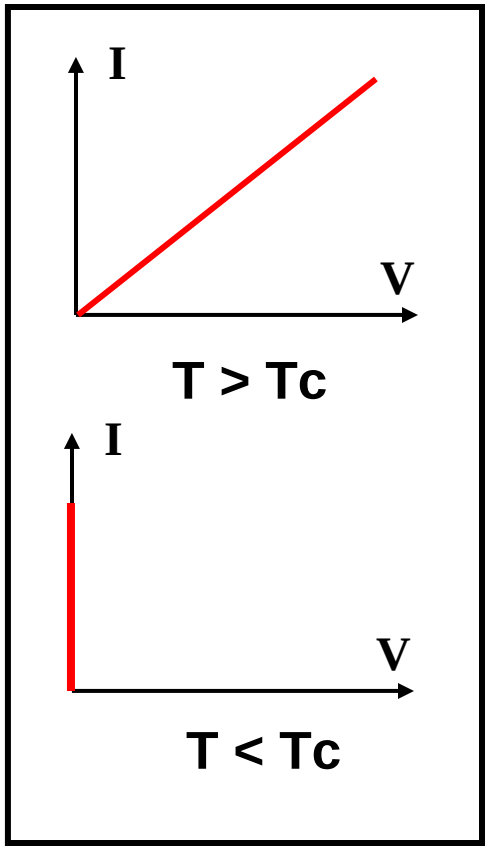
  ~ 100 times better than semiconductors
  (Low cross-section thin film, Large density of carriers, Nb junctions are polycrystalline - not sensitive to point defects or weak disorders)

Result: Digital-RF Technology

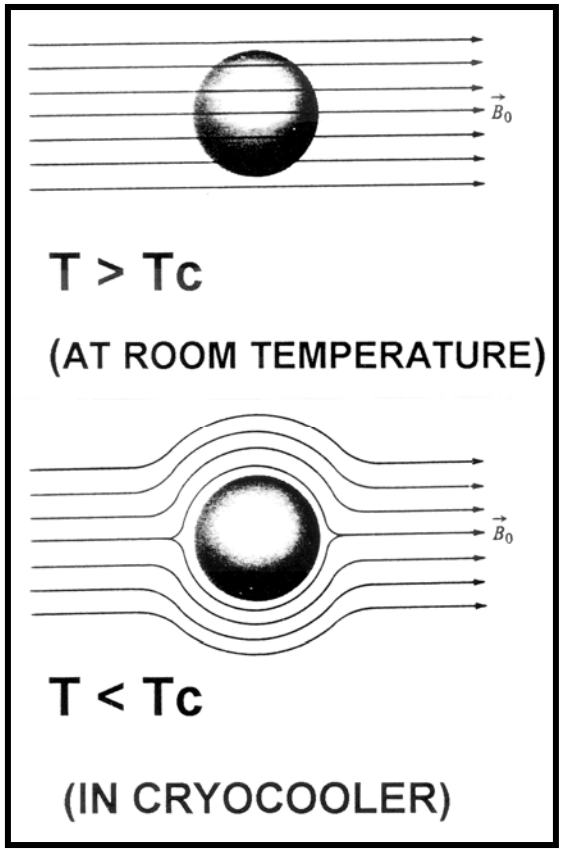
High-fidelity, wide band, high sensitivity digital representation and high-speed digital processing of RF waveforms - "**RF DSP**": channelization, true-time delay beamforming,…….

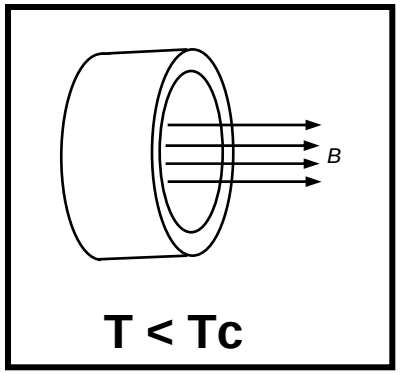
Superconductivity

Zero Resistance



Expulsion and Quantization of Magnetic Flux





$$\Phi = \int B_n dA = n\,\Phi_0$$

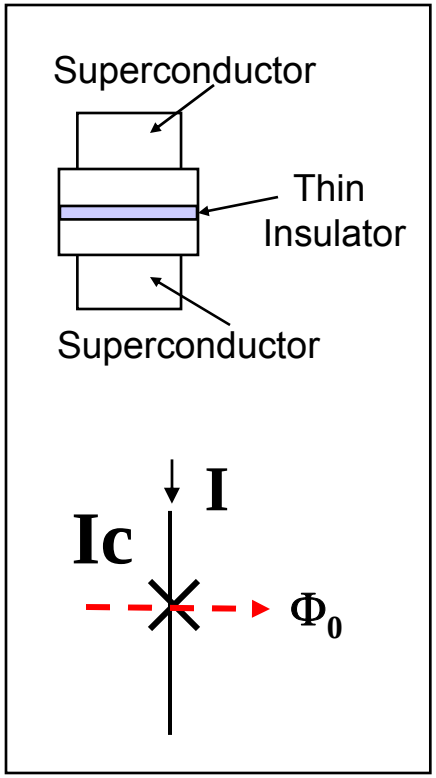
$$\Phi_0 = h/2e = 2.07\ \text{mV}\bullet\text{ps}$$

$$= 2.07 \times 10^{-15}\ \text{Wb}$$

Single Flux Quantum (SFQ)

Josephson Junction Devices

Active component (switch) in superconductor electronics



Josephson Junction

$I < I_c$

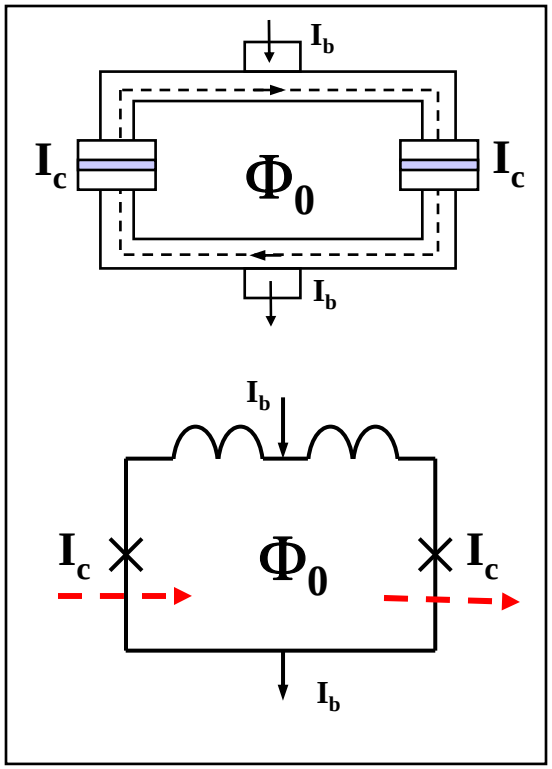
JJ stays superconductive

$$I = I_c \sin(\phi)$$

$I > I_c$

JJ goes resistive and passes magnetic flux through

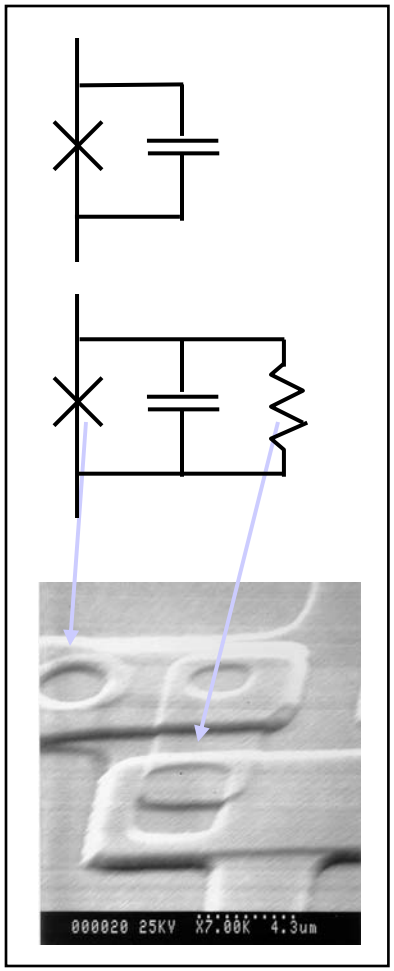
$$\tau = \Phi_0 / V_c$$



Memory cell

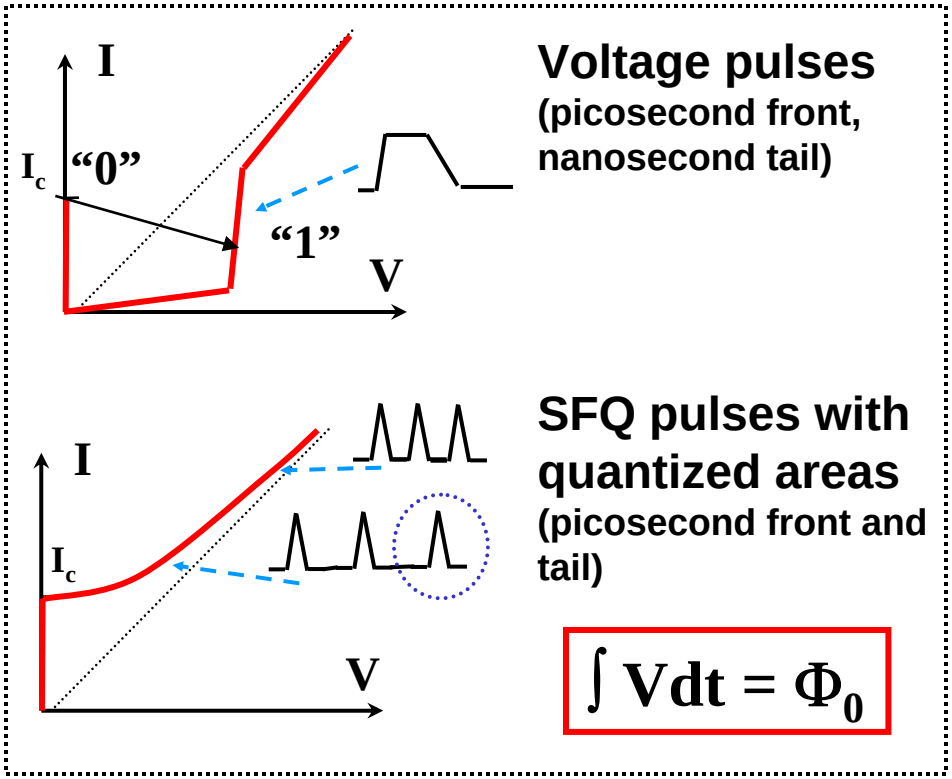
Josephson Junction Behavior

Picosecond waveforms and time responses



70-80's

Latching logic



Voltage pulses
(picosecond front, nanosecond tail)

90's

RSFQ Logic

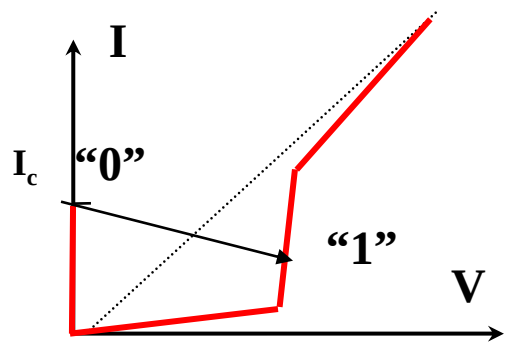
SFQ pulses with quantized areas
(picosecond front and tail)

$$\int V dt = \Phi_0$$

Adding a shunt resistor allows the generation of separate SFQ pulses

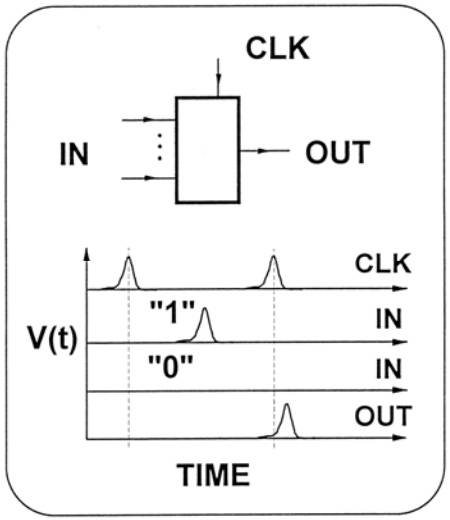
Voltage-State Logic (Latching Logic)

- Basis for earlier Josephson computer projects at IBM and Japan (through ~ 1990)
- Uses hysteretic (high Q) Josephson junctions
- Logic "0": V = 0, Logic "1": V > 0
  - Switched with current injection or flux coupling
- Problem: Resetting into V=0 state requires waiting for time ~RC for *ring down* to occur
- Limited clock speed to ~ 1 GHz.
- Large-scale ICs demonstrated, but no longer actively pursued.



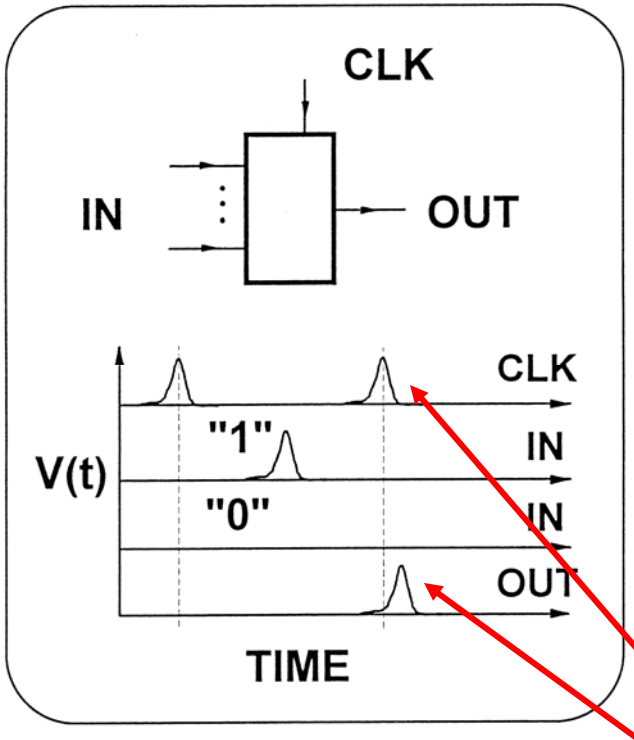
Single-Flux-Quantum Logic (Pulse Logic)

- **RSFQ (Rapid Single Flux Quantum)**
  - Invented by Mukhanov, Semenov, & Likharev at Moscow State University (mid-80's)
  - Dominant approach for superconductor electronics worldwide
- **Requires damped non-hysteretic junctions (Q~1)**
- **Based on transmission and storage of single quanta of magnetic flux**
  - Logical '1' or '0' defined by presence or absence of SFQ pulse during clock period
  - Clock also defined by SFQ pulses
- **Ultra-low power dissipation**
  - Energy/SFQ pulse ~ $I_c\Phi_0$ ~ 2 x 10^{-19} J



RSFQ Basic Convention

RSFQ - Rapid Single Flux Quantum



Logic "1" - presence of a data SFQ pulse between two clock SFQ pulses

Logic "0" - absence of a data SFQ pulse between two clock SFQ pulses

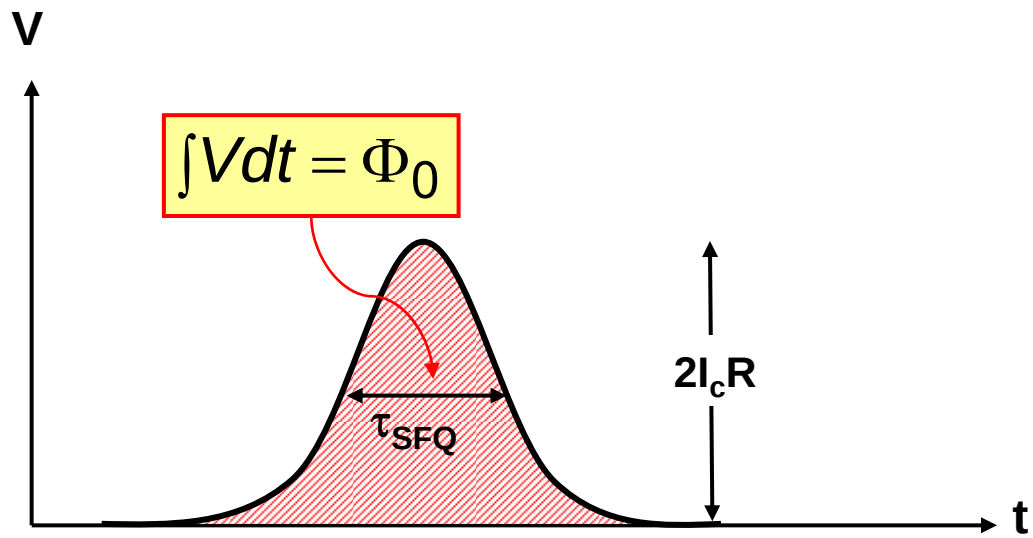
Both Data and Clock are SFQ voltage pulses V(t) with quantized areas

$$\int V dt = \Phi_0 = h/2e = 2.07\ \mathrm{mV \cdot ps}$$

SFQ pulses

Synchronous pulse coding of information

Speed of RSFQ Circuits



- SFQ pulse height: $2I_cR$
- SFQ pulse width: $\tau_{SFQ} \sim \Phi_0/2I_cR = \pi(L_J/R)$
- For Nb junctions, ultimate limit $\tau_{SFQ} \rightarrow$ 0.4 ps
- For complex RSFQ circuits, $f_{clock} \sim 1/10\ \tau_{SFQ}$
  - Maximum Clock Frequency for Nb VLSI ~ 250 GHz

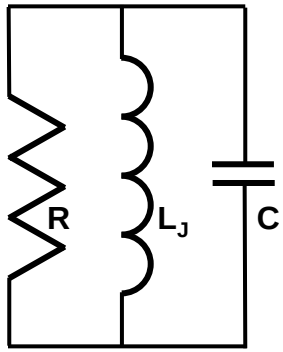
JJ Characteristic Times and Frequencies

Linear Model of JJ: Parallel LCR Resonator

- Three characteristic times: L_J/R, RC, $\sqrt{(L_J C)}$
- Resonant frequency: $\omega_0 = 1/\sqrt{(L_J C)}$ (also called "plasma frequency, ω_p")
- Quality factor: $Q = \omega_0(RC)$
- Junction damping parameter: $\beta_c = Q^2 = (RC)/(L_J/R) = 2\pi I_c R^2 C/\Phi_0$.
- Underdamped case (Q>1): small oscillations at ω_0, damp out slowly in time ~ $RC > L_J/R$
- Overdamped case (Q<1): damped motion dies out smoothly in time ~ $L_J/R > RC$
- Critically damped case (Q=1, $\beta_c = 1$): Fastest overall relaxation with little ringing, <u>all three time constants are equal</u> $L_J/R = RC = 1/\omega_0$)

For ideal JJ with $V_c = I_c R_n = \pi\Delta/2e \sim 2.2$ mV for Nb,

$$\tau_0 = \frac{L_J}{R} = \frac{\Phi_0}{2\pi I_c}\frac{1}{R} = \frac{1}{2\pi}\frac{\Phi_0}{V_c} = \frac{1}{2\pi}\frac{4}{\pi}\frac{e\Phi_0}{2\Delta_{Nb}} = \frac{1}{\pi^2}\frac{h}{2\Delta_{Nb}} \approx 0.15\,\text{ps}$$



"Introduction to Superconducting Electronics", Kadin, Wiley, 1999

Device Scaling

Properties	1st Gen	2nd Gen	3rd Gen	4th Gen
JJ Size (μm)	3	1.5	0.7	0.3
J_c (kA/cm^2)	1	4.5	20	100
Max. DFD Frequency (GHz)	120	240	500 (395 @ 0.8 μm)	>1000 (750 @ 0.25 μm)
Max. VLSI Clock (GHz)	20-25	40-50	80-100	160-200

All previous work in detector readout electronics

Switching Energy: CMOS vs JJs

- **CMOS or any other charge-transfer based devices (SET, molecular transistors, etc.)**
  - **~10^6 k_BT ln2 switching power**
  - **~10^5 k_BT ln2 if interconnect is local (e.g. 3D circuits)**

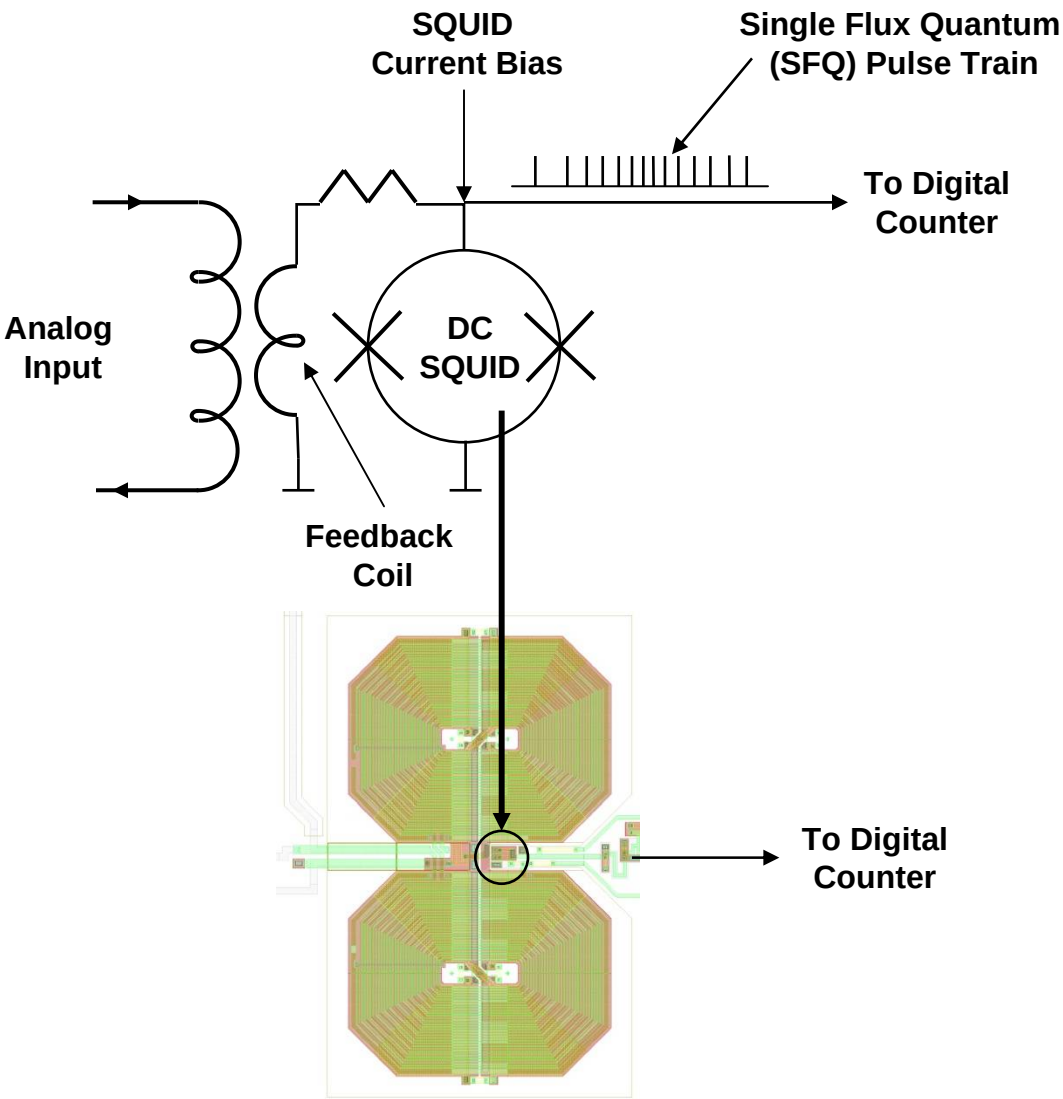
- **Switching energy per JJ – *SFQ switching***
  - **$\Phi_0 I_b$ ~0.2 aJ**
  - **5x10^3 $k_B T \ln 2$ at T=4K (70 $k_B T \ln 2$ at T=300K)**
  - **With interconnect: 5 $\Phi_0 I_b$ ~ 1aJ**
  - **This is ~ x100 better (x300 then 22nm CMOS)**

Fundamentally, SFQ circuits can get this 2 order of magnitude improvement!

Superconductor Electronics for Detector Readout

Desired Features	Benefits of Superconductor Electronics
High sensitivity	SQUID-based Analog-to-Digital Conversion is very sensitive (~1$\mu\Phi_0$/Hz$^{1/2}$)
High time resolution	Fast switching devices (sub-ps), low-jitter clock (~fs) and digital counters (100 GHz)
Low crosstalk, noise, and interference	Digital data links from cryogenic to warm (room) temperature
Radiation Hard	Thin-film technology, large density of carriers
Low power consumption	Low switching energy (0.2 aJ ~ 1eV), a few μW/chip
Scaling to large arrays	Time and frequency domain multiplexed readout

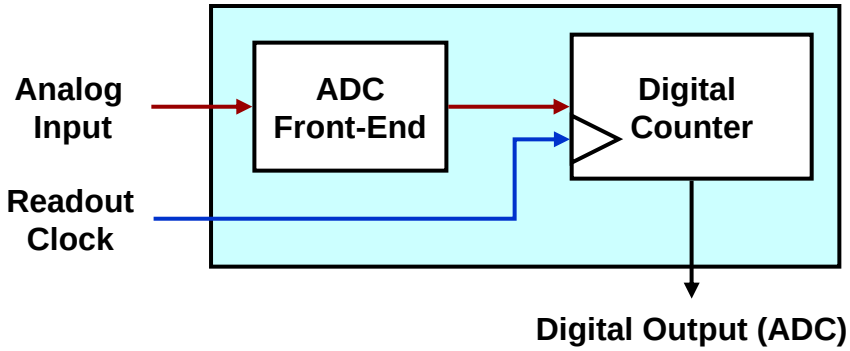
Analog-to-Digital Converter (ADC)



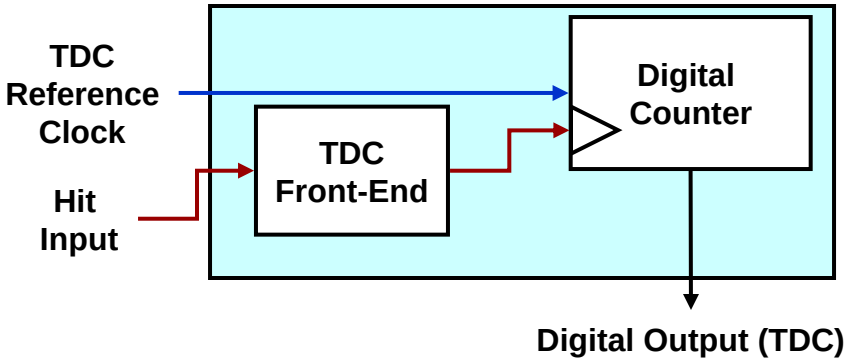
- Two different front ends with 1μA and 4μA sensitivity were developed
- The transformer has a 120:1 turns ratio
  - 4 nA/LSB @100 MHz ~ 250e
- Full scale range and periodicity of front end can be adjusted for different applications

Signal and Time Digitizers

Analog-to-Digital Converter (ADC)



Time-to-Digital Converter (TDC)

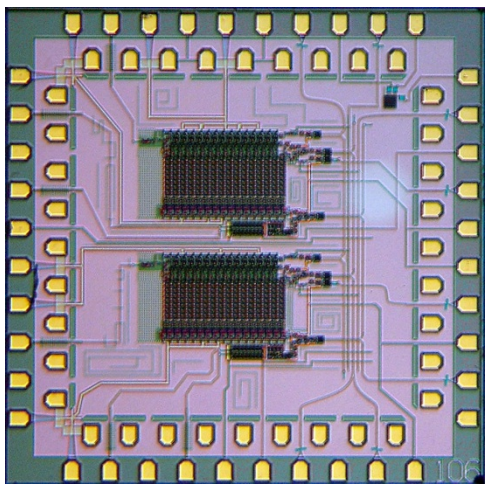


ADC: Periodic counting of aperiodic stream of pulses

TDC: Aperiodic counting of periodic stream of pulses

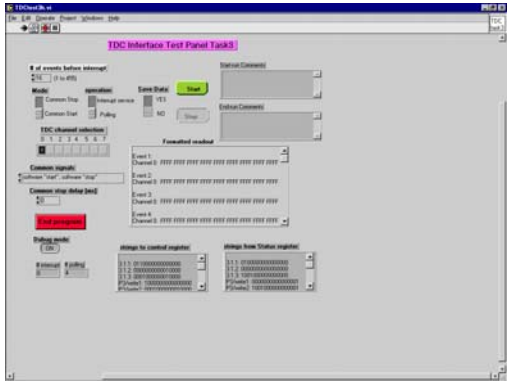
Instruments: Time Digitizing System

- Multi-hit time resolution = 30 ps
  - 4 ps with analog prescaler
- 9-word 16-bit multi-hit buffer
- Applications: Nuclear Physics Experiments, Instrument Calibration, Direction finding

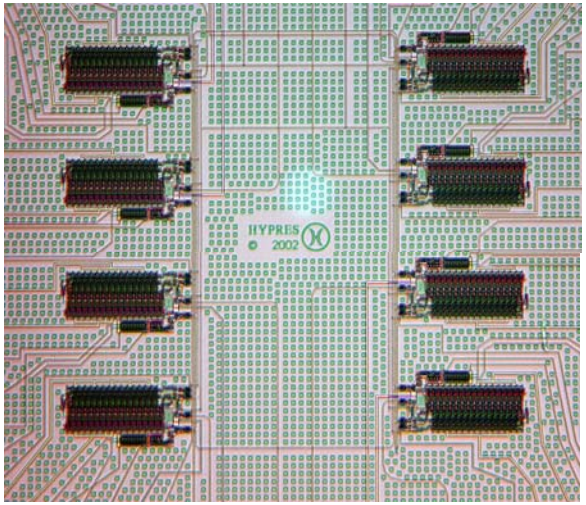


5 mm

Fully assembled VXI control electronics



LabView Based GUI



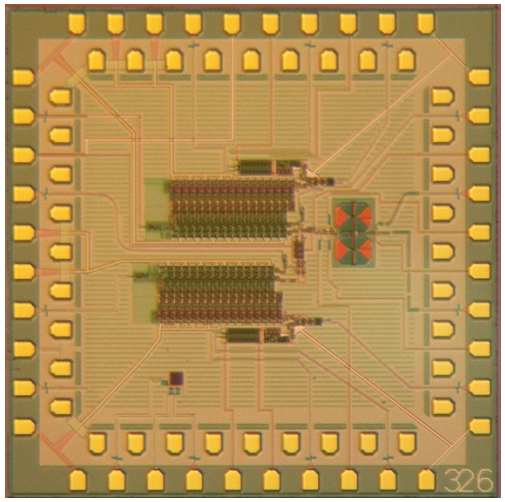
8 mm

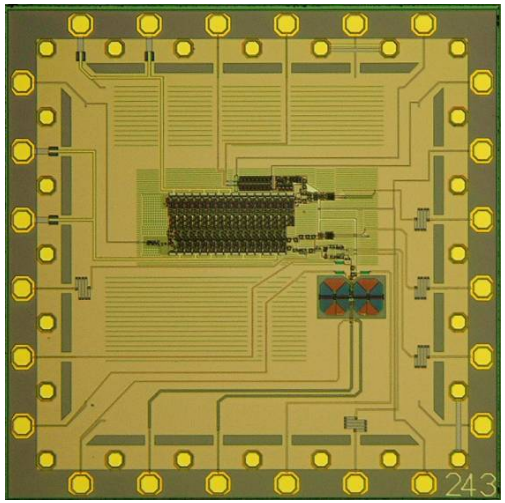
Funded in part by DOE 1999-2001

HYPRES

Instruments: Dual-function Digitizer

- 14-bit digitizer operates as TDC and/or ADC
- Application: Simultaneous time-of-flight and energy measurements for particle detectors
- Features:
  - TDC: Multi-hit time resolution < 30 ps
  - ADC: 1-100 µA full-scale with selectable sample rate (4 kHz - 400 MHz)
  - Interface: VXI (PXI under development) with LabVIEW based GUI for data acquisition and control
  - Power dissipation per channel < 250 µW
  - Four channels integrated on 1 cm^2 chip





S. Sarwana, D. Gupta, A. F. Kirichenko, T. Oku, C. Otani, H. Sato, and H.M. Shimizu, "High-sensitivity high-resolution dual-function signal and time digitizer," *Applied Physics Letters*, vol. 80, no. 11, pp. 2023-2025, March 2002.

Funded in part by DOE 2001-2002

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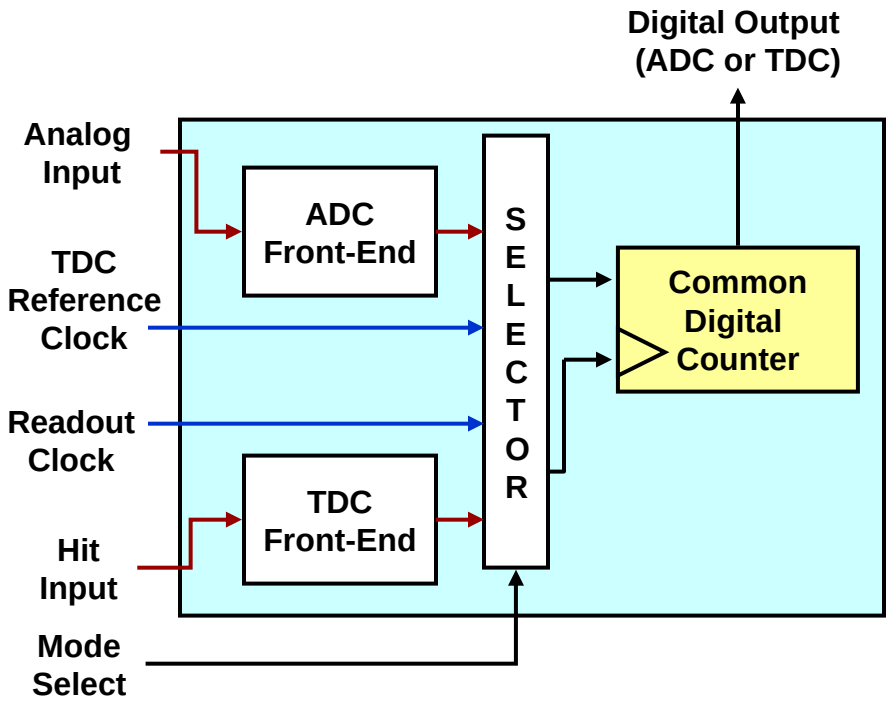
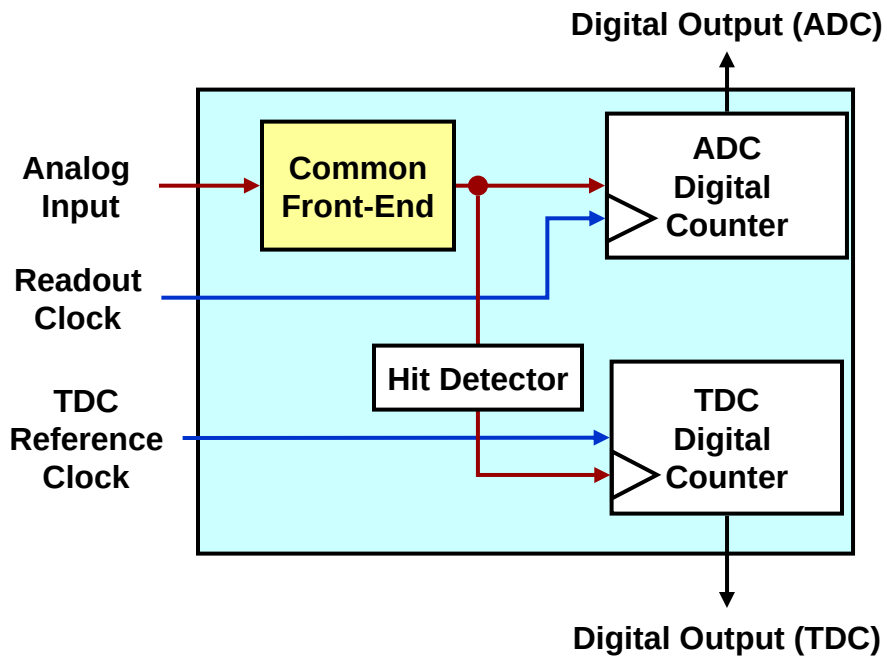
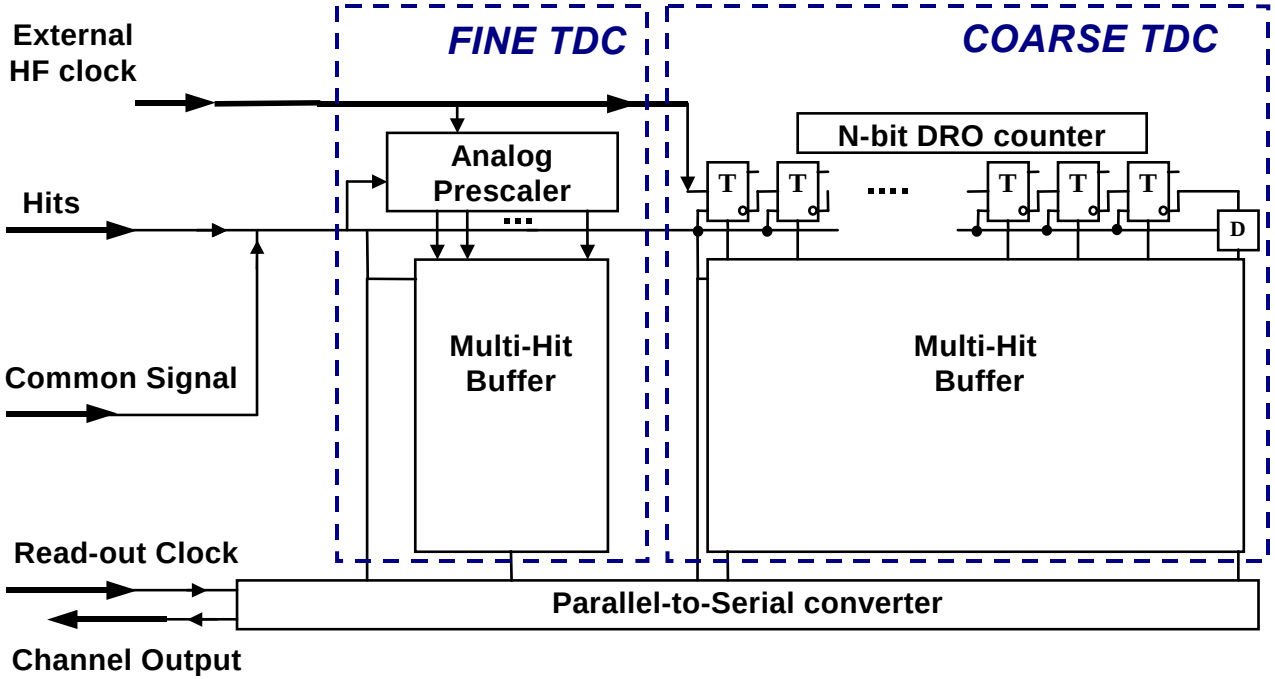
Dual-function Digitizer



Dual-function Dual-Output Digitizer

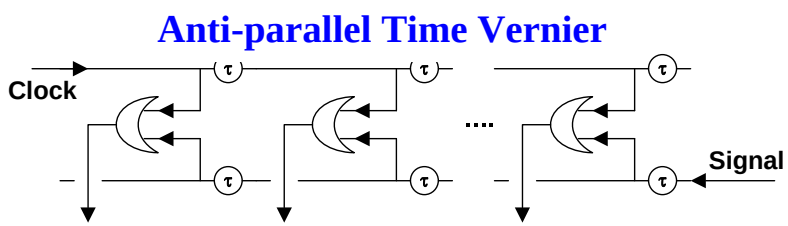


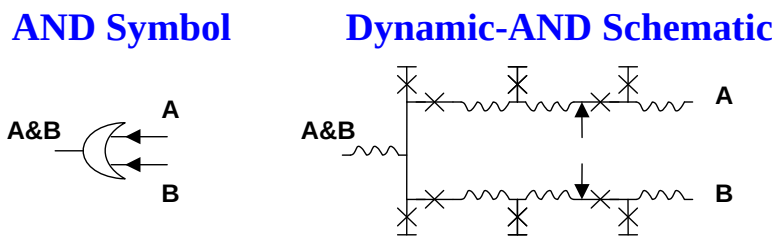
High-Resolution Time-to-Digital Converter (TDC)

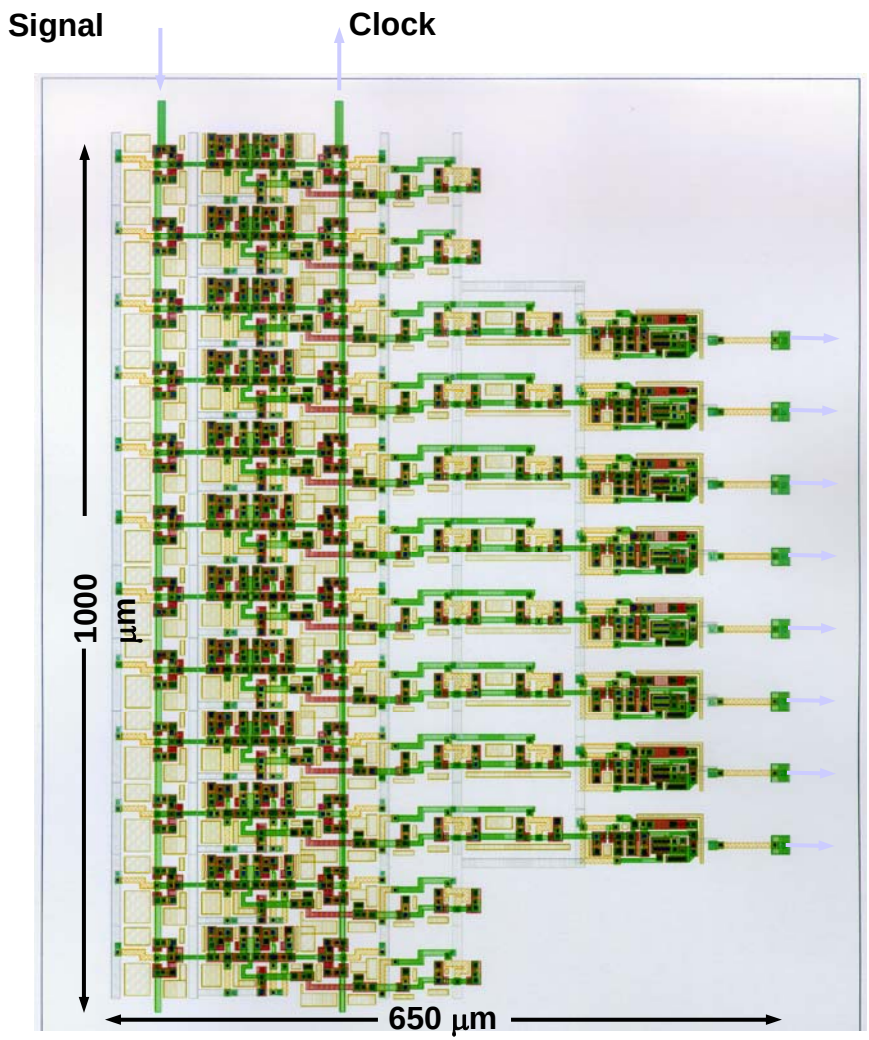


- **Coarse TDC: Counts clock pulses (time res. = $1/f_{clk}$)**
  - **2nd Gen digital counter works up to 120 GHz with on-chip clock (ERSFQ proven up to 67 GHz with external clock)**
- **Fine TDC: Divides clock period into n intervals (time res. = $1/nf_{clk}$) using an analog vernier**
  - **~6 ps resolution obtained with 1st Gen process (f_{clk} = 20 GHz, n=8)**

Dynamic-And Prescaler (2nd Generation)

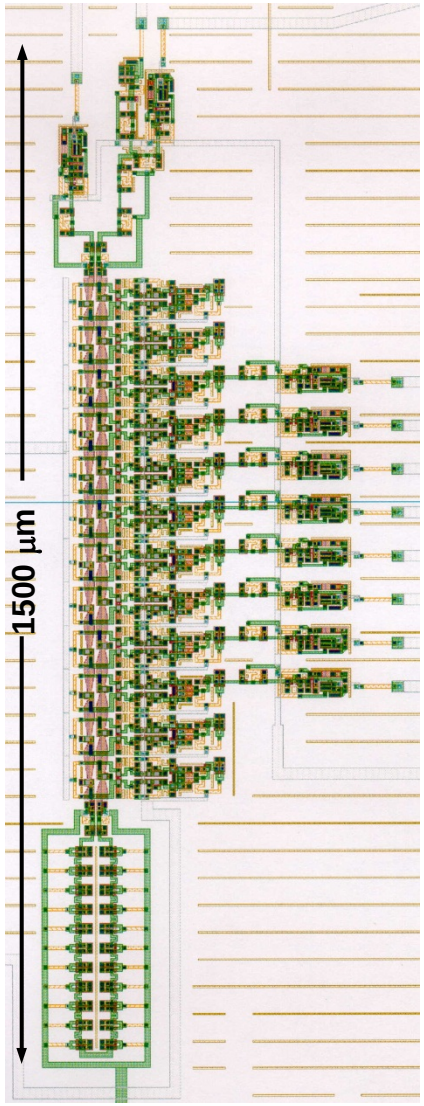




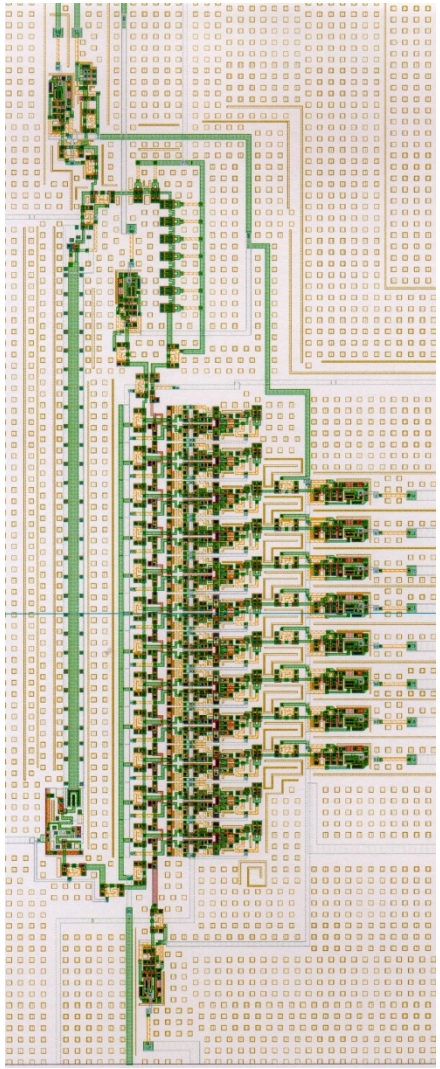


- **Anti-Parallel clock and signal propagation**
- **Output pulse generated when signal and clock almost simultaneous (within gate delay)**
- **The internal AND gate delay set large enough so at least one gate always switches.**

2 versions to Test Dynamic AND Prescalers



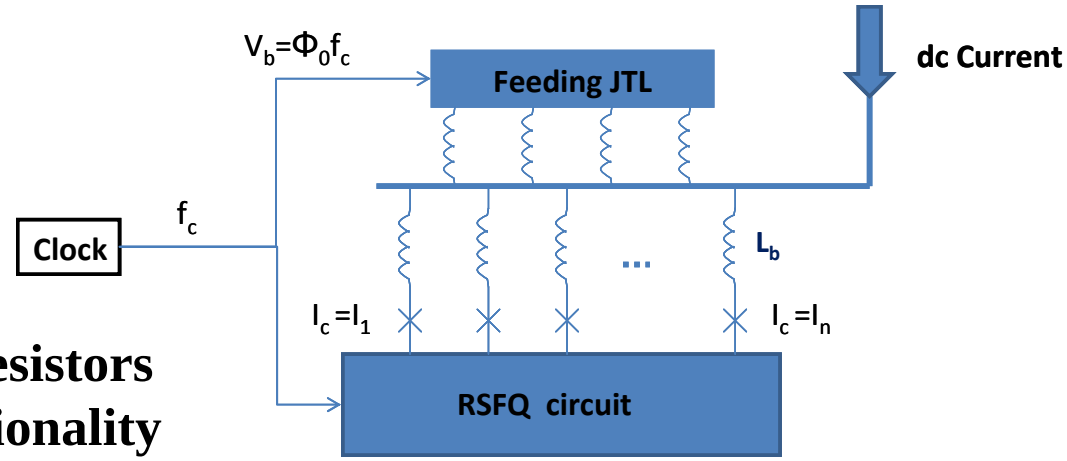
- You either race a SFQ pulse against the next one (next clock) or split a single clock and race it against itself.
- You can distort the shape of the inductor to distort the SFQ pulse shape and width and hence adjust the aperture time.



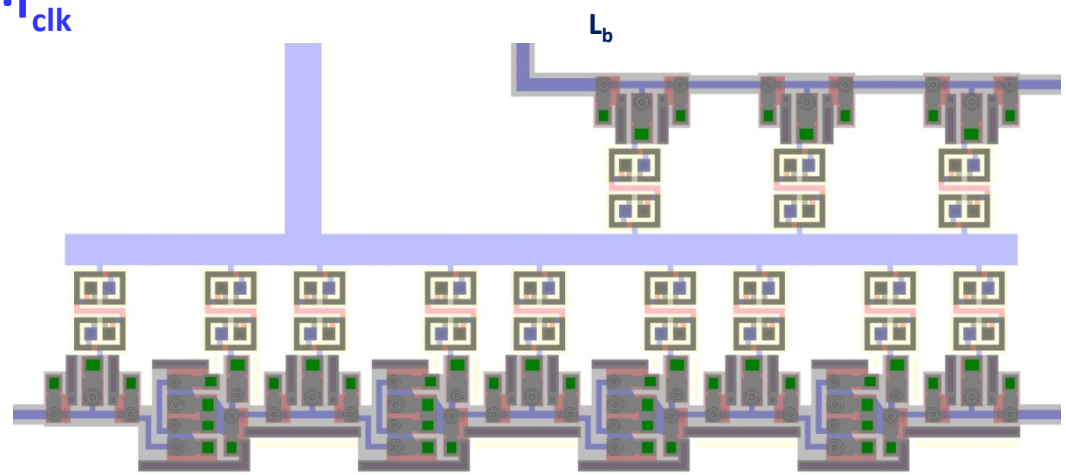
Energy-efficient Rapid Single Flux Quantum (ERSFQ) Logic

- Dissipates less than one attoJoule (10^{-18} J) per logic switching
- No static power dissipation
- Already developed and proven RSFQ designs can be easily converted to ERSFQ by replacing bias resistors with L-JJ chains
- DC bias current (same as in RSFQ)
- Total power dissipation is $I_b \cdot \Phi_0 \cdot f_{clk}$, where I_b is total bias current and f_{clk} is clock frequency
- Even at the maximum speed (~ 500 GHz), the total power dissipation is 20 times less than in RSFQ
- Requires relatively large (~100pH) inductors, that consume extra space (can be dealt with an extra wiring layer)

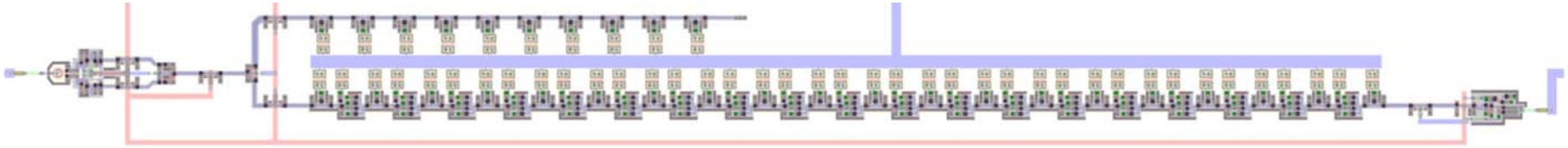
ERSFQ



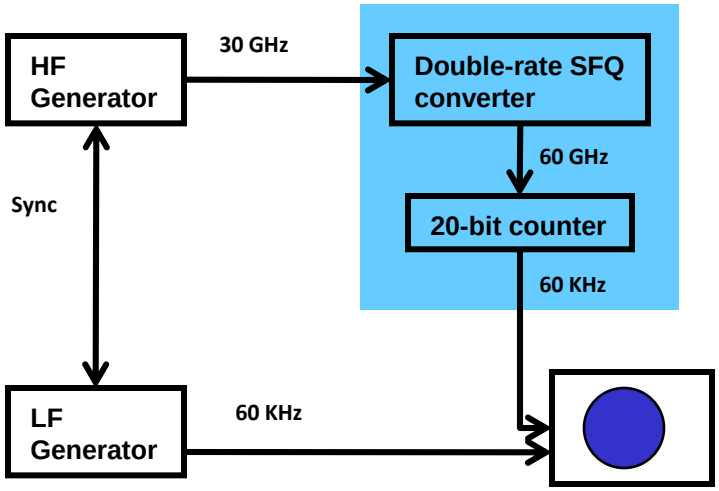
- ❑ Complete elimination of bias resistors
- ❑ No change to RSFQ cells functionality
- ❑ Bias inductance value is $L_b = \Phi_0/\delta I$, where δI is highest tolerable bias current fluctuation
- ❑ Power dissipation is $P = I_b \cdot \Phi_0 \cdot f_{clk}$

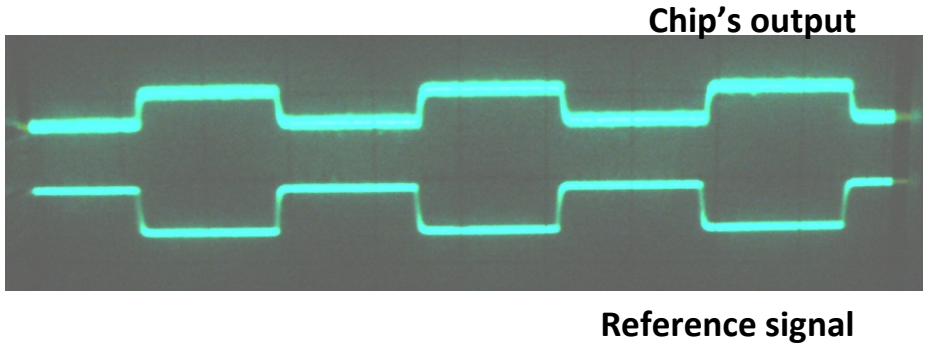


ERSFQ 20-bit Binary Counter



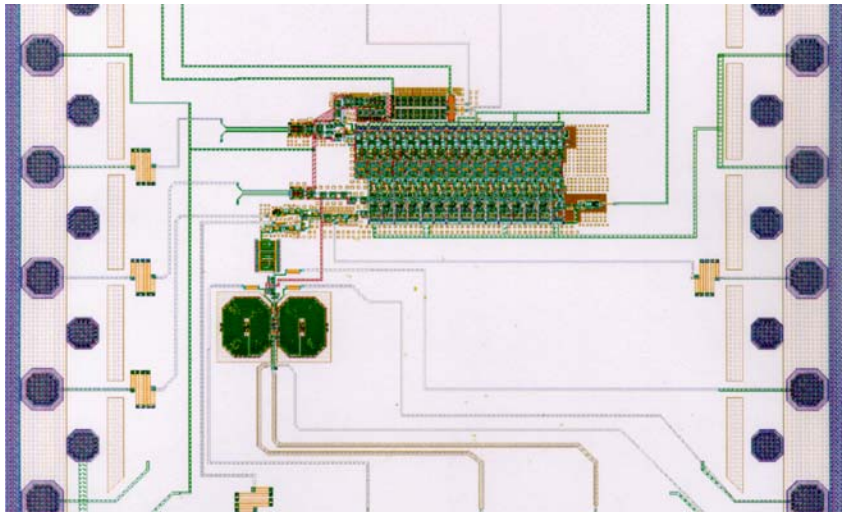
- An ideal circuit for verifying ERSFQ approach, - each TFF works at its own frequency
- Works at 23 GHz at nominal bias current with +/-16% margins
- Works up to 67 GHz at higher-than-nominal bias
- BER is the same as in traditional RSFQ counter ($< 10^{-12}$)



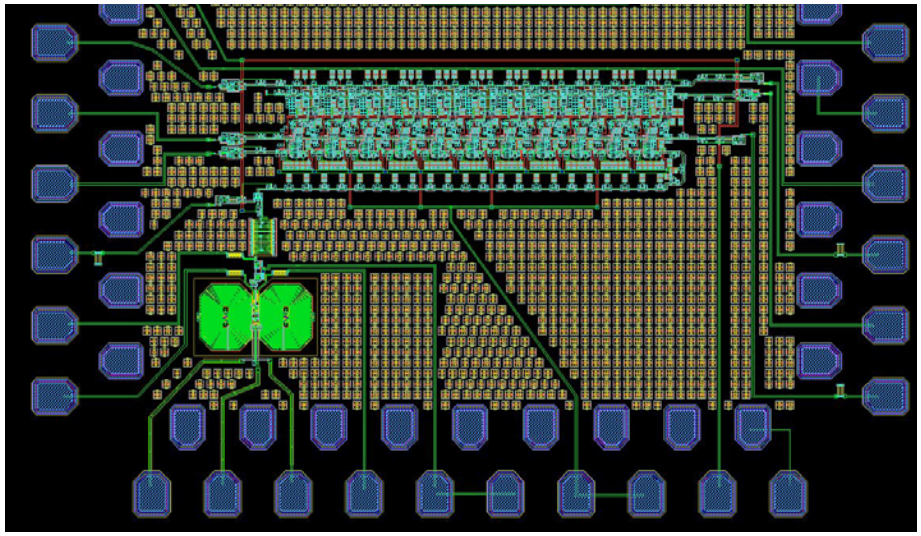


ERSFQ vs RSFQ Flux Counting ADC

3 Event Memory Buffer / 14 Bit Counter



1 Event Memory Buffer / 11 Bit Counter

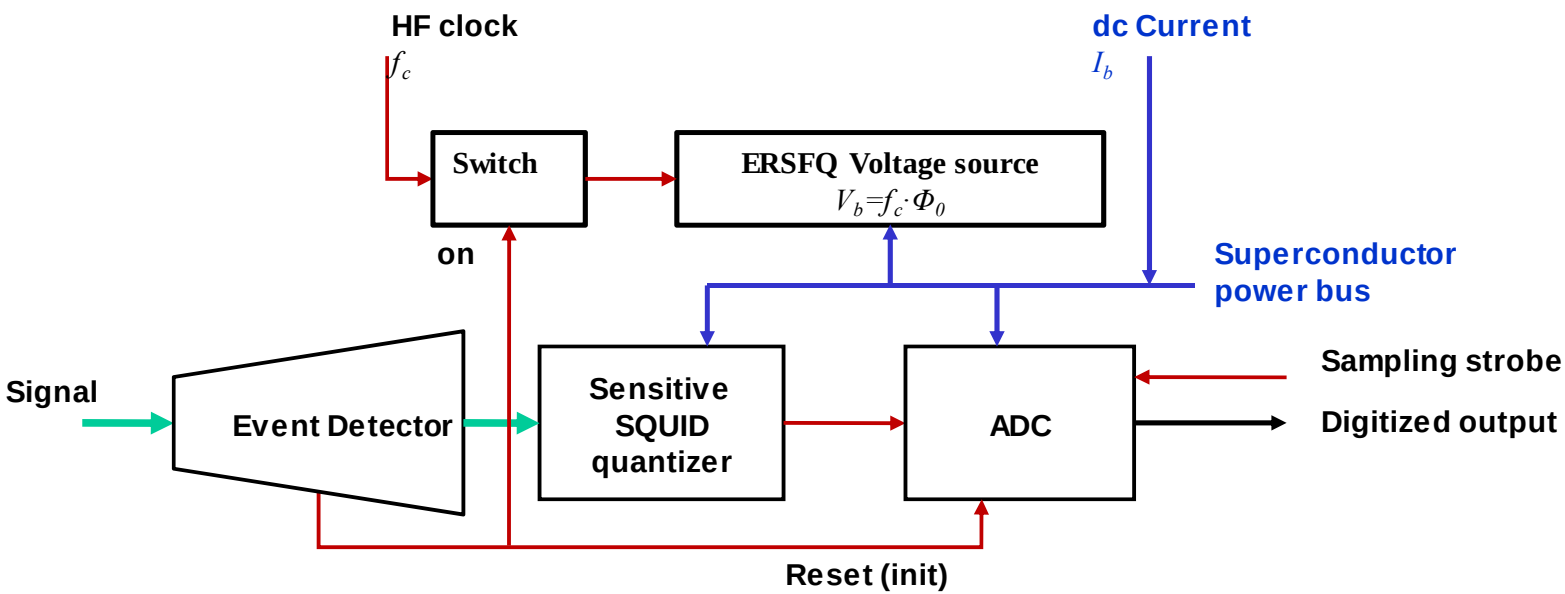


	RSFQ (μW)	ERSFQ (μW)
Digital Logic (Normalized)	100	1.7
SQUID Front End (Analog)	4	4
Input/Output	35	21
Total	139	26.7

Funded by DOE Phase I SBIR “Low power radiation hard ADC for detector readout” (Award # DE-SC0004398),

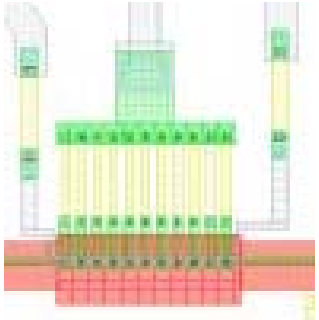
Digital Detector Readout

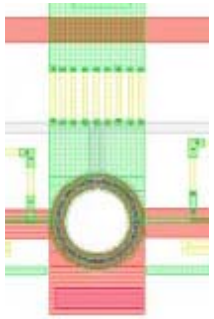
- ADC can be placed next to a sensitive detector
- Produces no noise in idle mode
- Can be instantly turned "on" with arrival of signal from the detector

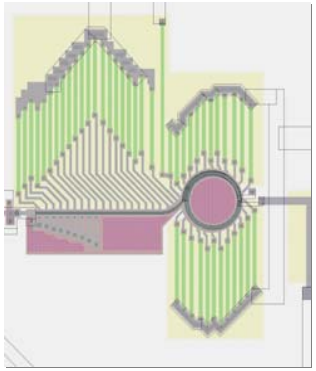


One Full Channel / 16 Bit Counter / 9 Event Buffer	RSFQ (μW)	ERSFQ (μW)	ERSFQ with Event Detector (μW)
Digital Logic (40 GHz)	368	3	0/3
SQUID Front End (Inactive/Active)	4	4	0/4
Input-Output (Inactive/Active)	35	21	2/23
Total (Inactive/Active)	407	28	2/30

Long Josephson Junction Clock Source



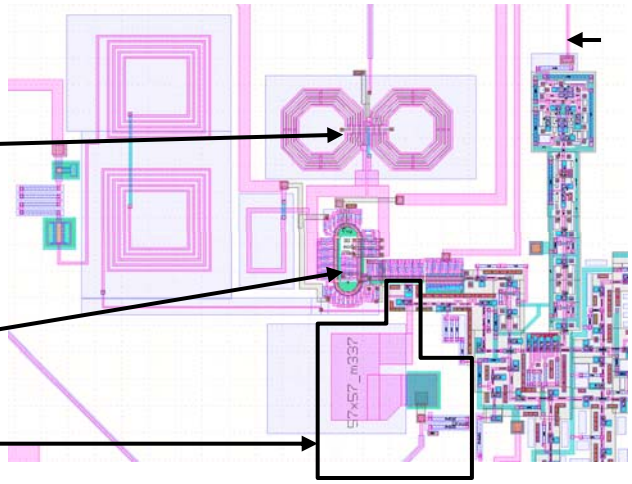


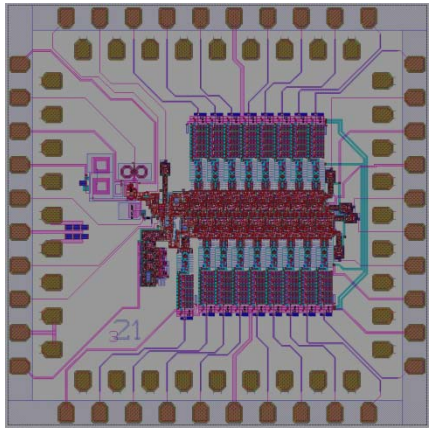


$Q = 0.9\times10^6$ @ f = 10 GHz
τ_{jitter} ~ 56 fs @ f = 26 GHz

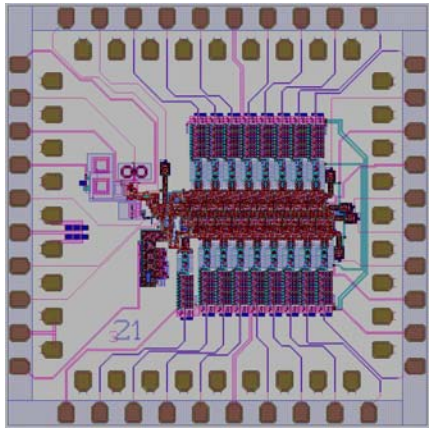
$Q = 1.3\times10^6$ @ f = 40 GHz

$Q = 4.8\times10^6$ @ f = 36 GHz
τ_{jitter} ~ 9 fs





X-band BPΔΣ ADC with On-chip Clock



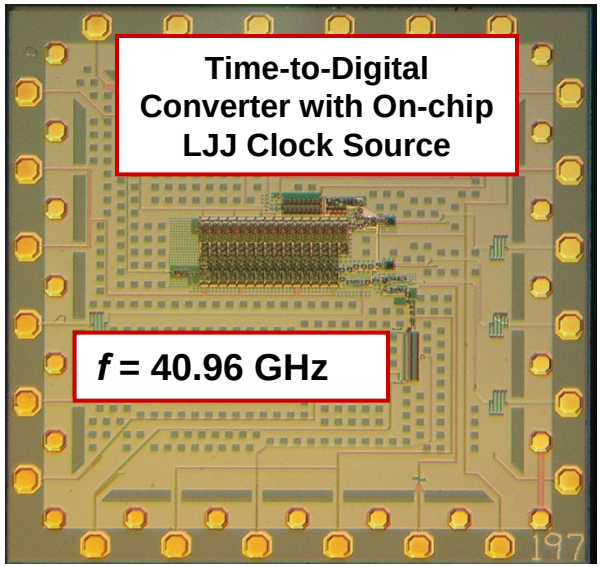
Ka-band BPΔΣ ADC with On-chip Clock

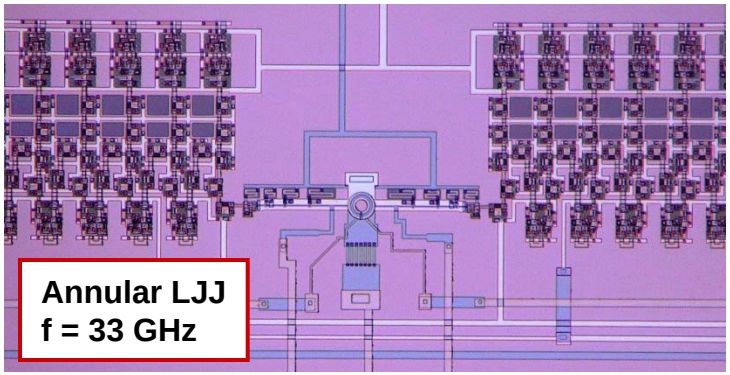
1) D. Gupta and Y. Zhang, "On-Chip Clock Technology for Ultra-Fast Digital Superconducting Electronics," *Applied Physics Letters*, vol. 76, no. 25, pp. 3819-3821, June 2000

2) Dmitri E. Kirichenko and Igor V. Vernik, "High Quality On-Chip Long Annular Josephson Junction Clock Source for Digital Superconducting Electronics" IEEE Trans. Appl. Supercond., vol 15, no 2, June 2005

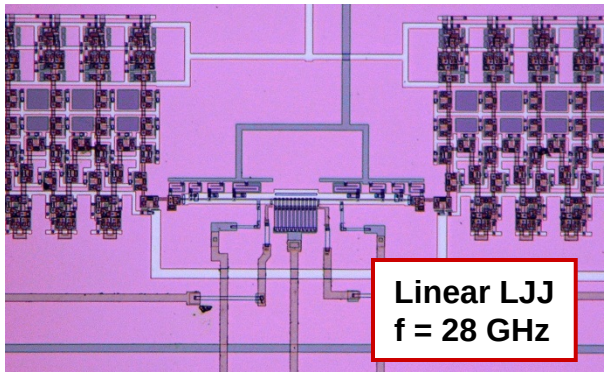
On-chip Clock Sources

- Long Josephson Junction (LJJ) Oscillators
- Linear and Annular LJJ with single and two-phase SFQ clock streams demonstrated[1]
  - *f* = 8-50 GHz
- Q = 4×10^5 - 1.3×10^6
  - Time jitter = 50-60 fs (measured by University of Rochester[2])





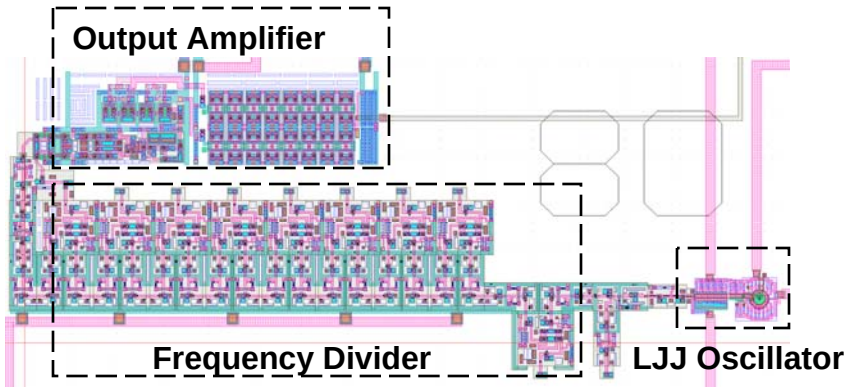
Funded in part by NSF



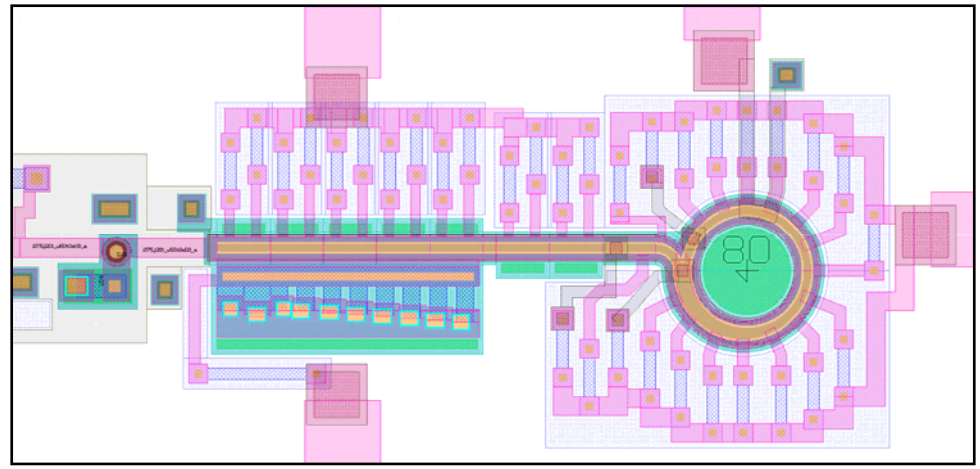
1. I. V. Vernik and D. Gupta, "Two-Phase 50 GHz On-Chip Long Josephson Junction Clock Source," presented at ASC 2002, to appear in *IEEE Trans. Appl. Supercond.* June 2003
2. J. L. Habif, C. A. Mancini, and M. F. Bocko, "Measurement of Jitter in a Long Josephson Junction Soliton Oscillator Clock Source," *IEEE Trans. Appl. Supercond.* vol. 11, pp. 1086-1089, March 2001.

HYPRES

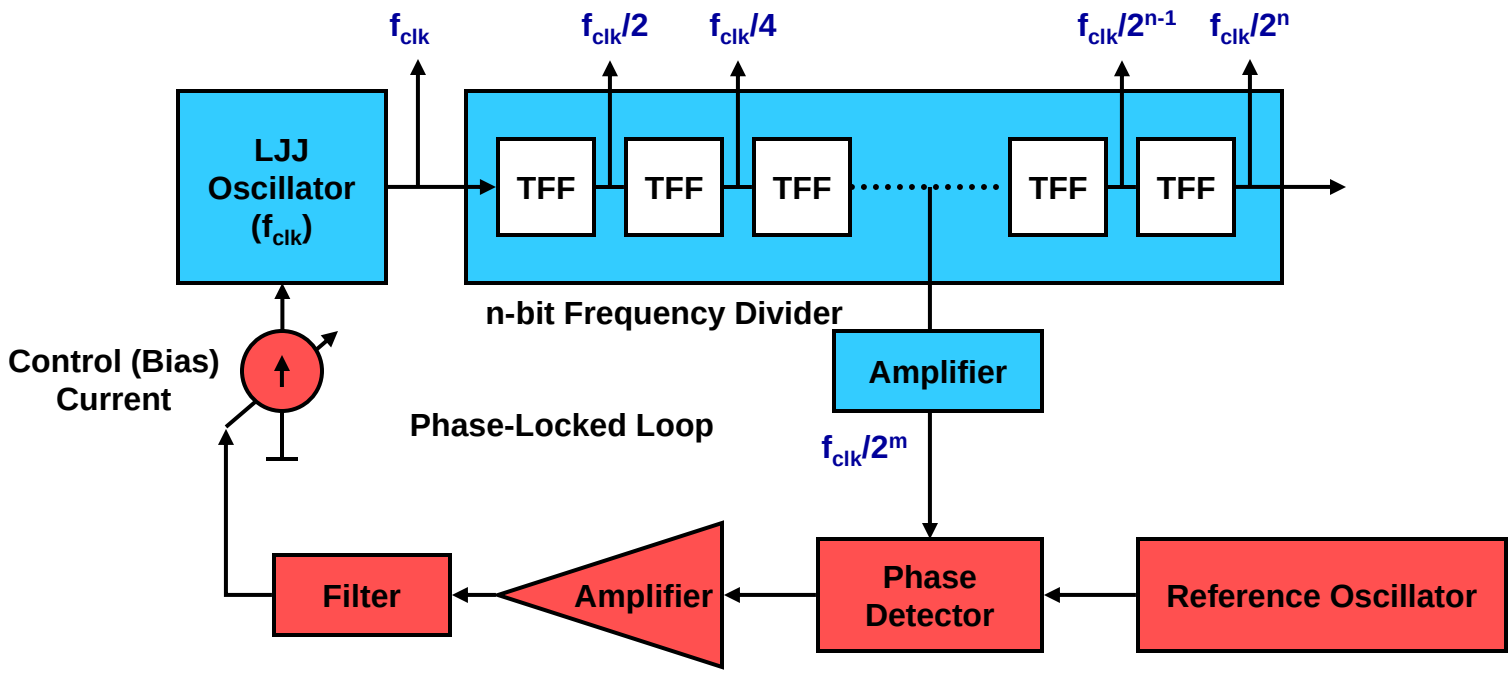
100-GHz On-chip Clock Source



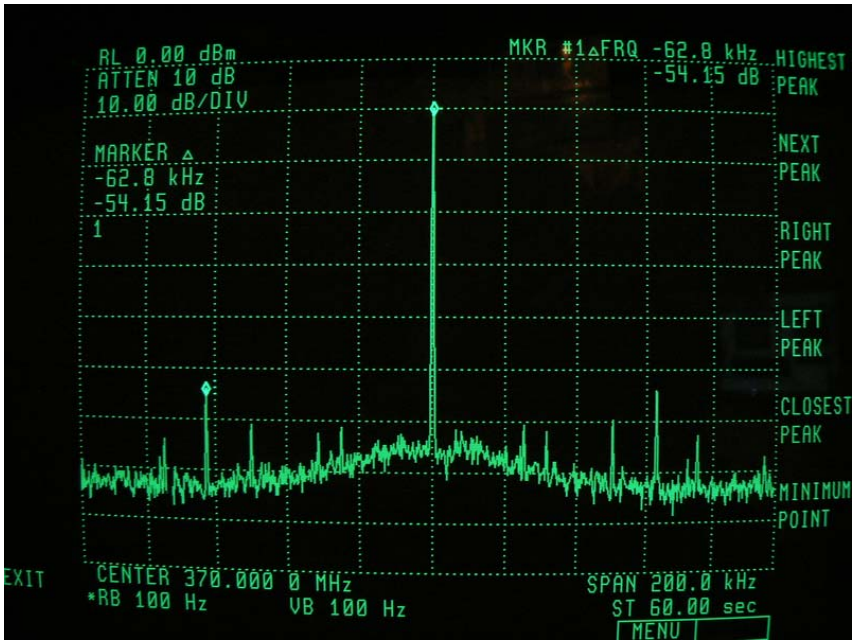
(a) Clock Source

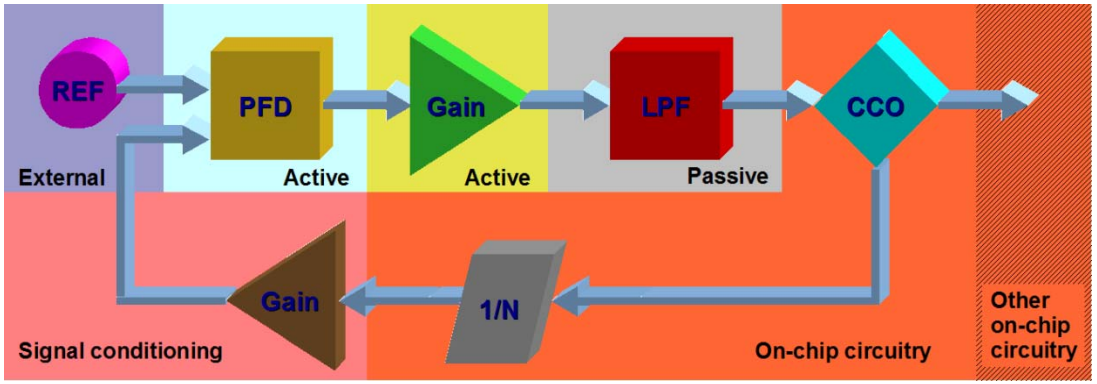


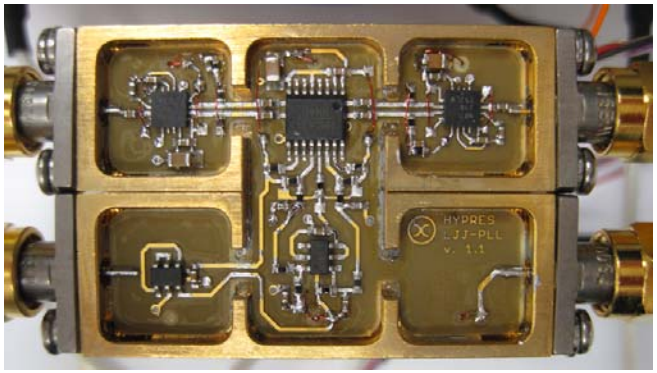
(b) 80-96 GHz LJJ Oscillator



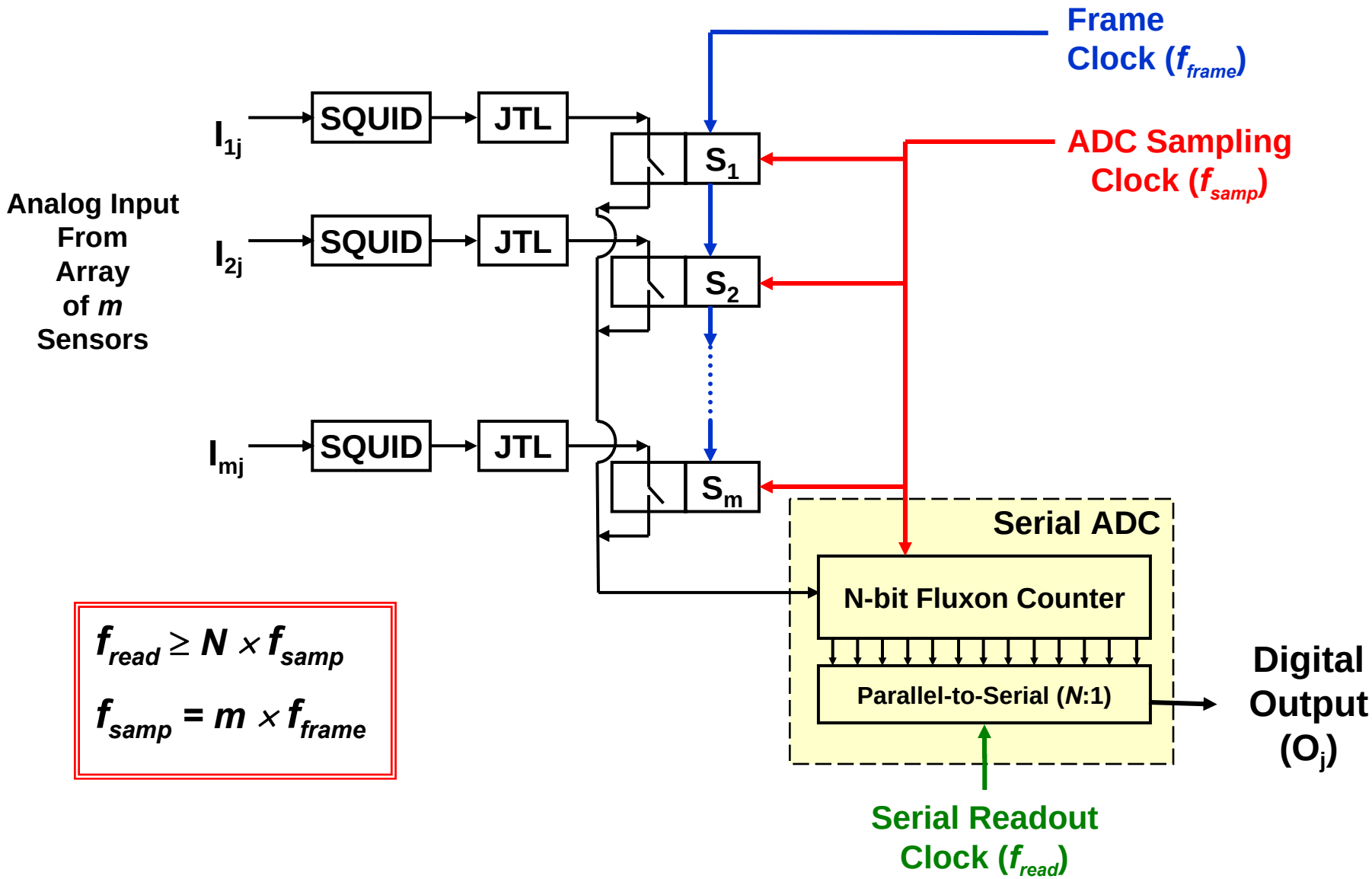
Phase-locked Loop for LJJ Clock







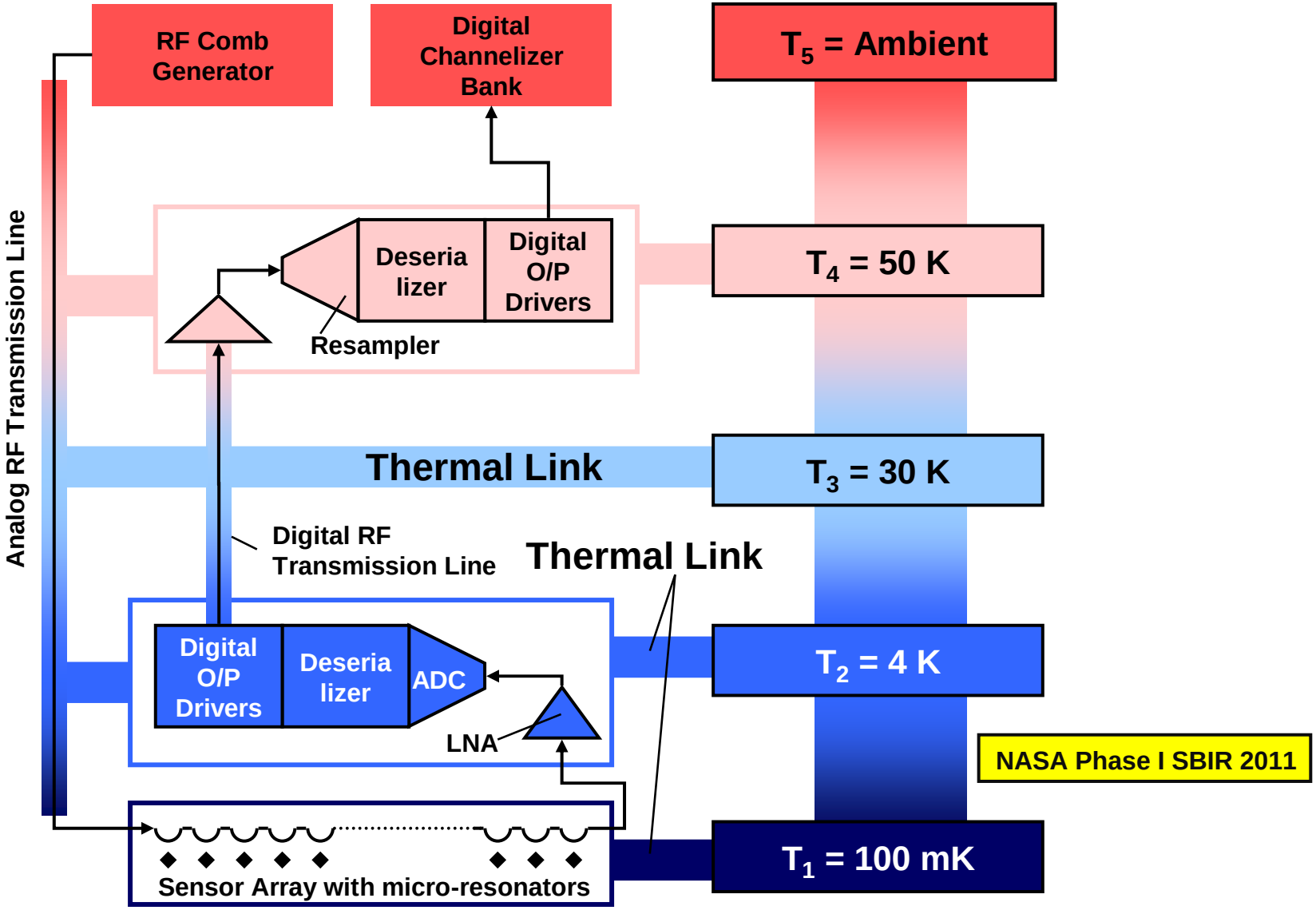
Digital Time Multiplexing Scheme



$$f_{read} \geq N \times f_{samp}$$

$$f_{samp} = m \times f_{frame}$$

Frequency Multiplexed Detector Readout



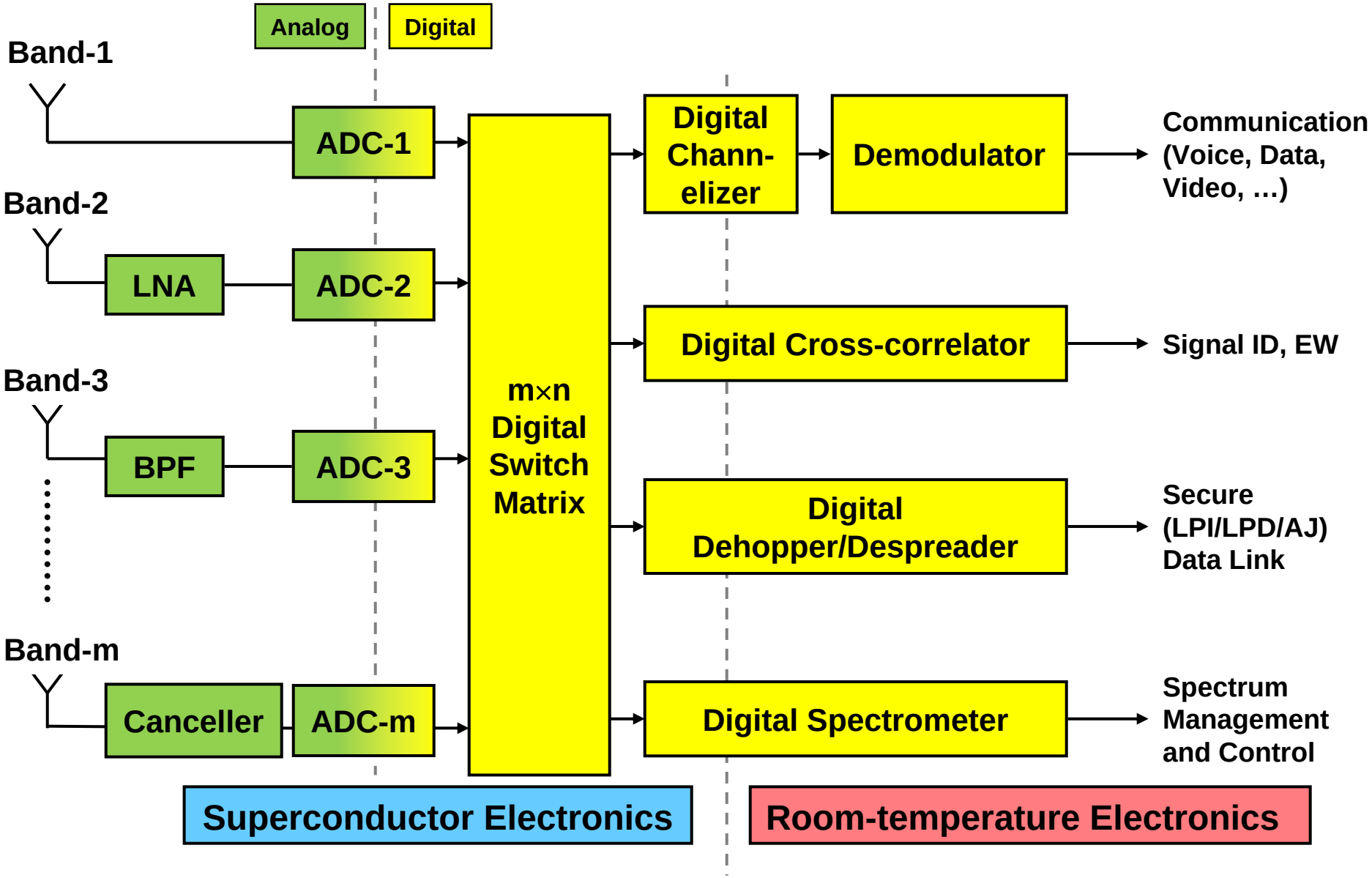
Methods to Decrease Cryocooler Heat Load

- **Three Major Contributors**
  - **Power Dissipation of Chip**
  - **Heat conduction and Joule Heating in DC Cables**
  - **Heat conduction through high-speed digital data lines**
- **Power dissipation of chip reduced by eliminating static power dissipation in conventional RSFQ: ERSFQ**
- **Contribution of DC Bias Cables reduced by**
  - **HTS Cables: 16x better than metal (measured, ONR SBIR), further reduction possible with dielectric substrate**
  - **Serial biasing ("current recycling"): 8x reduction proven (ONR)**
- **Contribution of data lines reduced by HTS ribbon cable**

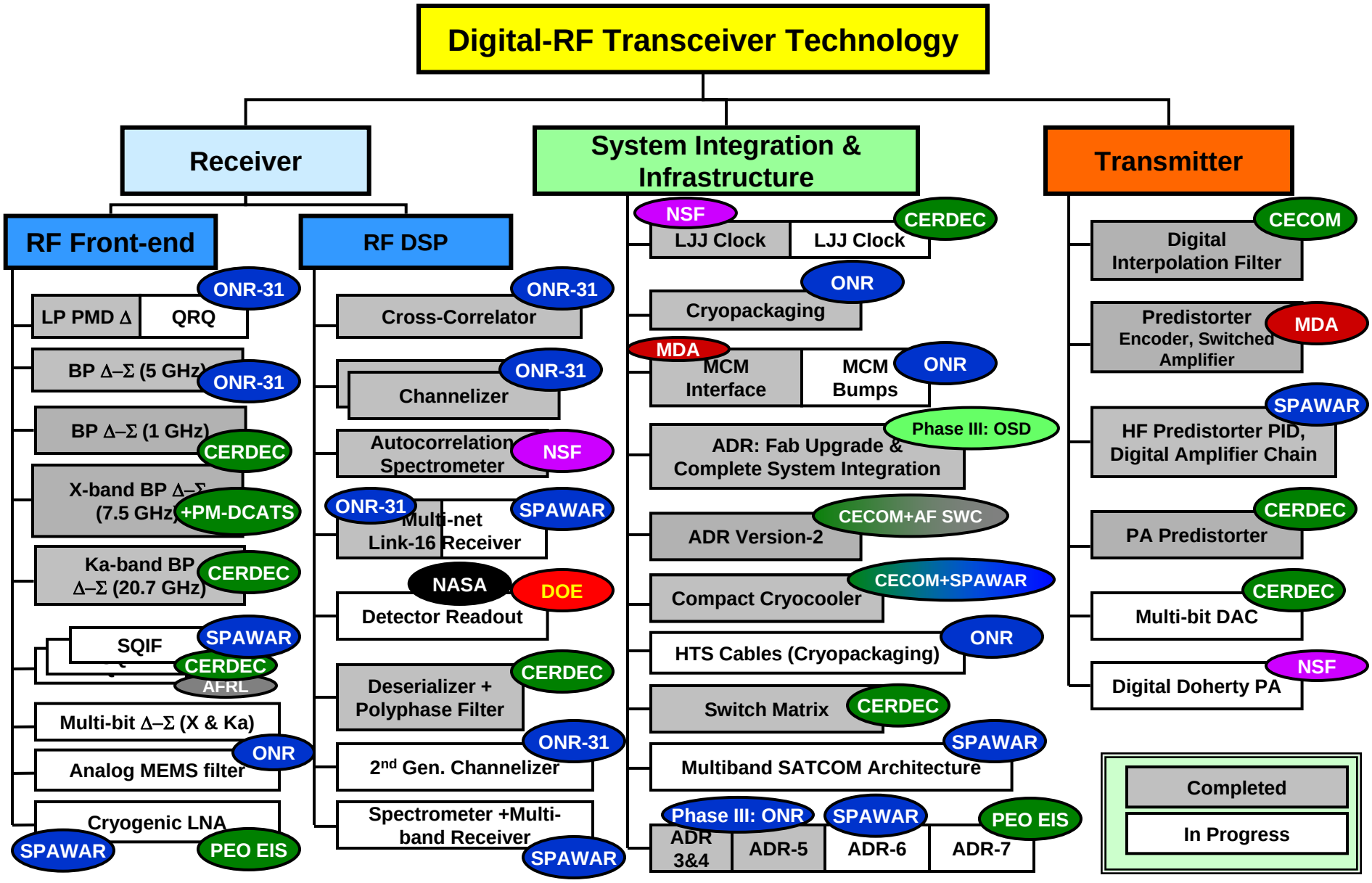
Digital-RF Receiver Concept

- **Direct digitization of RF signal**
  - No analog down-conversion
  - Wideband ADC (high sample rate, high dynamic range)
- **Digital processing of digitized RF signal (RF-DSP)**
  - Ultrafast digital logic
  - Polyphase digital processing
- **Digital switching and distribution**
  - Partitions ADC/DAC and RF-DSP
- **Hybrid Temperature Heterogeneous Technology System**
  - Different technologies (superconductor, semiconductor, photonic, etc.) at different temperatures between ambient and 4 K

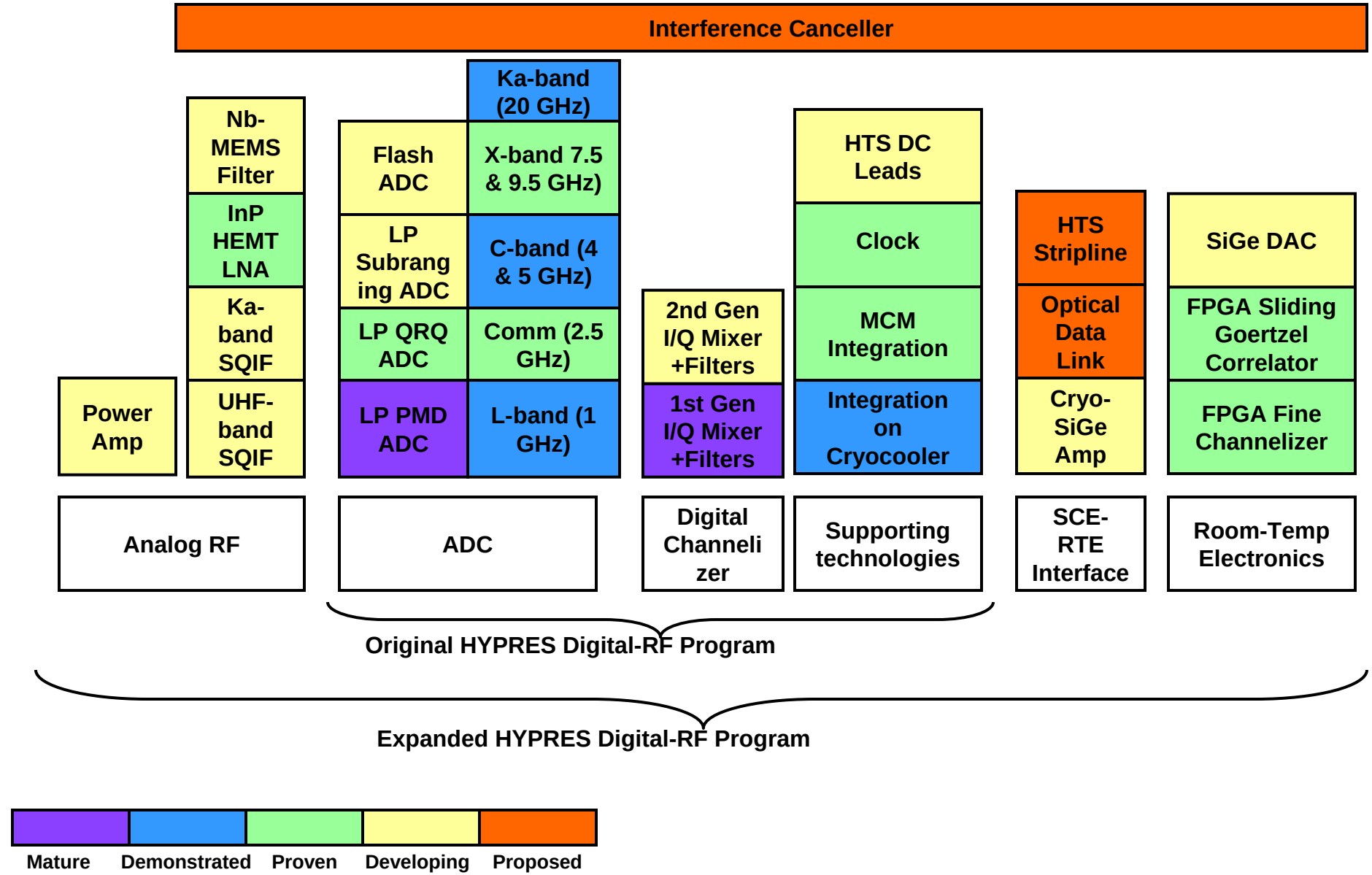
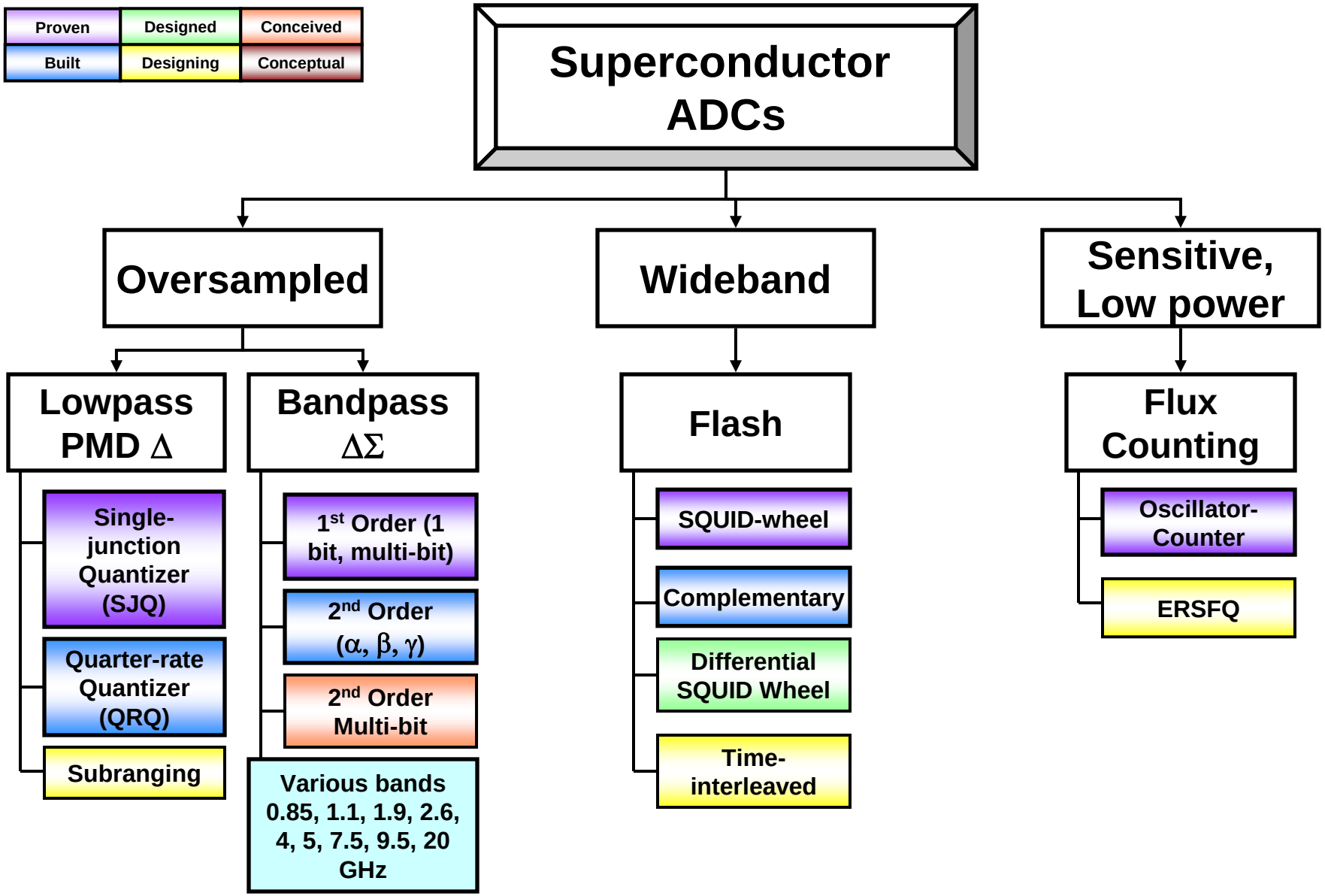
Digital-RF Receiver



HYPRES Digital-RF Program



Elements of Digital-RF Architecture



Different Types of Superconductor ADCs