BNL Instrumentation Division Seminar

40V LDMOS Hot Carrier mechanism investigation

Indiana University
Jack Wang

March 19, 2010

Outline

- Motivation
- Introduction
- HCI Damage Mechanism Investigation
- Charge pumping
- Summary
- Appendix: Personal experience in clean room process

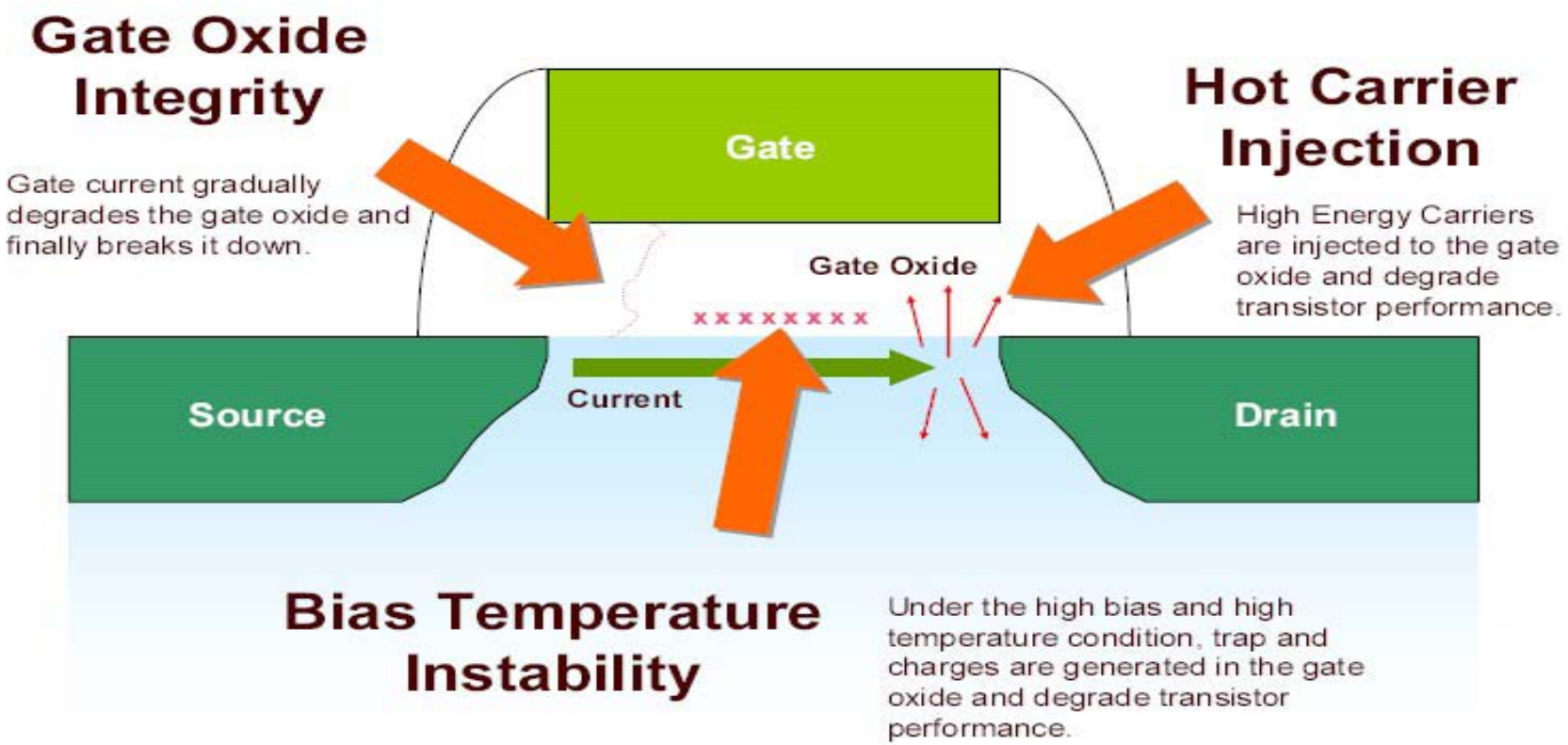
Motivation

(1) To investigate the Hot-Carrier-Induced (HCI) degradation mechanism of 40V LDNMOS.

(2) Build up Safe- Operation-Area (SOA) table for evaluating device performance and for circuit designer's reference.

Introduction

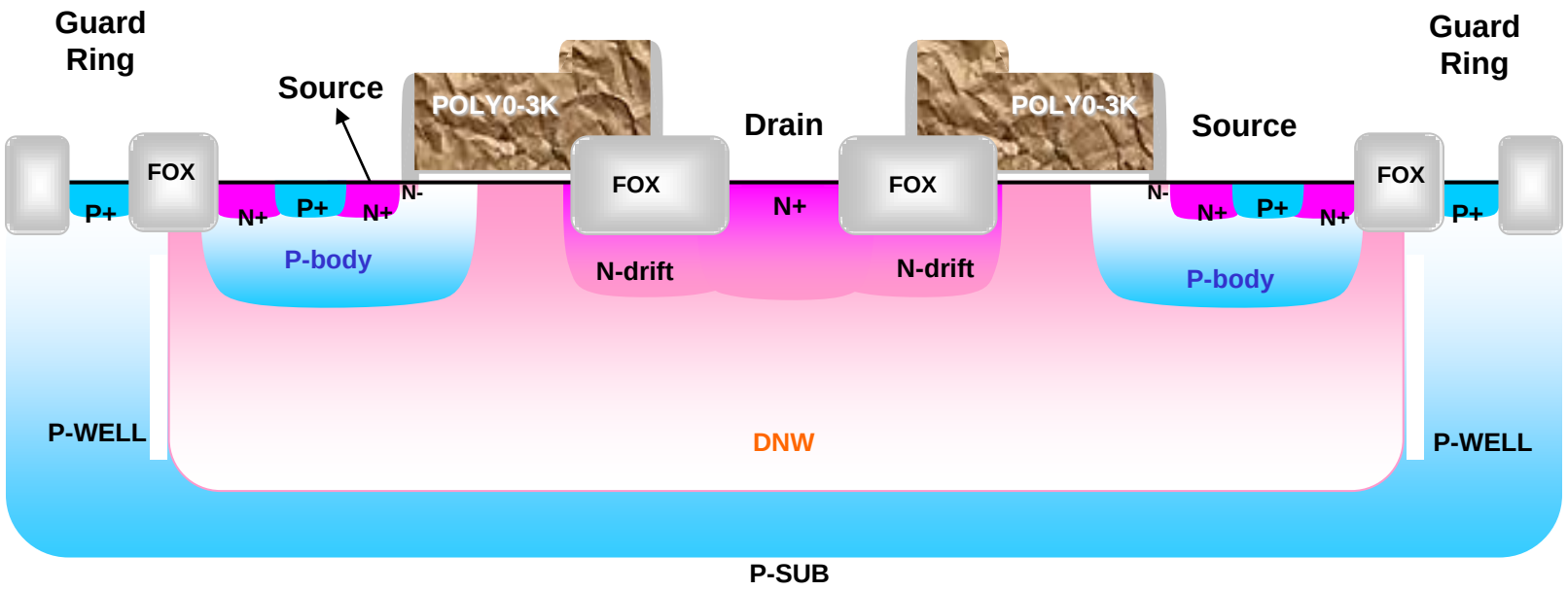
Transistor Reliability Concepts



Courtesy from Samsung Electronic Co.

Device structure

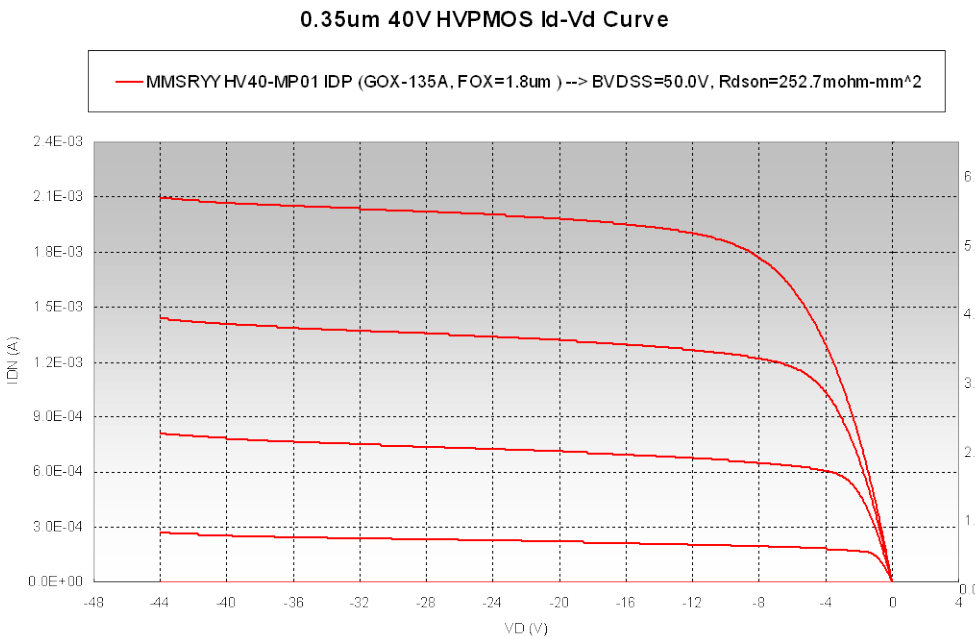
LDNMOS => Lateral Double Diffused MOS
(0.35um 40V LDNMOS)



I-V characteristics

40V HVPMOS I-V Curve

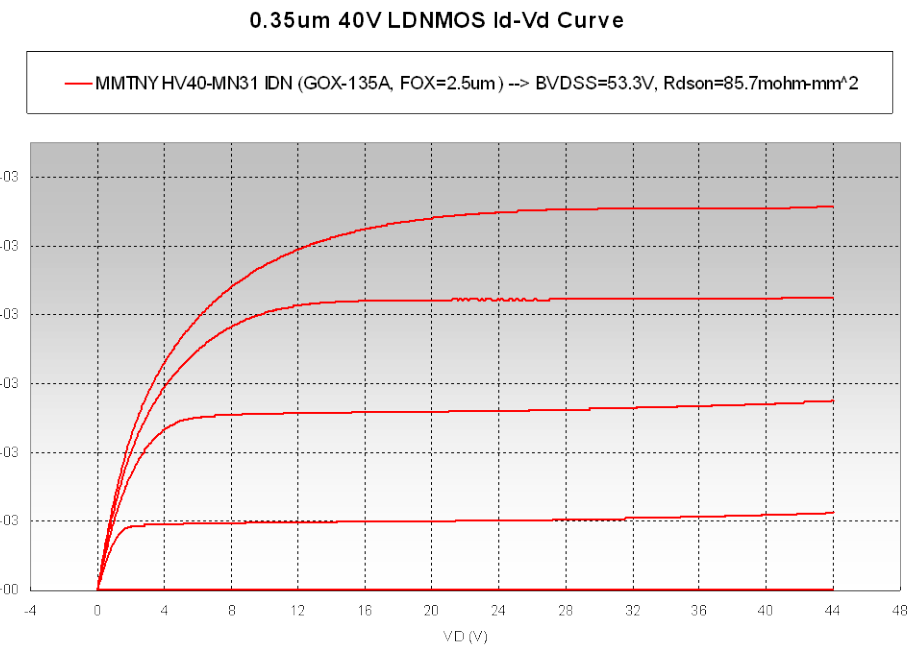
FOX LENGTH=1.8um
POLY LENGH=2.2um



BVDSS=50.0V, Rdson = 252.7mm-mohm^2

40V LDNMOS I-V Curve

FOX LENGTH=2.5um
POLY LENGH=2.2um



BVDSS=53.3V, Rdson = 85.7mm-mohm^2

Safe Operating Area (SOA)

Vg_{str} & Vd_{str} effect evaluation

Experiment plan

Vds effect

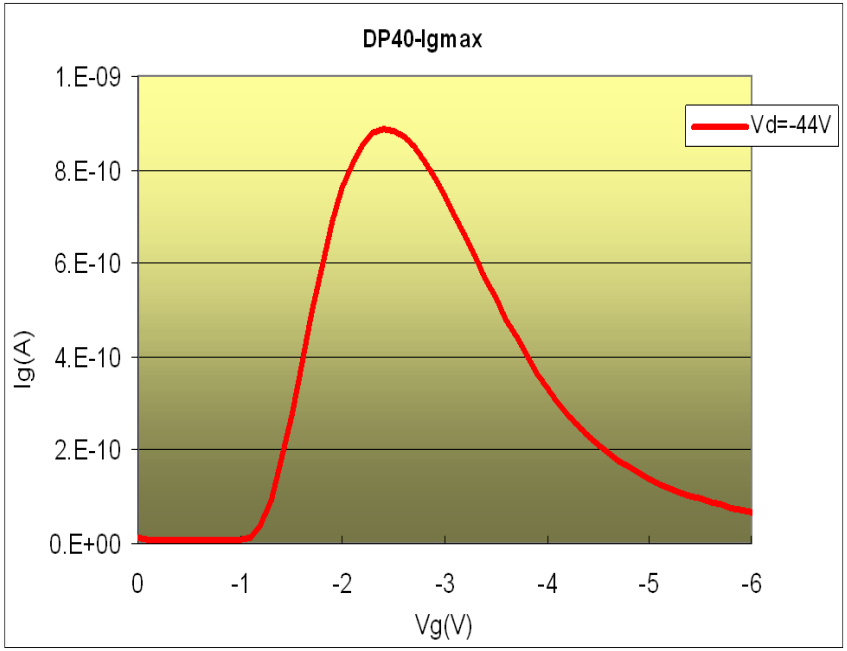
6					
5					
4					
3					
2					
1					
Vgs / Vds	10	30	35	40	44

Vgs effect

HCI Test Methodology Investigation

Vg Worst Case (PMOS)

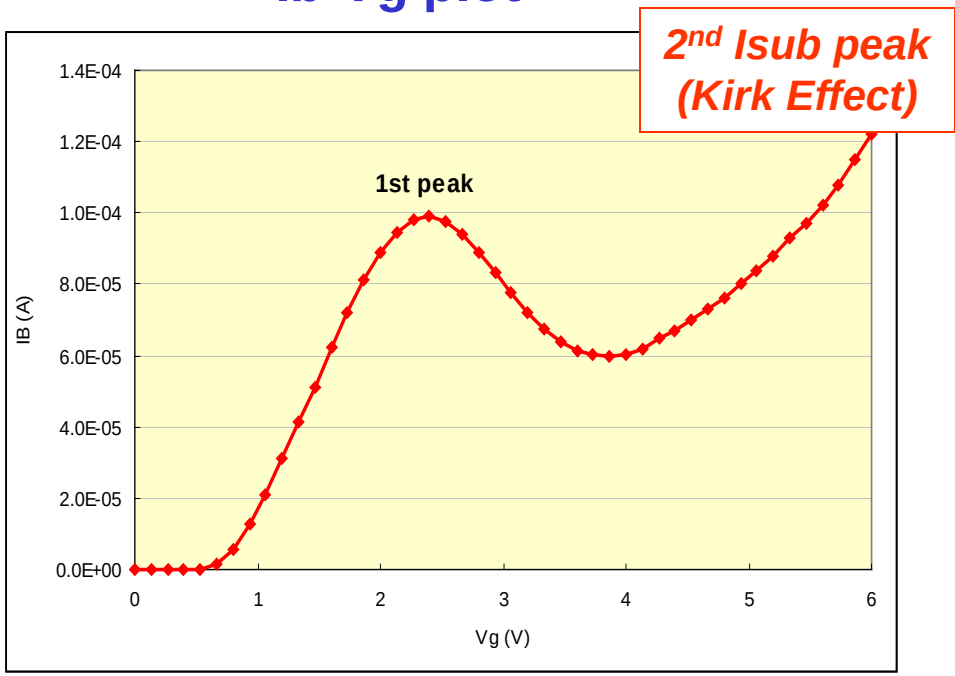
Ig-Vg plot



Vg worst case :Vg @ Ig_{max}

Vg Worst Case (NMOS)

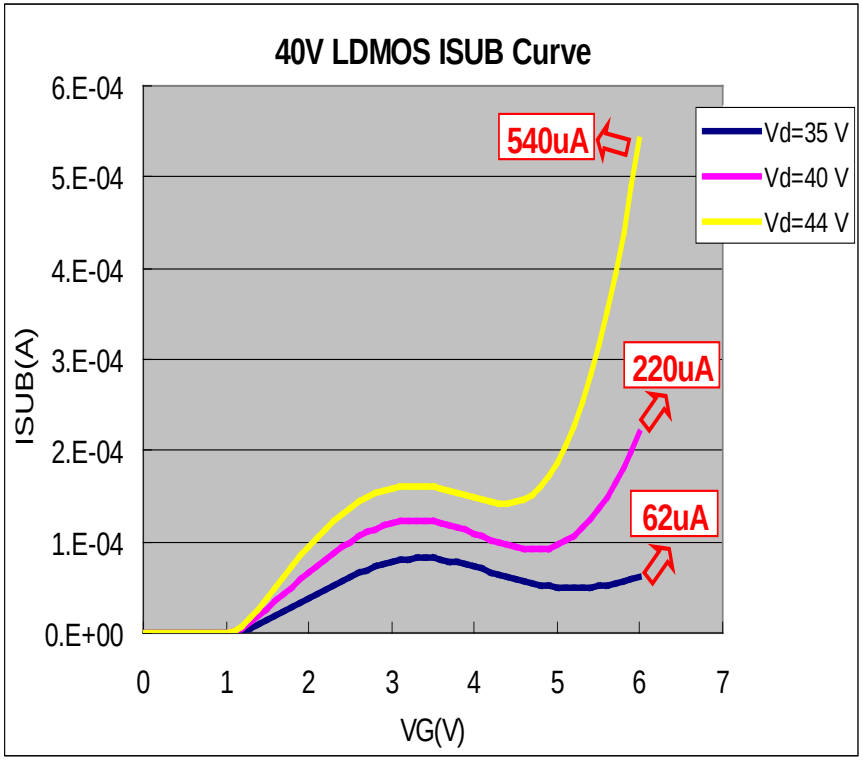
Ib-Vg plot

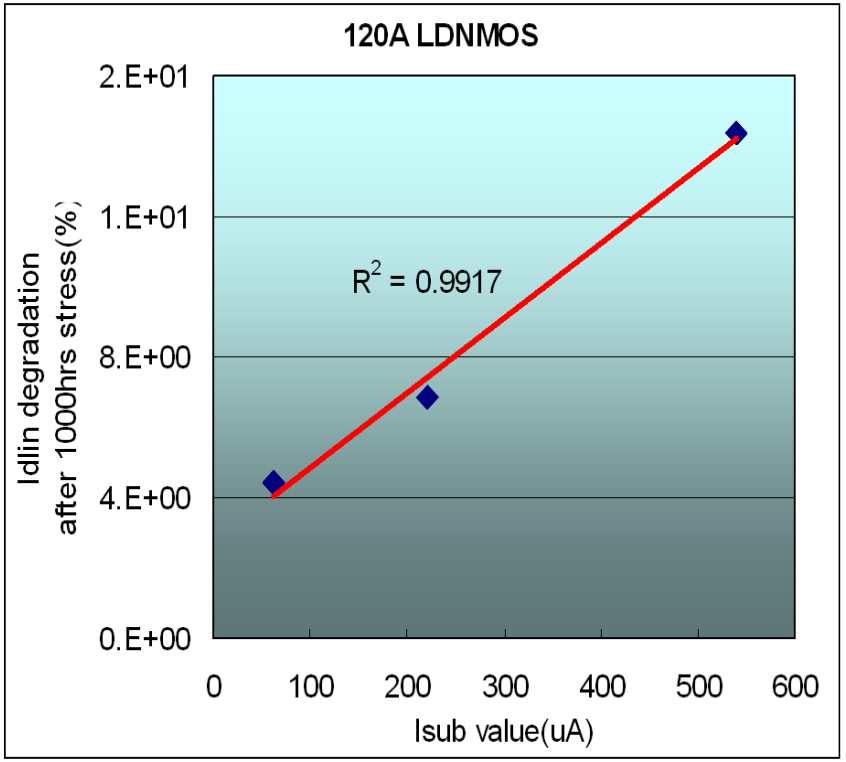


Vg worst case :Vg @ Vg_{max}

HCI Test Methodology Investigation

Vd Dependence (Vgstr/Vdstr= 6V/44V, 6V/40V, 6V/35V)



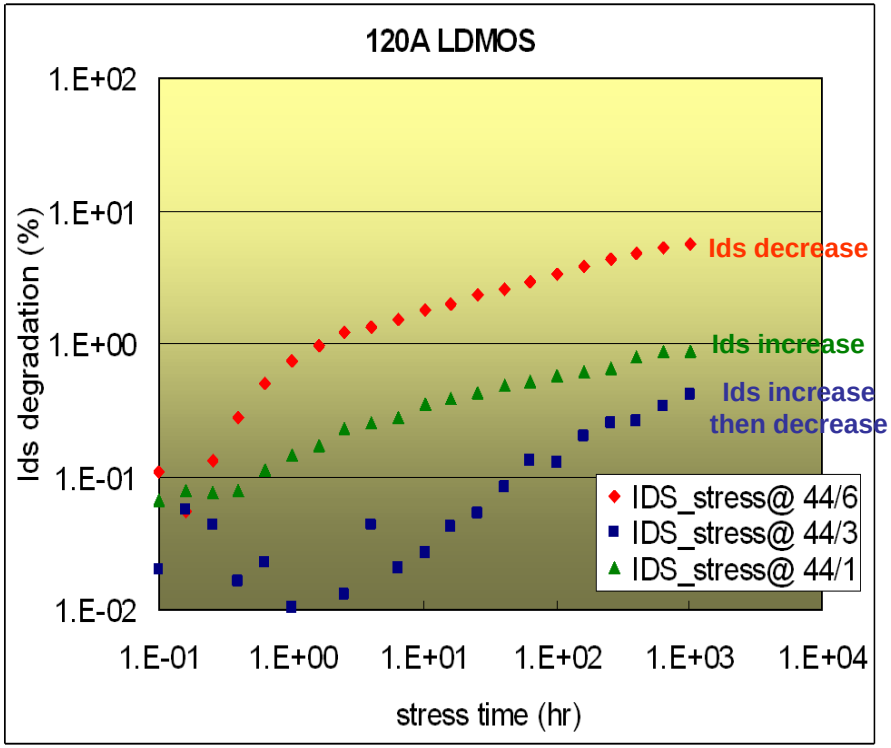


- The larger Vdstr, the larger Isub and worse damage were observed.
- Good correlation between Isub & Idlin TTF.

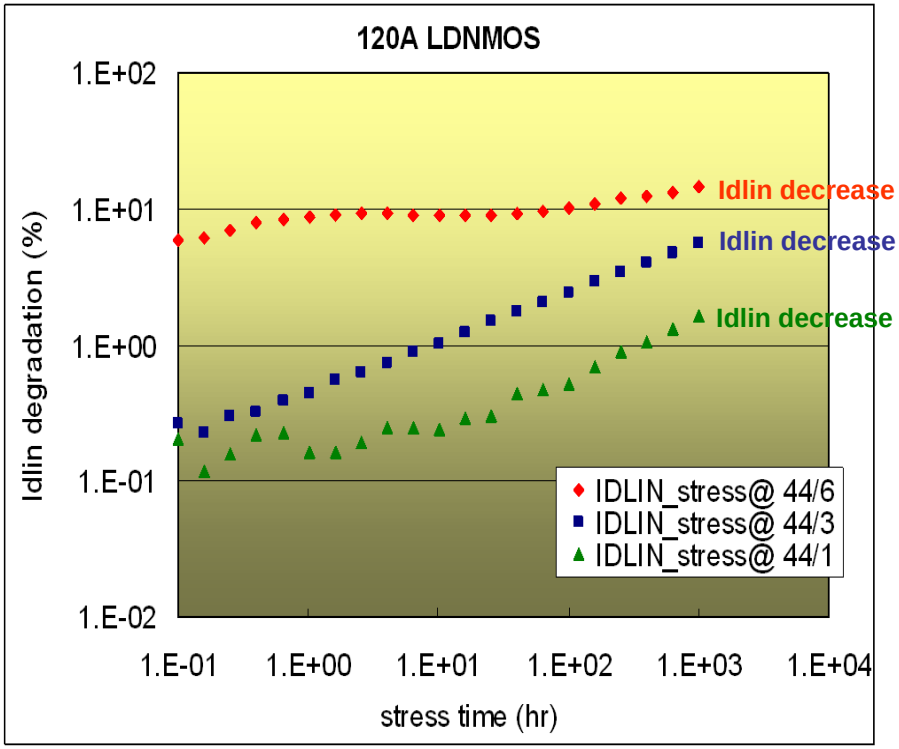
HCI Test Methodology Investigation

Vg Worst Case Verification (LDNMOS)

Ids shift



Idlin shift

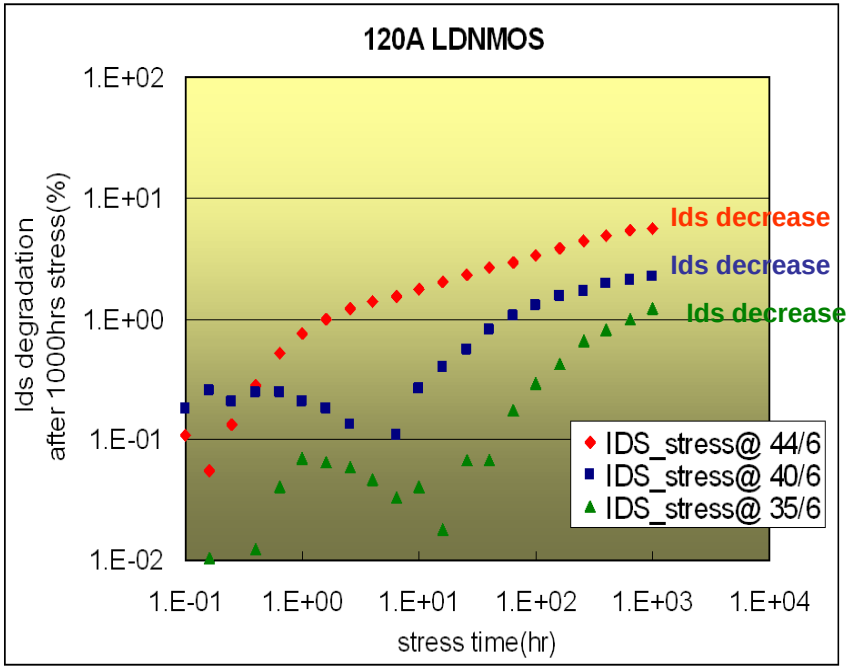


Vg worse case is at Vg=6V.

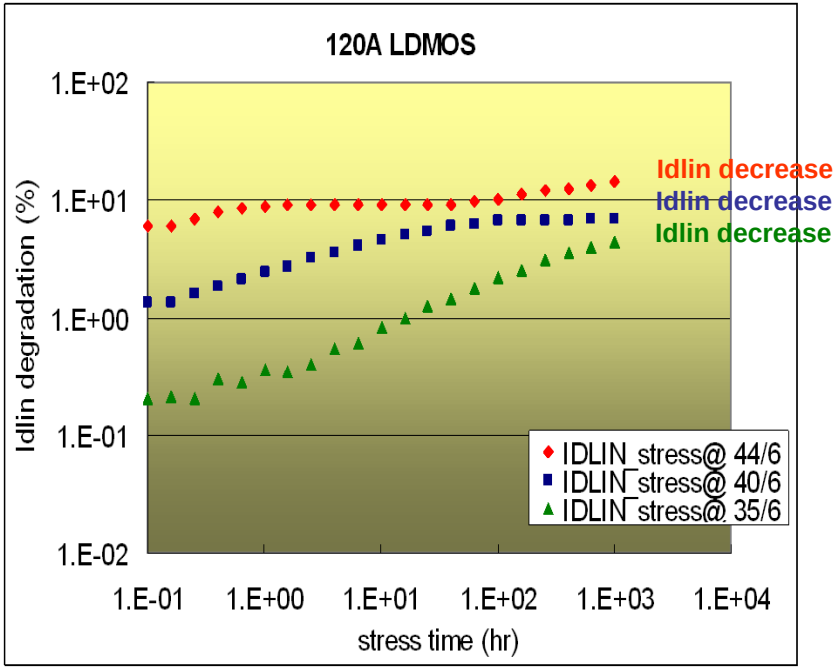
HCI Test Methodology Investigation

Vd Dependence (Vgstr/Vdstr= 6V/44V, 6V/40V, 6V/35V)

Ids shift



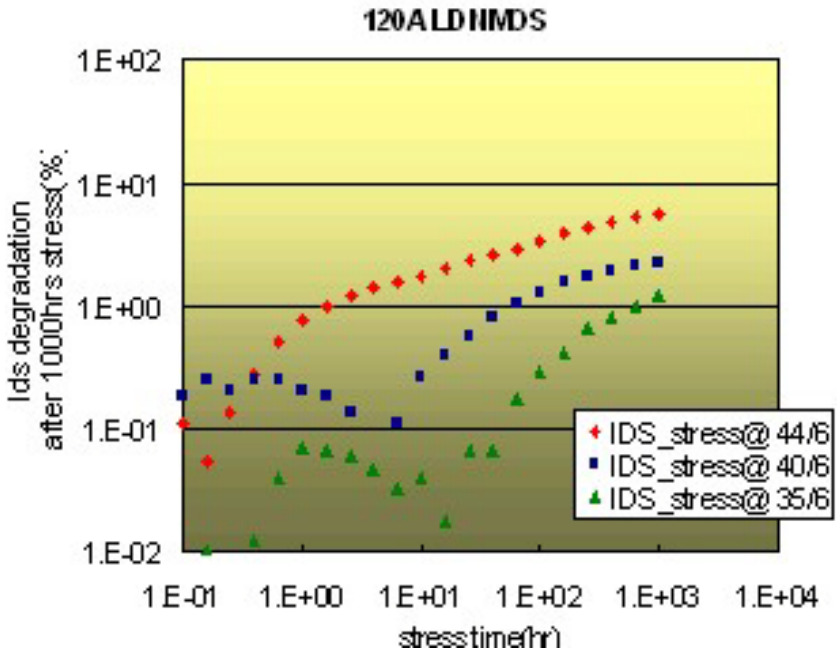
Idlin shift

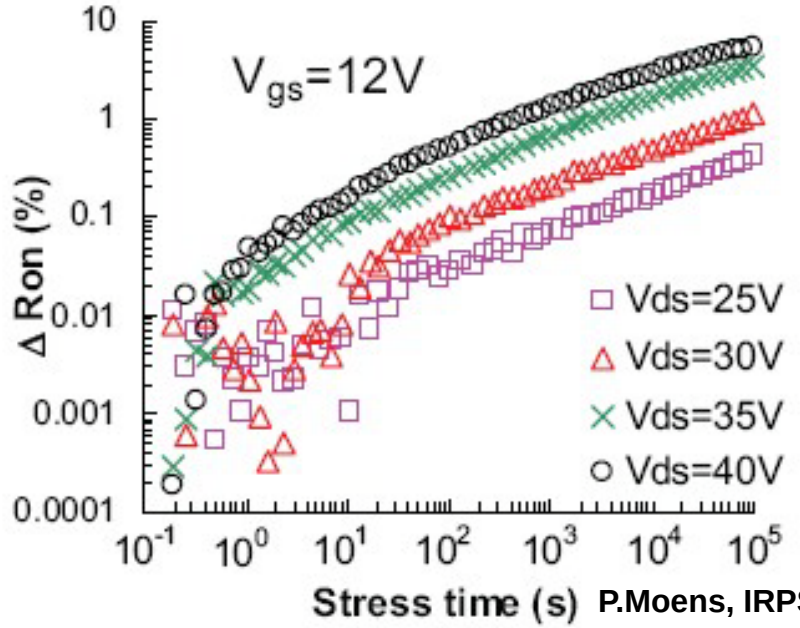


Vd worse case is at Vd=44V (Max. Vdstr).

HCI Test Methodology Investigation

Vd Dependence





P.Moens, IRPS,2007

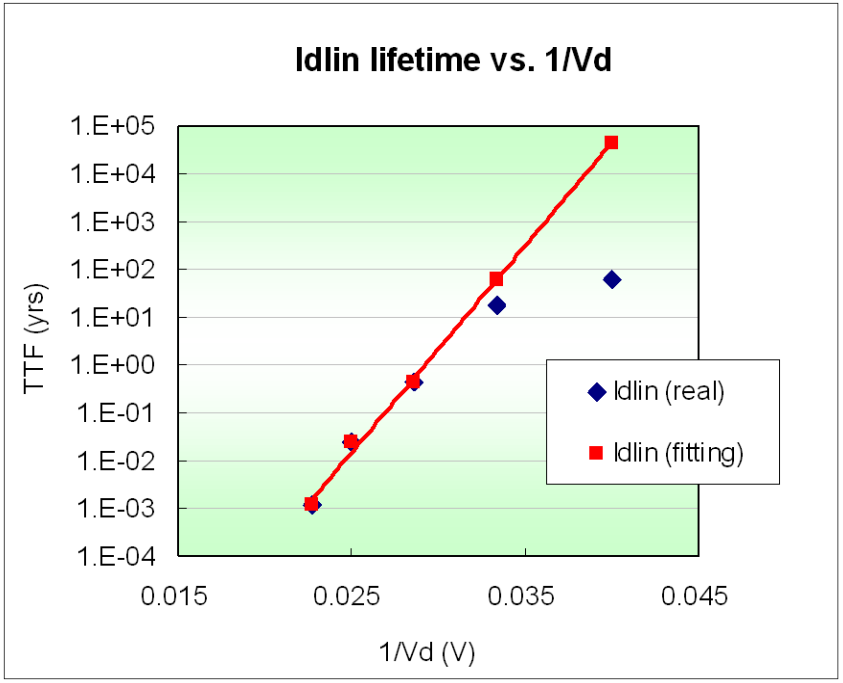
- ***Hole trapping was observed at different Vdstr. As Vdstr increase, more worse degradation cause by interface state generation and leads to the turn-over behavior at shorter stress time.***

- ***As stress time increase, the degradation slope are the same (Dit dominate), so the degradation mechanism are similar at different Vdstr***

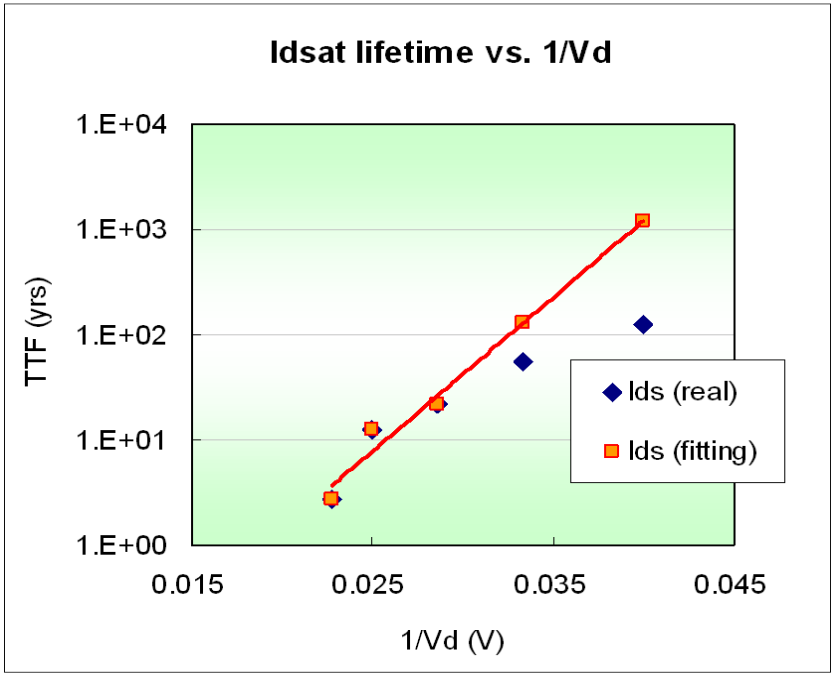
HCI Test Methodology Investigation

Lifetime Model Verification (1/Vd Model)

Idlin



Idsat



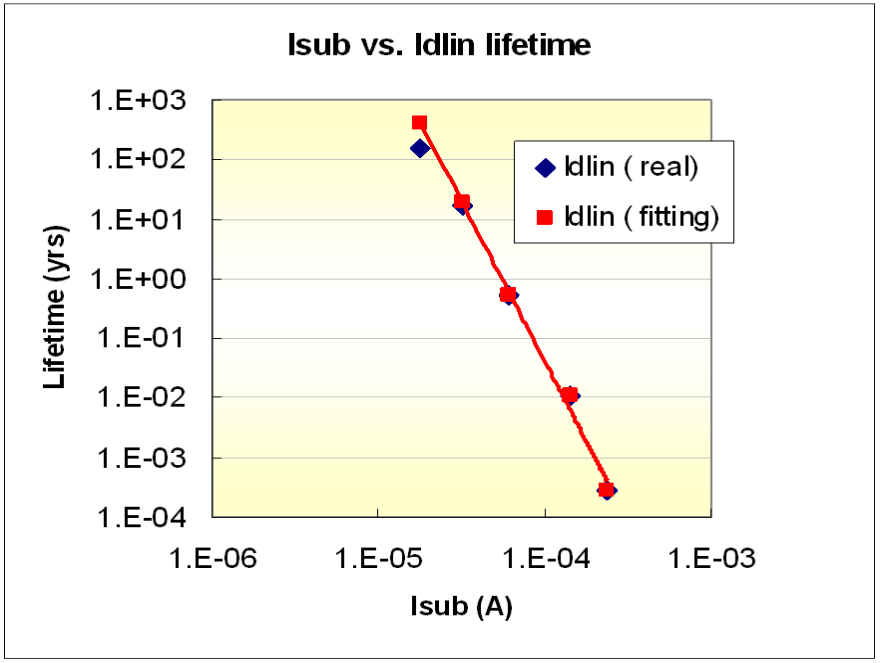
- ***HCI lifetime will overestimate if we use higher stress voltage's TTF to extrapolate lower stress voltage's lifetime.***

- ***So in PMIC HCI SOA assessment, each test condition need real stress to get more accurate lifetime.***

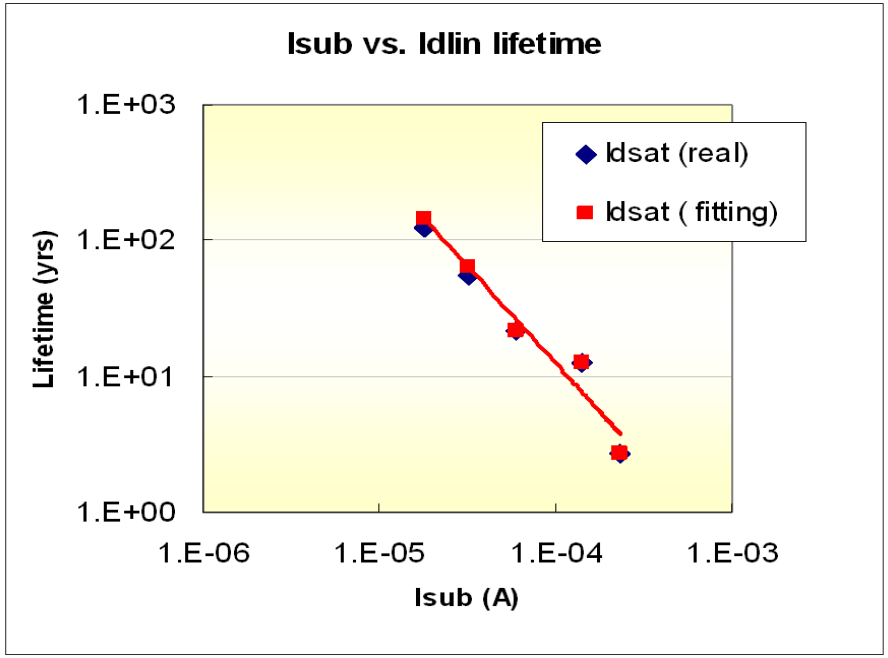
HCI Test Methodology Investigation

Lifetime Model Verification (Isub Model)

Idlin



Idsat



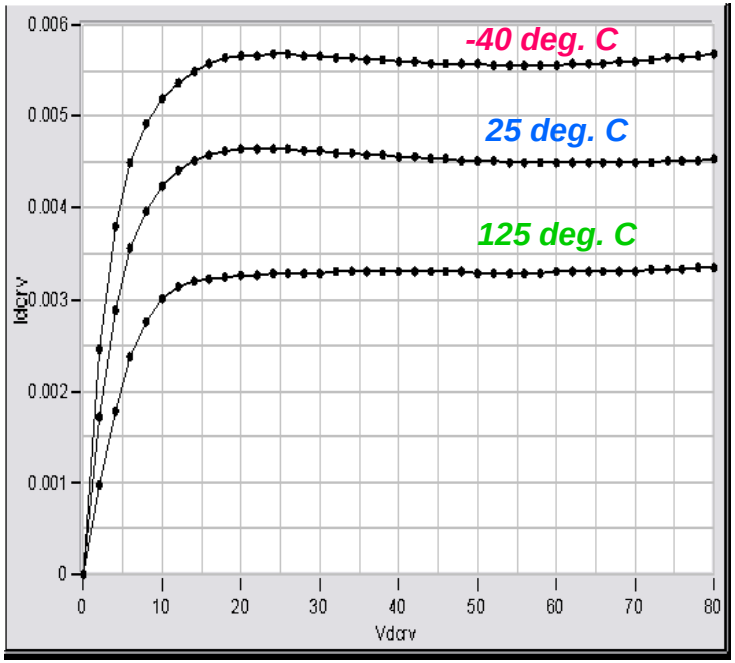
- ***Better correlation between Isub vs. lifetime, so Isub can be the method for quick HCI SOA evaluation.***

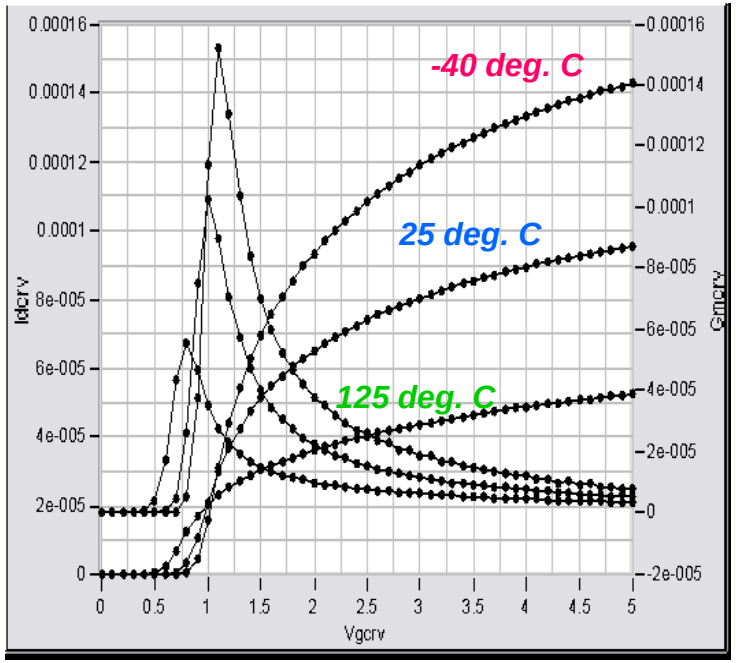
- ***Need non-butting contact testkey for the method.***

HCI Test Methodology Investigation

Temperature Effect

LDNMOS_Initial electric characterization



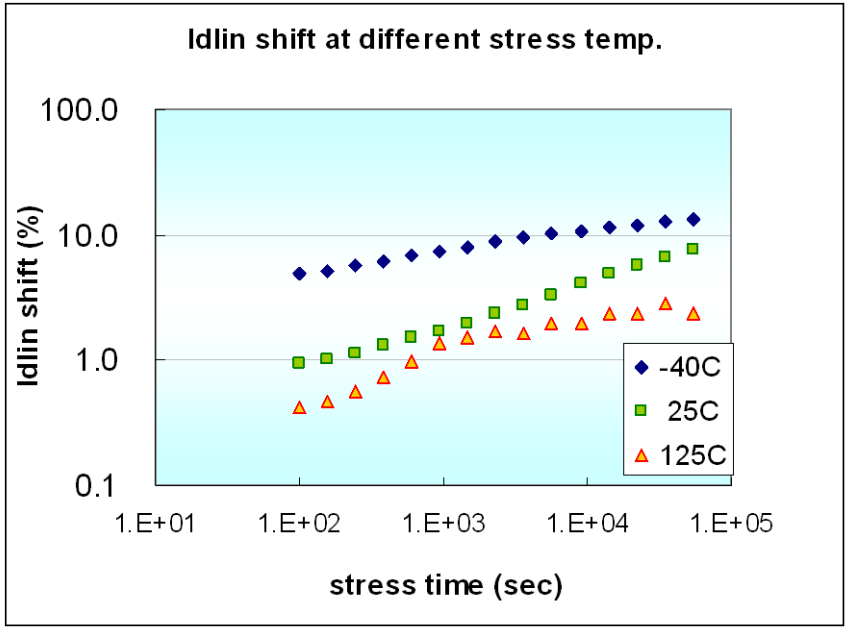


As temperature increase, Ids decrease due to lower carrier mobility at higher temperature. But Vth will also decrease due to band-gap narrowing. The behavior of PMIC device is similar as logic device.

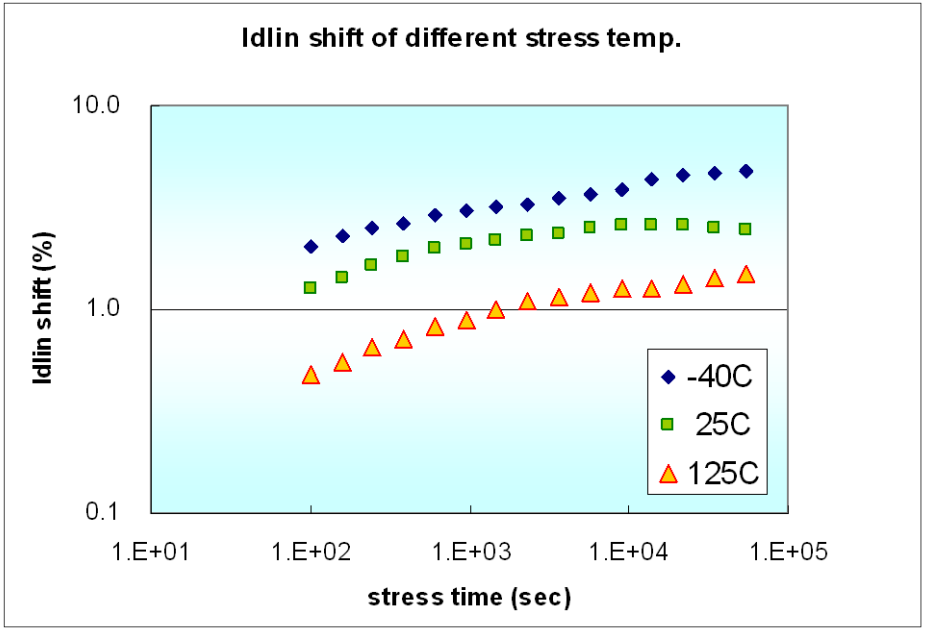
HCI Test Methodology Investigation

Temperature Effect

NMOS



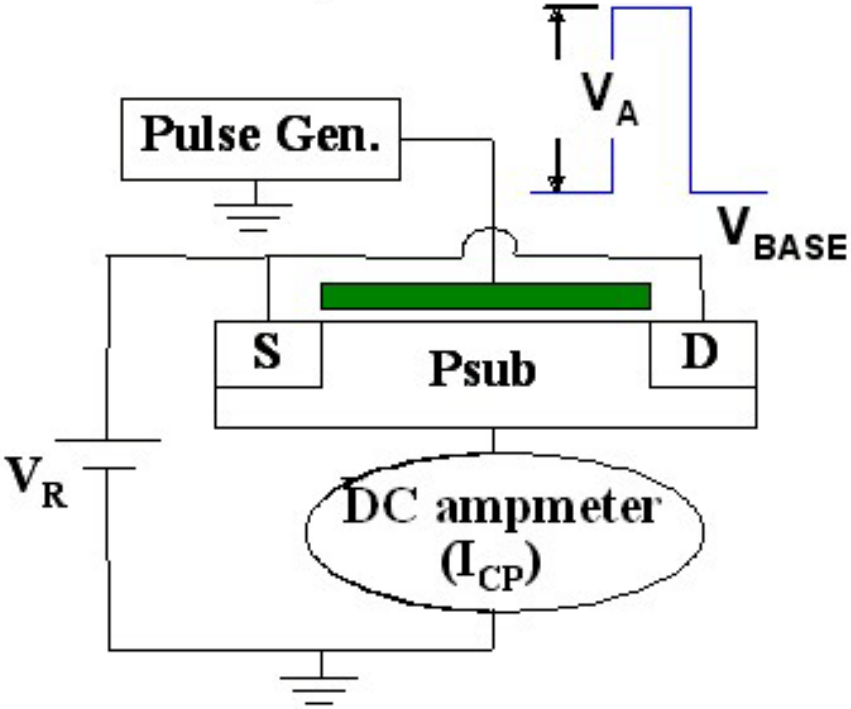
PMOS

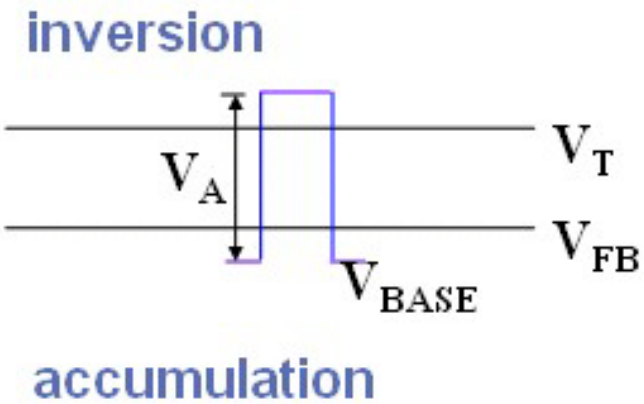


Ids & Idlin degradation increase as temperature decrease.

Charge Pumping Technique

- An AC pulse with variable base level (V_{BASE}) is applied to the gate while monitoring substrate current (I_{CP})
- The amplitude of the AC pulse (V_A) must be large enough to swing the surface potential from accumulation to inversion

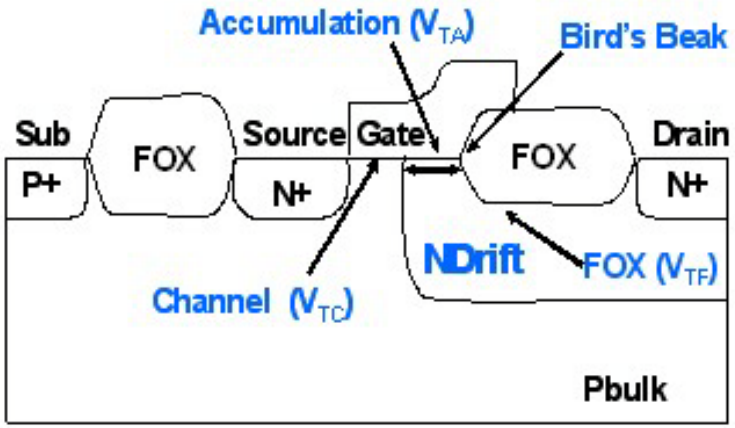


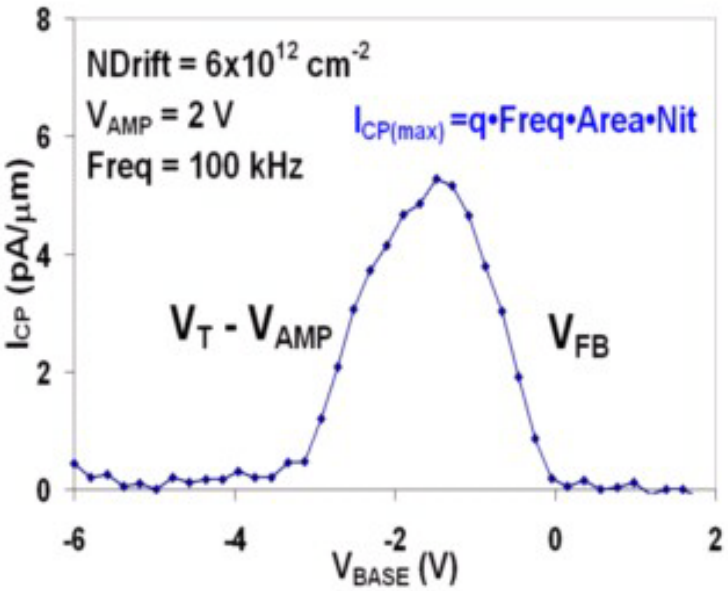


Reference: Doug Brisbin et al., IRPS 2006

NLDMOS Charge Pumping Technique

- I_{CP} is a composite of channel, accum. and bird's beak regions each with a different V_T, V_{FB}
- The thick FOX doesn't contribute to I_{CP} because of its large V_T (V_{TF})





- The I_{CP} max amplitude ($I_{CP(MAX)}$) is directly proportional to the fast interface trap density (Nit)

Reference: Doug Brisbin et al., IRPS 2006

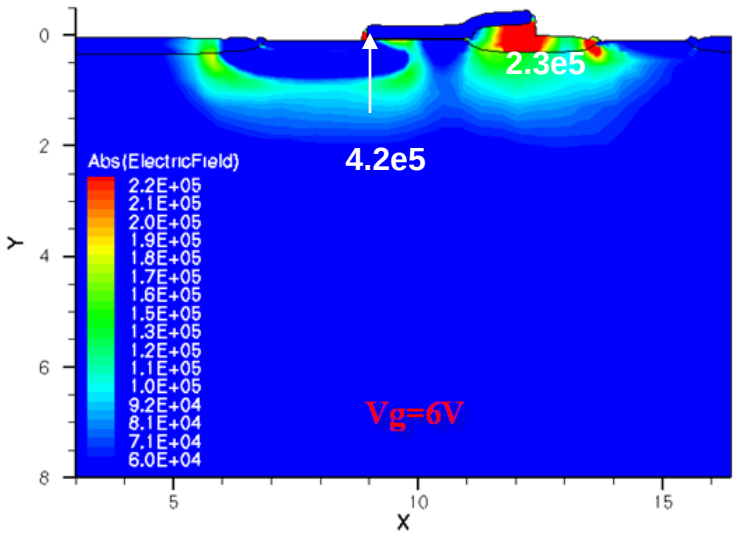
HCI Mechanism Investigation

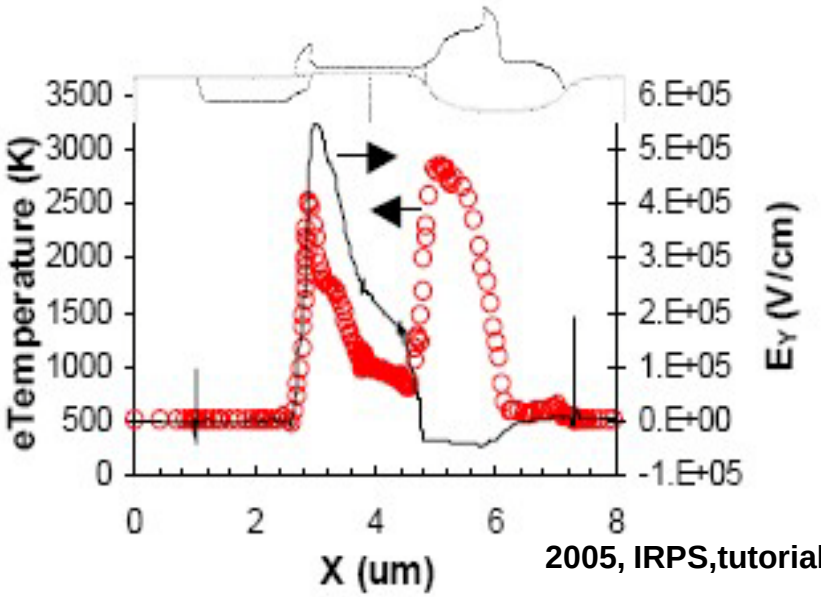
HCI Mechanism Investigation

Vgstr/Vdstr=6/44

Source Inject at high Vgs

Electric field @Vg=6V





2005, IRPS,tutorial

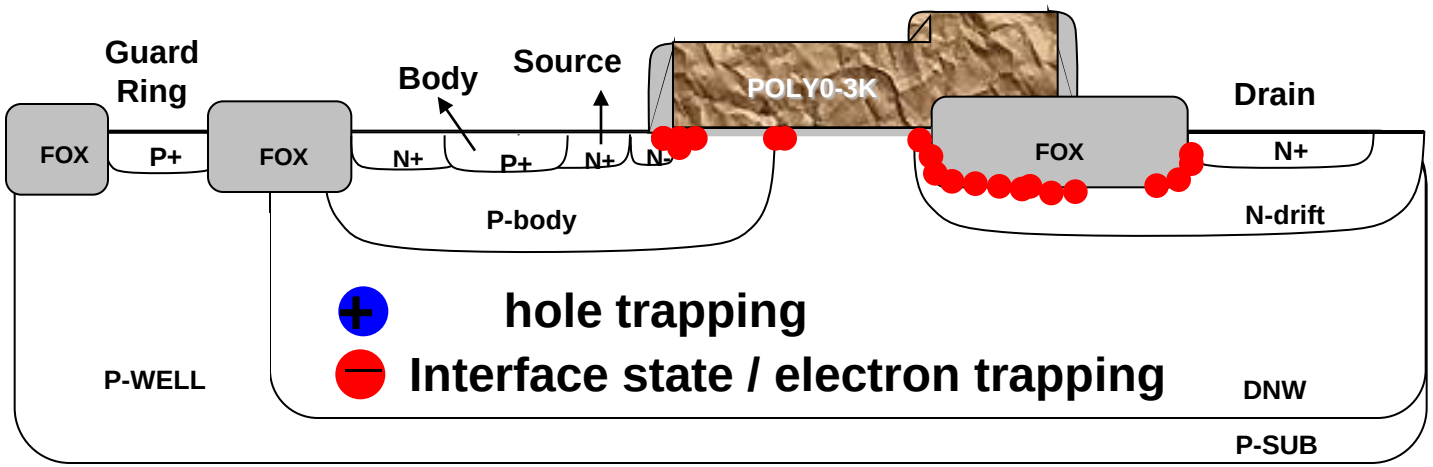
- NLDD does is too low for self-align P-body does: E-field build at source
- Carrier injection at source & leads to large Vth shift. The damage is independent of Vdstr

HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=6/44

HCI Damage Mechanism



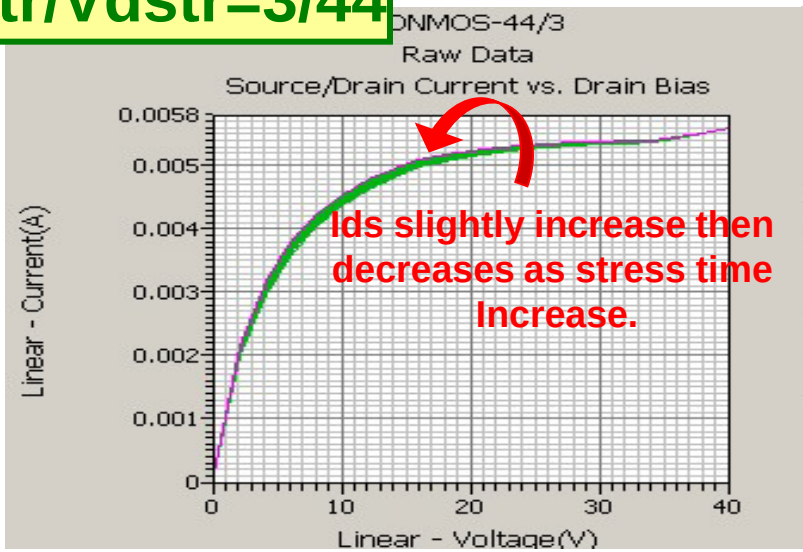
- The interface state exist near the channel region, bird's beak/FOX region and drain side.
- The hole trapping was almost not found. (Ids & Idlin degrade monotonously at each monitor point & monitor time)

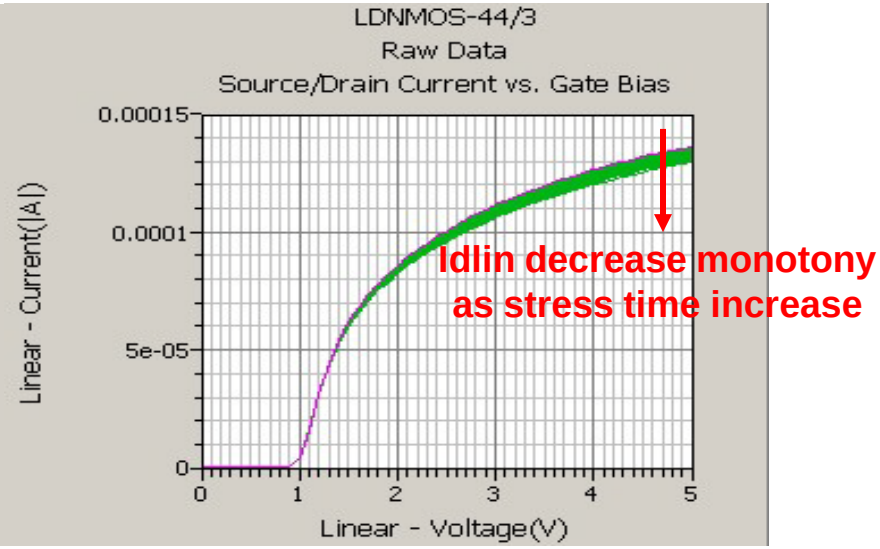
HCI Mechanism Investigation

HCI Mechanism Investigation

HCI Damage Mechanism Investigation by Variation of IV Curve

Vgstr/Vdstr=3/44





IdVd **IdVg**

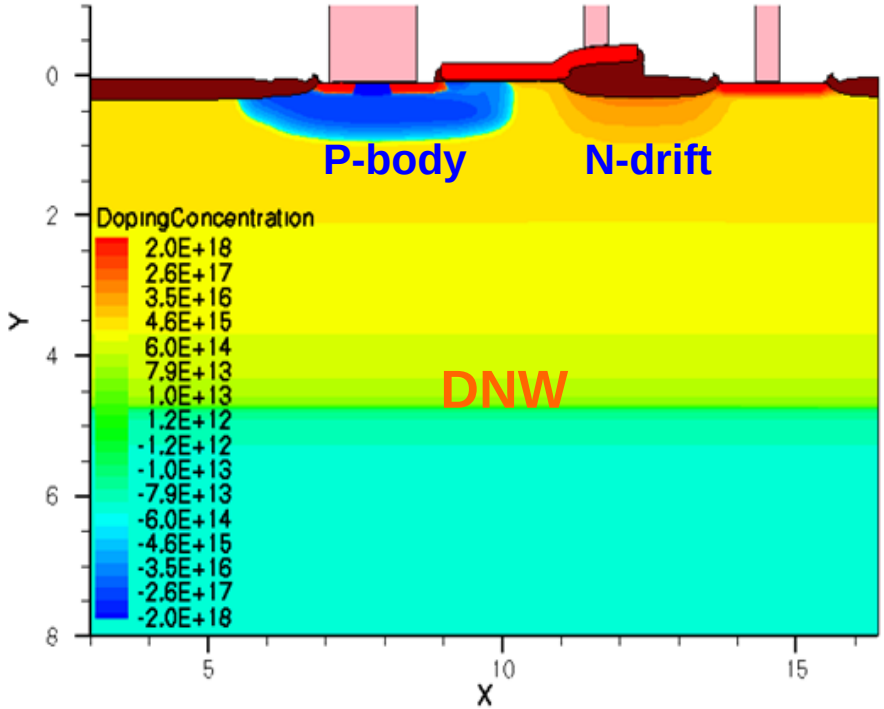
- **In IdVd curve, Ids *slightly* increase at 1st stage (hole trapping) , but decrease after 10hrs stress. (interface state generation). Moreover, as Vd decrease (approach to linear region) at longer stress time, *Id decrease more obvious*.**
- **In IdVg curve, Idlin decrease as stress time increase.**

HCI Mechanism Investigation

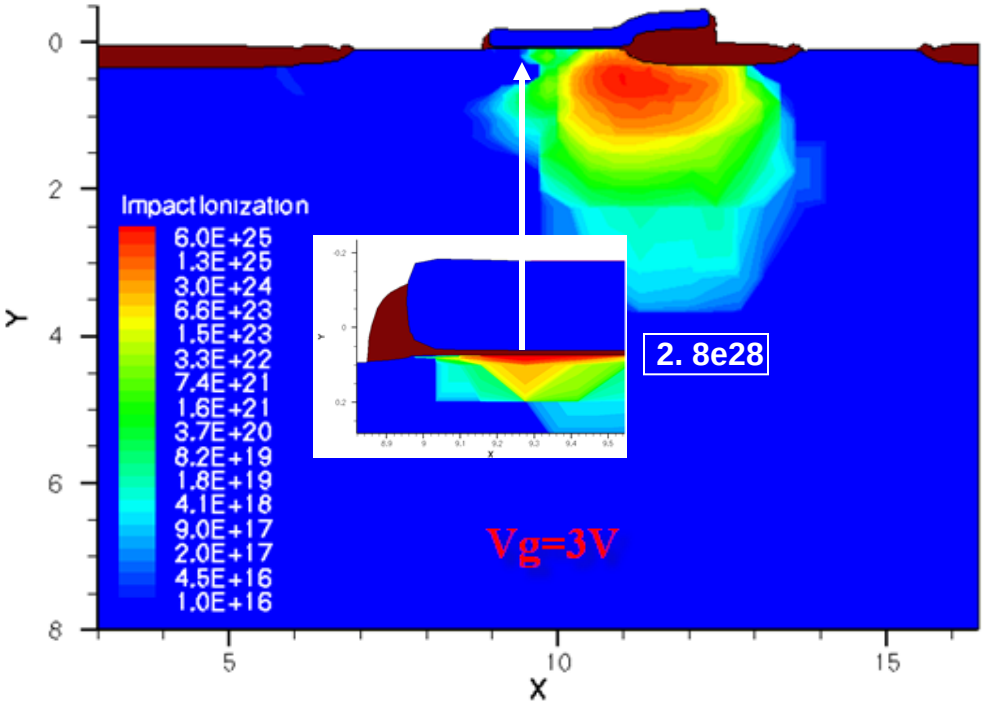
HCI Mechanism Investigation

Vgstr/Vdstr=3/44

doping profile



Impact Ionization Simulation

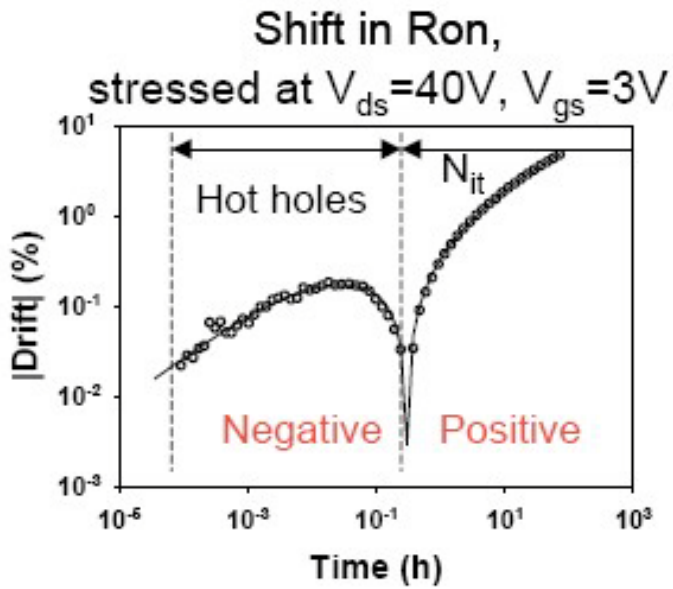


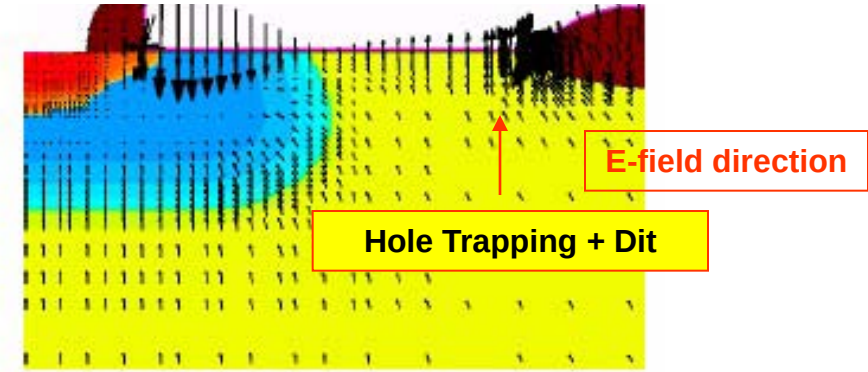
simulation provided by 8AB PEI

HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=3/44





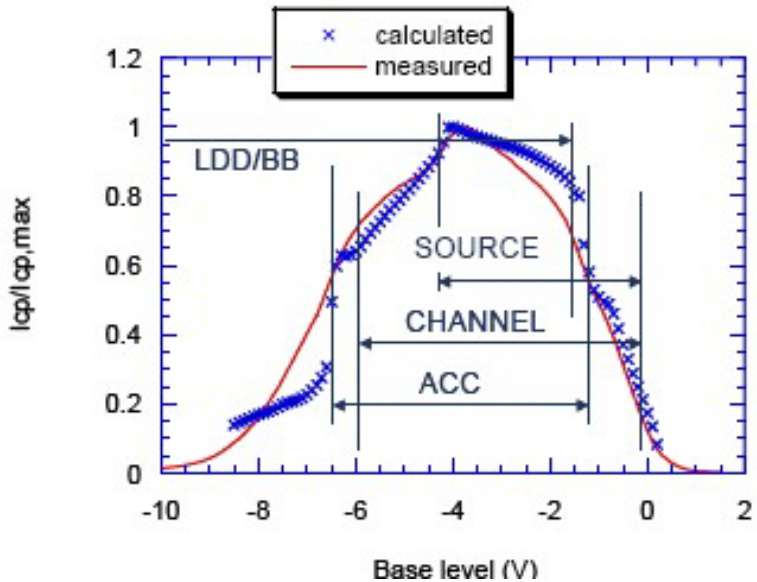
2005, IRPS

- At first stage, hole injection is dominate & its occur at bird-beak. (by electric field direction)
- As stress time increase, interface generation dominate.

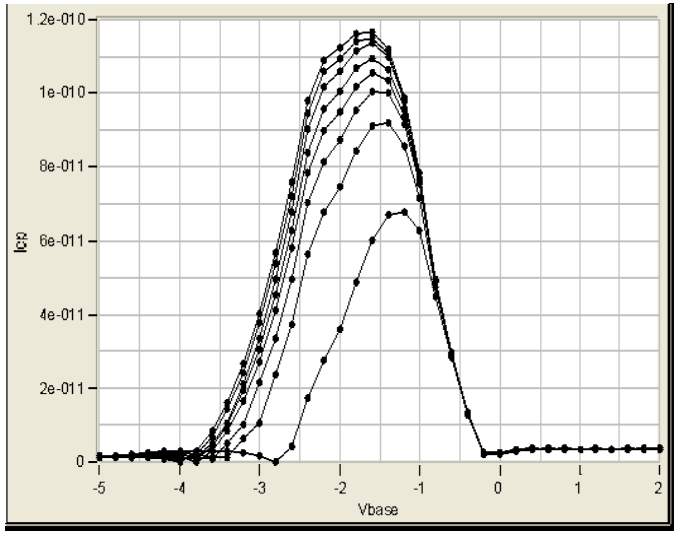
HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=3/44



charge-pumping plot of Vgstr/Vdstr=3V/44V

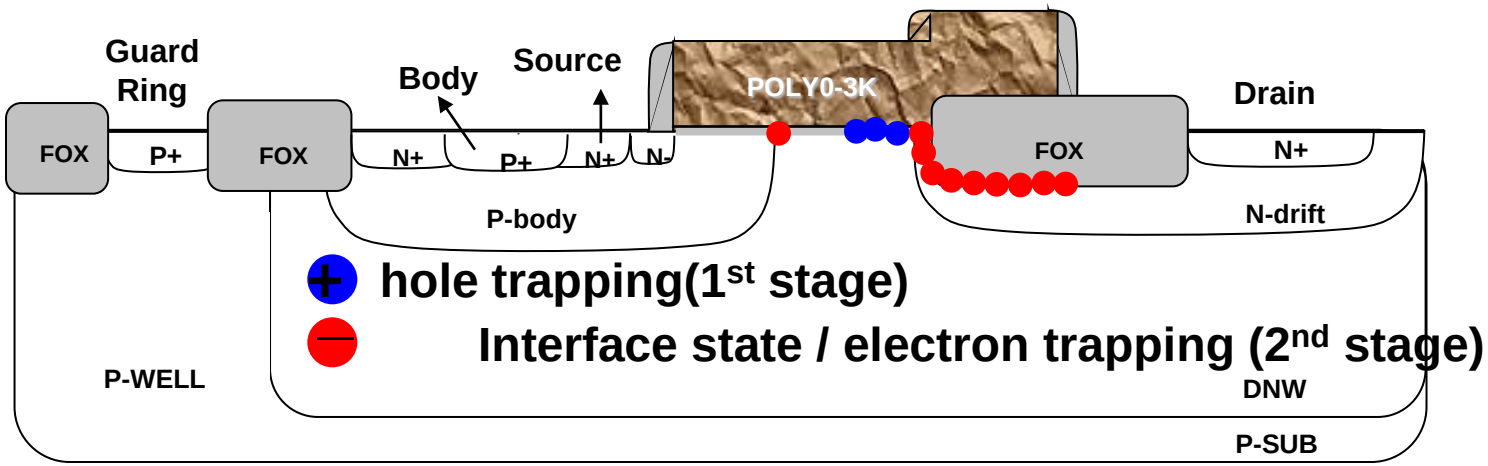


- **From charge-pumping plots, the major damage is Dit generation in accumulation region or bird beak region.**

HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=3/44



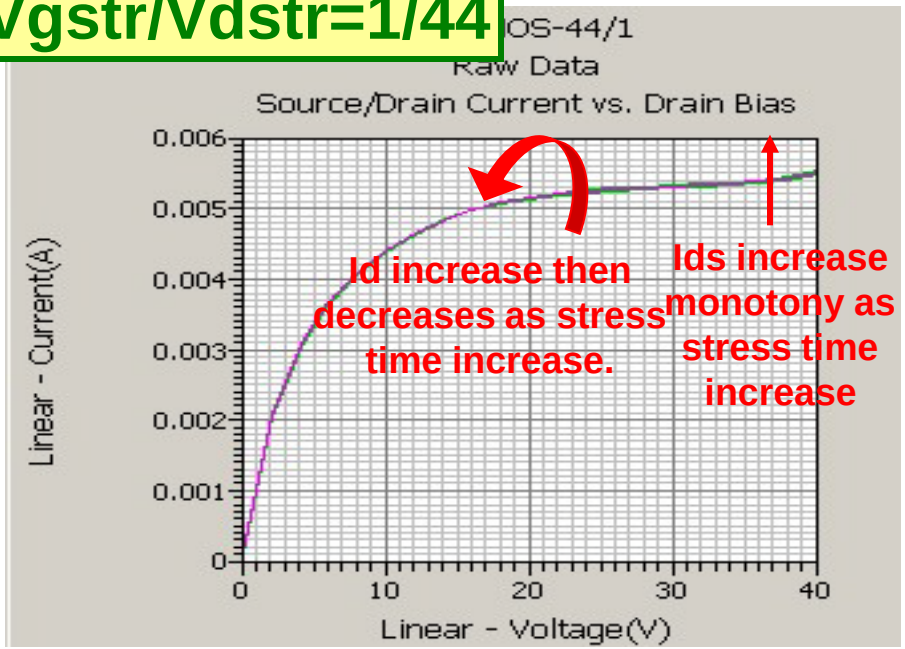
- Few interface state exist near channel region. (small Vth shift)
- Some hole trapping occur near accumulation/bird's beak region at 1st stage. (Ids increase)
- As stress time increase, Id become more degradation as monitor points approach to linear region. It means interface state appear around the bird's beak/FOX region.

HCI Mechanism Investigation

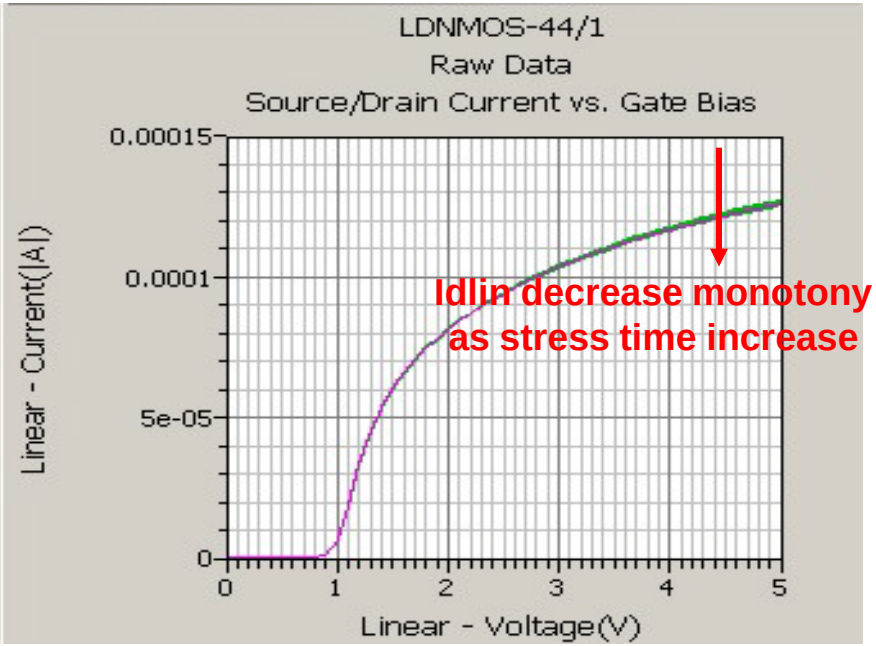
HCI Mechanism Investigation

HCI Damage Mechanism Investigation by Variation of IV Curve

Vgstr/Vdstr=1/44



IdVd



IdVg

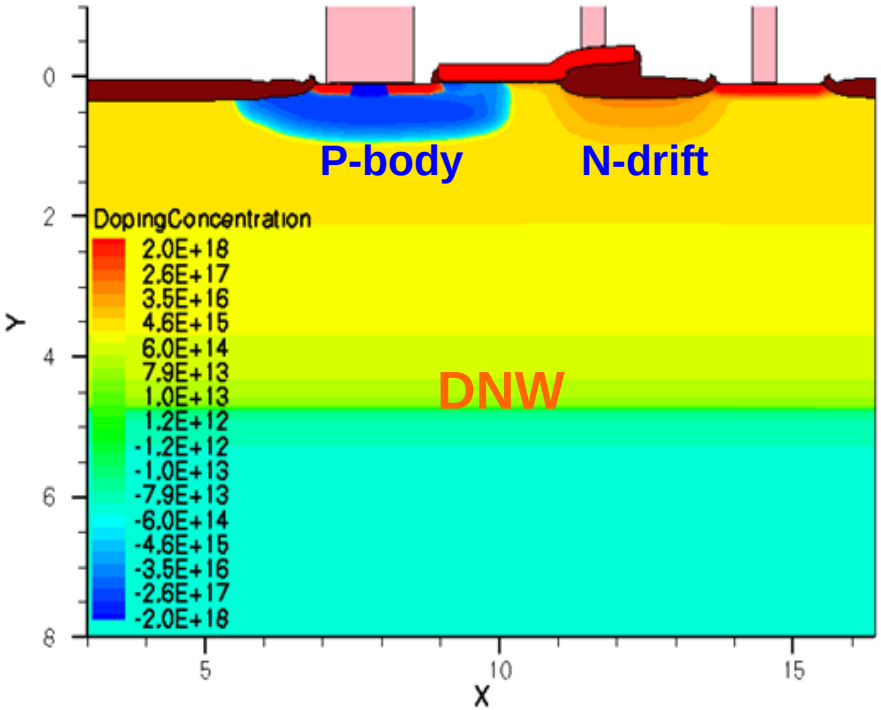
- **In IdVd curve, Ids increase monotonously as stress time increase (hole trapping). As Vd decrease (approach to linear region) at longer stress time, *Id tend to decrease* (interface state generation) and *degradation amount is less than stress@Vg/Vd=3/44*.**
- **In IdVg curve, Idlin decrease as stress time increase.**

HCI Mechanism Investigation

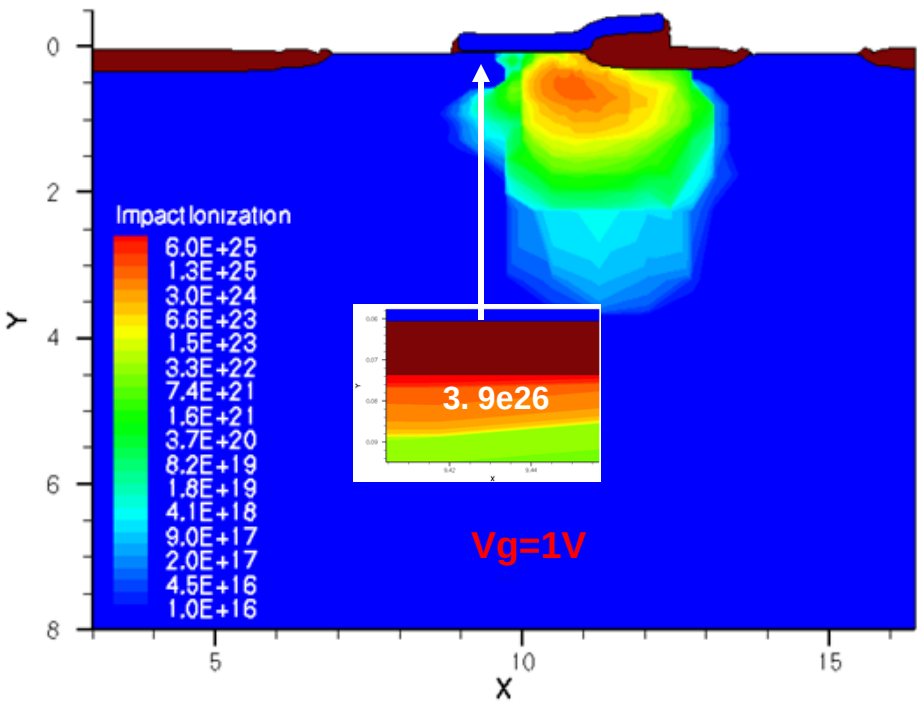
HCI Mechanism Investigation

Vgstr/Vdstr=1/44

doping profile



Impact Ionization Simulation

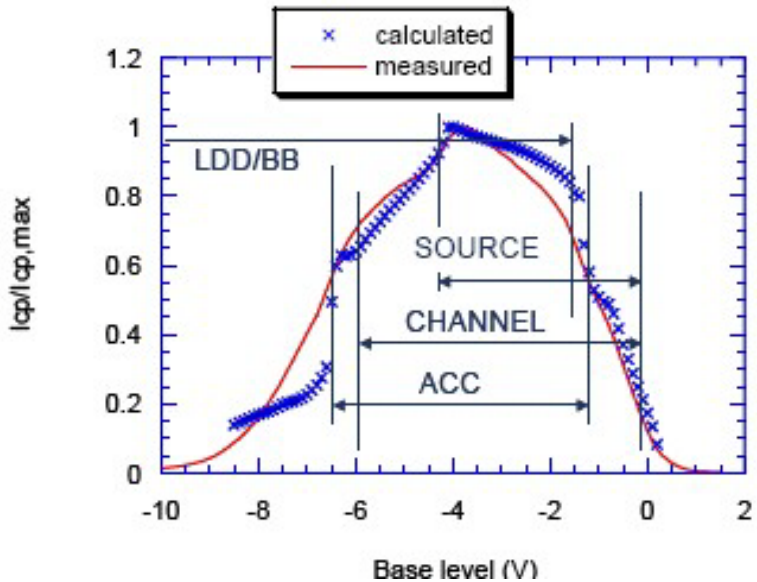


simulation provided by 8AB PEI

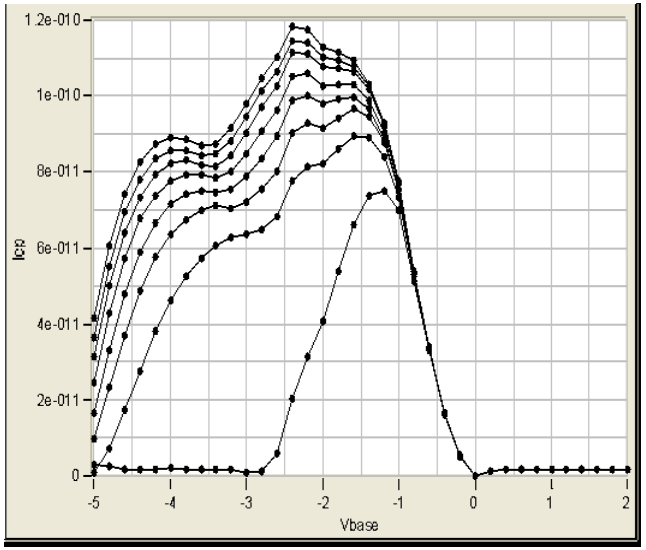
HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=1/44



charge-pumping plot of Vgstr/Vdstr=1V/44V

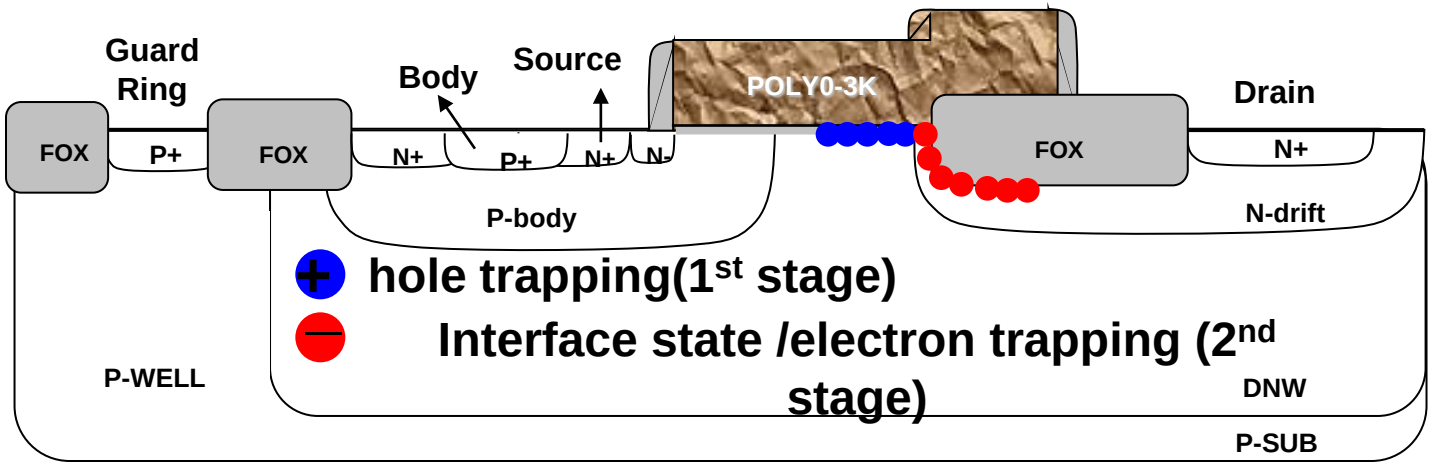


- **From charge-pumping plots, Dit generation is in accumulation region or bird beak region.**
- **Obvious left-shift of Icp curve also show the existence of hole trapping.**

HCI Mechanism Investigation

HCI Mechanism Investigation

Vgstr/Vdstr=1/44



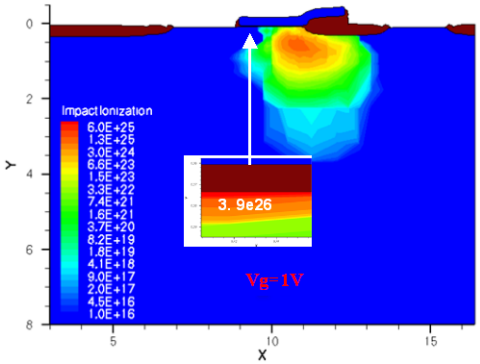
- **Hole trapping occur near accumulation/bird's beak region at 1st stage and *the hole trapping* amount is *larger* than stress @Vgstr/Vdstr=3/44. (larger vertical field @ @Vgstr/Vdstr=1/44)**

- **Approach to linear region, Id tend to more degradation. It means interface state appear around the bird's beak /FOX region and *the interface state* amount is *less* than stress@Vgstr/Vdstr=3/44.**

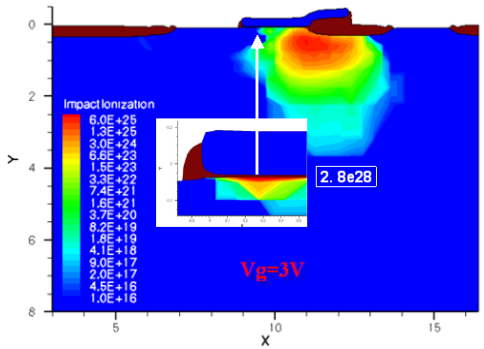
Experimental Results and Discussion

40V LDNMOS

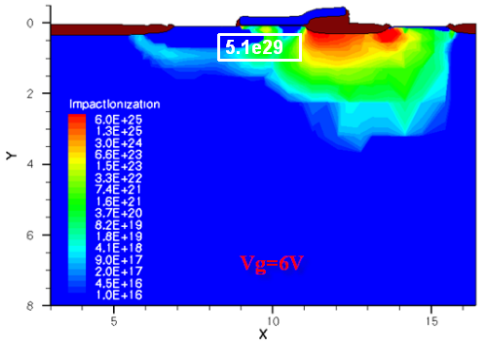
Impact Ionization Simulation



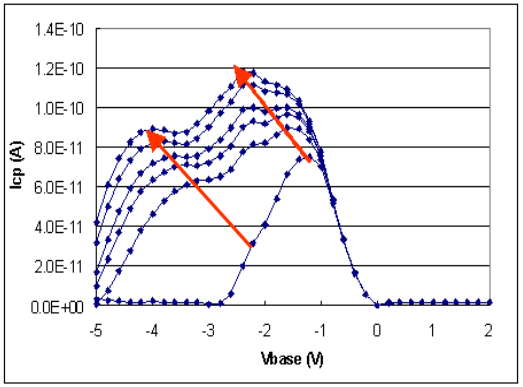
Impact Ionization Simulation

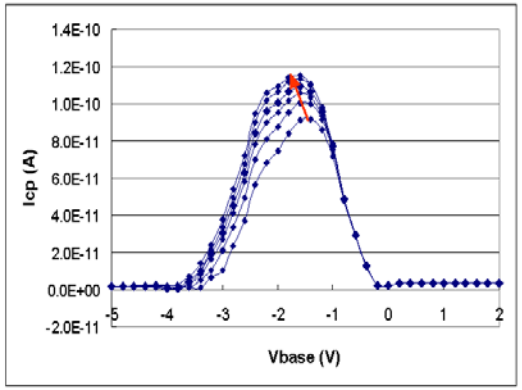


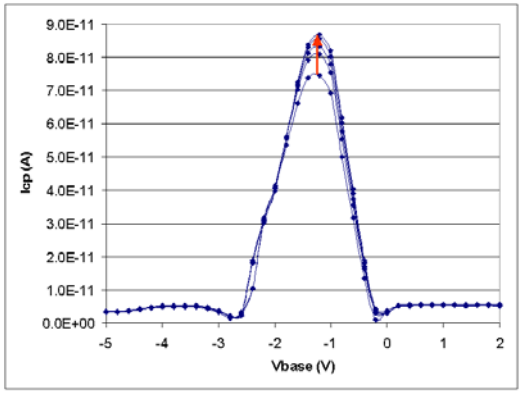
Impact Ionization Simulation



$$I_{cp} = qfAN_{it}$$

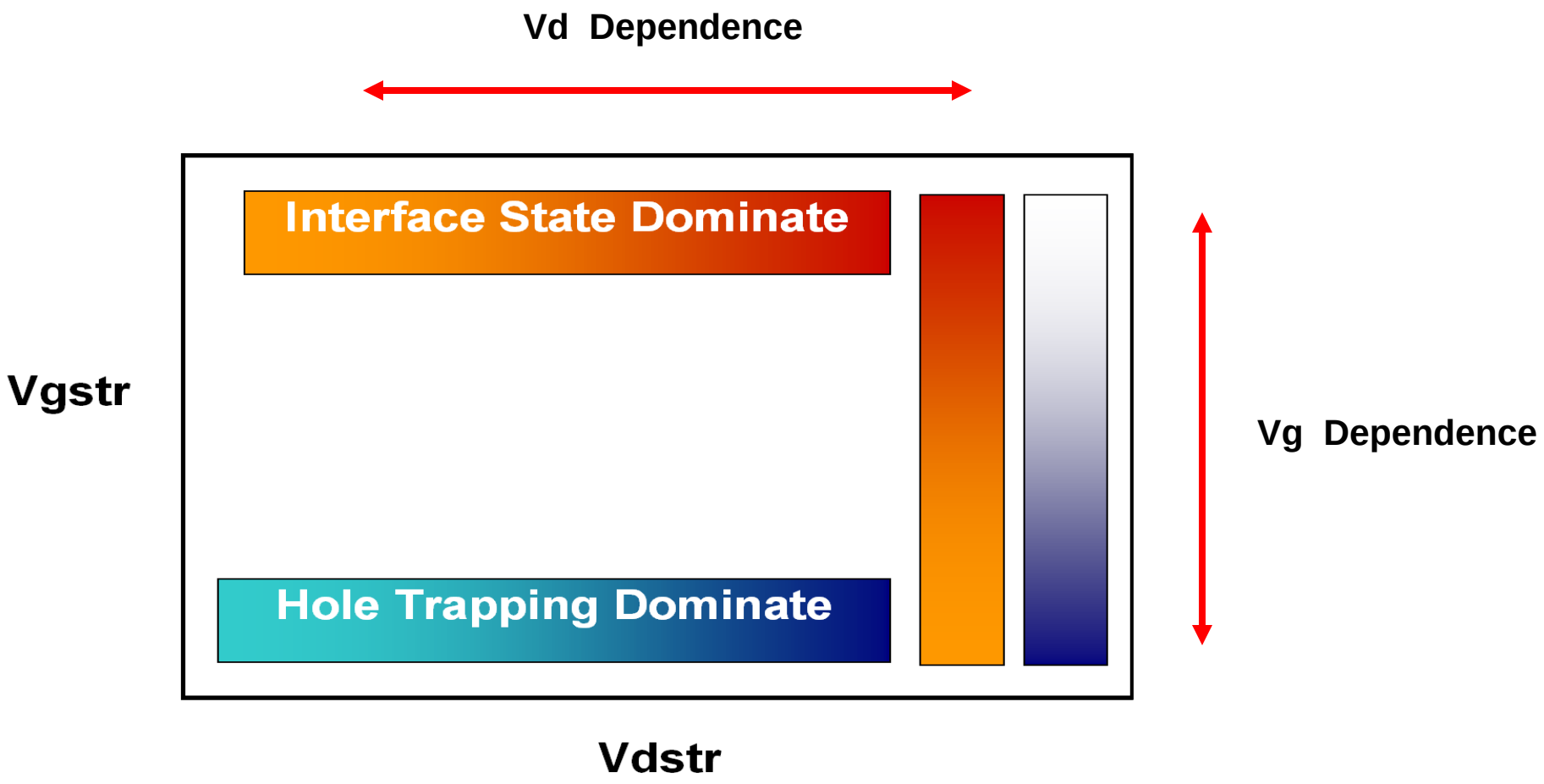






HCI Mechanism Investigation

Summary of LDNMOS HCI Damage Mechanism



Paper Reference

(1). P.Hower, S Pendharjar, “ Short and long-term safe operation area considerations in LDMOS transistor”, IEEE, IPRS, 2005, p545

(2). P. Mones, G,V, den bosh, “Hot hole degradation effects in lateral in nDMOS transistors”, IEEE trans. ED,vol.51, 2004,p1704

(3). D. Brishin, A. Strachan,”Design optimization of N-LDMOS transistor arrays for hit carrier lifetime enhancement” , IEEE, IRPS, 2003

(4). P. Hower,” Safe operating area – a new frontier in LDMOS design”, Proc. ISPSD’02, p1-8

(5). D Brisbin, P. Lindorfer,”Substrate current independent hot carrier degradation in LDMOS device”, IEEE, IRPS,2006, p329

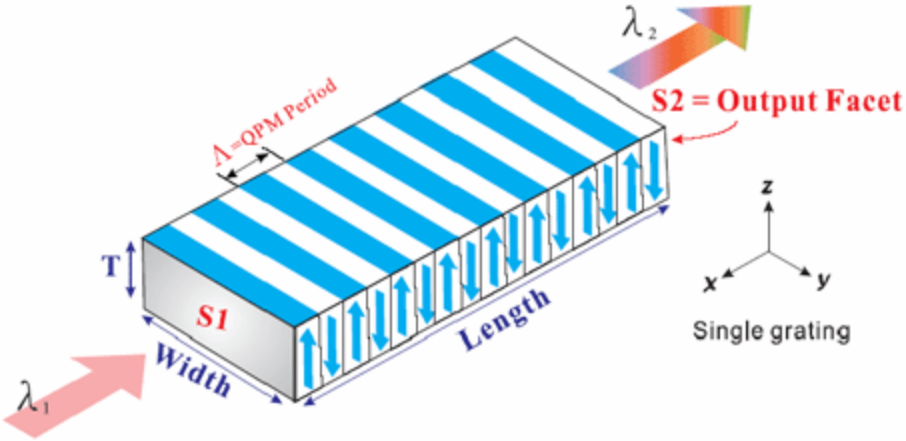
(6). P. Moens, M. Tack, R. Degraeve,” A novel hot-hole injection degradation model for lateral nDMOS transistors”, IEDM, 2001, p877

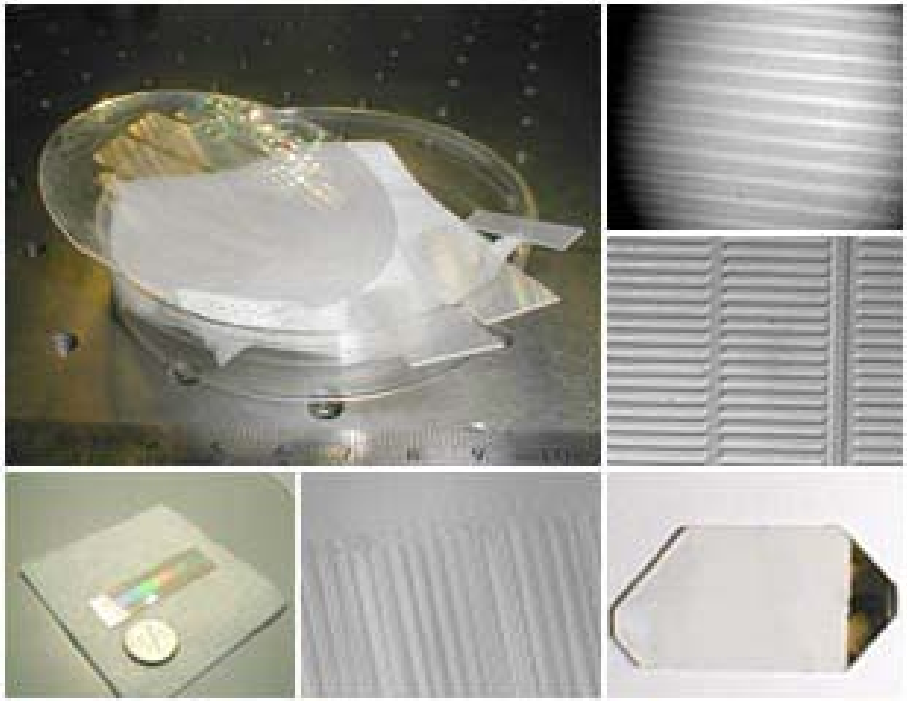
(7). P. Moens, “Reliability challenges in integrated high voltage device”, IEEE IRPS Tutorial, 2006

Class 100 @ NTHU

Class 10 @ NTHU

LiNbO3 device





Questions & Answers

Thanks very much for the attention!