MRI compatible G-Link and PCI based data acquisition hardware for the RatCAP scanner

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Brookhaven National Laboratory and Université de Sherbrooke

Instrumentation Seminar
March 21, 2007

Overview

- Simultaneous PET-MR Application
- RatCAP Scanner
  - Front end ASIC
  - TDC and Signal Processing Module (TSPM)
  - PCI acquisition, control, read out and test system (PACRAT)
- Offline processing
- Results from simultaneous PET-MR
- Future work
- Conclusion

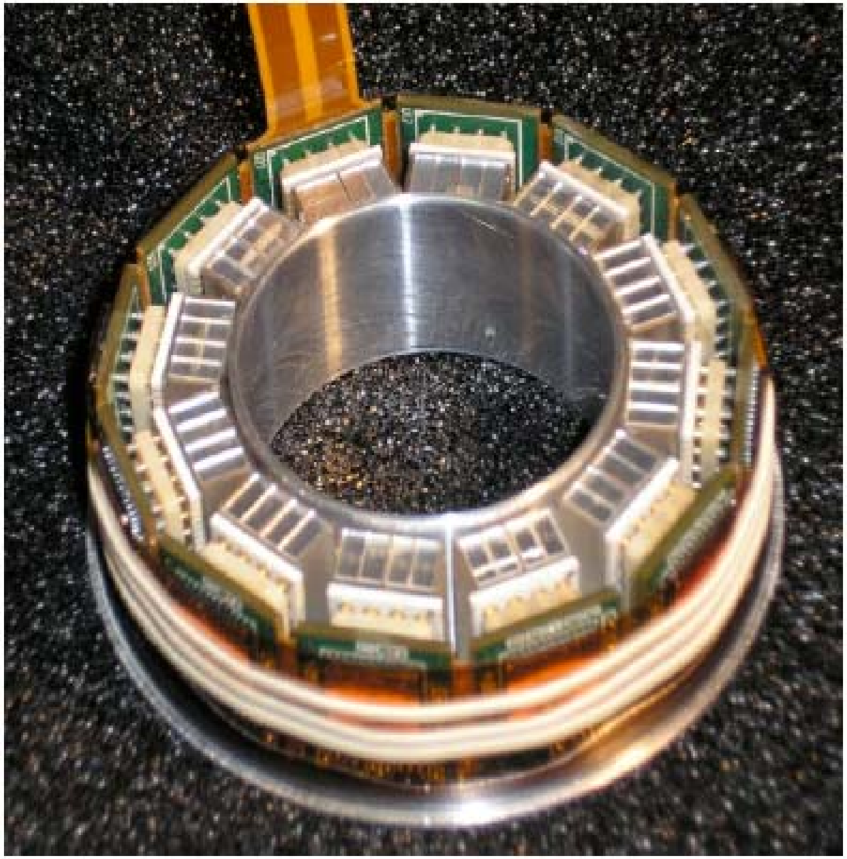
Simultaneous PET-MRI

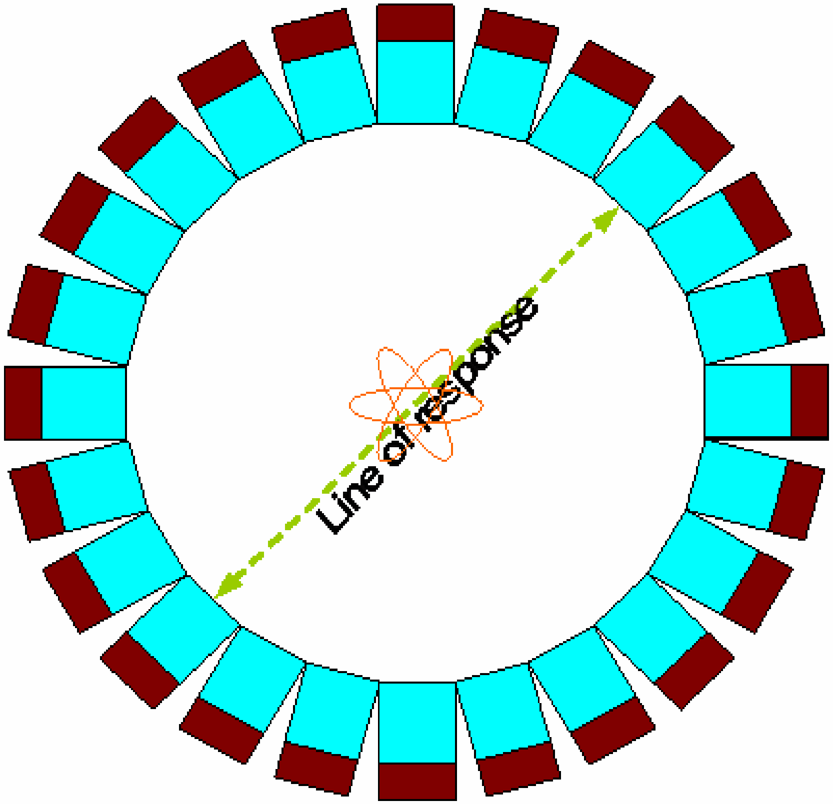
- MRI:
  - High resolution anatomical data
  - Soft tissue contrast
  - No ionizing radiation dose (as opposed to CT)
- PET:
  - *in-vivo* quantitative functional and physiological information
  - Limited spatial resolution
  - No anatomical information
  - High sensitivity and high specificity information
- Simultaneous PET-MR
  - Perfectly co-registered PET and MR images
  - Correlation of two imaging modalities
  - Monitoring rapidly evolving processes in medicine and physical science
  - Leads to improved resolution, sensitivity and ability to diagnose disease

Historical show stoppers

- High magnetic field limits the use of PMTs in PET scanners
- Susceptibility artifacts in MR due to magnetic materials in PET detector system
- MRI-RF induced interference in PET detector and electronics
- PET data acquisition digital activity induced artifacts in MRI
- Large size and power consumption of PET electronics
- Remoteness of data acquisition computer

RatCAP System





RatCAP System

Detectors : Hamamatsu 4 × 8 APD arrays (S8550) coupled to lutetium oxyorthosilicate (LSO) scintillators of 2 × 2 × 5 mm3 in size

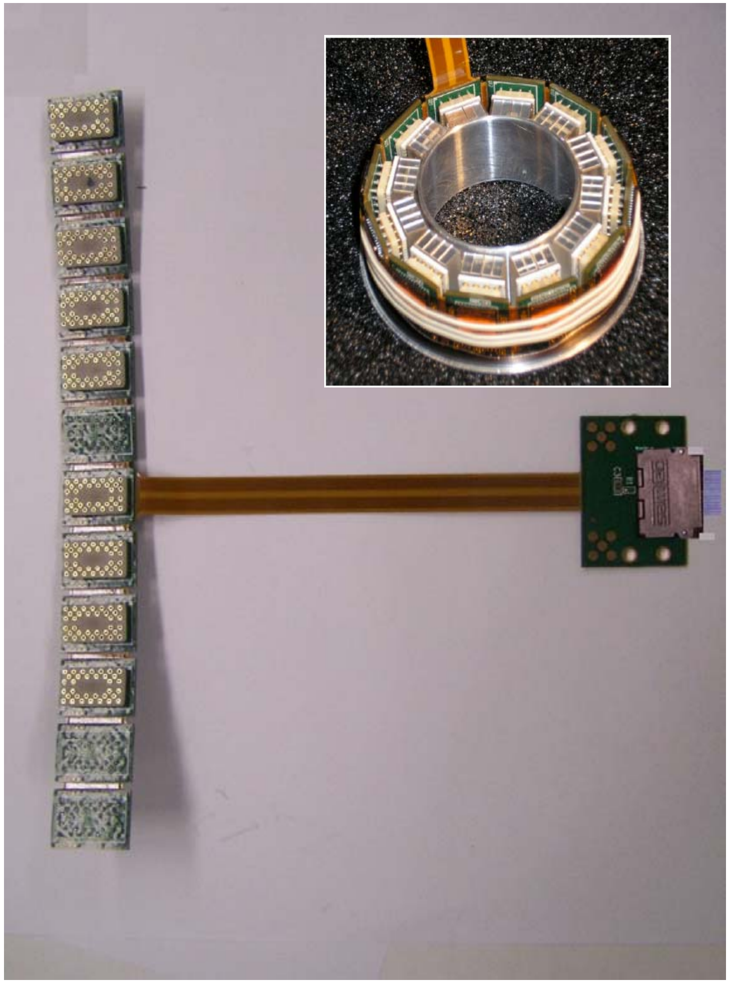
32 channel custom front-end Application-Specific Integrated Circuit (ASIC) realized in a CMOS 0.18 μm technology

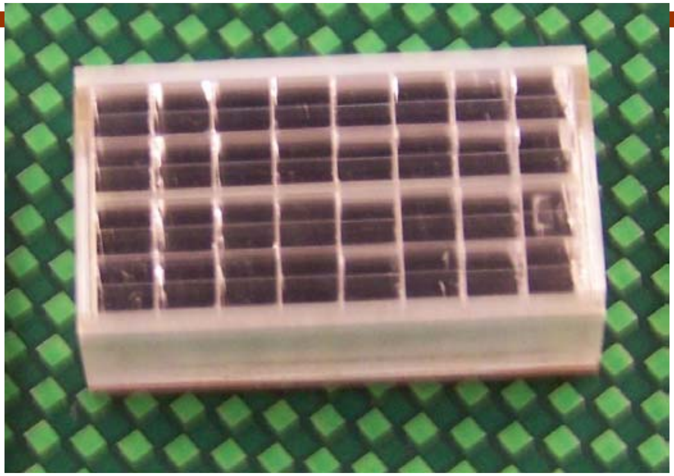
12 detector blocks with 32 channels each

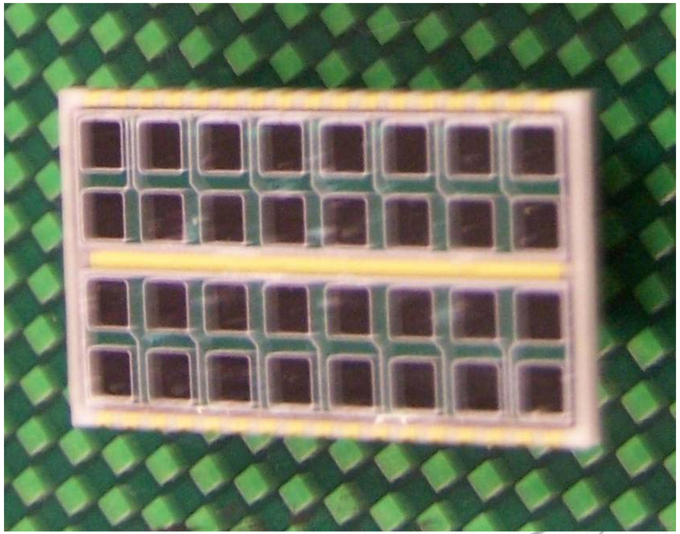
384 detector channels

One ASIC output per 32 channels

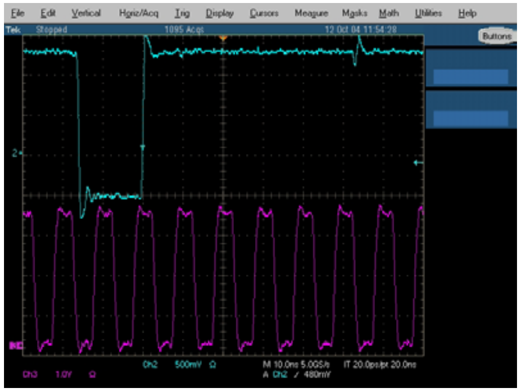
Rigid Flex PCB, LSO and APD detectors

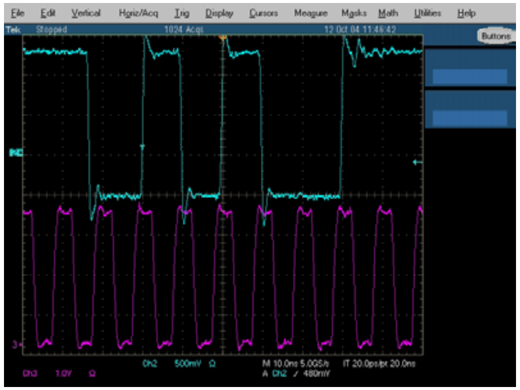


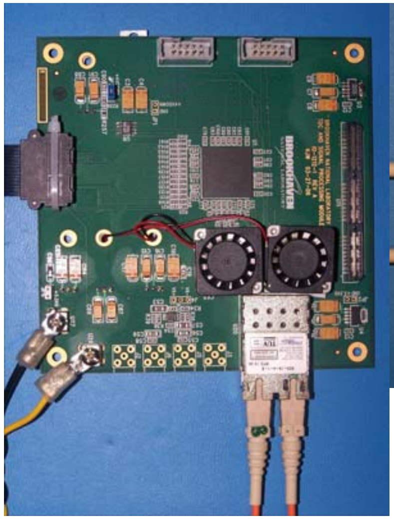




Signal Chain







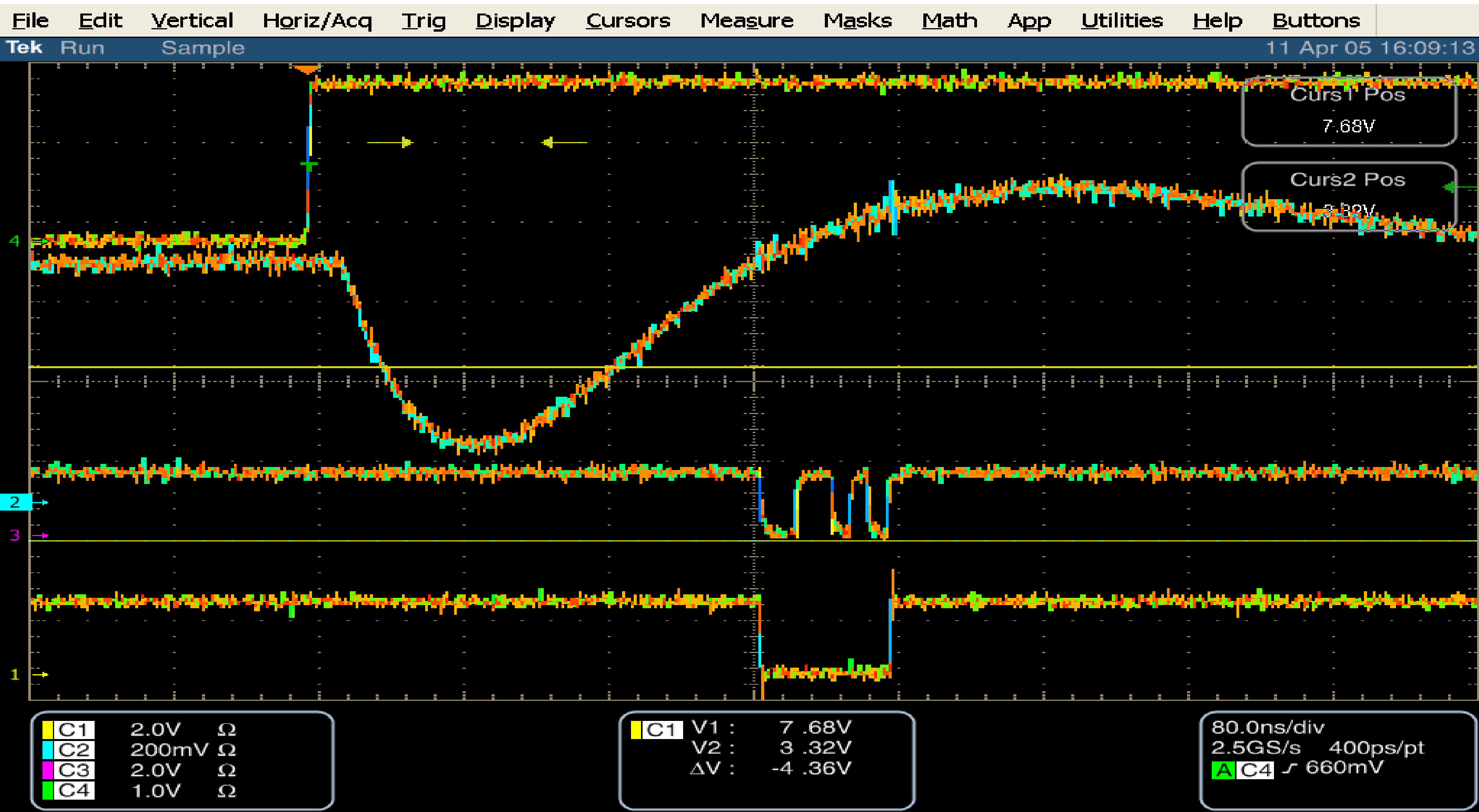
Non-magnetic RatCAP detector

- RatCAP PCB designed using Nickel less Rigid-Flex technology (Organic Solder Preservative-OSP) and components carefully chosen to have no or negligible susceptibility artifacts
- APDs nickel less pins (special pins)
- Nickel less APD sockets
- Minimum effects of small traces of Nickel in the BGA pins, component leads etc

RatCAP ASIC

- The mixed-signal front-end ASIC is composed of 32 channels of Charges Sensitive Preamplifier (CSP)
- 3rd order bipolar gaussian shaper and zero-crossing discriminator used to pick up the timing information of every event.
- 32 to 1 priority encoder
- 5 to 1 digital serial encoder to transmit 5 bit address
- TSMC 0.18 μm technology

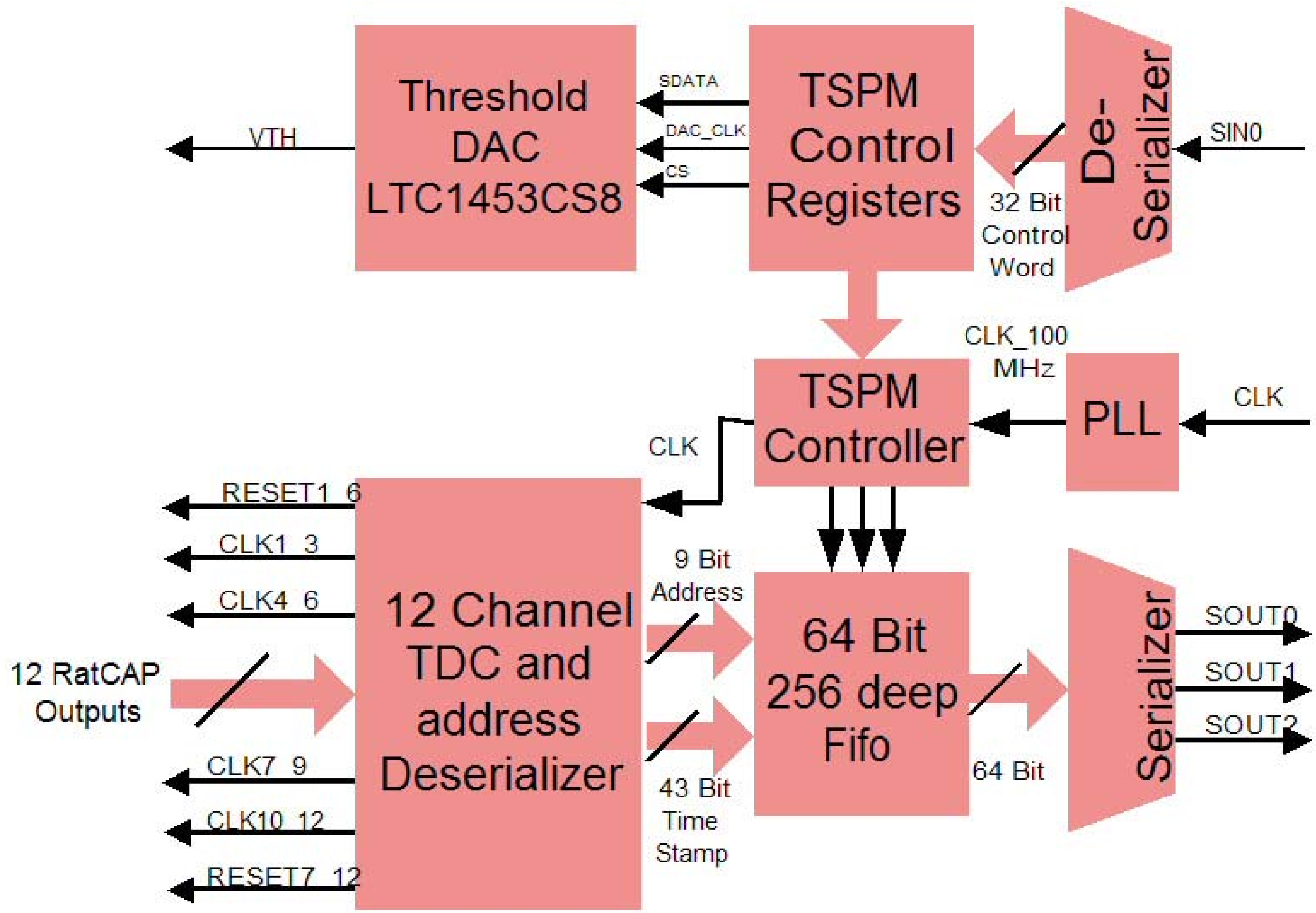
ASIC Output


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math App Utilities Help Buttons
Tek Run Sample
11 Apr 05 16:09:13
Curs1 Pos
7.68V
Curs2 Pos
4
2
3
1
C1 2.0V Ω
C2 200mV Ω
C3 2.0V Ω
C4 1.0V Ω
C1 V1 : 7.68V
V2 : 3.32V
ΔV : -4.36V
80.0ns/div
2.5GS/s 400ps/pt
A C4 660mV

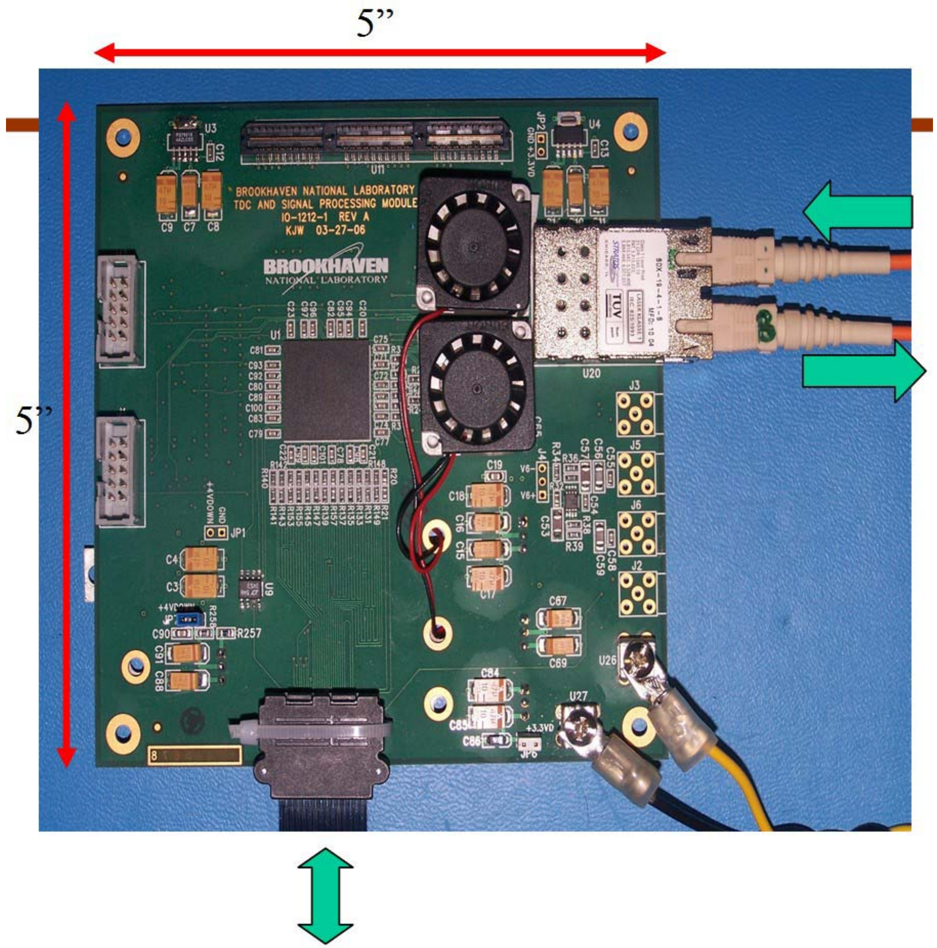
Time to Digital Converter and Signal Processing Module

- Time to Digital Converter (TDC) and Signal Processing Module-2 (TSPM-2) is based on Altera Cyclone FPGA (EP1C20F324), an Agilent HDMP-1022/1024 G-Link and SDX-19-4-1-S optical transceivers. All components tested for MRI compatibility
- Function: 13 channel time to digital converter and address decoder to process front end ASIC outputs
- Transmit data to and receive control signals and clocks from PCI Automatic Calibration, Readout and Test over (PACRAT) G-Link interface

Time to Digital Converter and Signal Processing Module (TSPM)



TSPM

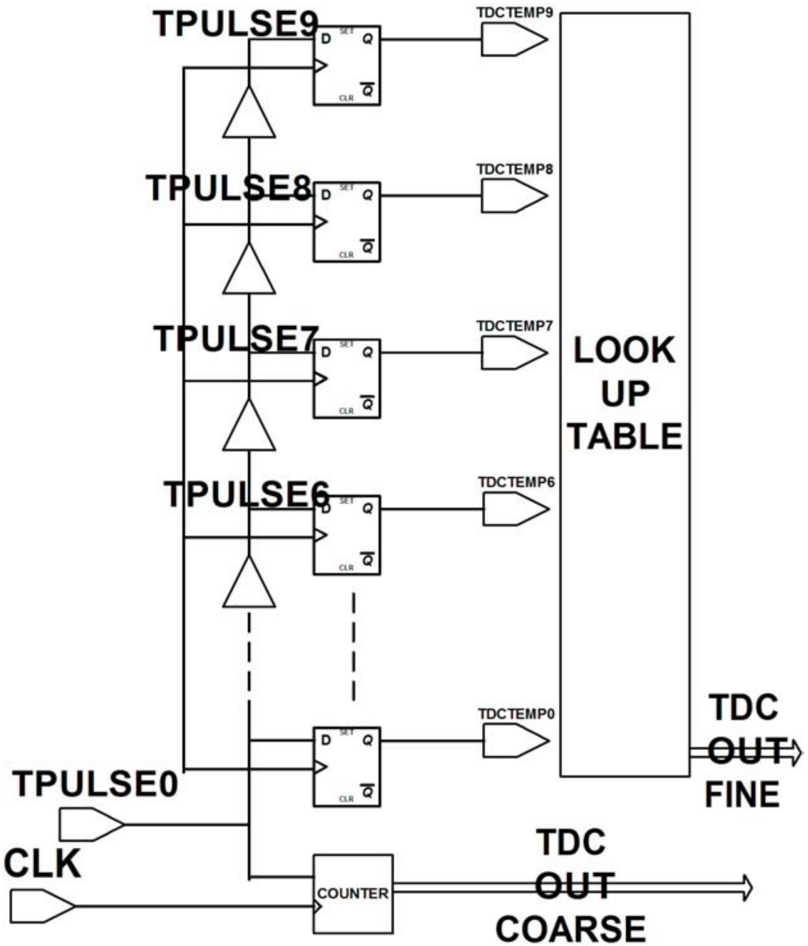


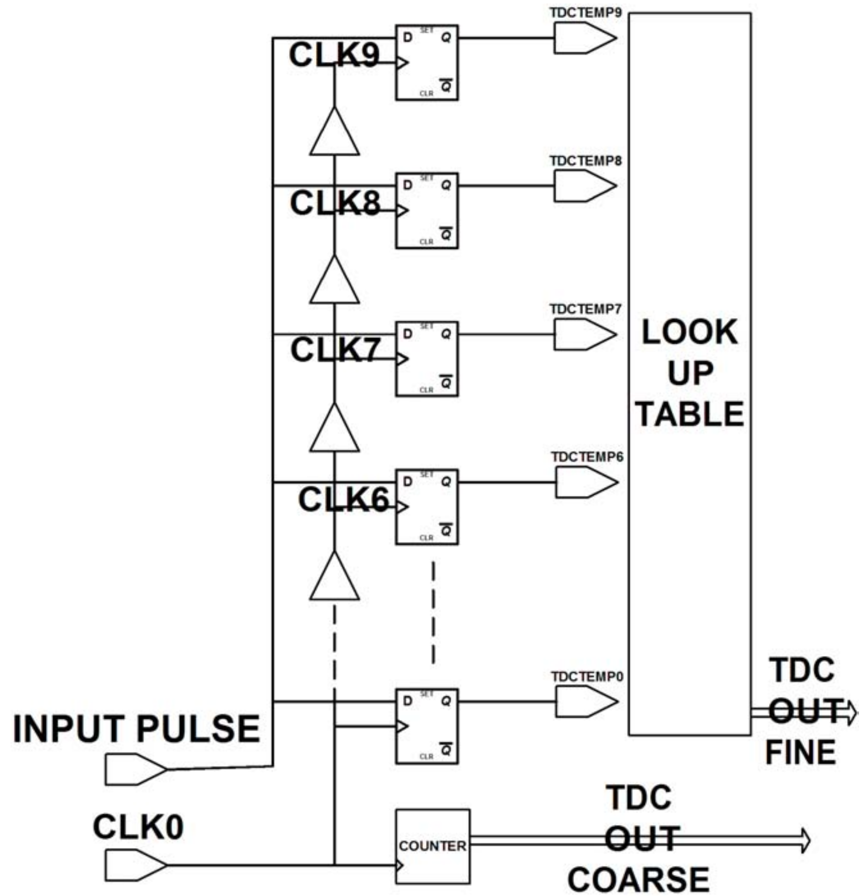
To and from RatCAP

TDC Introduction

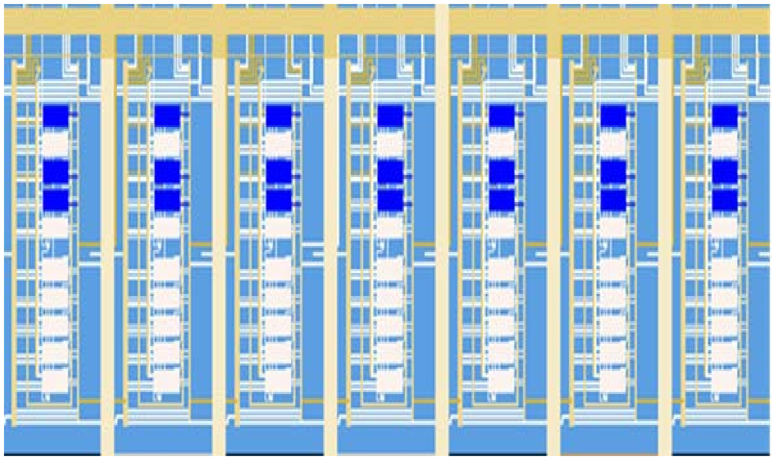
- Time-to-digital converters (TDCs) are used to record the time of occurrence of electrical pulse inputs
- TDCs can be realized using custom ASICs or FPGAs

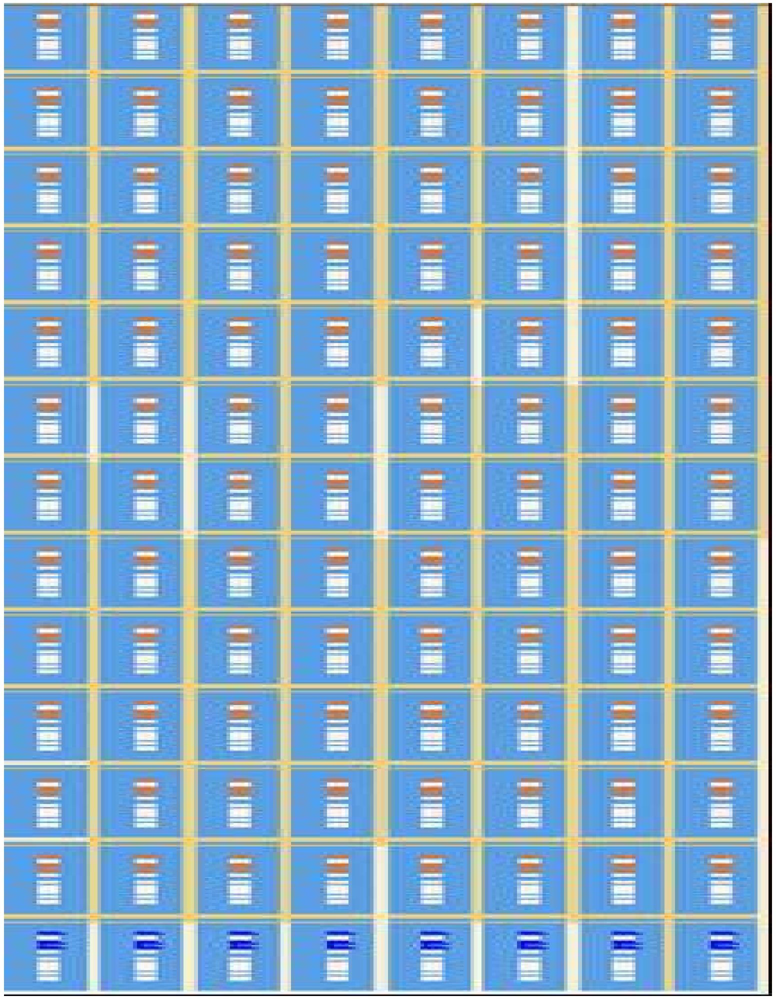
TDC Architectures





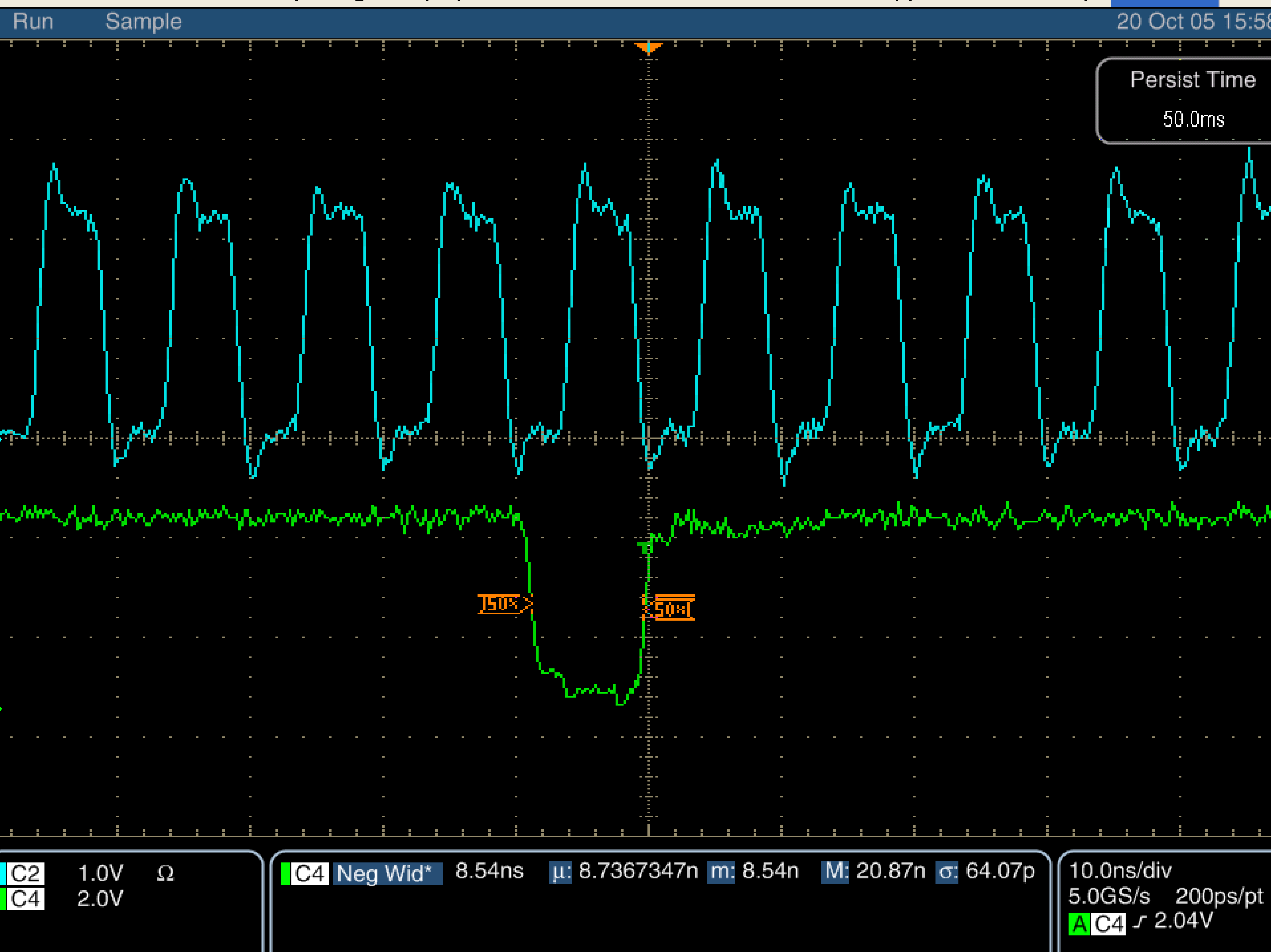
Placement for one TDC channel in chip editor view of Quartus-II



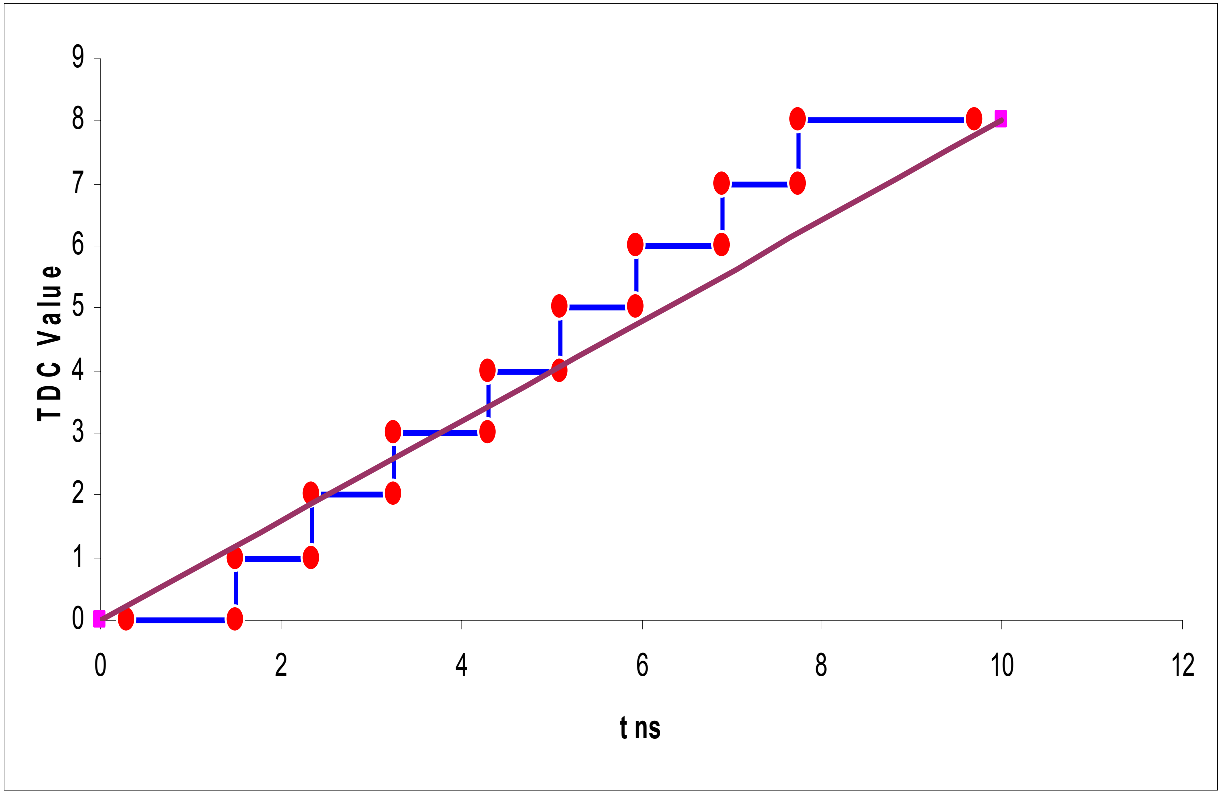


Test procedure

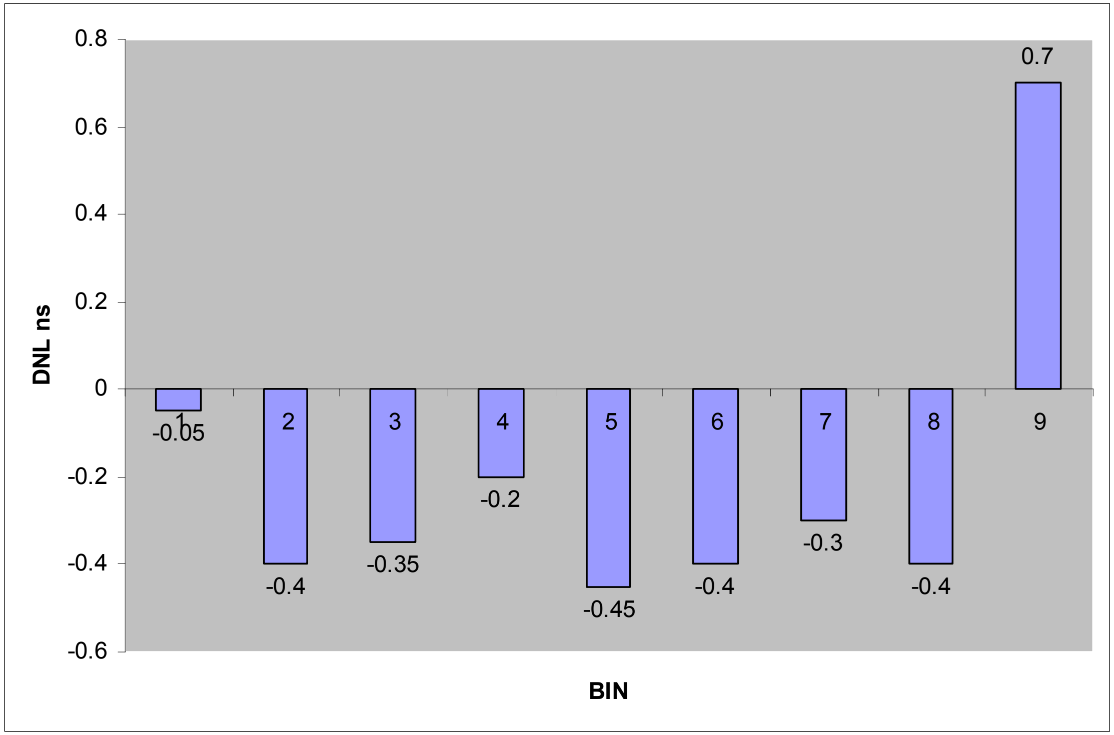
- Trigger the LeCroy pulse generator in the phase with 100 MHz RatCAP system clock
- Automatically delay the input pulse with respect to the clock in increments of 0.1 ns
- Acquire 10 TDC output samples per increment
- Acquire data for range of 0 ns to 25 ns in steps of 0.1 ns


Run
Sample
20 Oct 05 15:58
Persist Time
50.0ms
50%
50%
C2 1.0V Ω
C4 2.0V
C4 Neg Wid* 8.54ns µ: 8.7367347n m: 8.54n M: 20.87n σ: 64.07p
10.0ns/div
5.0GS/s 200ps/pt
A C4 2.04V

TDC Characteristics

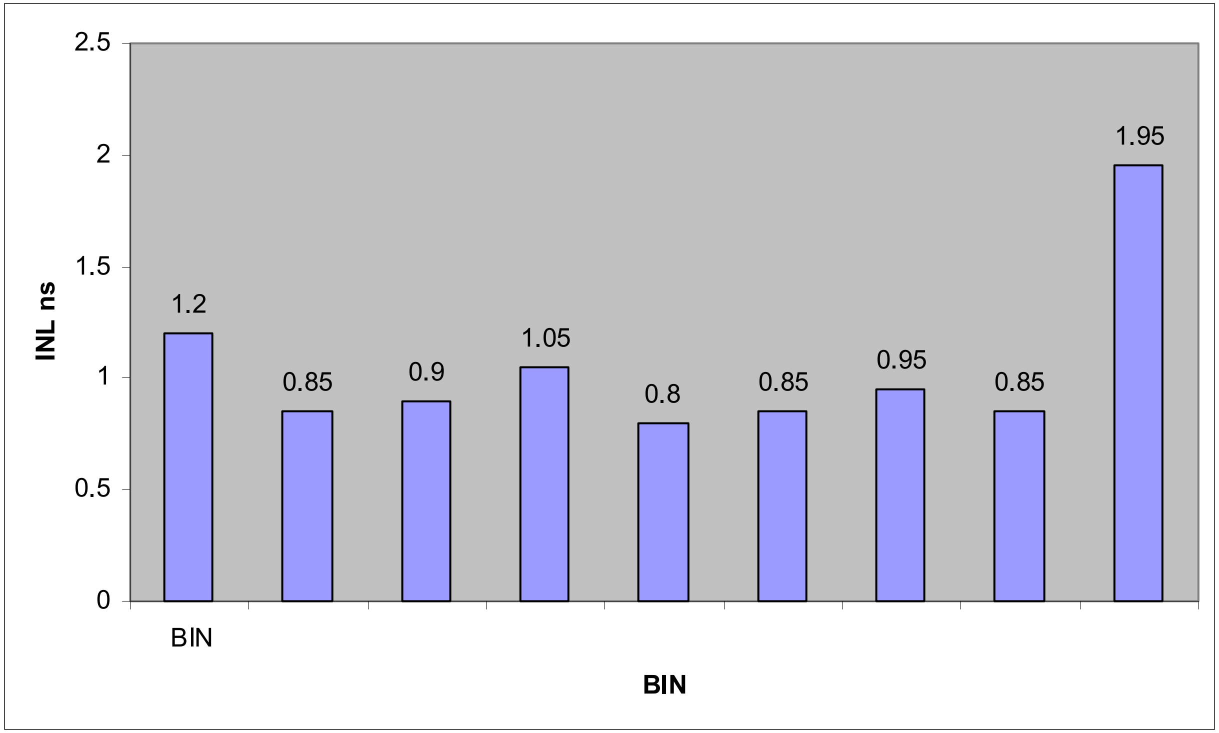


Differential Non-Linearity Error



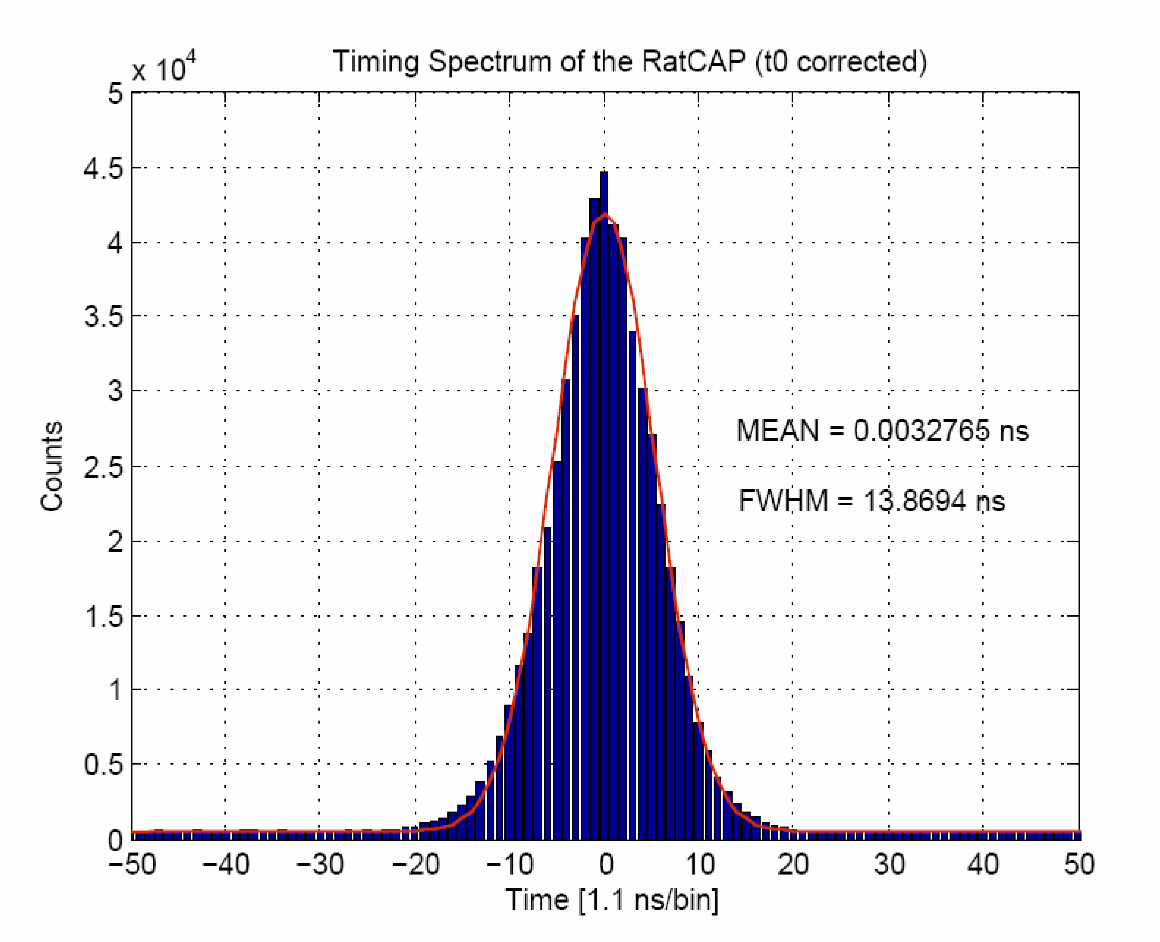
DNL=Real step size-Ideal Step size

Integral Non-Linearity Error



INL = Real transition point-Ideal Transition point

Coincidence timing spectrum for 384 RatCap Channels



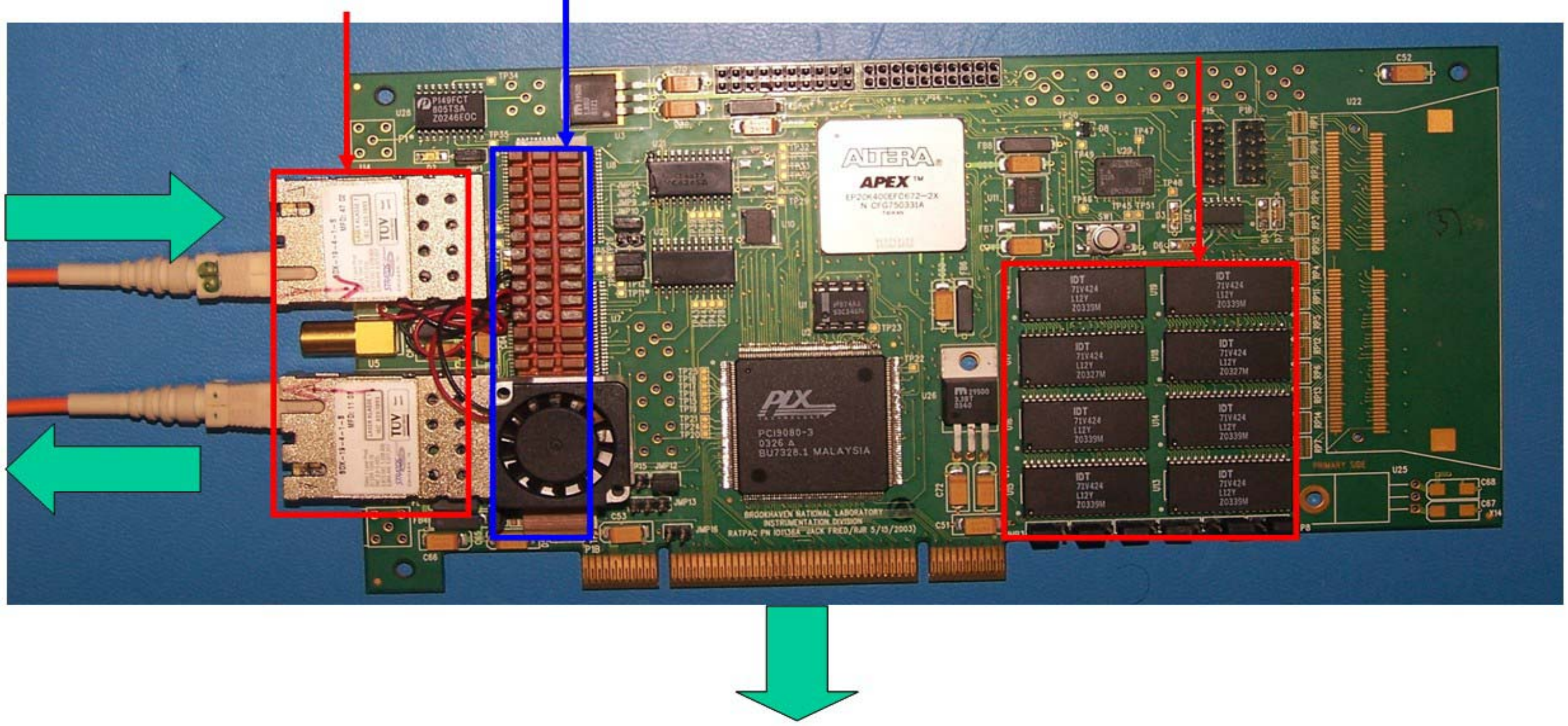
PACRAT

HDMP-1022/1024 Ser-Deser

Optical

Transceivers

Memory Banks



To Standard PCI Slot in a Windows/Linux PC

PACRAT

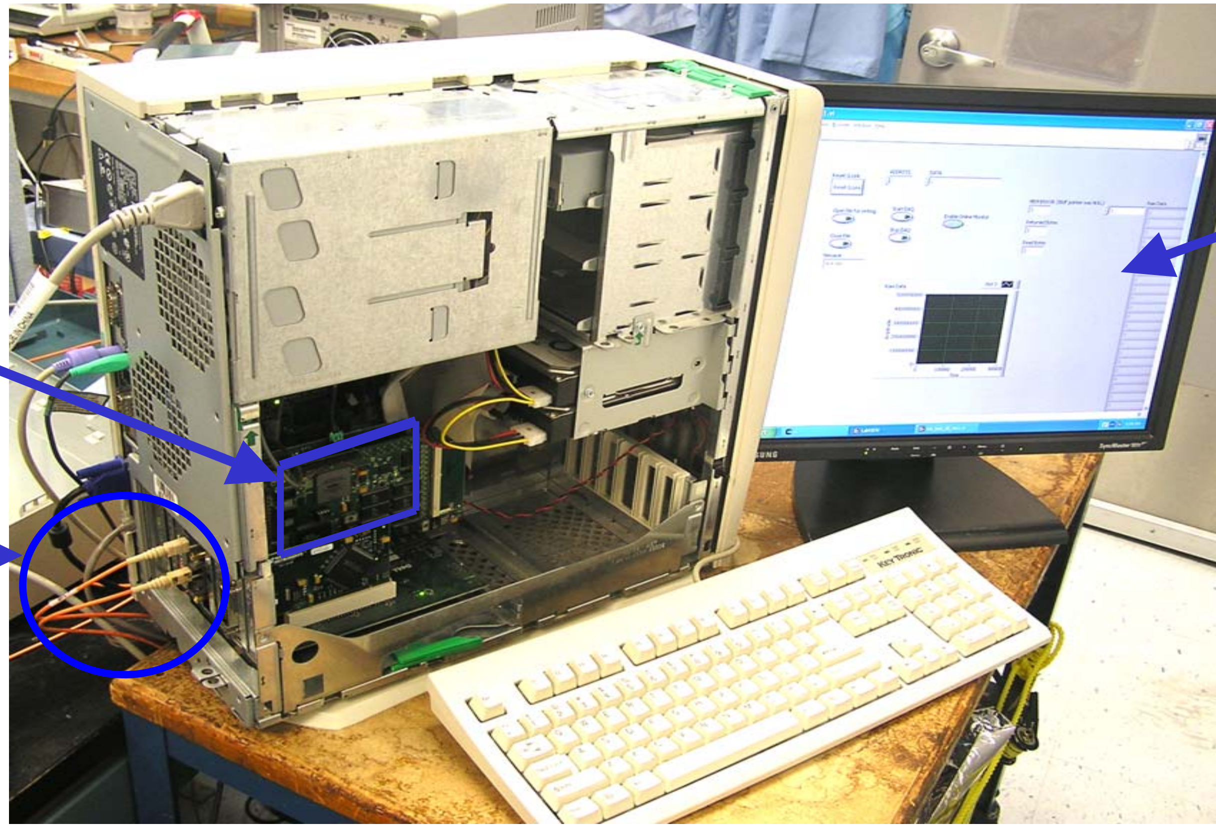
- PCI Version 2.1 compliant data acquisition and control PCB
- Supports PCI to and from local data transfers up to 70 MB/sec
- Two independent DMA channels with scatter-gather capability
- Supported by low level PCI drivers for MS Windows and Linux
- Two high speed 4 MB Static Random Access Memories (SRAM) banks
- HDMP-1024 Giga bit link (G-link) receivers and HDMP-1022 G-link Transmitter chipset for high speed data transfers

DAQ Computer

LabView GUI

PACRAT

Optical Fibers with SC type connectors



Windows PC running LabView Data Acquisition and Control software with PACRAT

Offline Processing

- LabView/Linux based data acquisition software
- List mode singles stored in ASCII format for further offline processing
- Offline correction for Individual detector channel offset delay variations caused by
  - Non-uniform gain distribution among channels
  - Differences in routing and propagation delays between blocks within a detector frame
  - Propagation delay differences within FPGA based TDC
  - Slight baseline variation from channel to channel

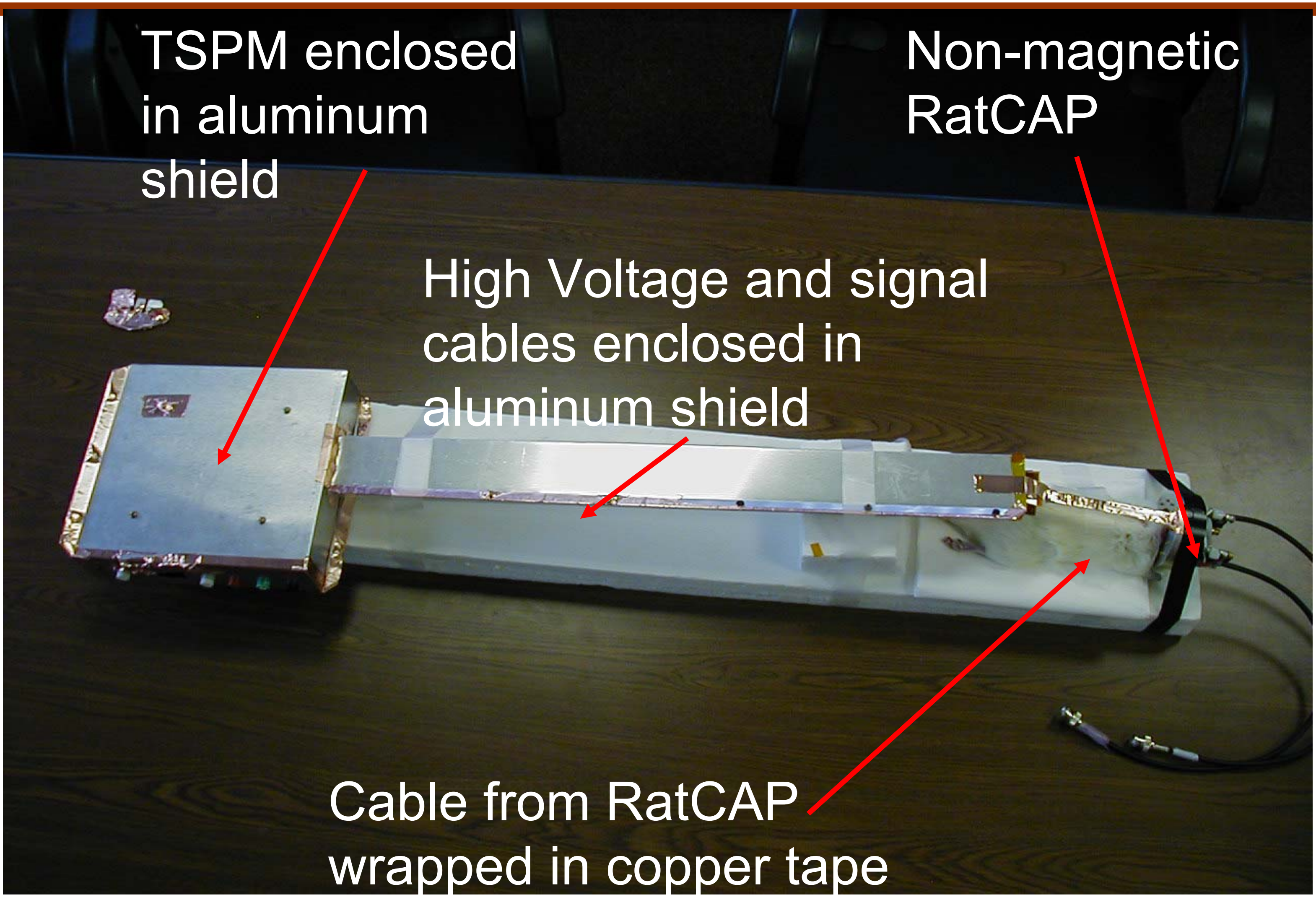
Offline Processing continued

- These t_0 shifts are estimated and subtracted from the singles timestamp using Singular Value Decomposition (SVD) method
- After the t_0 corrections are applied, data is further processed using offline coincidence processing algorithms and image is constructed with 3-D MLEM and with a highly accurate detector response model built using Monte Carlo simulation

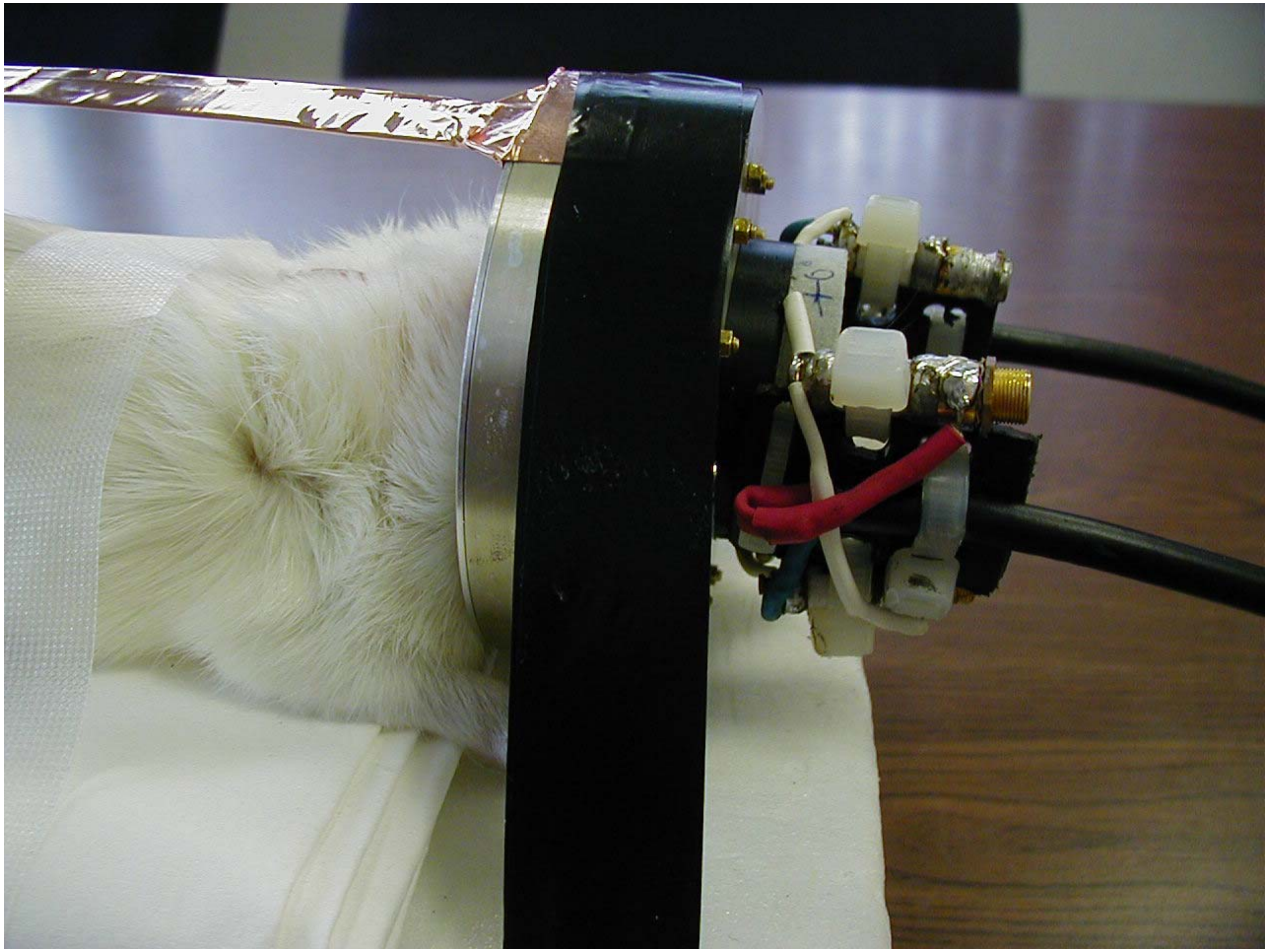
Preparing simultaneous PET-MRI

Present day showstoppers

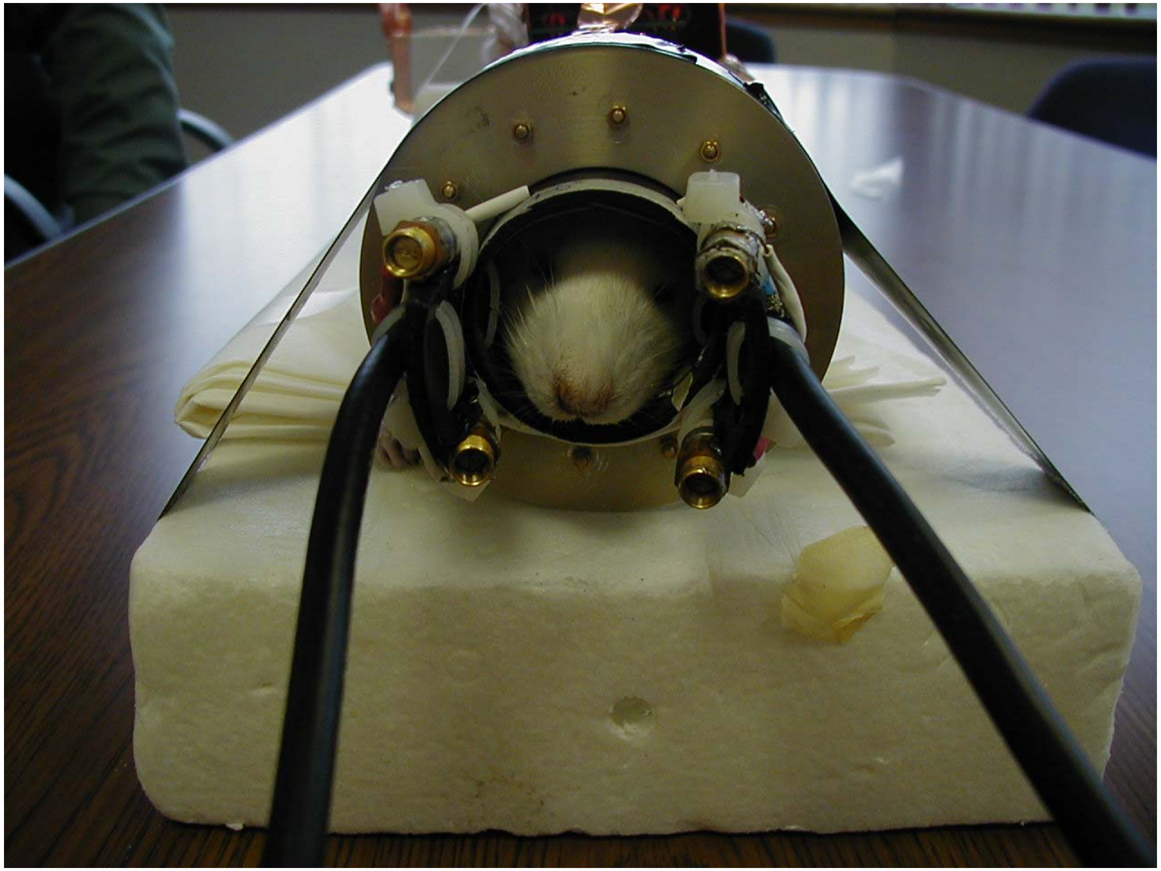
Simultaneous PET-MR ready RatCAP



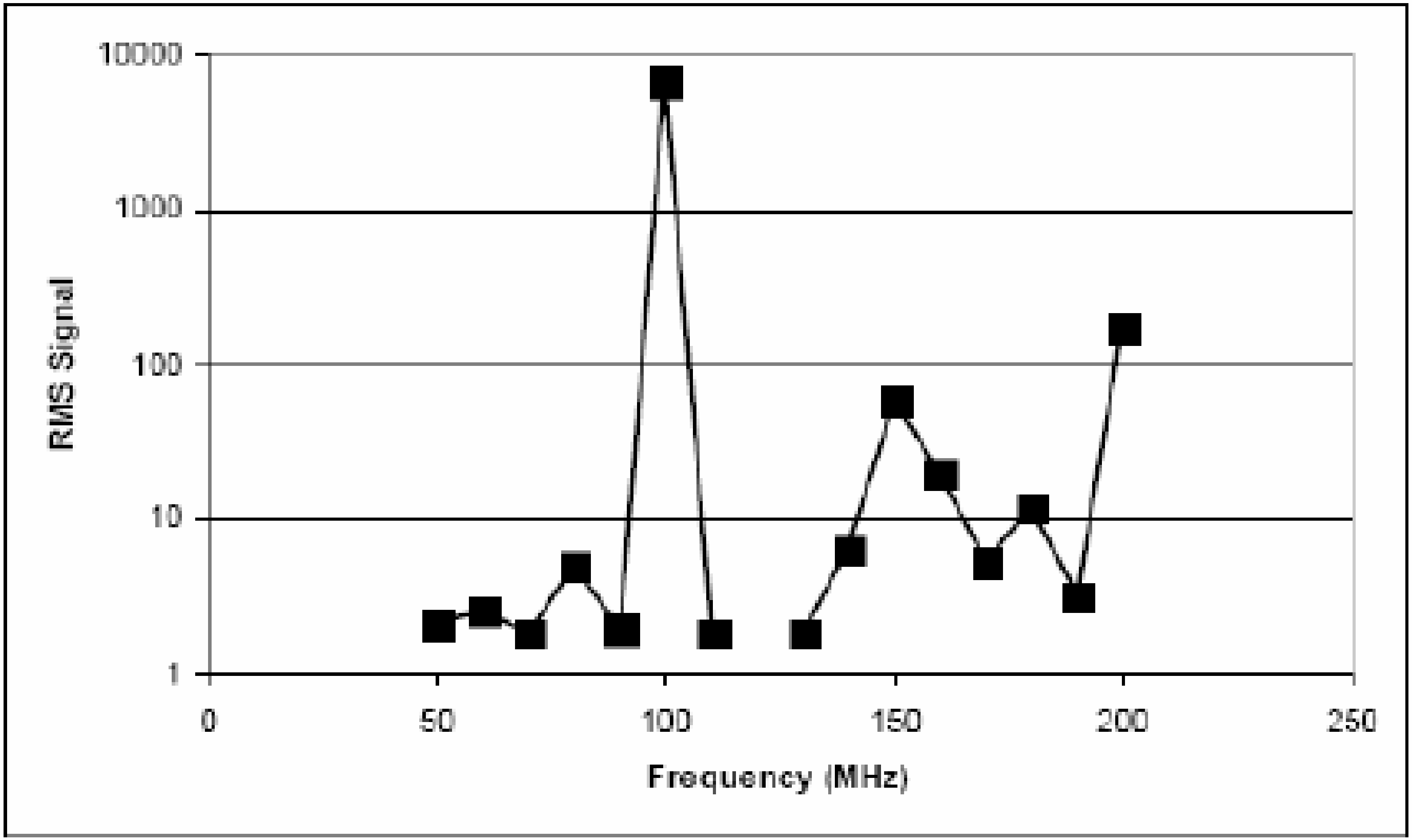
Side view of the rat in the RatCAP with RF Coil



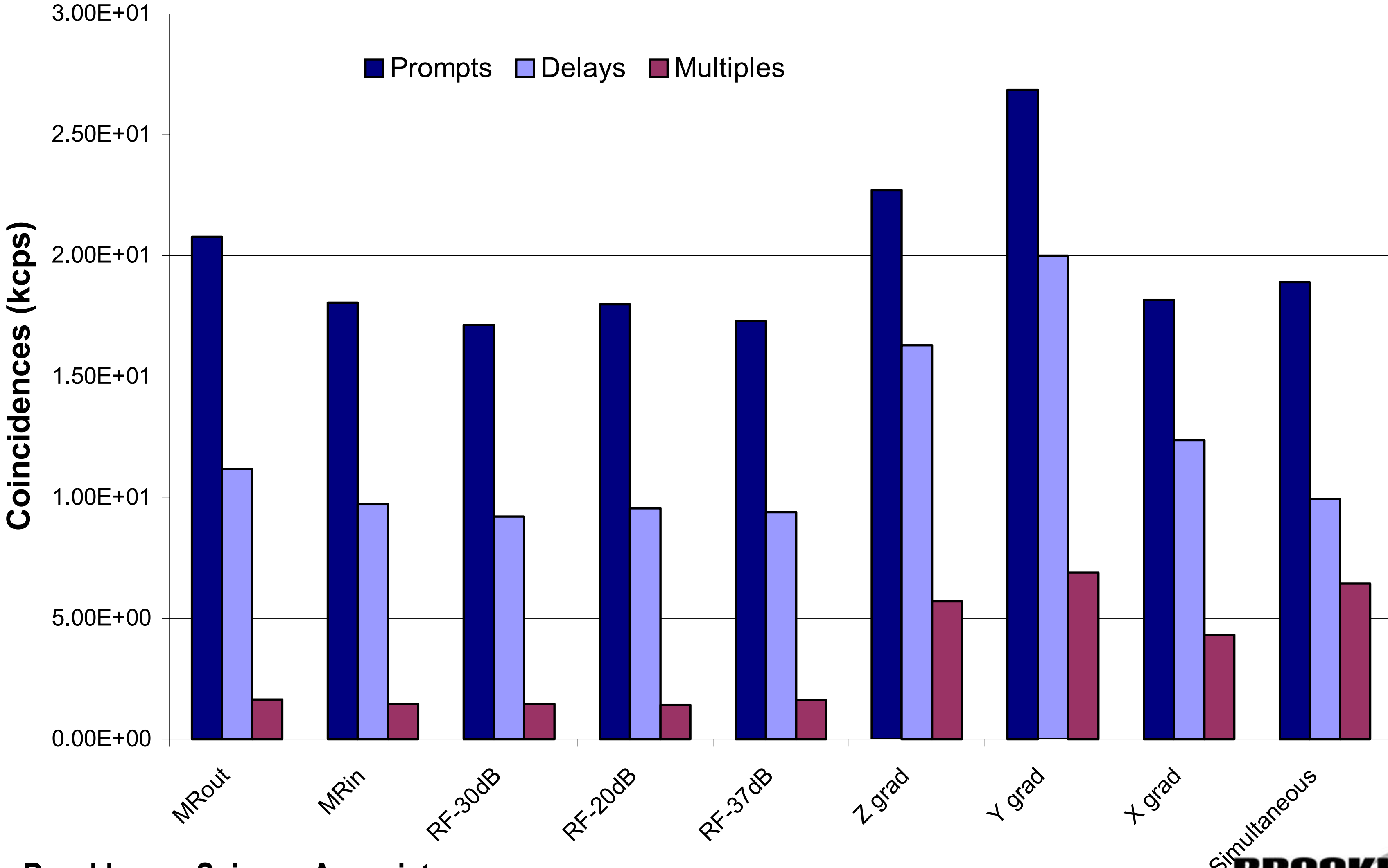
Front view of the RatCAP in MRI



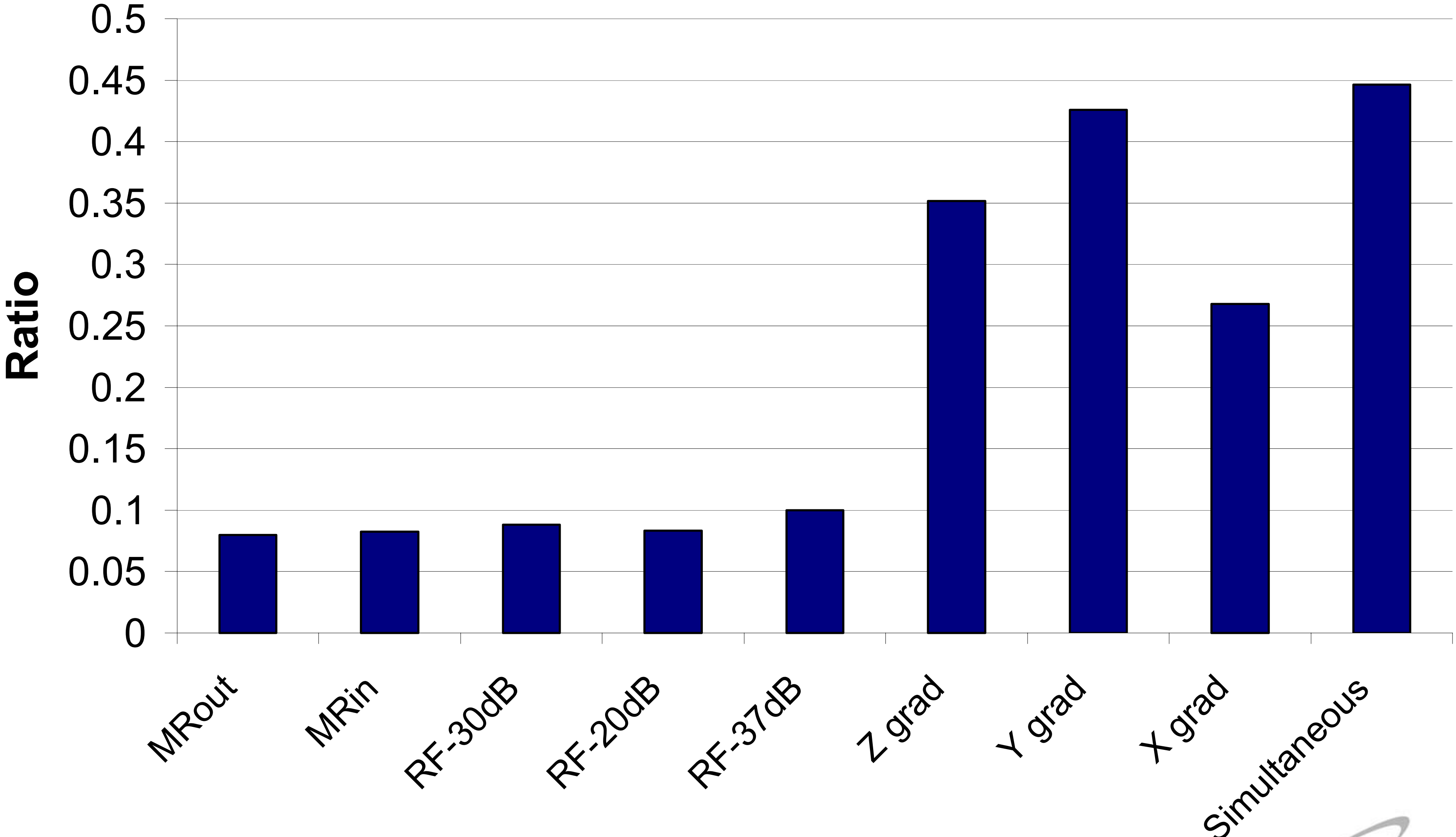
RF Pickup from RatCAP clock



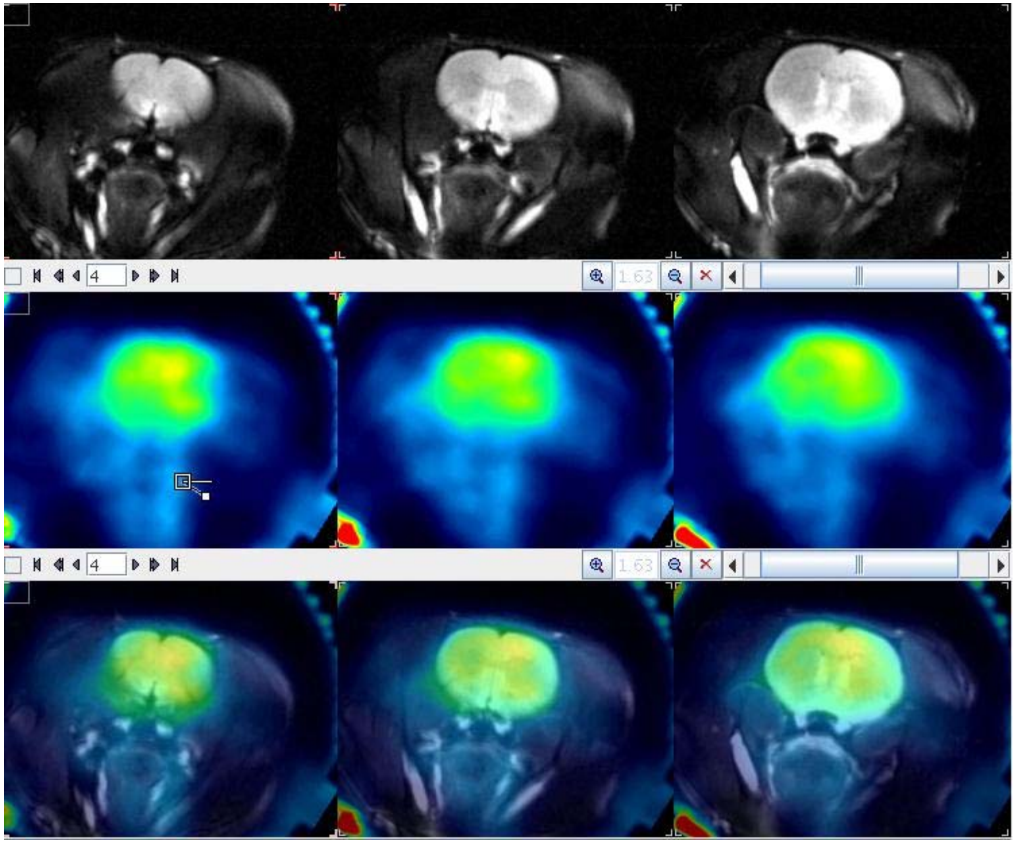
Rate of Coincidence Events



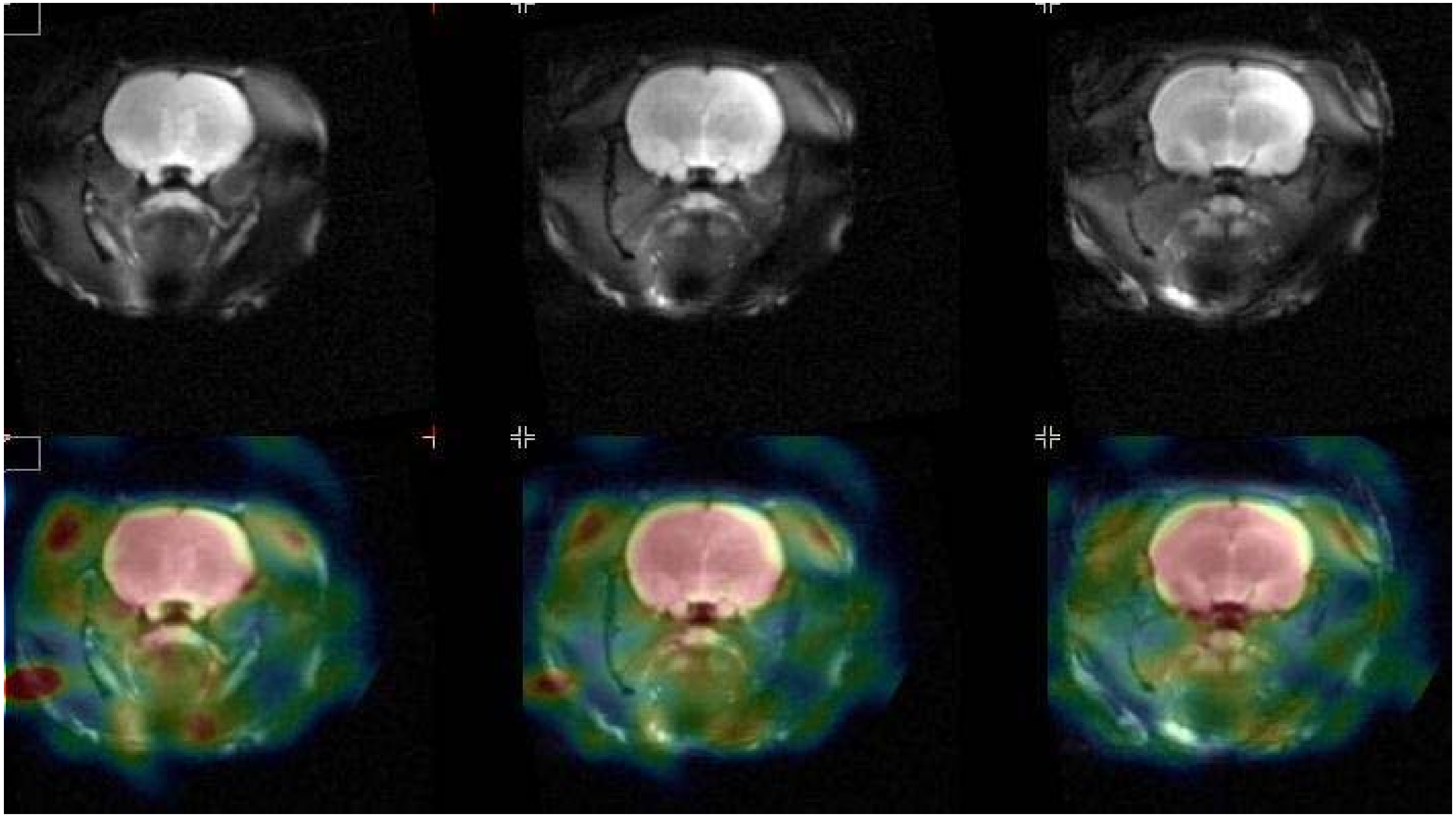
Ratio of multiples to prompts



MRI and PET images obtained simultaneously



Images

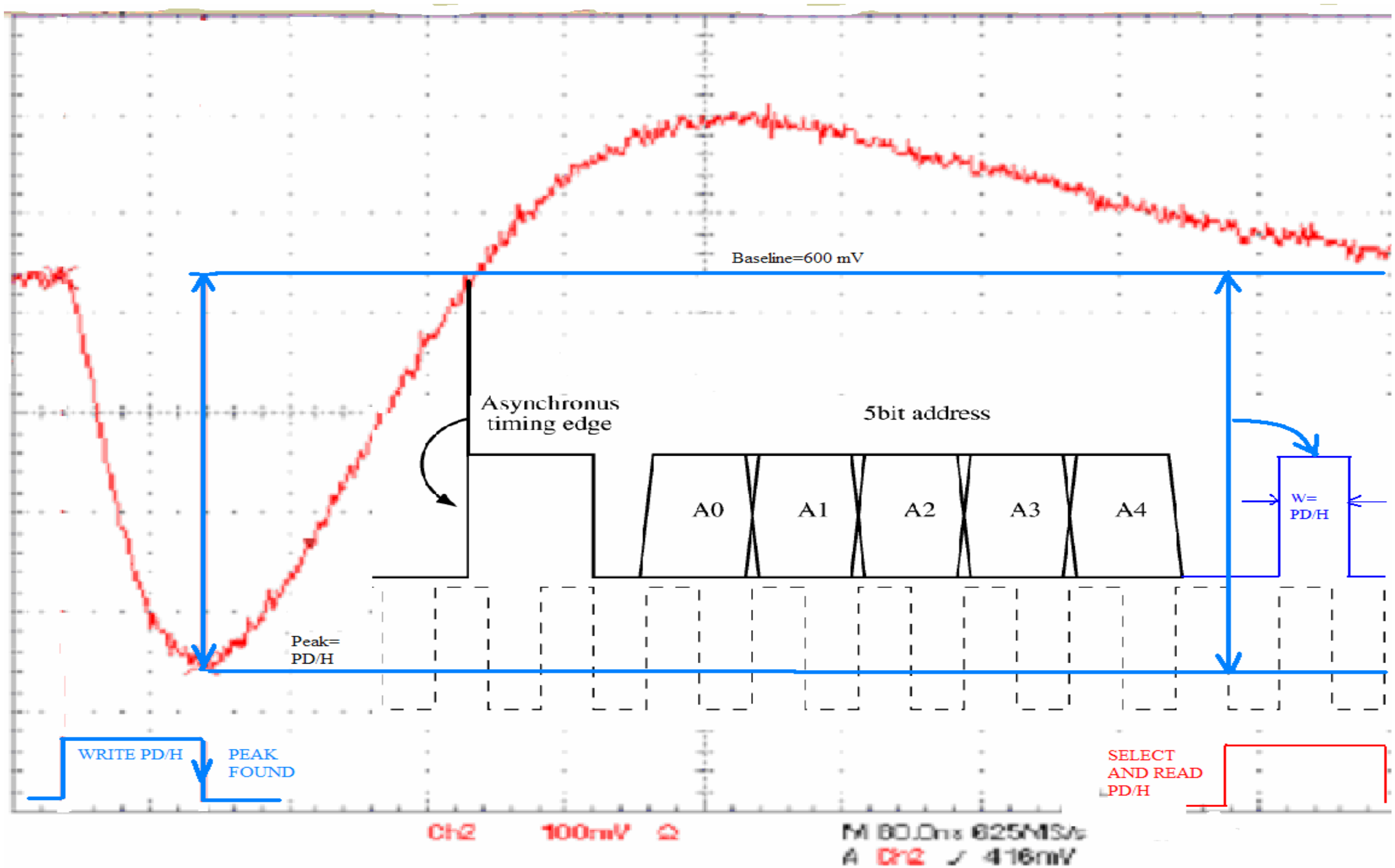


An overnight T2W scan (TR/TE=2.000/0.019s, NEX=75; total time 11 hours, 150 microns in plane resolution, 1mm thickness)

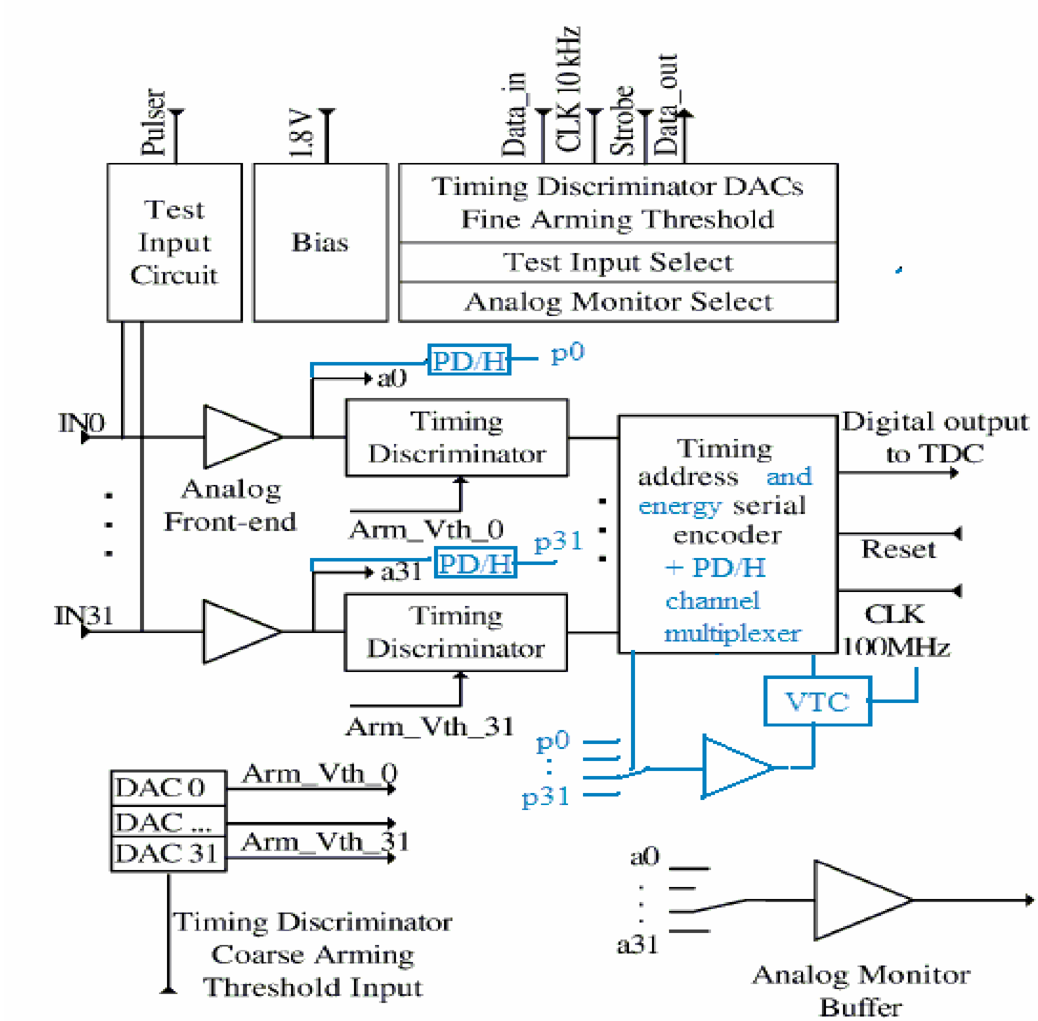
Future Work

- Resolve the issues with attenuation of the signal caused by the aluminum housing
- Study the issue with magnetic field interference with the PET signal
- Study the interference between the 100 MHz clock and the RF pickup
- The development of a whole body mouse scanner compatible with high field MRI
- Append energy information to the ASIC output?

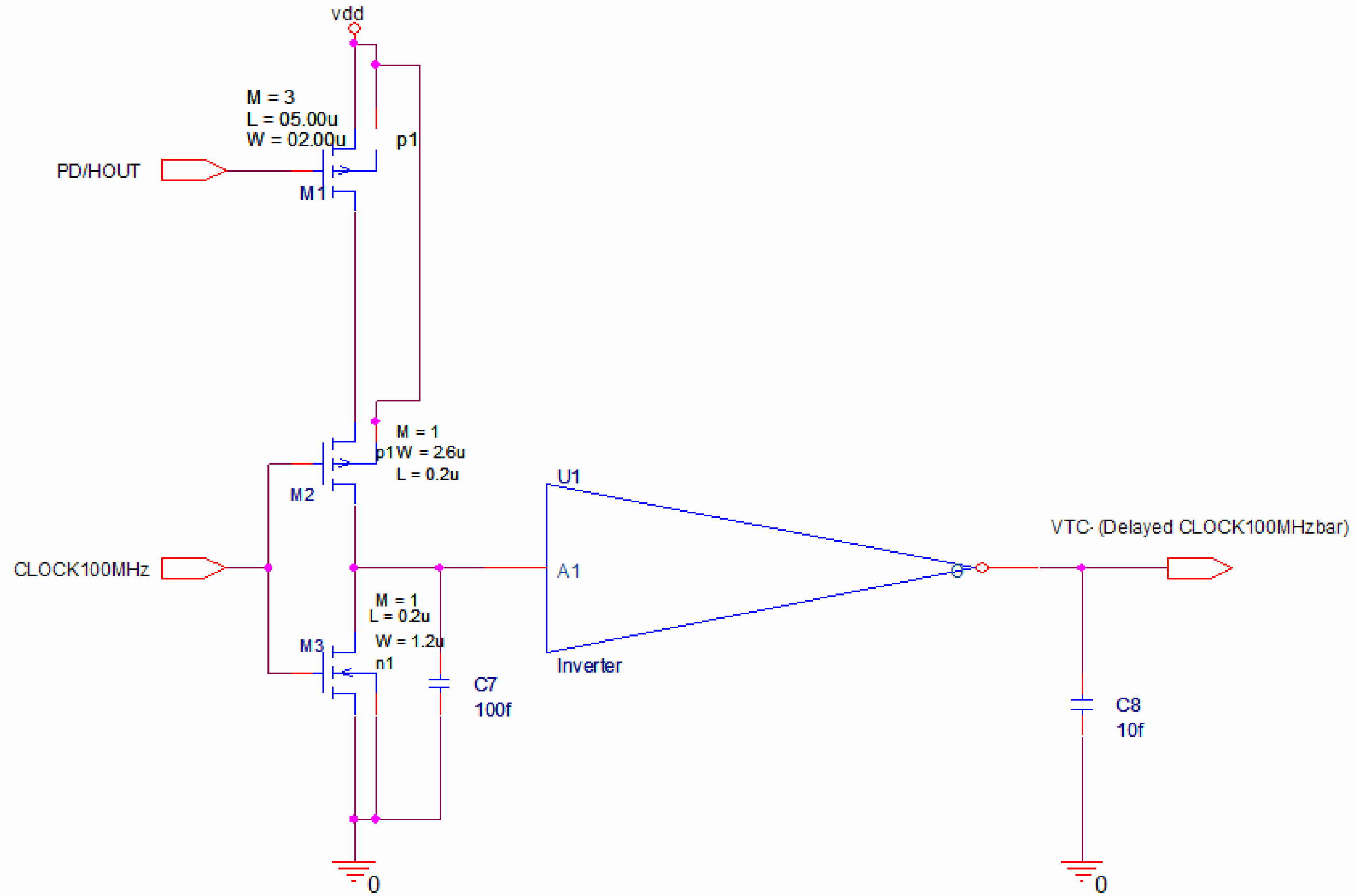
RatCAP ASIC Revision to contain energy information?



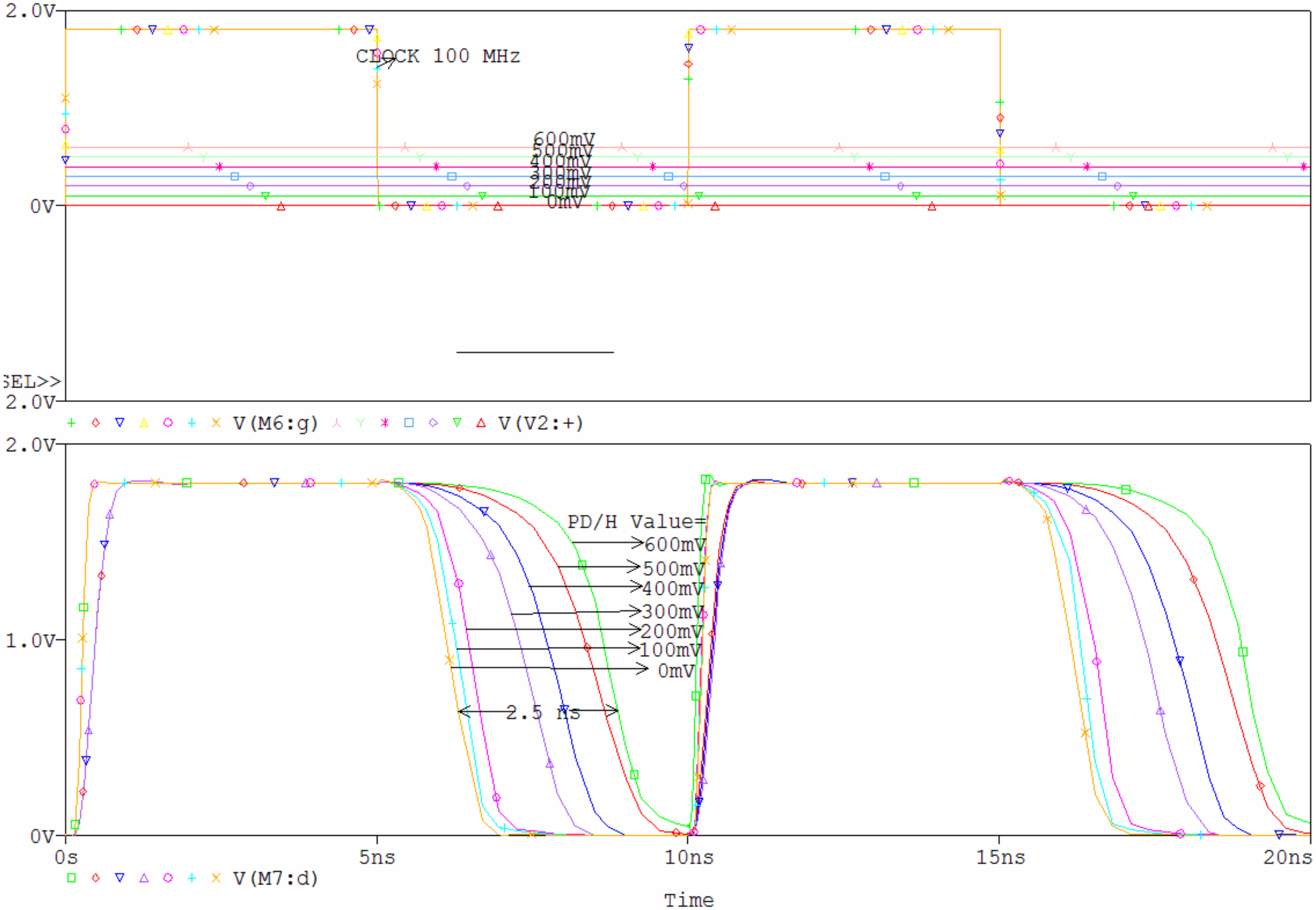
RatCAP ASIC Revision?



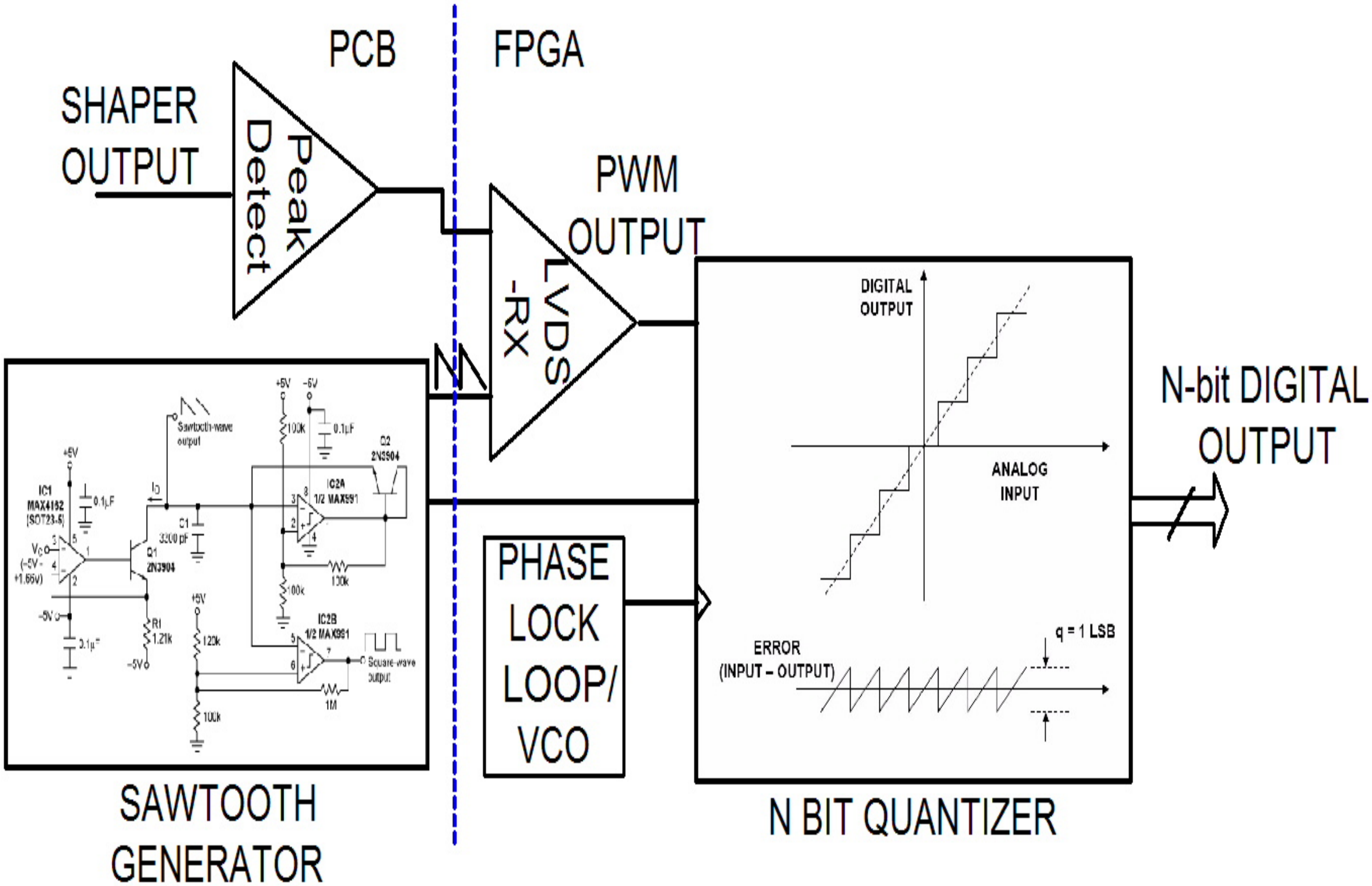
Simple voltage to time converter circuit



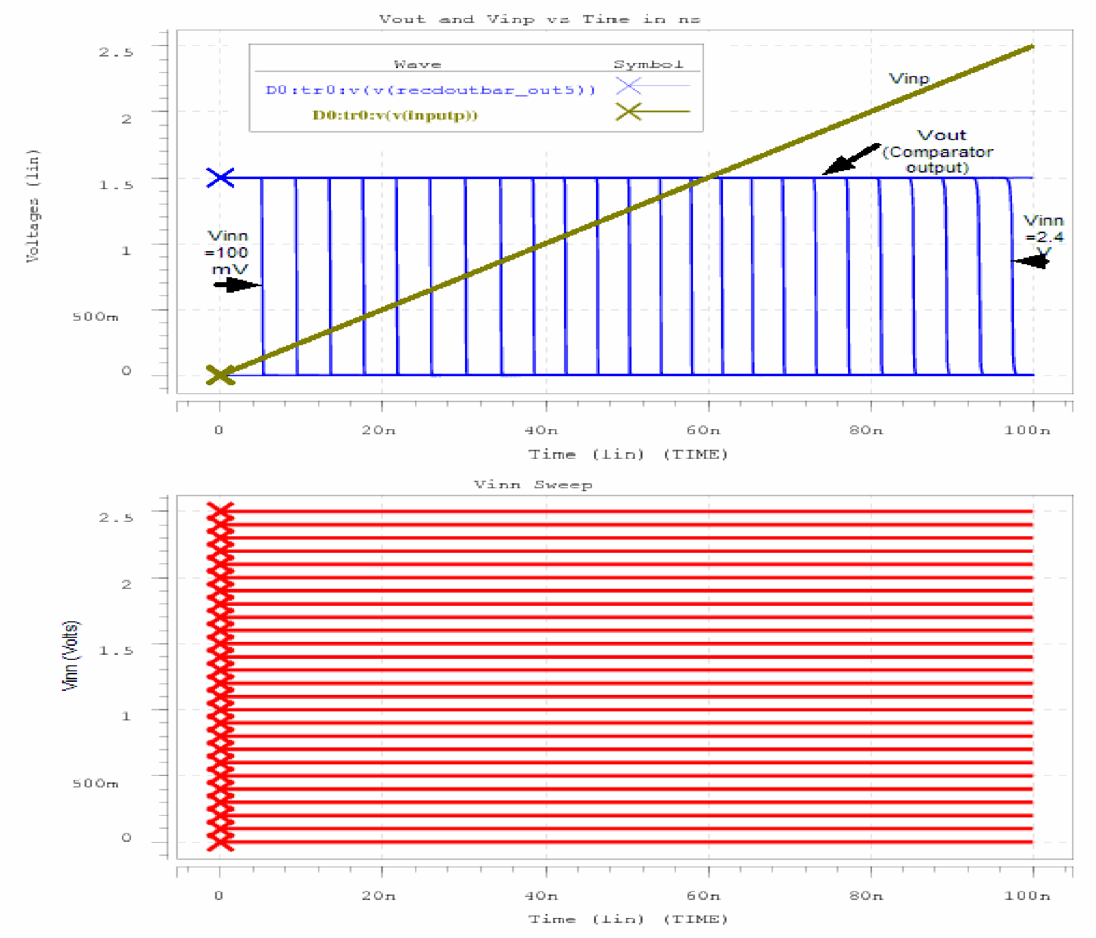
VTC Transient Simulation



ADC using FPGA



FPGA LVDS Receiver as a Comparator



Conclusion

- Simultaneous PET-MR
  - The RatCAP is completely compatible with operation inside the magnetic field of the MRI
  - High quality MRI images have been obtained with the RatCAP inside the field
  - This modular design can lead to a wide variety of simultaneous PET/MRI scanner devices
- FPGA based TDC can be exploited to realize ADC and correct for amplitude dependant time walk

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References

- Slides 23 to 35 taken from:
  - NSS-MIC 2006, conference, Talk ID: M08-4. Speaker: David Schlyer, BNL

RatCAP team