Integrated Q-Enhanced LC Filter with Automatic Tuning And Sampling Receiver

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Outline

Q-enhanced LC filter with automatic tuning

- Introduction: Q-enhanced LC filter
- Nonlinear effects of Q-enhanced LC resonator
- Automatic tuning
- Implementations and measurements

Sampling receiver

- Introduction: sub-sampling vs. RF sampling
- Passive mixer: voltage mode vs. current mode
- Review of decimation filtering techniques
- Implementation and measurements

Motivation

• RF filter is necessary for band selection (and/or image rejection), while most commercial products use off-chip RF filters—bulky and expensive; sometimes introducing matching problems.

• GHz operation facilitates on-chip inductor with reasonable silicon area.

• To integrate RF filters on chip:

-- Active filters (eg. Gm-C): limited DR and high power consumption at GHz.

-- Passive LC filter: poor selectivity, due to limited Q of on-chip spiral inductor.

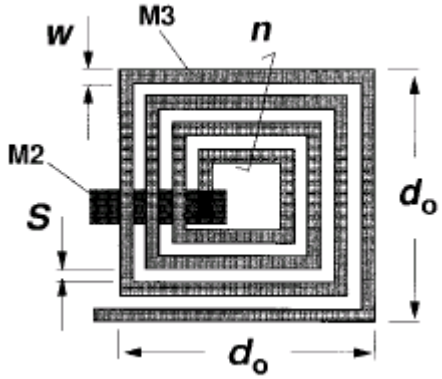
$\Rightarrow$ low-power, DR-improved, high-Q: **Q-enhanced LC filter**

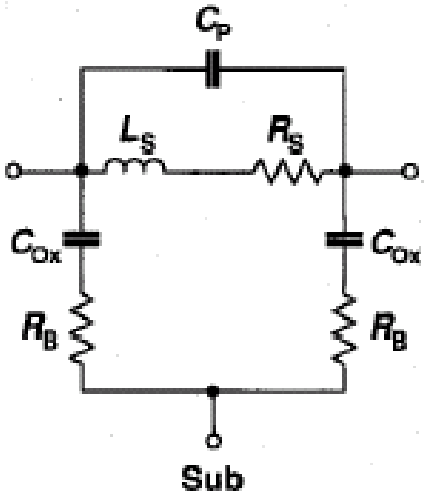
▪ Challenge:

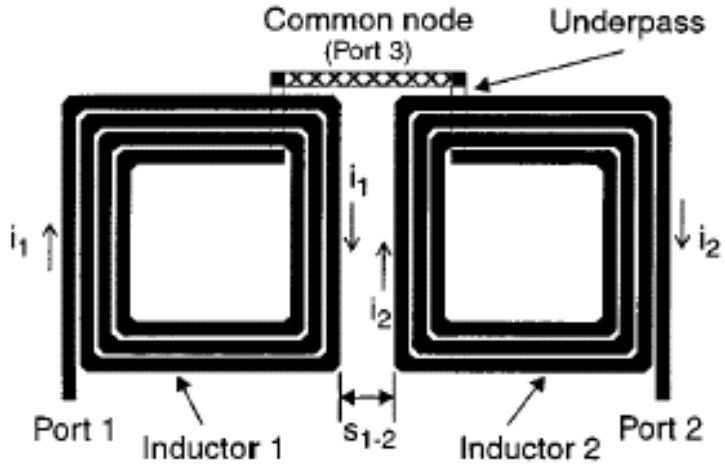
-- intolerable PVT-induced variation from on-chip passives

=> **Automatic tuning** is essential to maintain desired filter selectivity.

On-chip spiral inductor

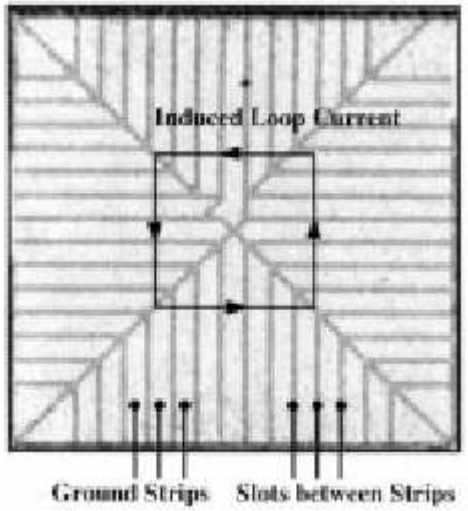






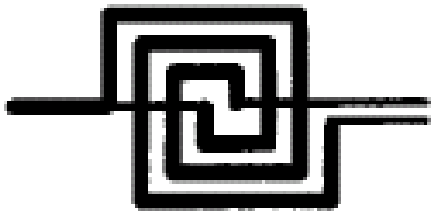
(a)

Ground patterned shield:

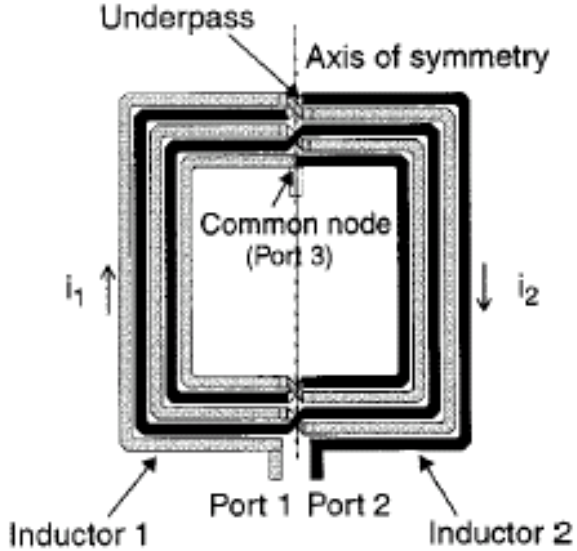


[Yue_98'JSSC]

Differentially driven:



[Kuhn_95'EL]

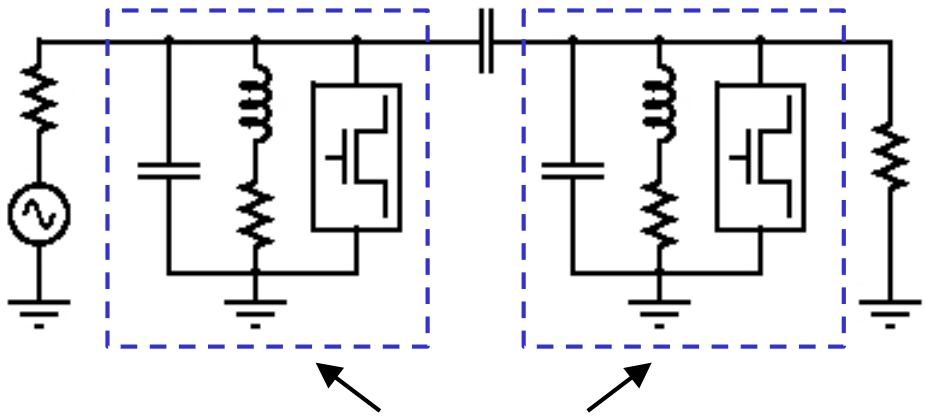


[Danesh_02'TMTT]

Q-enhanced LC filter

Issue: inductor loss does not scale with inductance
=> use same size inductors => coupled-resonator filter

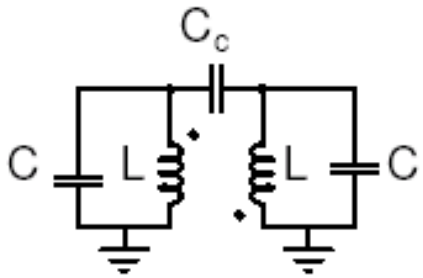
Example: a 4th-order Q-enahcned LC filter



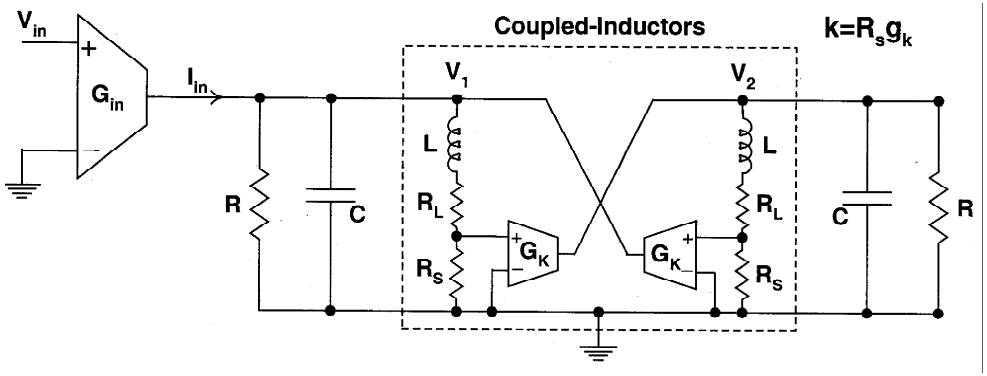
Q-enhanced LC resonators

- Need automatic tuning to control both the resonant frequency and the quality of each resonator
- Problem: tilting passband, due to in-phase coupling of the inductors => needs coupling neutralization

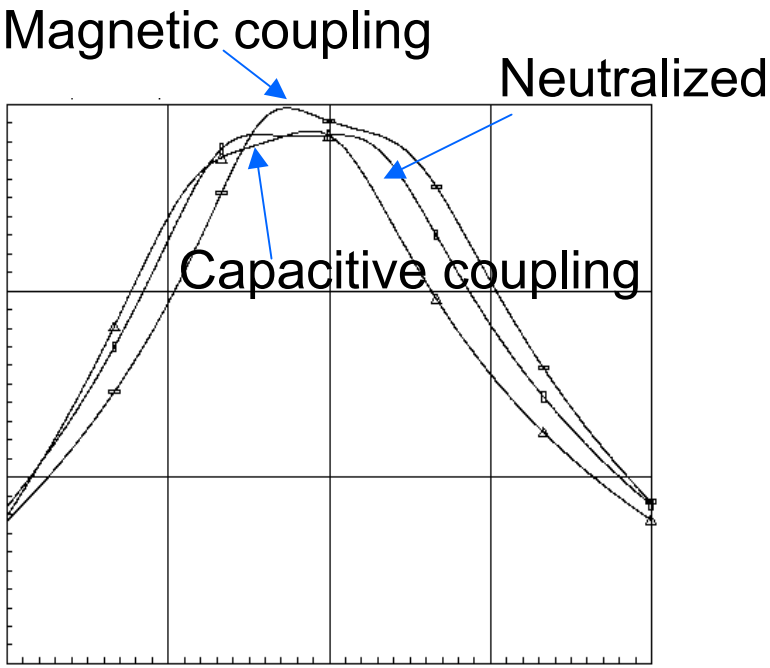
Coupling neutralization

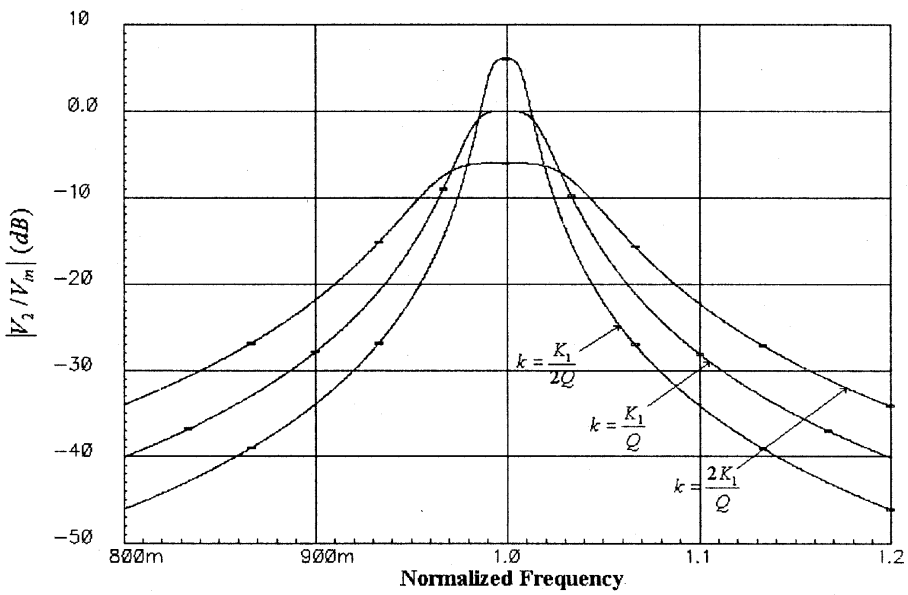


[D. Li_00'Ph.D thesis]



[Mohieldin_03JSSC]



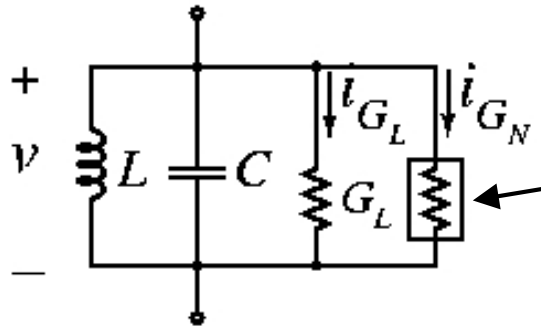


-Needs accurate modeling.

-Needs extra tuning for coupling.

Nonlinear effect in Q-enhanced LC resonator

$v = V\sin(\omega t)$



Nonlinear negative conductor

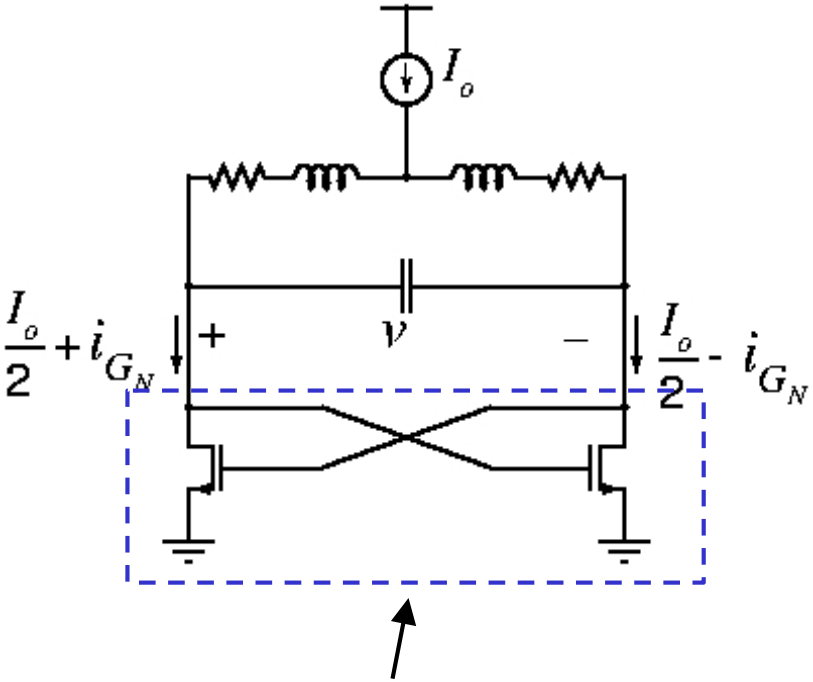
Weak nonlinearity, differential => $i_{G_N} = k_1 v + k_3 v^3$

Steady state => $W_{diss} / cycle = \int_0^T \left(i_{G_L} v\right) dt + \int_0^T \left(i_{G_N} v\right) dt = 0$

=> $V^2 \left(G_L + k_1 + \frac{3}{4} k_3 V^2 \right) = 0$

Nonlinearity: $k_3 \neq 0$ => steady-state amplitude $\boxed{V = \sqrt{-\frac{4(G_L + k_1)}{3k_3}}}$

Implementation with NMOS transistors



Negative conductance
(in differential mode)

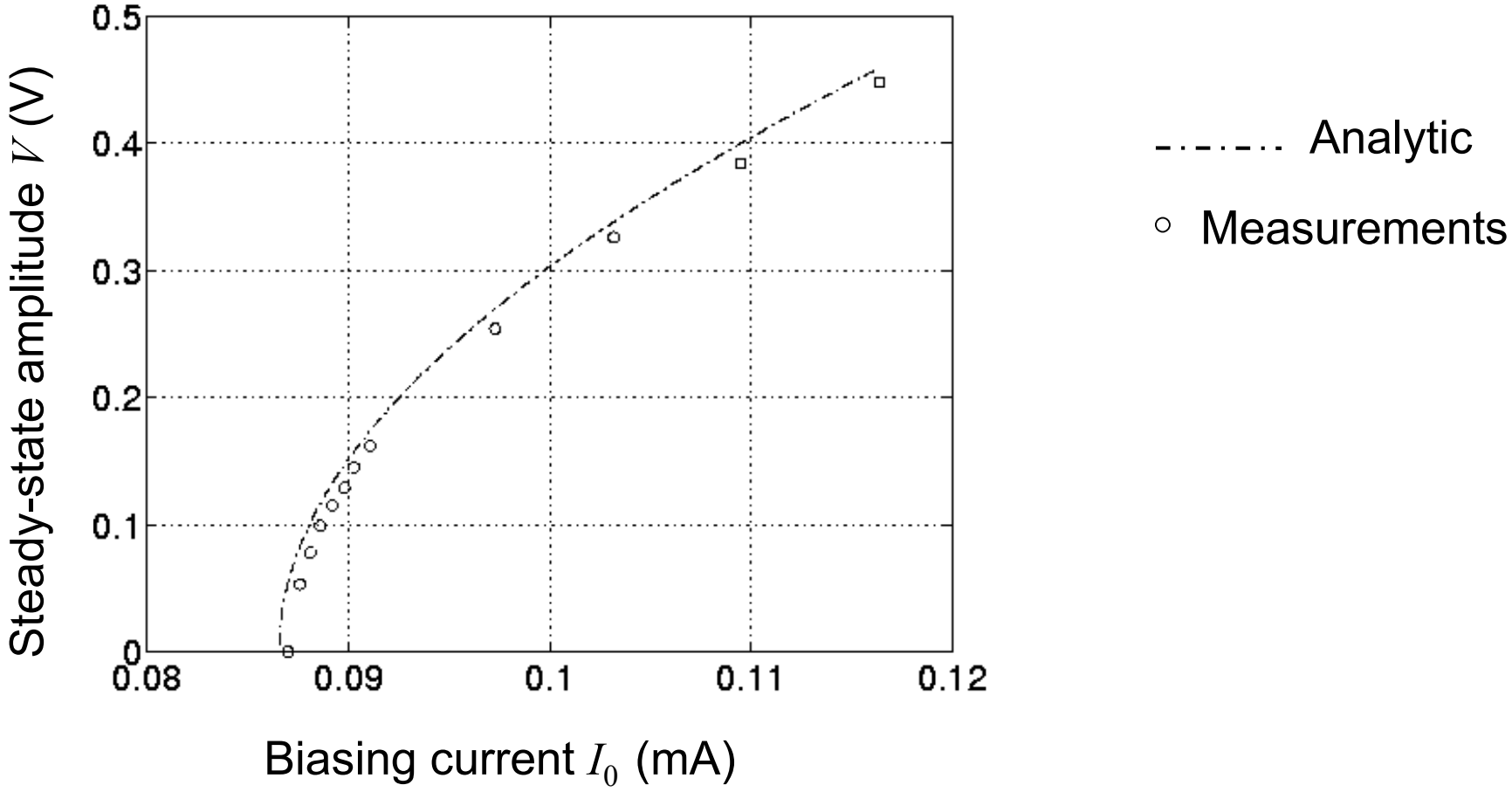
$$v = \frac{1}{\sqrt{\beta}}\left[\sqrt{\frac{I_0}{2} - i_{G_N}} - \sqrt{\frac{I_0}{2} + i_{G_N}}\right]$$

$$\Rightarrow \quad i_{G_N} \approx -\underbrace{\sqrt{\frac{\beta I_0}{2}}}_{k_1} v + \underbrace{\sqrt{\frac{\beta^3}{32 I_0}}}_{k_3} v^3$$

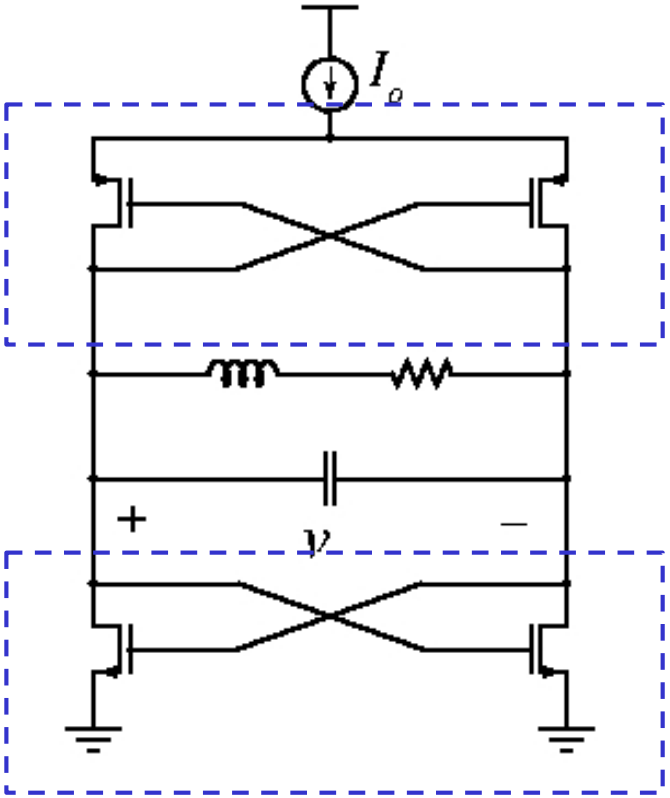
Apply to $V = \sqrt{-\frac{4(G_L + k_1)}{3k_3}}$

=> Steady-state amp. V is a function of bias I_0

Comparison to measurements on 112 kHz breadboard implementation



CMOS implementation



$$k_1 = -\left(\sqrt{\beta_p} + \sqrt{\beta_n}\right)\sqrt{\frac{I_0}{2}}, \qquad k_3 = \frac{\sqrt{\beta_p^{\,3}} + \sqrt{\beta_n^{\,3}}}{\sqrt{32 I_0}}$$

Given the required linear negative conductance (k_1) and bias current (I_0), the active current in the CMOS implementation is more linear than in the NMOS implementation.

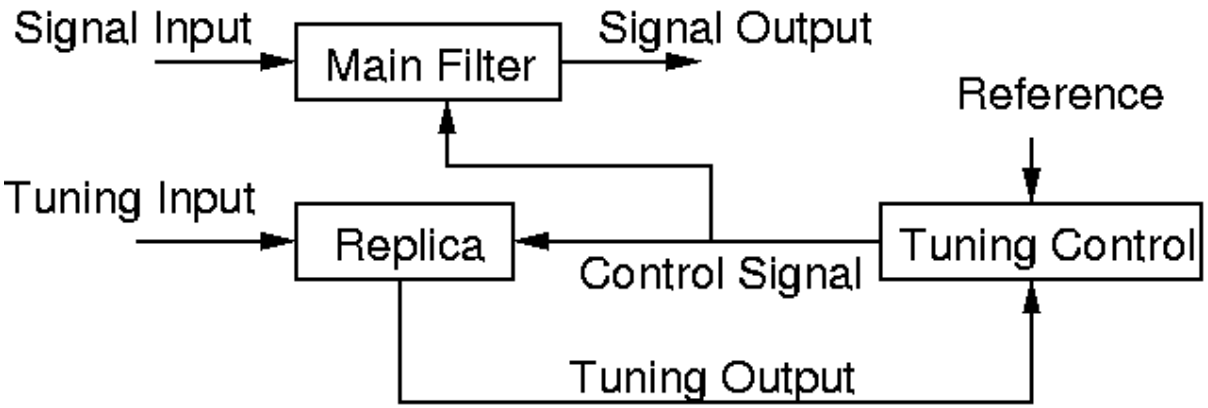
$$k_1 = k_{1,\mathrm{CMOS}} = k_{1,\mathrm{NMOS}}$$

$$I_0 = I_{0,\mathrm{CMOS}} = I_{0,\mathrm{NMOS}}$$

=> $k_{3,\mathrm{CMOS}} < k_{3,\mathrm{NMOS}}$

Automatic tuning

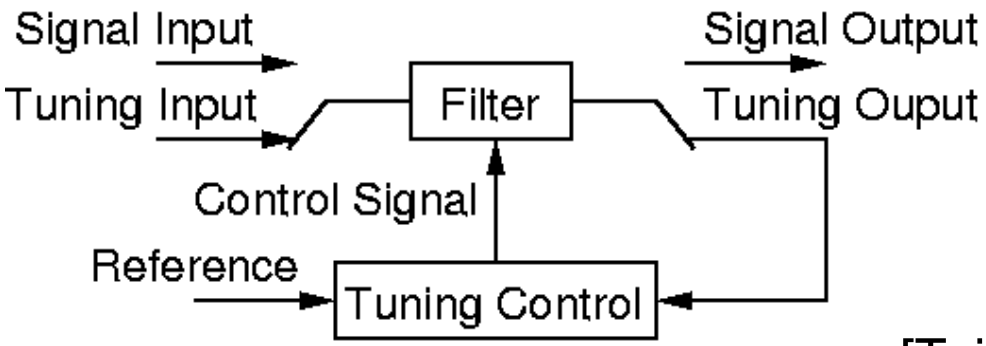
Indirect tuning (master-slave):



Replica type:

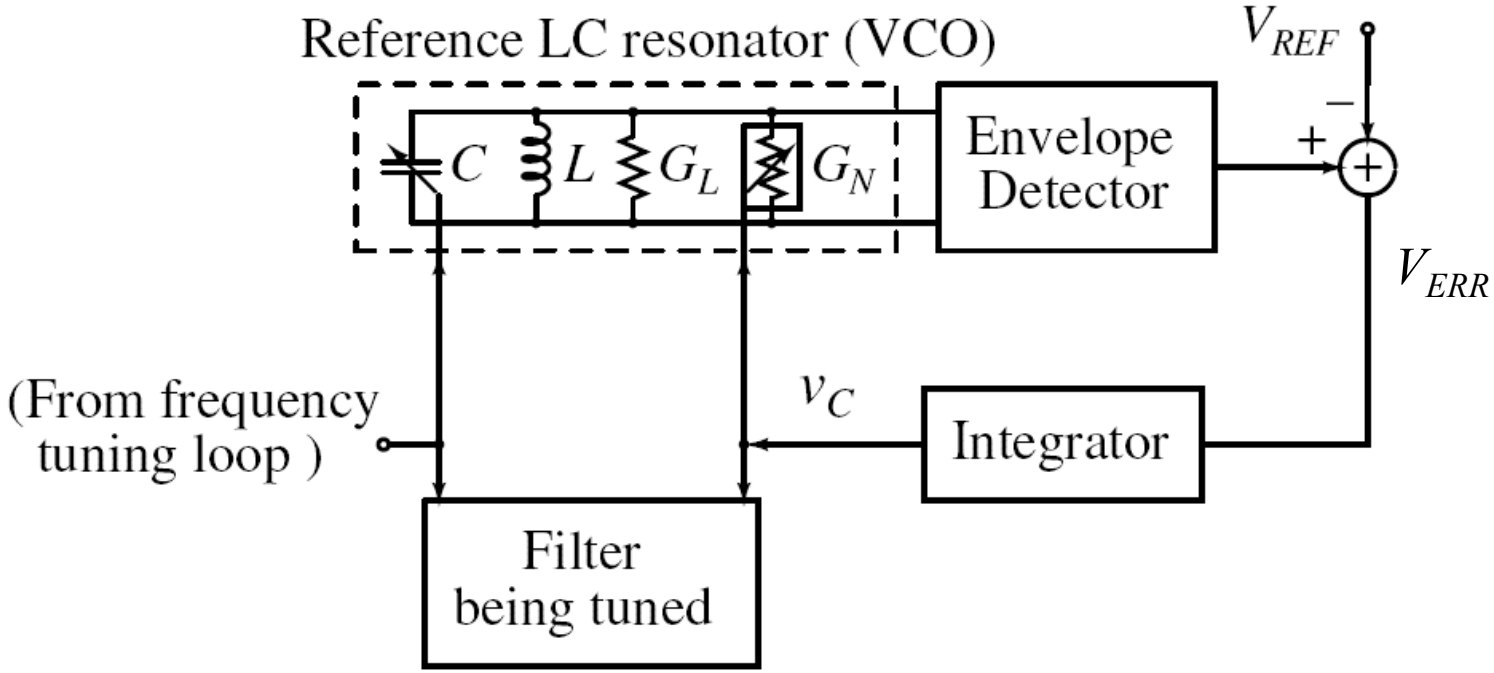
- VCF
- VCO

Direct tuning (self-tuning):



[Tsividis_81'EL]

Conventional VCO Q-tuning using magnitude-locked loop:



$V_{ERR} = V - V_{REF} \rightarrow I_0 \rightarrow k_1$ and $k_3 \rightarrow V$

$\Rightarrow$ Q of the resonator in the master (VCO) is tuned to infinity;
$\Rightarrow$ But, is Q of the resonator in the slave (filter being tuned) infinite?

Is the tuned Q of the resonators in the filter infinite?

Filter requires good linearity

=> filter resonators work with much smaller amplitude than the VCO resonators:

=> $G_{N_{filter}} \approx k_1$

Refer to the VCO resonator Eq. $V^2\left(G_L + k_1 + \frac{3}{4}k_3V^2\right) = 0$

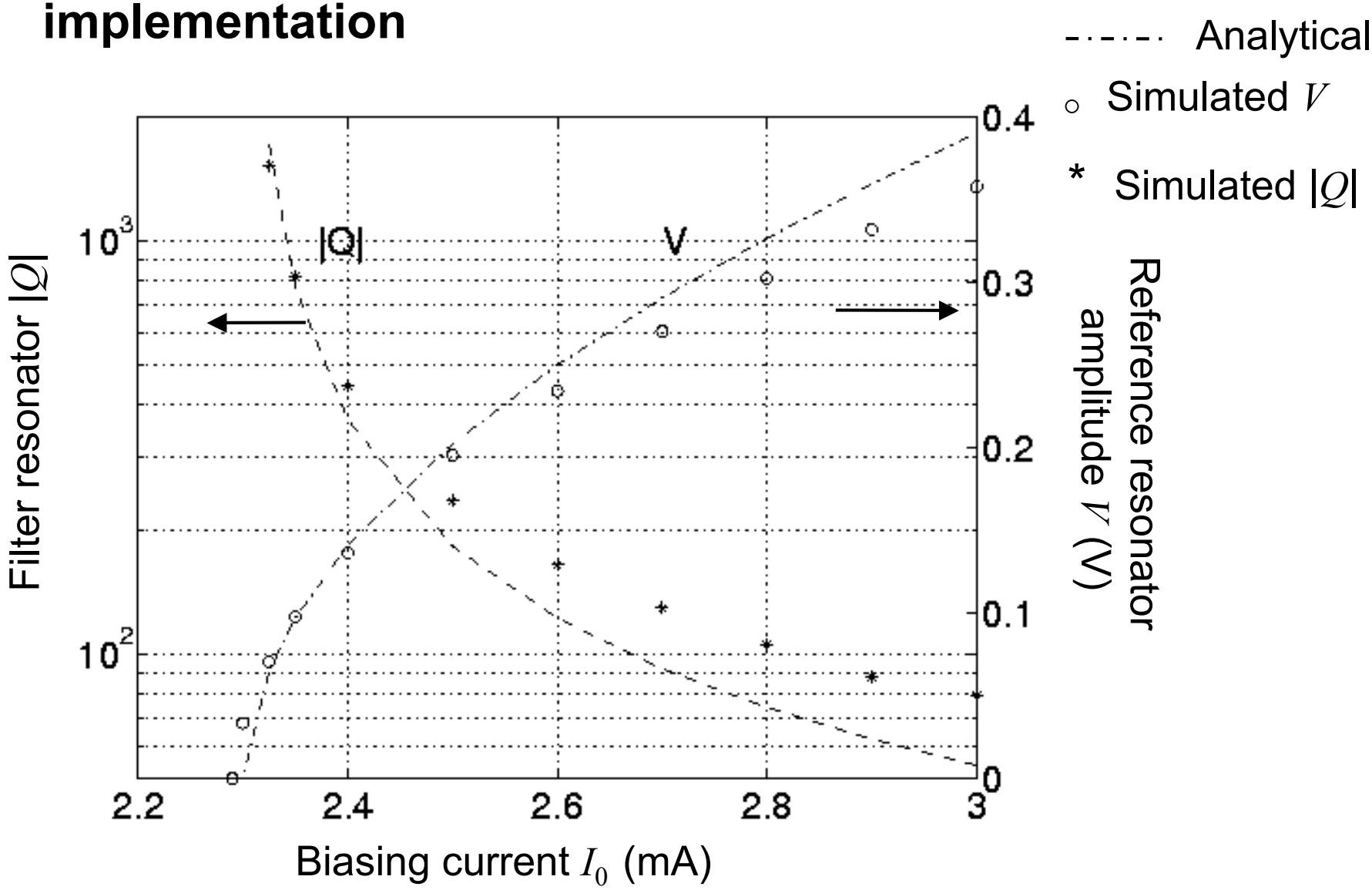
=> $Q_{LC_{filter}} = \frac{1}{G_L + G_{N_{filter}}}\sqrt{\frac{C}{L}} \approx -\frac{1}{\frac{3}{4}k_3V_{REF}^{\ 2}}\sqrt{\frac{C}{L}}$

$\Rightarrow$ The nonlinear part makes the filter resonator different from the VCO resonator

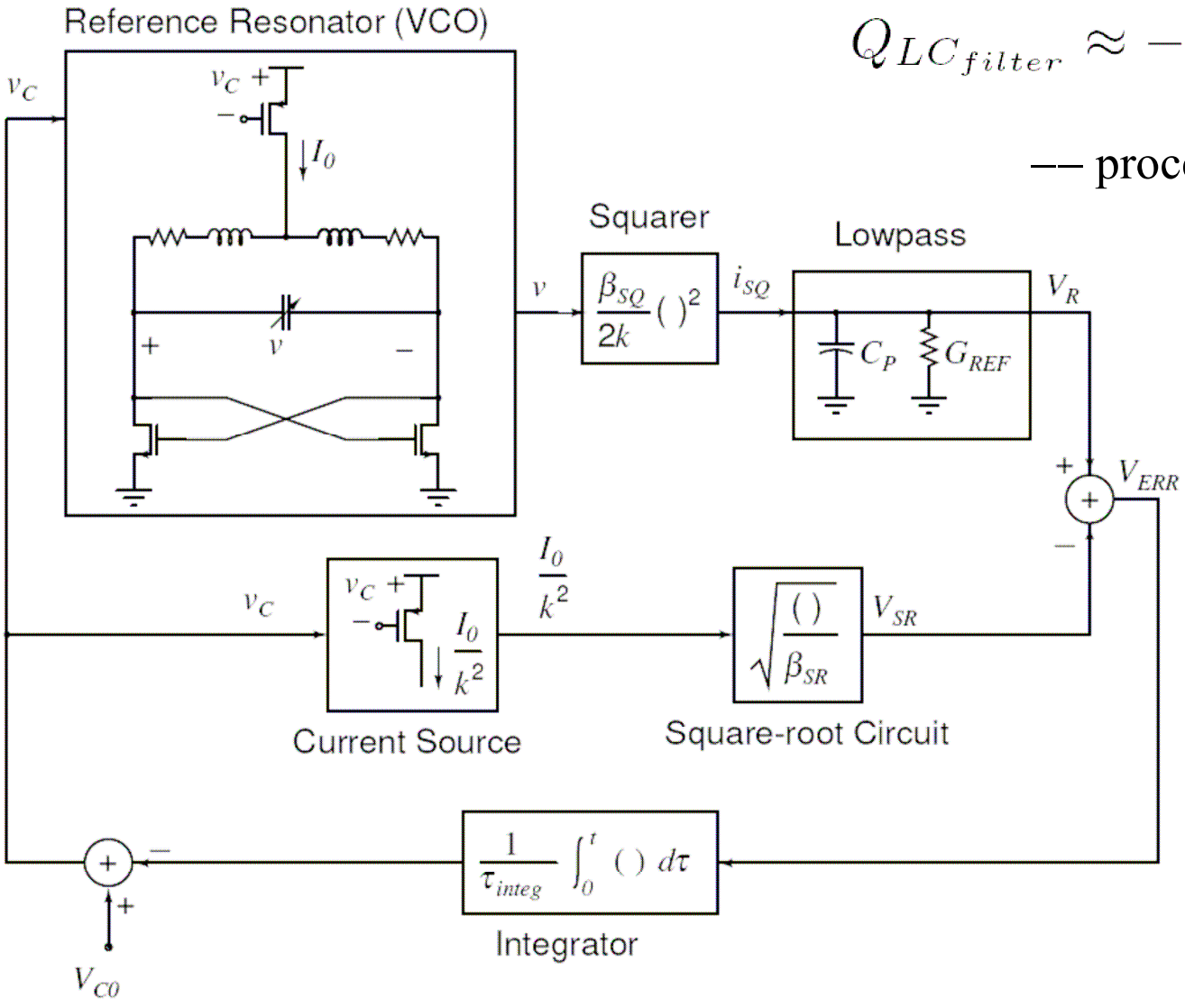
$\Rightarrow$ Finite Q of fitler resonator, varying with PVT;

$\Rightarrow$ $V_{REF}\downarrow$ or $k_3\downarrow$ => $|Q|\uparrow$

Comparison to simulation on a 4.8 GHz NMOS implementation



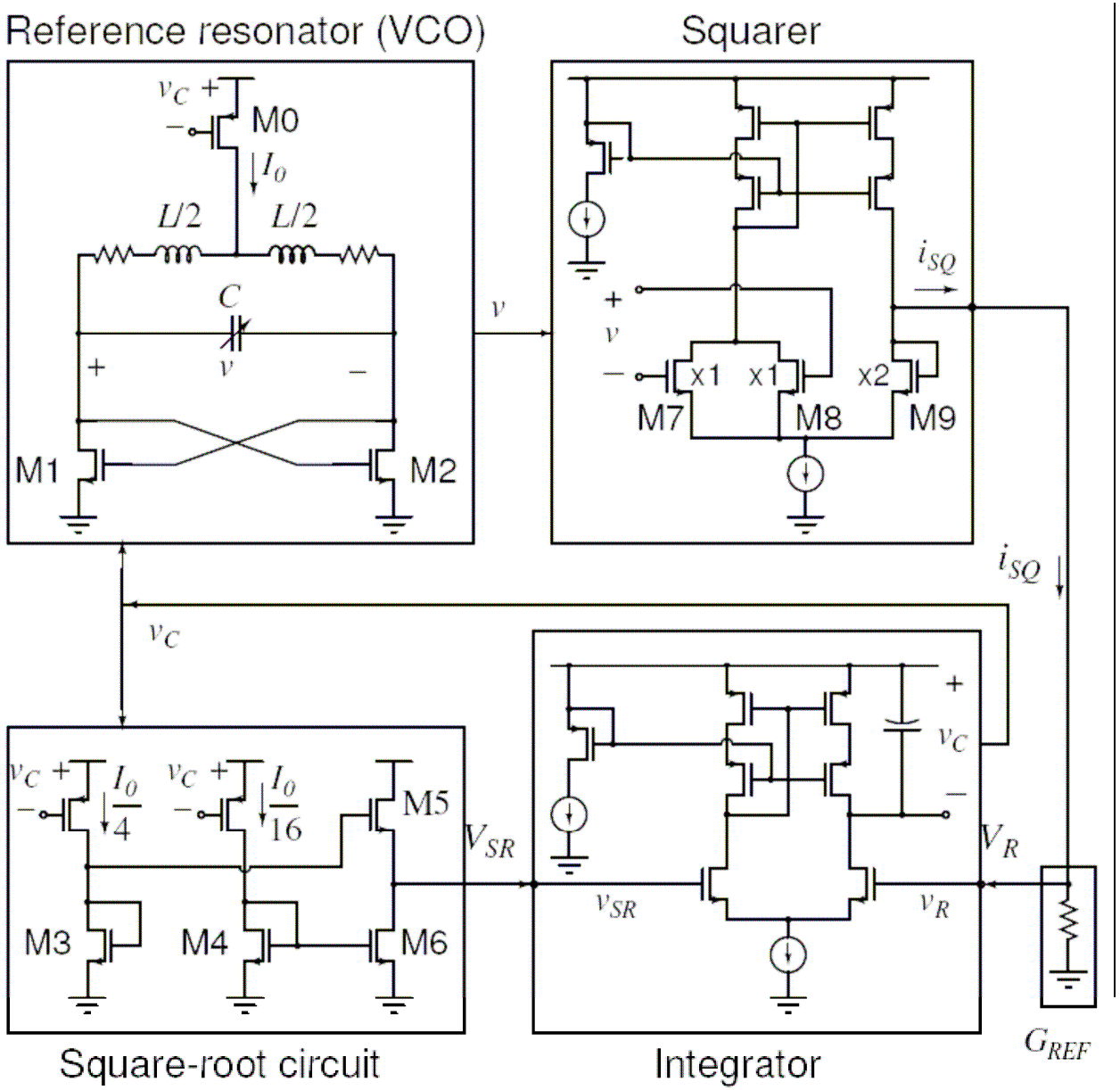
VCO Q-tuning using conductance reference [S. Li_05'RFIC]



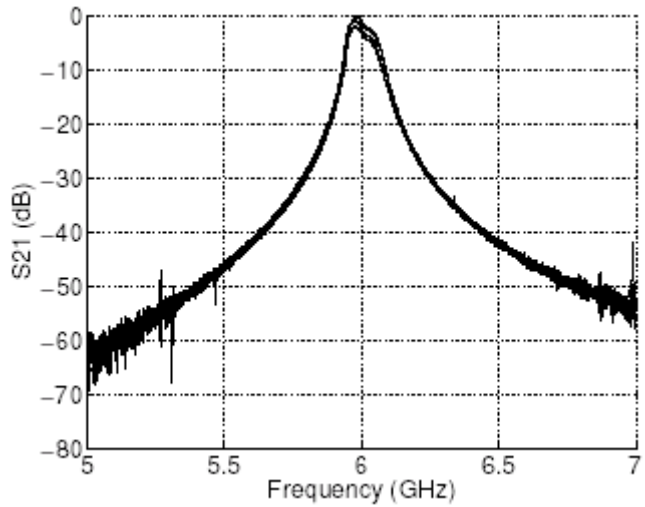
$$Q_{LC_{filter}} \approx -1/[G_{REF}\omega_0 L]$$

–– process independent!

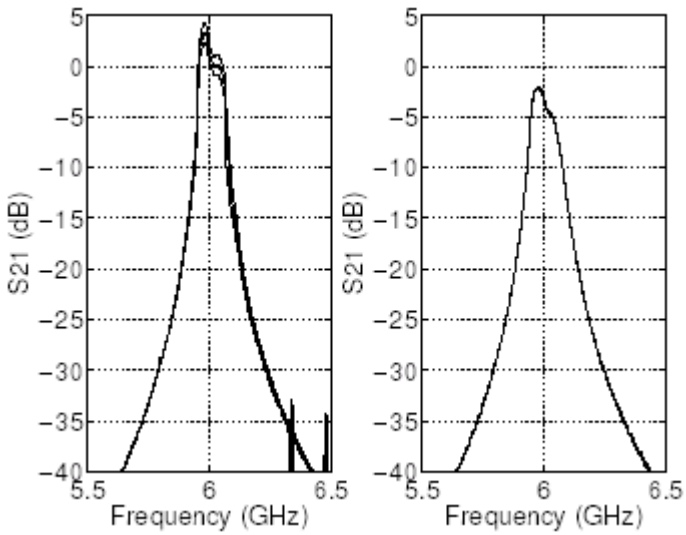
Implementation (0.18um CMOS)



Measured filter frequency response w/ VCO Q tuning

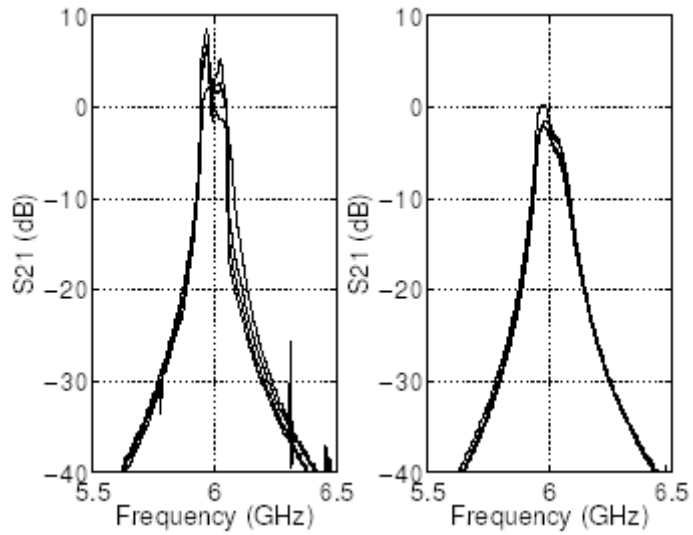


Power supply tolerance:



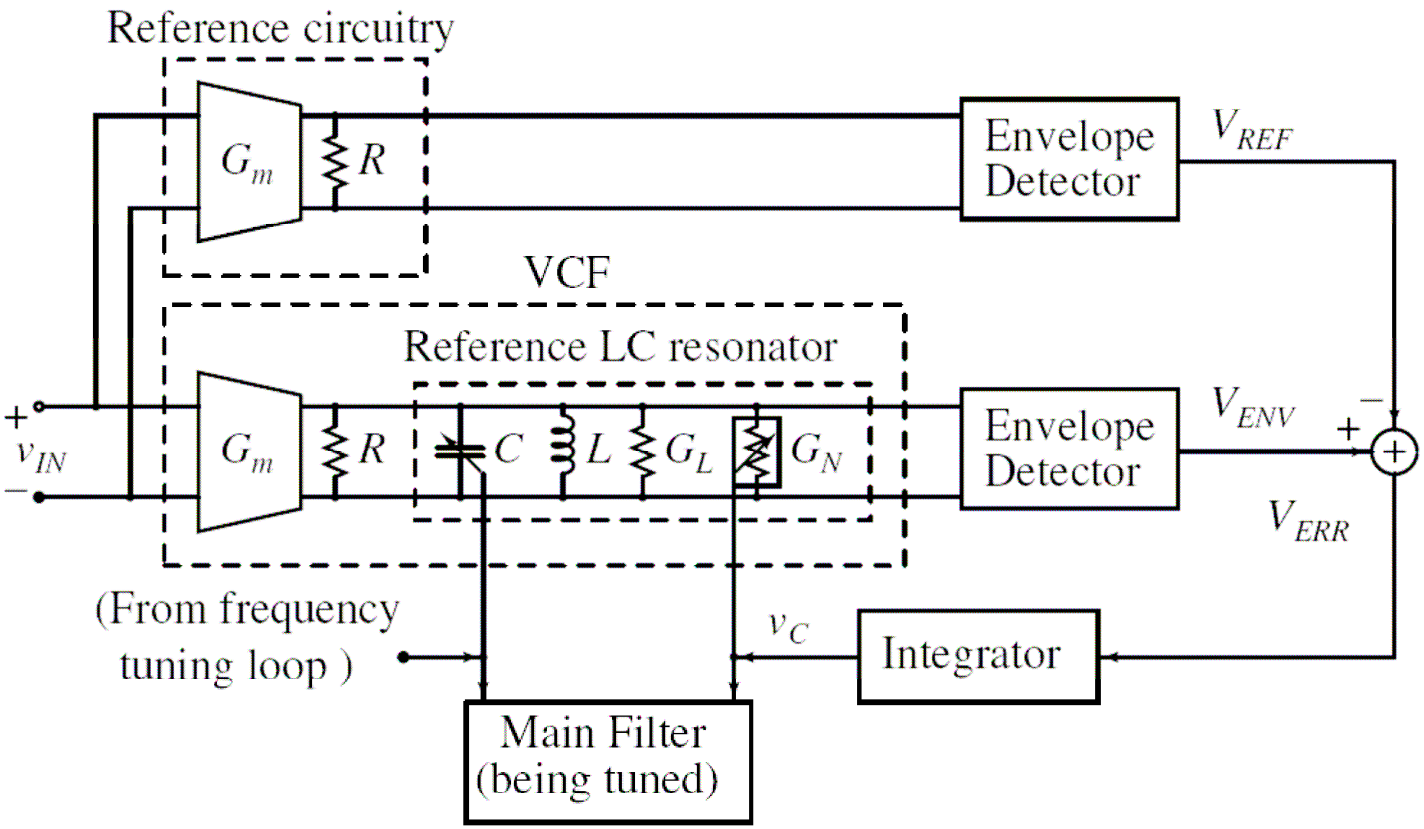
w/o tuning w/ tuning

Process tolerance:



w/o tuning w/ tuning

VCF Q-tuning scheme [S.LI_TCASII06]

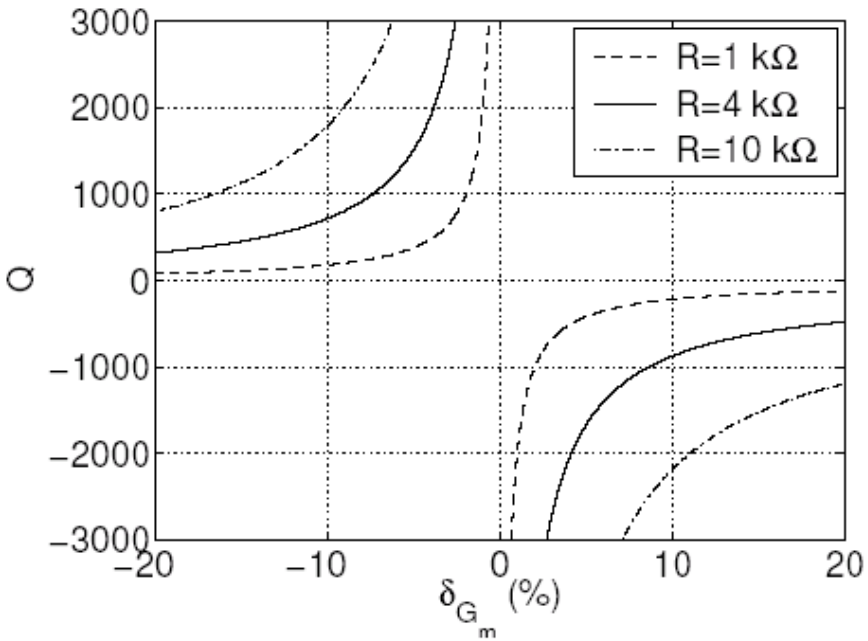


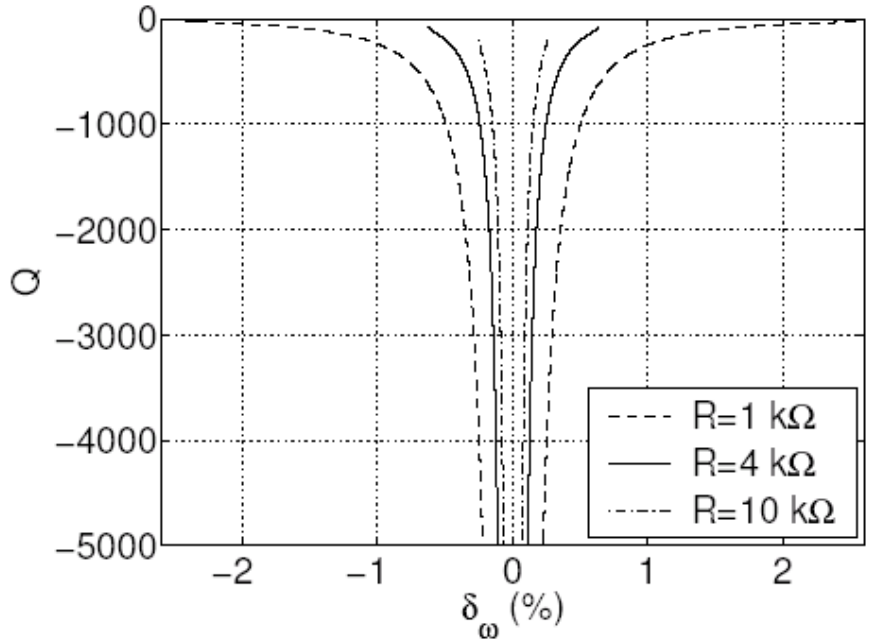
Nonidealities

Mismatches, offset of loop integrator, accuracy of envelope detector, interference with frequency tuning, etc.

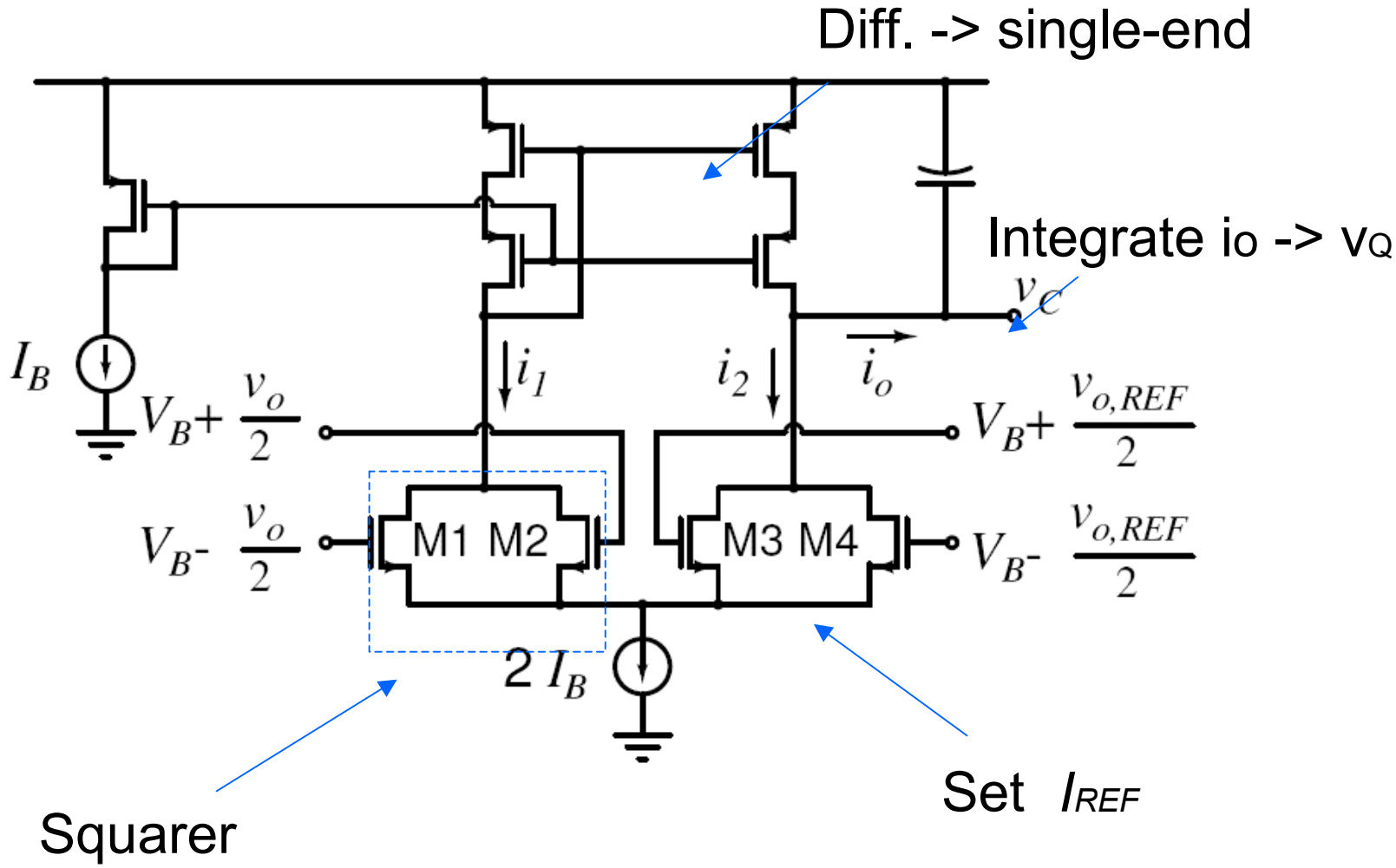
$$Q_{LC,all} = \frac{1}{\frac{1}{Q_{LC,mismatches}} + \frac{1}{Q_{LC,offset}} + \frac{1}{Q_{LC,freq-error}}}$$

$$\approx -\frac{R\sqrt{\frac{C}{L}}}{\delta_{G_m} + \delta_R + \delta_{K_{ED}} + \delta'_{V_{OS}} + \left[1 - \sqrt{1 - (2\frac{R}{\omega_0 L}\delta_\omega)^2}\right]}$$





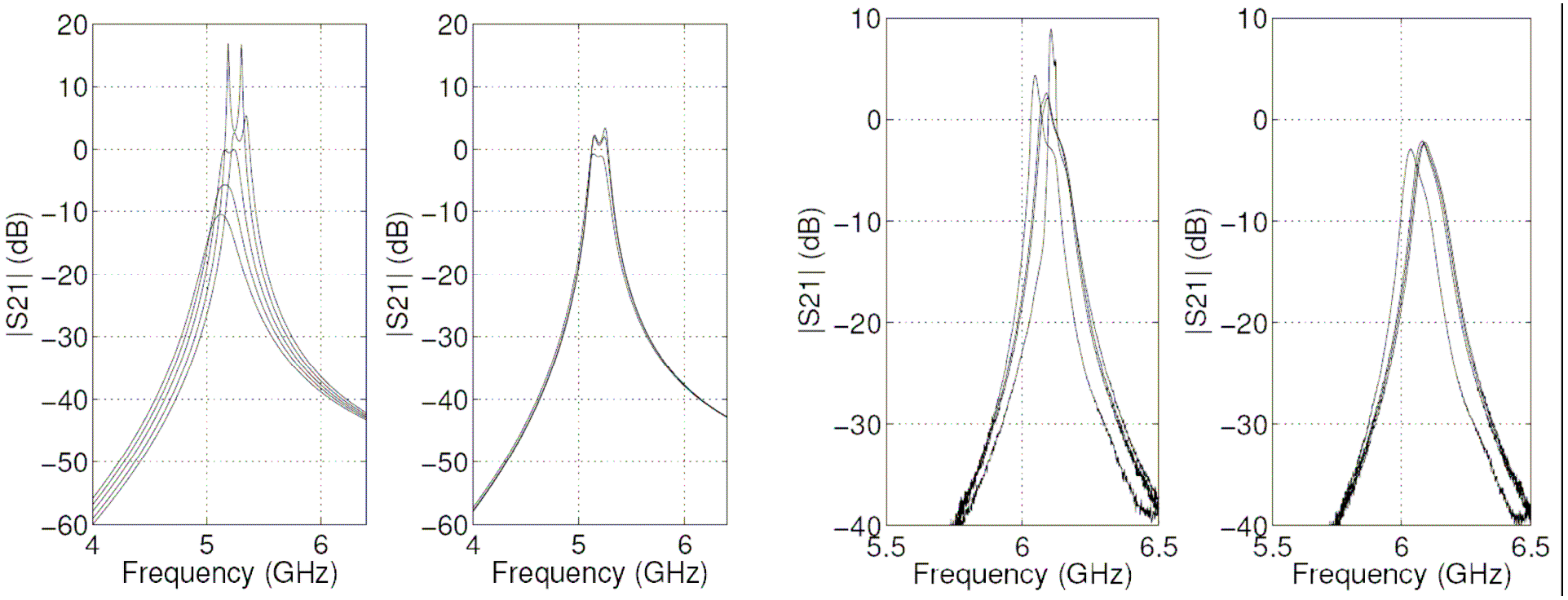
VCF Q-tuning circuitry: envelope detector, comparator and integrator



Simulated and measured filter frequency response w/ VCF Q tuning

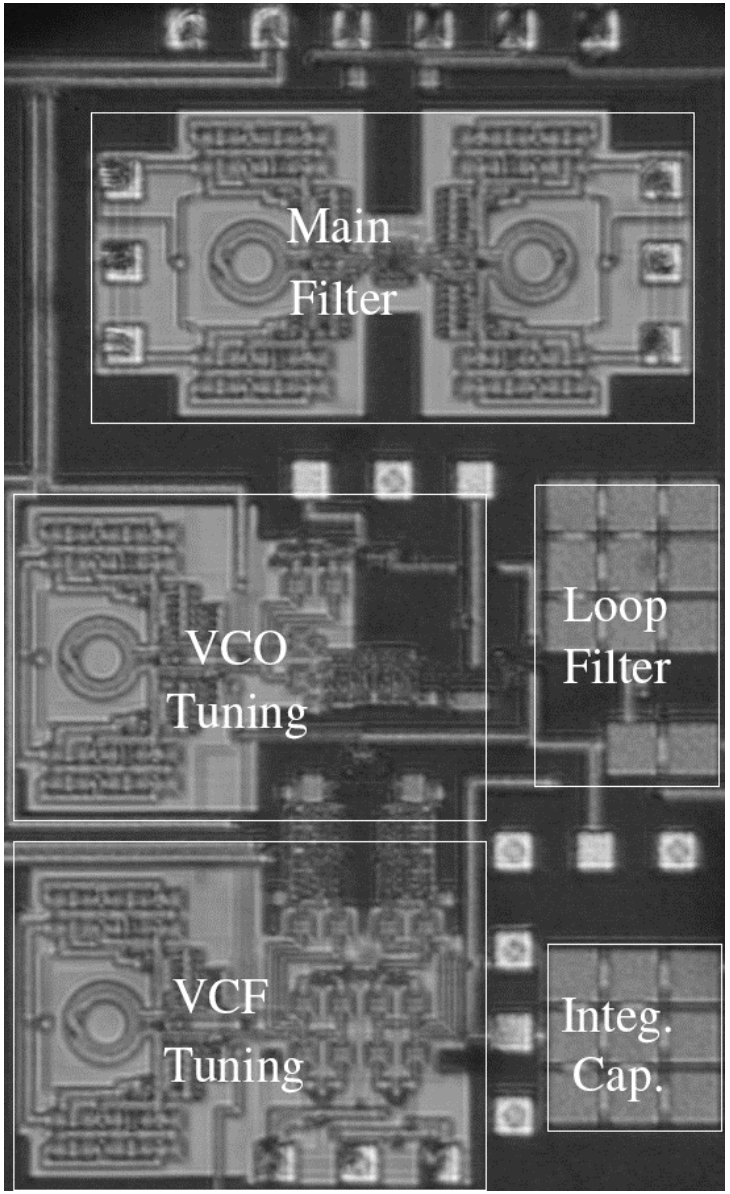
simulation

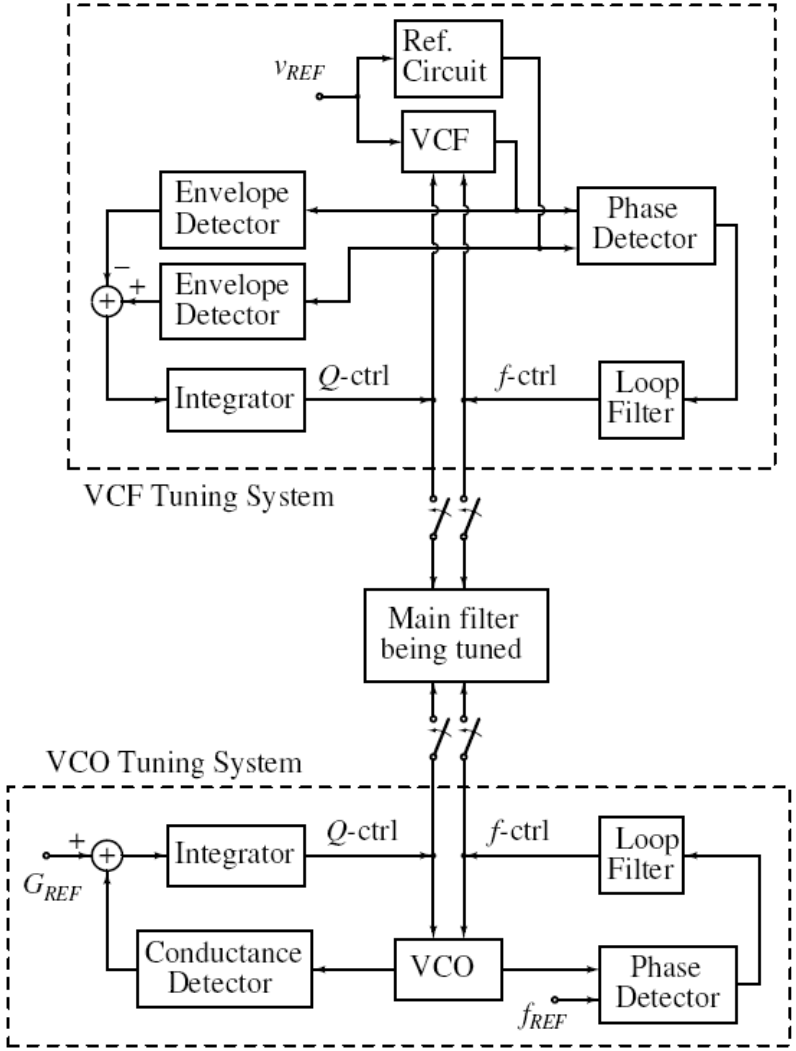
measurement



w/o tuning w/ tuning w/o tuning w/ tuning

Test Chip (UMC 0.18 um CMOS)





Filter Performance summary

Supply voltage	1.5 V
Current	29 mA
Center frequency	6 GHz
Passband ripple	± 2.5 dB
Bandwidth	100 MHz
1-dB compression point	-27.5 dBm
Noise floor	-70.5 dBm
1-dB compression point DR	43 dB
Die area	1.5 x 2 mm^2

Conclusions:

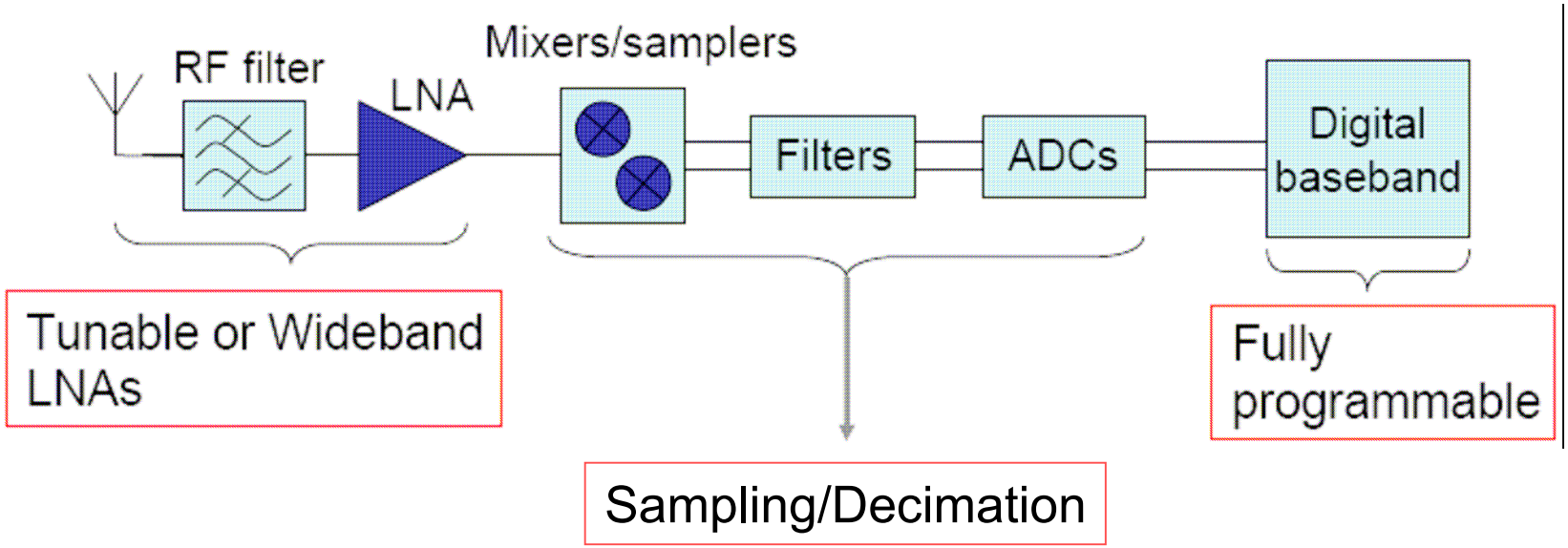
- A straightforward analytical solution to the amplitude control of the Q-enhanced LC resonator. Nonlinearity of the active devices is the key to effective amplitude control.
- With conventional VCO Q-tuning, the tuned filter resonator $|Q|$ is high, but finite, and its value depends on process and configuration the negative conductor.
- A 1.5 V, 6 GHz Q-enhanced LC filter with two types (VCO and VCF) of tuning schemes was implemented using UMC 0.18um standard CMOS process.
- Two effective quality factor tuning schemes, VCO- and VCF-based, of the filter over power supply and process tolerance.
- Problem of coupling neutralization due to the inaccurate magnetic coupling simulation.
- Frequency tuning out of range due to excess on-chip inductor loss.

Sampling receiver

- Introduction: sub-sampling vs. RF sampling
- Passive mixer: voltage mode vs. current mode
- Review of decimation filtering techniques
- Implementation and measurements

Motivation

- Single-chip solution: RF+ABB+DBB
- Reconfigurable multi-standard mobile products => programmability
- Problems and drawbacks found in TI's sampling receiver solution
- Recent innovations on discrete-time decimation filter
- Architecture:



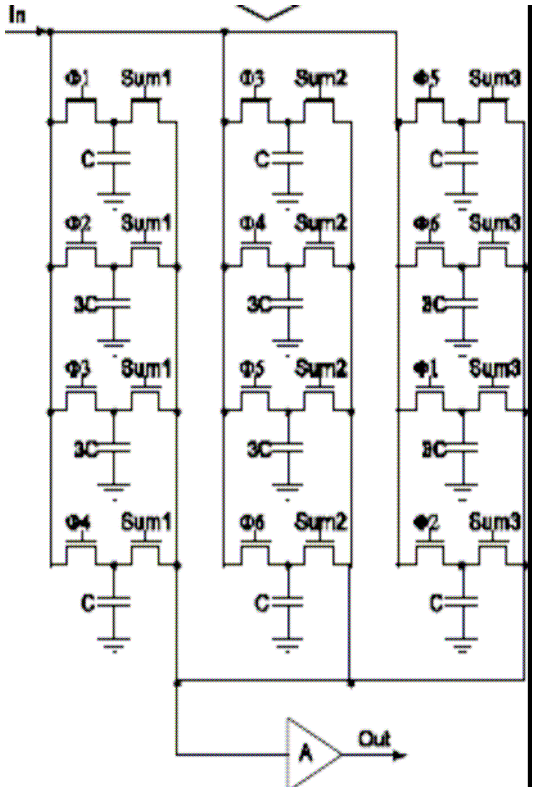
Sub-sampling/band-pass sampling:

- Found in many reported sampling receivers
- Poor noise performance due to noise-folding → solution: RF sampling (higher sampling rate → less noise)

RF sampling

[Linkoping Univ.]

- input: 2.4 GHz
- sampling rate: ~ 3GHz
- output sampling rate: ~ 150 MHz
- Rx front-end NF: ~ 10 dB
- **noise too high for GSM/EDGE applications**

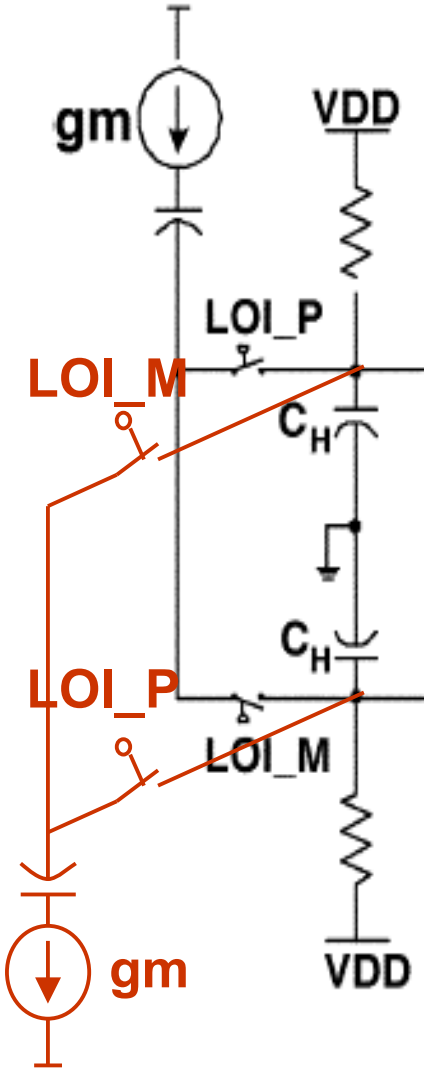


TI's BT/GSM: RF Sampling? – NO!

• Double-balanced switches were not fully shown in TI's publications, but were found in the real circuit.

• C_H is charged and discharged in continuous-time fashion; there are no sampling and holding phases.

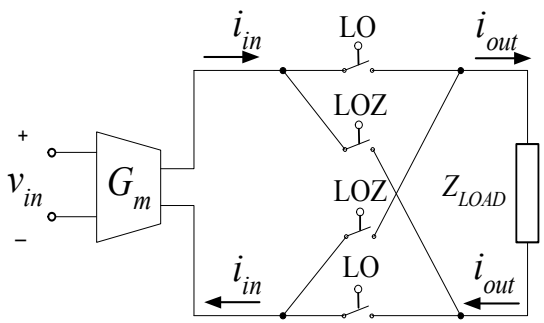
• **It is a current-mode double-balanced passive mixer**.



Passive mixers:

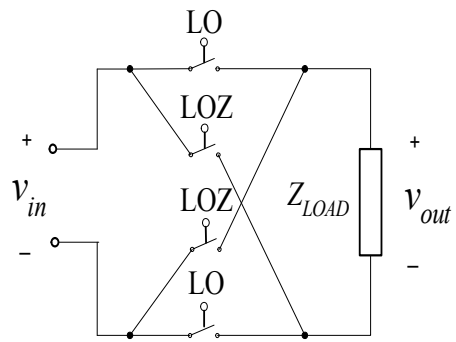
+ low flicker noise than active mixers
+ free of noise-folding compared to sampling mixers

current mode



+ not sensitive to LO jitter
+ output indep. of SW on-resistance
  → do not need large SW
  → SW do not introduce thermal noise
+ can use low impedance load
  → low voltage swing at D/S of SW
  → high linearity and low LO radiation
- need transconductance amplifier
+ high conversion gain as active mixers

voltage mode



- sensitive to LO jitter
- output depends on SW on-resistance
  → need large SW
  → SW introduce thermal noise
- high voltage swing at D/S of SW
  → low linearity and high LO radiation
+ no transconductance amplifier
- low conversion gain (< 0dB)

So, we consider the current-mode passive mixer the best solution.
Direct capacitor loading (TI's solution) is not desirable: low impedance loading → low conversion gain and large capacitors
→ Solution: active loading (opamp with R & C in the feedback path) which also serves as the first stage of IF filter.

Recent innovations on discrete-time decimation filters

- Decimation sampling [Lindfors_TACSII'03]
  sum of N samples → N-tap FIR (low-pass): $H(z) = \sum_{i=1}^{N} z^{1-i}$

- Charge sampling → built-in anti-aliasing [Yuan_ICCMMT'00]
  current-mode S&H → charge sampling and integration
  → sinc response with zero at fs, 2fs, ...

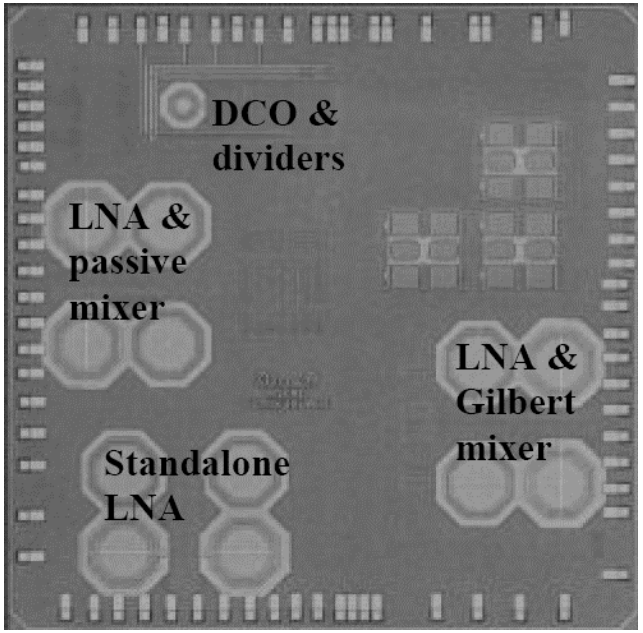
- Embedded FIR functions: real & complex bandpass [Karvonen_Thesis'06]

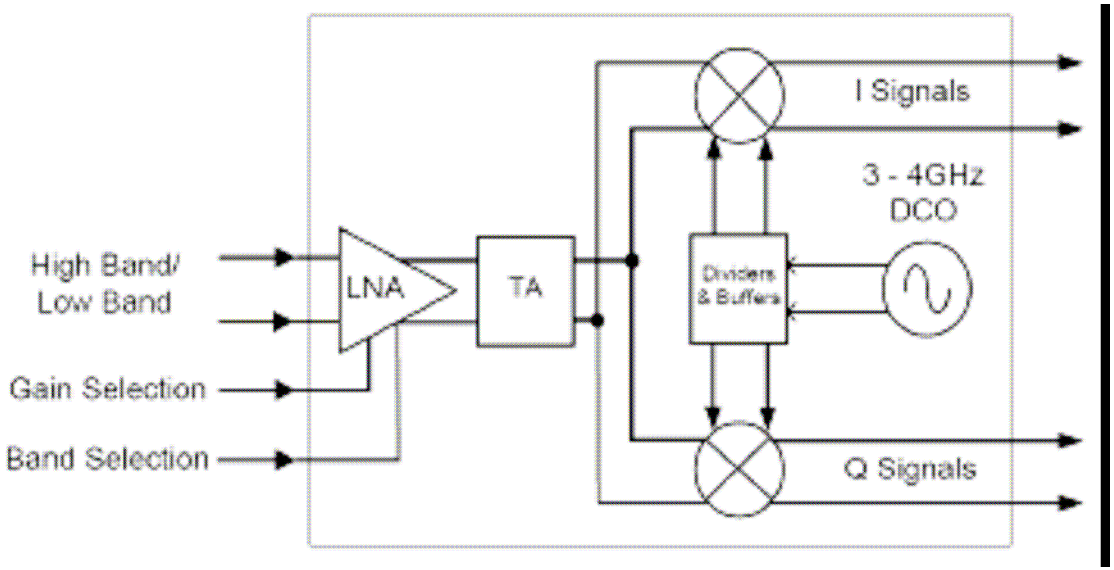
- Cascading and synthesis [Abidi_JSSC'07]
  -- cascaded decimation filter stages to meet system spec.
  -- very simple circuit implementation of the cascaded stages

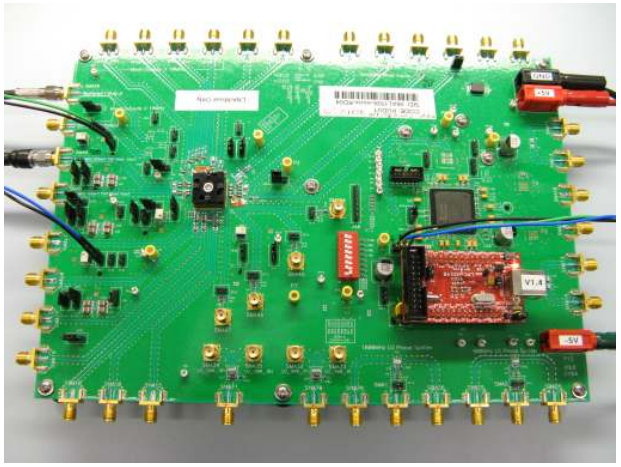
- Gain boosting [Yoshizawa_ISSCC'08]
  -- apply discrete-time MOSFET parametric amp.
  -- filter gain boosted by 20 dB.

Test Chip

- fabricated in 90nm standard digital CMOS
- dual-band LNA
- current-mode passive mixer vs. Gilbert mixer
- one stage of decimation filter
- digitally-controlled osc.







Performance summary

	This work passive mixer	This work Gilbert mixer	Sacchi_ CICC03 (Current-mode)	Valla_ JSSC05 (Current-mode)	Zhou_ JSSC05 (Voltage-mode)
RF frequency (GHz)	0.8 and 1.6		2.2	5	5
Conversion gain (dB)	22	24	29	26	29
DSB noise figure (dB)	4.4	5.1	3.9	3.5	5.3
1/f noise corner (Hz)	70 k	5 M	70 k	200 k	45 k
IIP3 (dBm)	-2	-5	-1	-2	-21
IIP2 (dBm)	30	48	35	24	13
DCO phase noise (dBc/Hz)	-128 @1 MHz offset		N/A	-112 @1MHz offset	N/A
Supply voltage (V)	1.2		1.8	1.2	1.8
Current† (mA)	12	16	8.3	30	7.5
Active area (mm^2)	1.2‡	1.2‡	4.6†	1.8‡	0.8†
Process (μm CMOS)	0.09		0.18	0.13	0.18

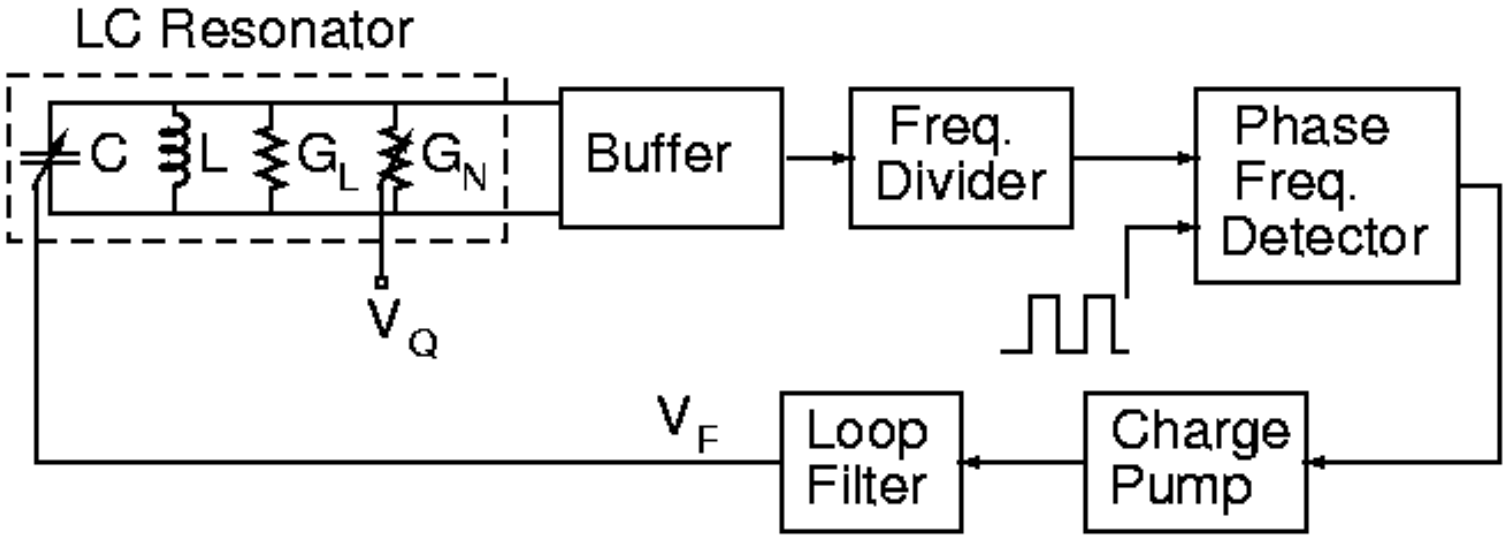
† Without synthesizer. ‡ With synthesizer.

Conclusions

- Direct capacitor loading to the mixer which requires low load impedance results in low conversion gain and large chip area – better to apply active loading with opamp and feedback serving as a first stage of IF filter.
- Capacitor load is not necessary for continuous-time passive mixer since there is no hold phase; in current-mode operation, a capacitor load makes the conversion gain varying with frequency – not desirable.
- Charge-sharing between the mixer and the decimation filter results in 20 dB loss – not desirable.
- Pnoise simulation is not suitable for switch-cap circuits; transient noise simulation in Verilog-AMS predicted noise closer to measurements.

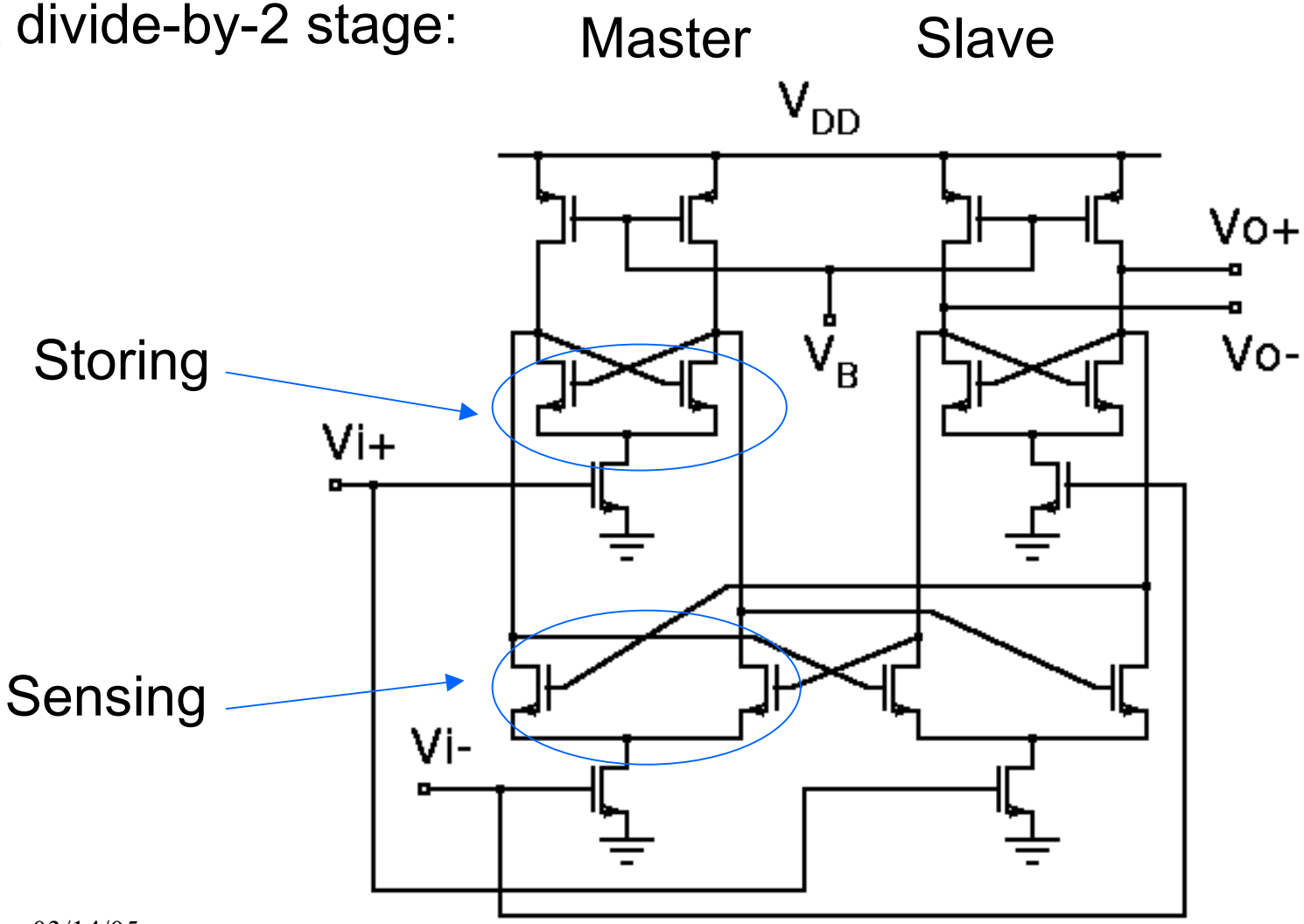
Backup slides

VCO frequency-tuning loop: 3rd-order charge-pump PLL

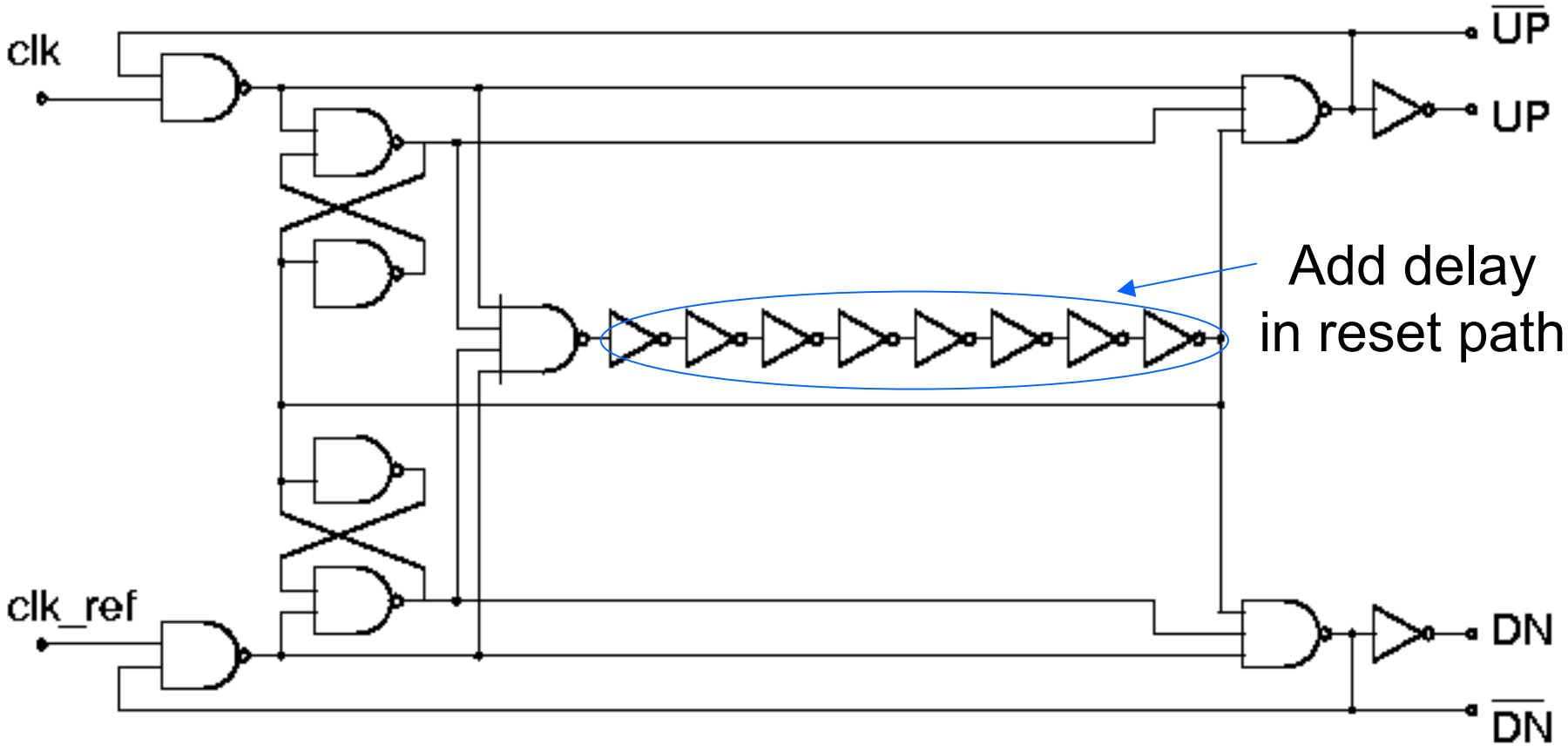
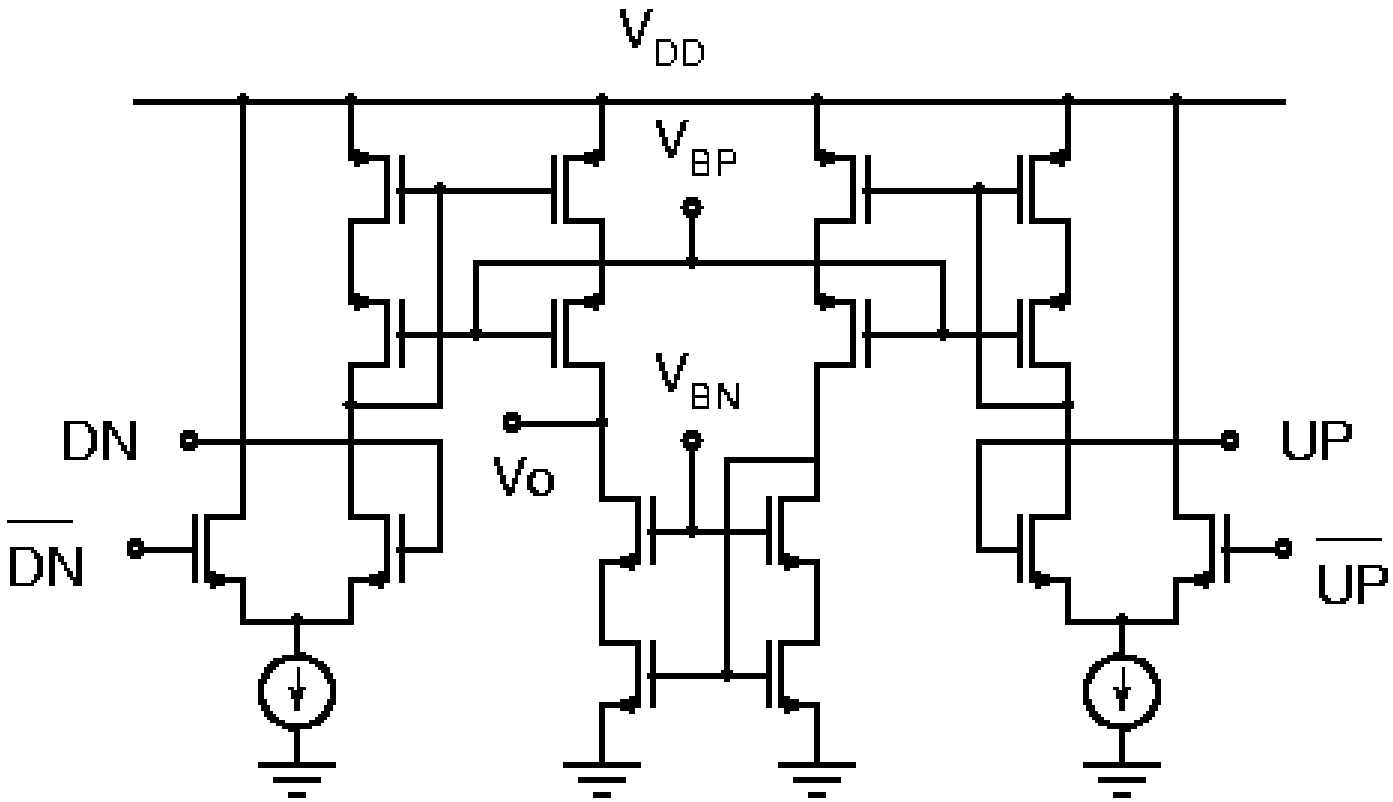


VCF freq-tuning circuitry: frequency divider (six divide-by-2 stages, with scaled sizes)

A divide-by-2 stage:



VCF freq-tuning circuitry: phase-frequency detector



VCF freq-tuning circuitry: charge pump