Integrated $Q$-Enhanced LC Filter with Automatic Tuning And Sampling Receiver

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Outline

\( Q \)-enhanced LC filter with automatic tuning

- Introduction: \( Q \)-enhanced LC filter
- Nonlinear effects of \( Q \)-enhanced LC resonator
- Automatic tuning
- Implementations and measurements

Sampling receiver

- Introduction: sub-sampling vs. RF sampling
- Passive mixer: voltage mode vs. current mode
- Review of decimation filtering techniques
- Implementation and measurements
Motivation

- RF filter is necessary for band selection (and/or image rejection), while most commercial products use off-chip RF filters—bulky and expensive; sometimes introducing matching problems.
- GHz operation facilitates on-chip inductor with reasonable silicon area.

- To integrate RF filters on chip:
  -- Active filters (eg. Gm-C): limited DR and high power consumption at GHz.
  -- Passive LC filter: poor selectivity, due to limited $Q$ of on-chip spiral inductor.
  ⇒ low-power, DR-improved, high-$Q$: $Q$-enhanced LC filter
  ▪ Challenge:
    -- intolerable PVT-induced variation from on-chip passives
  => Automatic tuning is essential to maintain desired filter selectivity.
On-chip spiral inductor

Ground patterned shield:

Differentially driven:

[Yue_98’JSSC]  [Kuhn_95’EL]  [Danesh_02’TMTT]
**$Q$-enhanced LC filter**

Issue: inductor loss does not scale with inductance
=> use same size inductors => coupled-resonator filter

Example: a 4th-order $Q$-enhanced LC filter

- Need automatic tuning to control both the resonant frequency and the quality of each resonator
- Problem: tilting passband, due to in-phase coupling of the inductors => needs coupling neutralization
Coupling neutralization

-Needs accurate modeling.

-Needs extra tuning for coupling.

[D. Li_00'Ph.D thesis]

[Mohieldin_03JSSC]
Nonlinear effect in $Q$-enhanced LC resonator

\[ v = V \sin(\omega t) \]

Weak nonlinearity, differential  \( \Rightarrow \quad i_{G_N} = k_1 v + k_3 v^3 \)

Steady state  \( \Rightarrow \quad W_{diss} / cycle = \int_0^T (i_{G_L} v) dt + \int_0^T (i_{G_N} v) dt = 0 \)

\[ \Rightarrow \quad V^2 \left( G_L + k_1 + \frac{3}{4} k_3 V^2 \right) = 0 \]

Nonlinearity:  \( k_3 \neq 0 \)  \( \Rightarrow \) steady-state amplitude

\[ V = \sqrt{-\frac{4(G_L + k_1)}{3k_3}} \]
Implementation with NMOS transistors

\[ v = \frac{1}{\sqrt{\beta}} \left[ \sqrt{\frac{I_o}{2} - i_{G_N}} - \sqrt{\frac{I_o}{2} + i_{G_N}} \right] \]

\[ \Rightarrow i_{G_N} \approx -\sqrt{\frac{\beta I_o}{2}} v + \sqrt{\frac{\beta^3}{32 I_o}} v^3 \]

Apply to \[ V = \sqrt{-\frac{4(G_L + k_1)}{3k_3}} \]

\[ \Rightarrow \text{Steady-state amp. } V \text{ is a function of bias } I_o \]
Comparison to measurements on 112 kHz breadboard implementation

![Graph showing steady-state amplitude vs. biasing current]

- **Steady-state amplitude** $V$ (V)
- **Biasing current** $I_0$ (mA)

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*Analytic*

*Measurements*
Given the required linear negative conductance \( k_1 \) and bias current \( I_0 \), the active current in the CMOS implementation is more linear than in the NMOS implementation.

\[
k_1 = \left( \sqrt{\beta_p} + \sqrt{\beta_n} \right) \frac{I_0}{2}, \quad k_3 = \sqrt{\beta_p^3 + \beta_n^3} \sqrt{\frac{3}{32 I_0}}
\]

\( k_1 = k_{1, \text{CMOS}} = k_{1, \text{NMOS}} \)

\( I_0 = I_{0, \text{CMOS}} = I_{0, \text{NMOS}} \)

\( \Rightarrow k_{3, \text{CMOS}} < k_{3, \text{NMOS}} \)
Automatic tuning

Indirect tuning (master-slave):

Direct tuning (self-tuning):

Replica type:
- VCF
- VCO

[Tsividis_81'EL]
Conventional VCO $Q$-tuning using magnitude-locked loop:

$V_{ERR} = V - V_{REF}$

$\Rightarrow Q$ of the resonator in the master (VCO) is tuned to infinity;

$\Rightarrow$ But, is $Q$ of the resonator in the slave (filter being tuned) infinite?
Is the tuned $Q$ of the resonators in the filter infinite?

Filter requires good linearity

$\Rightarrow$ filter resonators work with much smaller amplitude than the VCO resonators:

$\Rightarrow G_{N_{\text{filter}}} \approx k_1$

Refer to the VCO resonator Eq. $V^2 \left( G_L + k_1 + \frac{3}{4} k_3 V^2 \right) = 0$

$\Rightarrow Q_{LC_{\text{filter}}} = \frac{1}{G_L + G_{N_{\text{filter}}}} \sqrt{\frac{C}{L}} \approx -\frac{1}{\frac{3}{4} k_3 V_{REF}^2} \sqrt{\frac{C}{L}}$

$\Rightarrow$ The nonlinear part makes the filter resonator different from the VCO resonator

$\Rightarrow$ Finite $Q$ of filter resonator, varying with PVT;

$\Rightarrow V_{REF} \downarrow$ or $k_3 \downarrow \Rightarrow |Q| \uparrow$
Comparison to simulation on a 4.8 GHz NMOS implementation

![Graph showing comparison between analytical and simulated results for a reference resonator and filter resonator, with biasing current as a parameter. The graph includes dashed and dotted lines for analytical and simulated data, respectively, with markers for simulated values of $V$ and $|Q|$.](image-url)
VCO $Q$-tuning using conductance reference  

$Q_{LC_{\text{filter}}} \approx -1/[G_{\text{REF}} \omega_0 L]$  

--- process independent!
Implementation (0.18um CMOS)
Measured filter frequency response w/ VCO $Q$ tuning

Power supply tolerance:

Process tolerance:
VCF $Q$-tuning scheme [S.LI_TCASII06]

Reference circuitry

$G_m R$

Envelope Detector

$V_{REF}$

VCF

Reference LC resonator

$G_m R C L G_L G_N$

Envelope Detector

$V_{ENV}$

$V_{ERR}$

(From frequency tuning loop)

Main Filter (being tuned)

Integrator

$v_C$
Nonidealities

Mismatches, offset of loop integrator, accuracy of envelope detector, interference with frequency tuning, etc.

\[ Q_{LC,all} = \frac{1}{Q_{LC,mismatches}} + \frac{1}{Q_{LC,offset}} + \frac{1}{Q_{LC,freq-error}} \]

\[ \approx R \sqrt{\frac{C}{L}} \left( \delta_G + \delta_R + \delta_{KED} + \delta_{V_{OS}} + \left[ 1 - \sqrt{1 - (2 \frac{R}{\omega_0 L} \delta_{\omega})^2} \right] \right) \]
VCF Q-tuning circuitry:
envelope detector, comparator and integrator

Diff. -> single-end

Integrate io -> v_Q

Squarer

Set I_{REF}
Simulated and measured filter frequency response w/ VCF $Q$ tuning

- Simulation
  - w/o tuning
  - w/ tuning

- Measurement
  - w/o tuning
  - w/ tuning
Test Chip (UMC 0.18 um CMOS)
### Filter Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Current</td>
<td>29 mA</td>
</tr>
<tr>
<td>Center frequency</td>
<td>6 GHz</td>
</tr>
<tr>
<td>Passband ripple</td>
<td>± 2.5 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>100 MHz</td>
</tr>
<tr>
<td>1-dB compression point</td>
<td>-27.5 dBm</td>
</tr>
<tr>
<td>Noise floor</td>
<td>-70.5 dBm</td>
</tr>
<tr>
<td>1-dB compression point DR</td>
<td>43 dB</td>
</tr>
<tr>
<td>Die area</td>
<td>1.5 x 2 mm²</td>
</tr>
</tbody>
</table>
Conclusions:

• A straightforward analytical solution to the amplitude control of the $Q$-enhanced LC resonator. Nonlinearity of the active devices is the key to effective amplitude control.

• With conventional VCO $Q$-tuning, the tuned filter resonator $|Q|$ is high, but finite, and its value depends on process and configuration the negative conductor.

• A 1.5 V, 6 GHz $Q$-enhanced LC filter with two types (VCO and VCF) of tuning schemes was implemented using UMC 0.18um standard CMOS process.

• Two effective quality factor tuning schemes, VCO- and VCF-based, of the filter over power supply and process tolerance.

• Problem of coupling neutralization due to the inaccurate magnetic coupling simulation.

• Frequency tuning out of range due to excess on-chip inductor loss.
Sampling receiver

- Introduction: sub-sampling vs. RF sampling
- Passive mixer: voltage mode vs. current mode
- Review of decimation filtering techniques
- Implementation and measurements
Motivation

- Single-chip solution: RF+ABB+DBB
- Reconfigurable multi-standard mobile products => programmability
- Problems and drawbacks found in TI’s sampling receiver solution
- Recent innovations on discrete-time decimation filter
- Architecture:
Sub-sampling/band-pass sampling:

- Found in many reported sampling receivers
- Poor noise performance due to noise-folding → solution: RF sampling (higher sampling rate → less noise)

RF sampling
[Linkoping Univ.]
- input: 2.4 GHz
- sampling rate: ~ 3GHz
- output sampling rate: ~ 150 MHz
- Rx front-end NF: ~ 10 dB
- noise too high for GSM/EDGE applications
TI’s BT/GSM: RF Sampling? – NO!

• Double-balanced switches were not fully shown in TI’s publications, but were found in the real circuit.

• $C_H$ is charged and discharged in continuous-time fashion; there are no sampling and holding phases.

• It is a current-mode double-balanced passive mixer.
**Passive mixers:**
+ low flicker noise than active mixers
+ free of noise-folding compared to sampling mixers

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**current mode**

- not sensitive to LO jitter
- output indep. of SW on-resistance
  - do not need large SW
  - SW do not introduce thermal noise
- can use low impedance load
  - low voltage swing at D/S of SW
  - high linearity and low LO radiation
- no transconductance amplifier
- high conversion gain as active mixers

**voltage mode**

- sensitive to LO jitter
- output depends on SW on-resistance
  - need large SW
  - SW introduce thermal noise
- high voltage swing at D/S of SW
- low linearity and high LO radiation
- no transconductance amplifier
- low conversion gain (< 0dB)

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So, we consider the current-mode passive mixer the best solution.
Direct capacitor loading (TI’s solution) is not desirable: low impedance loading → low conversion gain and large capacitors
→ Solution: active loading (opamp with R & C in the feedback path) which also serves as the first stage of IF filter.
Recent innovations on discrete-time decimation filters

- Decimation sampling [Lindfors_TACSII'03]
  \[ H(z) = \sum_{i=1}^{N} z^{1-i} \]
  sum of N samples → N-tap FIR (low-pass):

- Charge sampling → built-in anti-aliasing [Yuan_ICCMMT'00]
  current-mode S&H → charge sampling and integration
  → sinc response with zero at fs, 2fs, ...

- Embedded FIR functions: real & complex bandpass [Karvonen_Thesis’06]

- Cascading and synthesis [Abidi_JSSC’07]
  -- cascaded decimation filter stages to meet system spec.
  -- very simple circuit implementation of the cascaded stages

- Gain boosting [Yoshizawa_ISSCC’08]
  -- apply discrete-time MOSFET parametric amp.
  -- filter gain boosted by 20 dB.
Test Chip

- fabricated in 90nm standard digital CMOS
- dual-band LNA
- current-mode passive mixer vs. Gilbert mixer
- one stage of decimation filter
- digitally-controlled osc.
# Performance summary

<table>
<thead>
<tr>
<th></th>
<th>This work passive mixer</th>
<th>This work Gilbert mixer</th>
<th>Sacchi_ CICC03</th>
<th>Valla_ JSSC05</th>
<th>Zhou_ JSSC05</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF frequency (GHz)</td>
<td>0.8 and 1.6</td>
<td>2.2</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Conversion gain (dB)</td>
<td>22</td>
<td>24</td>
<td>29</td>
<td>26</td>
<td>29</td>
</tr>
<tr>
<td>DSB noise figure (dB)</td>
<td>4.4</td>
<td>5.1</td>
<td>3.9</td>
<td>3.5</td>
<td>5.3</td>
</tr>
<tr>
<td>1/f noise corner (Hz)</td>
<td>70 k</td>
<td>5 M</td>
<td>70 k</td>
<td>200 k</td>
<td>45 k</td>
</tr>
<tr>
<td>IIIP3 (dBm)</td>
<td>-2</td>
<td>-5</td>
<td>-1</td>
<td>-2</td>
<td>-21</td>
</tr>
<tr>
<td>IIIP2 (dBm)</td>
<td>30</td>
<td>48</td>
<td>35</td>
<td>24</td>
<td>13</td>
</tr>
<tr>
<td>DCO phase noise (dBc/Hz)</td>
<td>-128 @1 MHz offset</td>
<td>N/A</td>
<td>-112 @1 MHz offset</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.2</td>
<td>1.8</td>
<td>1.2</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>Current† (mA)</td>
<td>12</td>
<td>16</td>
<td>8.3</td>
<td>30</td>
<td>7.5</td>
</tr>
<tr>
<td>Active area (mm²)</td>
<td>1.2³</td>
<td>1.2³</td>
<td>4.6⁺</td>
<td>1.8⁺</td>
<td>0.8⁺</td>
</tr>
<tr>
<td>Process (µm CMOS)</td>
<td>0.09</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
<td></td>
</tr>
</tbody>
</table>

† Without synthesizer.  
⁺ With synthesizer.
Conclusions

- Direct capacitor loading to the mixer which requires low load impedance results in low conversion gain and large chip area – better to apply active loading with opamp and feedback serving as a first stage of IF filter.
- Capacitor load is not necessary for continuous-time passive mixer since there is no hold phase; in current-mode operation, a capacitor load makes the conversion gain varying with frequency – not desirable.
- Charge-sharing between the mixer and the decimation filter results in 20 dB loss – not desirable.
- Pnoise simulation is not suitable for switch-cap circuits; transient noise simulation in Verilog-AMS predicted noise closer to measurements.
Backup slides
VCO frequency-tuning loop: 3\textsuperscript{rd}-order charge-pump PLL
VCF freq-tuning circuitry: frequency divider (six divide-by-2 stages, with scaled sizes)

A divide-by-2 stage: Master Slave

Storing

Sensing

\[ V_{DD} \]

\[ V_{B} \]

\[ V_{i+} \]

\[ V_{o+} \]

\[ V_{o-} \]
VCF freq-tuning circuitry: phase-frequency detector

Add delay in reset path
VCF freq-tuning circuitry: charge pump