Overview

Part I: TDC Circuits
- Applications
- Predominant architectures
- Characteristics
- Hardware implementation in FPGA
- Results
- Conclusion

Part II: Analog to Digital Converter (ADC) circuits
- ADC state of the art
- Predominant architectures
- TDC based ADC Architecture
- PMT pulse processing using TDC based ADC
- Conclusion
Part I: TDC Circuits

- Applications
- Architectures
- Characteristics
- Implementation in FPGA
- Results
- Conclusion
Part I: TDC Applications

[L.L. Ruckman, G.S. Varner 2009]
Part I: TDC Circuits

- Applications
- Architectures
  - Tapped delay line (TDL)
  - Vernier delay line (VDL)
  - Cyclic TDC
  - Two ring oscillator based self calibrating TDC
- Characteristics
- Implementation in FPGA
- Results
- Conclusion
TDC Architectures. Tapped Delay Line
Vernier Delay Line
Cyclic TDC
Two Ring Oscillator Topology
Self Calibration Scheme
Two Ring Oscillator Topology

\[ T_S = n_w T_1 + \Delta \]
\[ \Delta = n_2 (T_1 - T_2) \]
\[ T_1 = \frac{2T_{Slarge}}{n_{1large} - n_{2large} + n_{wlarge}} \]
\[ T_2 = \frac{n_{1small}T_1 - T_{Ssmall}}{n_{2small}} \]
Part I: TDC Circuits

- Applications
- Architectures
- Characteristics
- Implementation in FPGA
- Results
- Conclusion
TDC Characteristics

\[ DNL = T_W (Q_{m+1}) - T_W (Q_m) - 1LSB \]

\[ b_m = 2^m + \varepsilon_m \]

Non-ideal weighting of the \( m^{th} \) bit where \( \varepsilon_m \) is the error of the \( m^{th} \) bit

\[ INL = \Delta_{N-1} = \frac{2^{N-1}}{2^N - 1} \sum_{m=0}^{N-1} \varepsilon_m - \varepsilon_{N-1} \]

\[ SNR = 6.02N + 1.76dB \]

Causes:
- Cell to Cell Delay Variations
- Routing Delay Variations
- Clock Jitter

PLASSCHE, R., V-DE., 2003
TDC Characteristics, Analytical expressions

\[
T_{out} = T_{in} \left(1 + \text{INL}(\text{LSB})\right)
\]

\[
n_{\text{reduction}} = \left( \frac{\log(1 + 3 \times \text{INL}^2)}{2 \log 2} \right)
\]

\[
\text{ENOB} = N - n_{\text{reduction}}
\]

\[
\text{FOM}_{\text{TDC}} = \frac{\left( P_{\text{coarse}} + P_{\text{fine}} \right) t_r}{2 \left( \text{ENOB}_{\text{fine}} + N_{\text{coarse}} \right)}
\]

\[
\text{SINAD} = \frac{P_S}{P_{\text{NAD}}} = \sqrt{1.5 \left(2^N\right)^2 \frac{-\log(1 + 3 \times \text{INL}^2)}{2 \log 2}}
\]
Effect of noise on ring oscillator

Ali Hajimiri et.al, IEEE journal of solid-state circuits, vol. 34, no. 6, june 1999
Analytical expression for phase noise/clock jitter in ring oscillators

\[
\sigma_{\Delta \phi}^2 = \frac{\Gamma_{\text{rms}}^2 \bar{i}_n^2 / \Delta f}{2q_{\text{max}}^2} \Delta T
\]

\[
\Gamma_{\text{rms}} = \sqrt{\frac{2\pi^2}{3\eta^2}} \frac{1}{N^{1.5}}
\]

Ali Hajimiri et.al, IEEE journal of solid-state circuits, vol. 34, no. 6, June 1999
Part I: TDC Circuits

- Applications
- Architectures
- Characteristics
- Implementation in FPGA
- Results
- Conclusion
Why TDC implementation in FPGAs?

- Commercially available, cost effective
- Versatile with high speed digital logic and high density of programmable Logic Array Blocks (LAB)
- Low voltage differential signaling (LVDS) I/O provides high speed comparators for unconventional analog processing usage
- Ubiquitous in data acquisition chain for digital signal processing
- Faster turn around times from concept to design
FPGA based TDC and Signal Processing Module (TSPM)
TSPM Specifications

- Serves up to 24 TDC/ADC channels and expandable
- 2 Gigabit/sec transmitter links
- 1 Gigabit/sec receiver link
- 24 Time to digital converters, with a very wide input dynamic range (limited only by the number of bits in a counter)
- Suitable for Time of Flight, Coincidence spectroscopy applications
- Virtually deadtime less with more than 1 Millions/sec singles rate with less than 1% deadtime
- Based on Altera Stratix II devices
Part I: TDC Circuits

- Applications
- Architectures
- Characteristics
- Hardware Implementation in FPGA
- Results
  - Tapped delay line (TDL)
  - Two ring oscillators
- Conclusion
TDL-TDC Characterization Using Pulser. Reported resolution=625 ps
TDL based TDC in use in RatCAP: Coincidence timing spectrum for 1 RatCAP pair

FWHM = 7.3489 ns
Part I: TDC Circuits

- Applications
- Architectures
- Characteristics
- Hardware Implementation in FPGA
- Results
  - Tapped delay line
  - Two ring oscillators
- Conclusion
Calibration results

- $T_{slarge} = 1\ \text{us}$
  - $T_1 = 1.160\ \text{ns} \pm 0.1\%$
- $T_{ssmall} = 3\ \text{ns}$
  - $T_2 = 1.119\ \text{ns} \pm 0.1\%$
- $T_r = T_1 - T_2 = 41\ \text{ps}$
TDC output code histogram

![Graph showing TDC output code histogram with various input pulse widths in nanoseconds.](image-url)
TDC Transfer Function

Input pulse width ns

Output code ns

Ideal
Real
Clock transition nonlinearity corrected TDC output versus event number
Integral Nonlinearity Error in TDC
Temperature Dependence of Ring oscillator Periods

T1 and T2 in ns

Temperature in deg C

T1

T2
Temperature Dependence of TDC resolution

Temperature in deg C

Resolution Tr in

Temperature coefficient of 2.5 ps/deg C
Conclusion

- TDC resolutions of 625 ps and 40 ps are achieved using Altera Stratix II FPGAs
- INL < 1 LSB and DNL < 0.5 LSB is observed for both TDL and two ring oscillator technique
- Excellent linearity over wide dynamic range
- Vernier techniques achieve sub 100 ps resolution, and hits a limit at around 20-40 ps
- Sub 10 ps resolution regime should be explored in ASICs unless better control over FPGA design tools is available in near future
Part II: ADC circuits

- ADC state of the art
  - Effect of technology scaling
- Predominant ADC architectures
- TDC based ADC Architecture
- PMT pulse processing using TDC based ADC
- Conclusion
ADC Block Diagram

BANDGAP REFERENCE

VREF

CLOCK fs (≥ 2 x Nyquist Rate)

ANALOG INPUT VIN

N BIT QUANTIZER

DIGITAL OUTPUT

ERROR (INPUT - OUTPUT)

N-bit DIGITAL OUTPUT
Technology Scaling Impact on Analog Design

- Gate oxide thickness ↓ => Gate tunneling current ↑
- Early Voltage (VA) Reduction ↓
- Dynamic Range ↓
**S/H Circuit**

![S/H Circuit Diagram]

$$H_{OL} = \left(1 + \frac{1}{\frac{G_{OL}}{\text{Openloop-Gain} - 1}}\right) \times \frac{1}{1 + p \frac{2\zeta}{\omega_n} + \frac{p^2}{\omega_n^2}}$$

- $\zeta$ is the S/H damping factor
- $\omega_n$ is the S/H natural frequency

$$G_{OL} = g_m (r_{o2} \parallel r_{o4}) \ast (-g_m (r_{o7} \parallel r_{o8}))$$

- $r_o \propto 1/\lambda$
- $r_o \propto V_A$

**Operational Amplifier**

**NIELSEN, H., J., et al., 2005**

Brookhaven Science Associates
Technology Dependence of Droop Rate

For 90 nm Technology, 1 V Dynamic Range, 13 Bit, 10 MSPS ADC, LSB = 0.12 mV

\[ V_{droop} = 10^3 V \times 100 \text{ns} \]

\[ V_{droop} = 0.1 mV \]

Bandgap Reference

HÄNSLER, K., et al., 2003
Part II: ADC circuits

- ADC State of the art
- ADC Architectures
  - Comparison and suitability for deep submicron
- TDC based Analog to Digital Converter (ADC) Architecture
- PMT Pulse Processing using FPGAs
- Conclusion
Predominant ADC Architectures

- FLASH
- SAR
- FOLDING
- SIGMA DELTA
- PIPELINED
## Comparison

<table>
<thead>
<tr>
<th>Conversion</th>
<th>FLASH</th>
<th>SAR</th>
<th>Σ ∆</th>
</tr>
</thead>
<tbody>
<tr>
<td>N bits - $2^N - 1$ Comparators, Resistors, Caps increase by a factor of 2 for each bit.</td>
<td>Binary search algorithm, internal circuitry runs higher speed.</td>
<td>Oversampling ADC, Digital Decimation Filter</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Encoding</th>
<th>Thermometer Code Encoding</th>
<th>Successive Approximation</th>
<th>Over-Sampling Modulator, Digital Decimation Filter</th>
</tr>
</thead>
</table>

<p>| Disadvantages | Bubble codes / metastability, high power consumption, large size | May require anti-aliasing filter. Slow conversion | Higher order (4th order or higher) - multibit ADC and multibit feedback DAC. Strict stability requirements. OTA in integrator stages and S/H |</p>
<table>
<thead>
<tr>
<th>Conversion Time</th>
<th><strong>FLASH</strong></th>
<th><strong>SAR</strong></th>
<th><strong>Σ Δ</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>High speed. Not dependant on N</td>
<td>Increases linearly with increased resolution. Can be offset by using high speed clock in deep submicron</td>
<td>Tradeoff between data output rate and noise free resolution</td>
</tr>
<tr>
<td>Resolution</td>
<td>Limited to 8 bit maximum due to resistor matching, area and power concern. High N=&gt; High cap=&gt;Slow speed</td>
<td>Passive components matching better in deep submicron. Matching requirement double with every bit increase in N</td>
<td>Component matching requirements double with every bit increase in N</td>
</tr>
<tr>
<td>Size</td>
<td>$2^N - 1$ comparators, power increases exponentially with N</td>
<td>Die increases linearly with increase in resolution.</td>
<td>Core die size will not change with increase in N</td>
</tr>
</tbody>
</table>
SAR: Choice for deep Sub Micron

- Ease of implementation
- Low power
- Reliance on passive component matching
- No OTA needed. S/H OTA can be combined in Charge Redistribution type DAC
- High clock speed can offset for N+1 cycle conversion time
- Stable BGR needed
ADC State of the art (F=1/Figure of Merit)

Best case

$F = 5.5 \times 10^{12}$

Part II: ADC circuits

- ADC State of the art
- ADC Architectures
- TDC based Analog to Digital Converter (ADC) Architecture
- PMT Pulse Processing using FPGAs
- Conclusion
TDC based ADC Topology
Nonlinearities: DNL and INL. SNR

\[ DNL = A_{input}(Q_{m+1}) - A_{input}(Q_m) - 1LSB \]

\[ INL = \Delta_{N-1} = \frac{2^{N-1}}{2^N - 1} \sum_{m=0}^{N-1} \varepsilon_m - \varepsilon_{N-1} \]

\[ SNR = 6.02N + 1.76dB \]

Causes:
- Cell to Cell Delay Variations
- Routing Delay Variations
- Clock Jitter
Altera Cyclone family LVDS Comparator AC response
Quantizer (Comparator) performance

\[ p_i = \frac{2V_L}{A_0q} e^{-\frac{t}{\tau}} \]

\( p_i \) is the probability that the comparator will yield ambiguous output.

\( V_L = \) Threshold for the digital gate at the comparator output = 0.6

\( A_0 = \) Open loop comparator gain ≈ 32

\( q = \) Quantization step ≈ 2.5/2^{15}

\( t = \) Comparison time ≈ 10 ns

\( \tau = 1/2 \pi f_{3dB} \)

\( f_{3dB} = \) 3dB bandwidth of the comparator ≈ 100 MHz

Example case of Altera Cyclone device LVDS comparator

\( p_i = 1.02 \times 10^{-6} \)

Part II: ADC circuits

- ADC State of the art
- ADC Architectures
- TDC based Analog to Digital Converter (ADC) Architecture
- Application: PMT Pulse Processing using FPGA
- Conclusion
Battery operated, signal chain for PMT Pulse Processing using FPGA based TDC and ADC (MARIACHI experiment)
PMT Output and corresponding ToT comparator response
Simulated PMT output charge vs LVDS comparator output

\[ y = 0.9698x - 0.2538 \]

\[ R^2 = 0.9829 \]
ADC resolution vs input charge, Simulated

<table>
<thead>
<tr>
<th>Input Charge in pC</th>
<th>ADC # of Bits N</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>2</td>
<td>15.5</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
</tr>
<tr>
<td>6</td>
<td>16.5</td>
</tr>
</tbody>
</table>

- ADC: Analog-to-Digital Converter
VTC based ADC power dissipation

\[ P_{ADC} = P_S/\eta + P_{VTC} + P_{TDC} \]

Where \( P_{VTC} \) and \( P_{TDC} \) can be calculated from inverter power dissipation formula and number of inverter stages. For VTC, \( n=1 \) and for TDC \( n=2^N \) where \( N=\) Number of bits

\[ P_{VTC/TDC} = 2 \times n \times P_{inv} = 2(P_{dyn} + P_{dp} + P_{stat}) \]

\[ P_{dyn} = C_L V_{DD}^2 f_s \]

\[ P_{dp} = V_{DD} I_{peak} \left( \frac{t_r + t_f}{2} \right) f_s \]

\[ P_{stat} = V_{DD} I_{leak} \]
Example case TDC based ADC Figure of Merit

\[ FOM_{ADC} = \frac{P_{ADC}}{2^{\text{ENOB}} \cdot f} \]

Example case of proposed ADC

ENOB \approx 15, \ f_s = 1 \text{ MHz} \ (\text{using} \ 20 \text{ ns TDC deadtime, multiple VTH}),

C_L = 10 \text{ fF}, \ V_{DD} = 1.8 \text{ V}

FOM \approx 0.048 \text{ pJ}

1/FOM \approx 21 \times 10^{12} \text{ J}^{-1}
Conclusion

- TDC based ADC architecture is a way of the future as technology feature size shrinks
- FPGA based ADC architecture promises a resolution close to 15 bits using ToT method
- FOM for such ADC surpasses state of the art by an order of magnitude
- Future work involves detailed hardware implementation of ADC
- Real-time ToT PMT Pulse processing algorithms need to be developed for the architecture to be meaningful in practice
References

- MOTA, M., et al., October 1999, A high-resolution time interpolator based on a delay locked loop and an RC delay line, IEEE J. Solid-State Circuits vol. 34 no. 10 pp. 1360–1366
- O’CON OR, P., 2006, Noise and Power Tradeoffs in Electronics Front End, VI international meeting on front end electronics
Acknowledgements

- Veljko Radeka
- Pavel Rehak
- Gianluigi De’Geronimo
- Jack Fried
- Joe Mead
- Kevin Wolniewicz
- Ron Ryan
- Ron Angona
- Howard Hansen
- John Triolo
- RatCAP group
- Funding agency: DOE Contract DE-AC02-98CH10886
Excuse

शतेषु जायते शूरः सहस्रेष्ठु च पंडितः।
वक्ता दशसहस्रेष्ठु दाता भवति वानवा ॥

Shateshu jaayate shoora(h) sahastreshu cha pundit (ah)|
Vakta dasha sahastreshu daata bhavati vanava ॥

In hundreds one finds a brave; a pundit in thousands, a (good) speaker in ten thousands and seldom or never one finds a (generous) donor.
Thank You!