Time to Digital Converter Circuits

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Overview

Part I: TDC Circuits

- Applications
- Predominant architectures
- Characteristics
- Hardware implementation in FPGA
- Results
- Conclusion

Part II: Analog to Digital Converter (ADC) circuits

- ADC state of the art
- Predominant architectures
- TDC based ADC Architecture
- PMT pulse processing using TDC based ADC
- Conclusion

Part I: TDC Circuits

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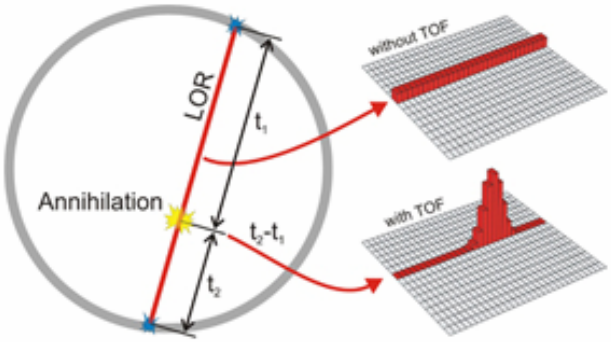
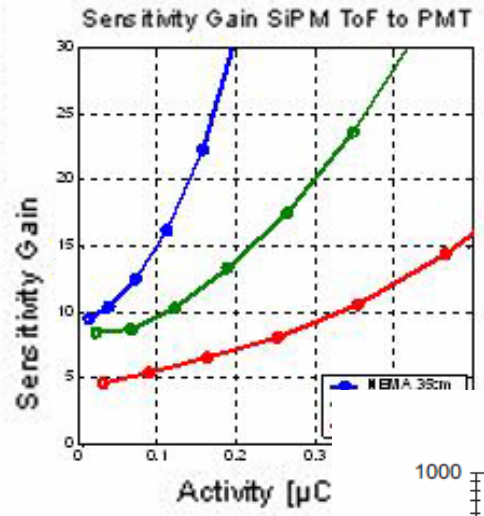
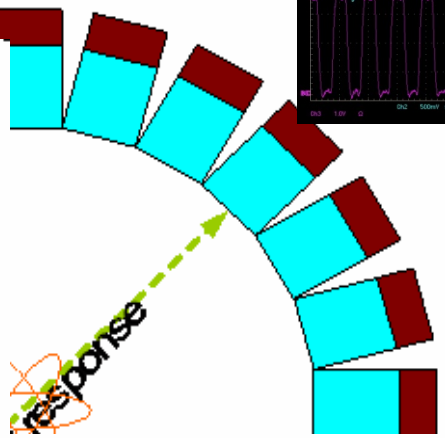
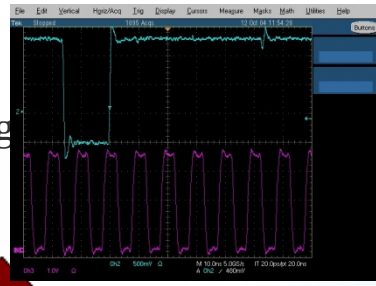
Part I: TDC Applications

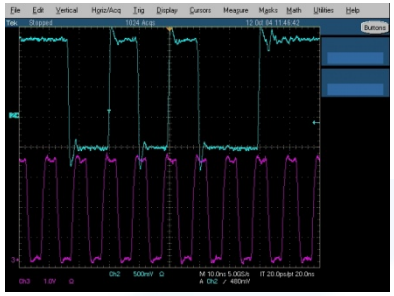
http://www.hybrid-pet-mr.eu/uploads/pics/ToF_principle_and_effective_sensitivity_gain.jpg











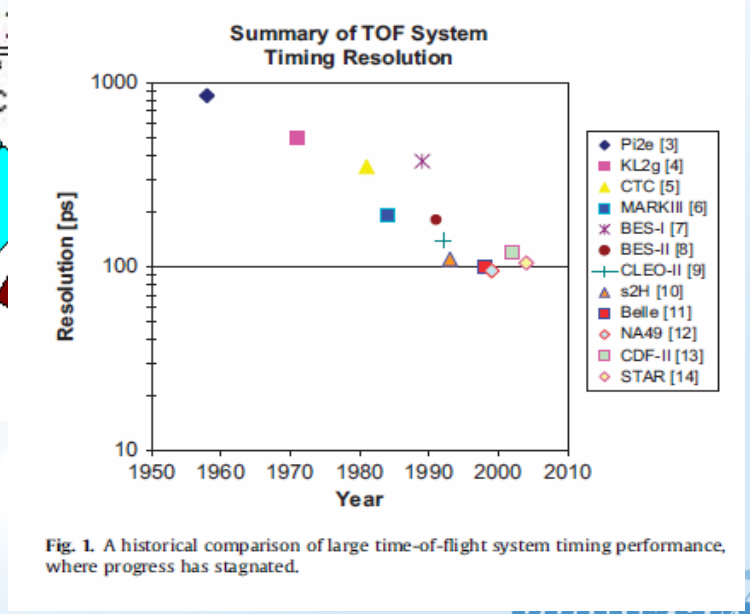


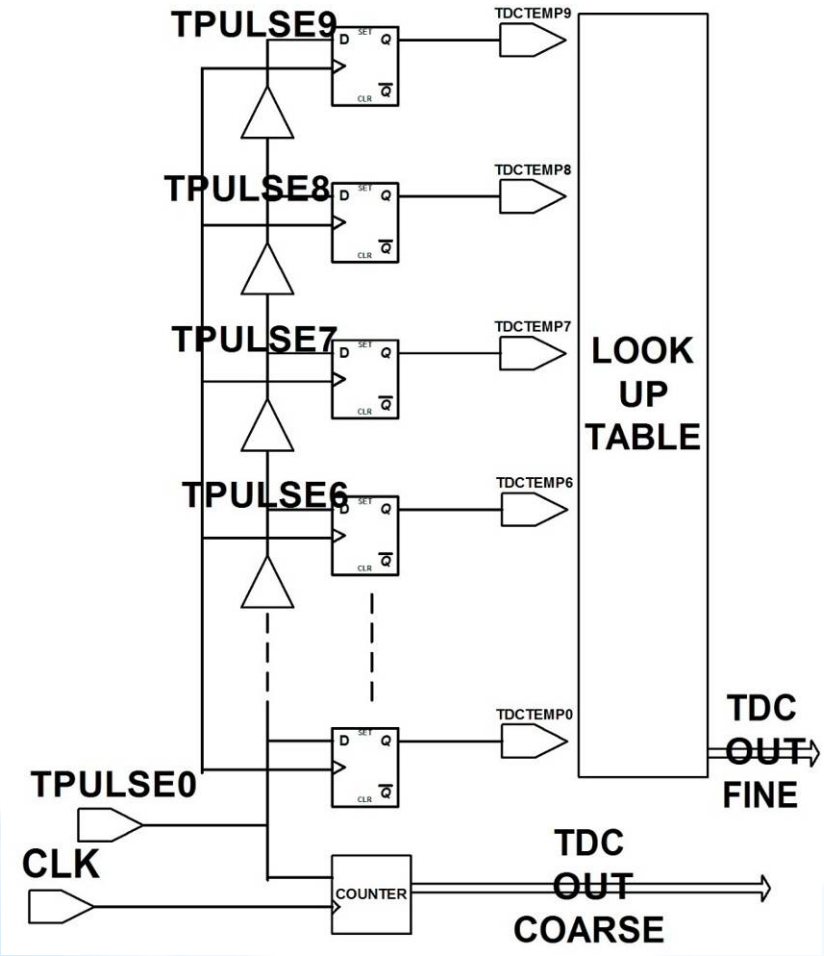
Fig. 1. A historical comparison of large time-of-flight system timing performance, where progress has stagnated.

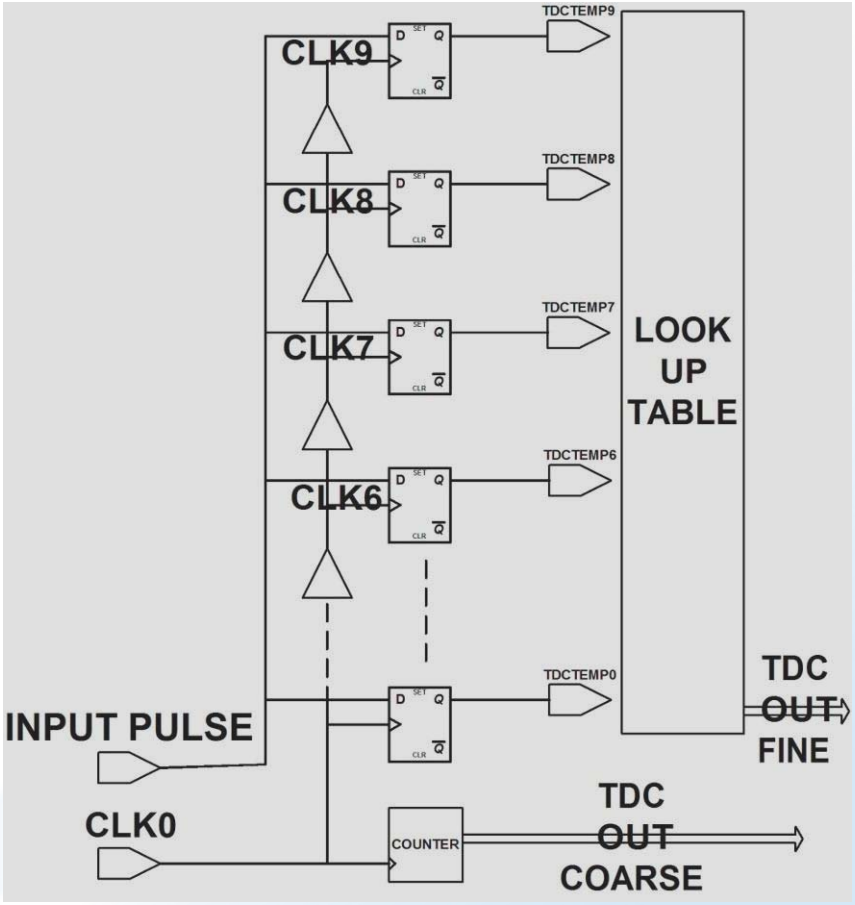
[L.L. Ruckman, G.S. Varner 2009]

Part I: TDC Circuits

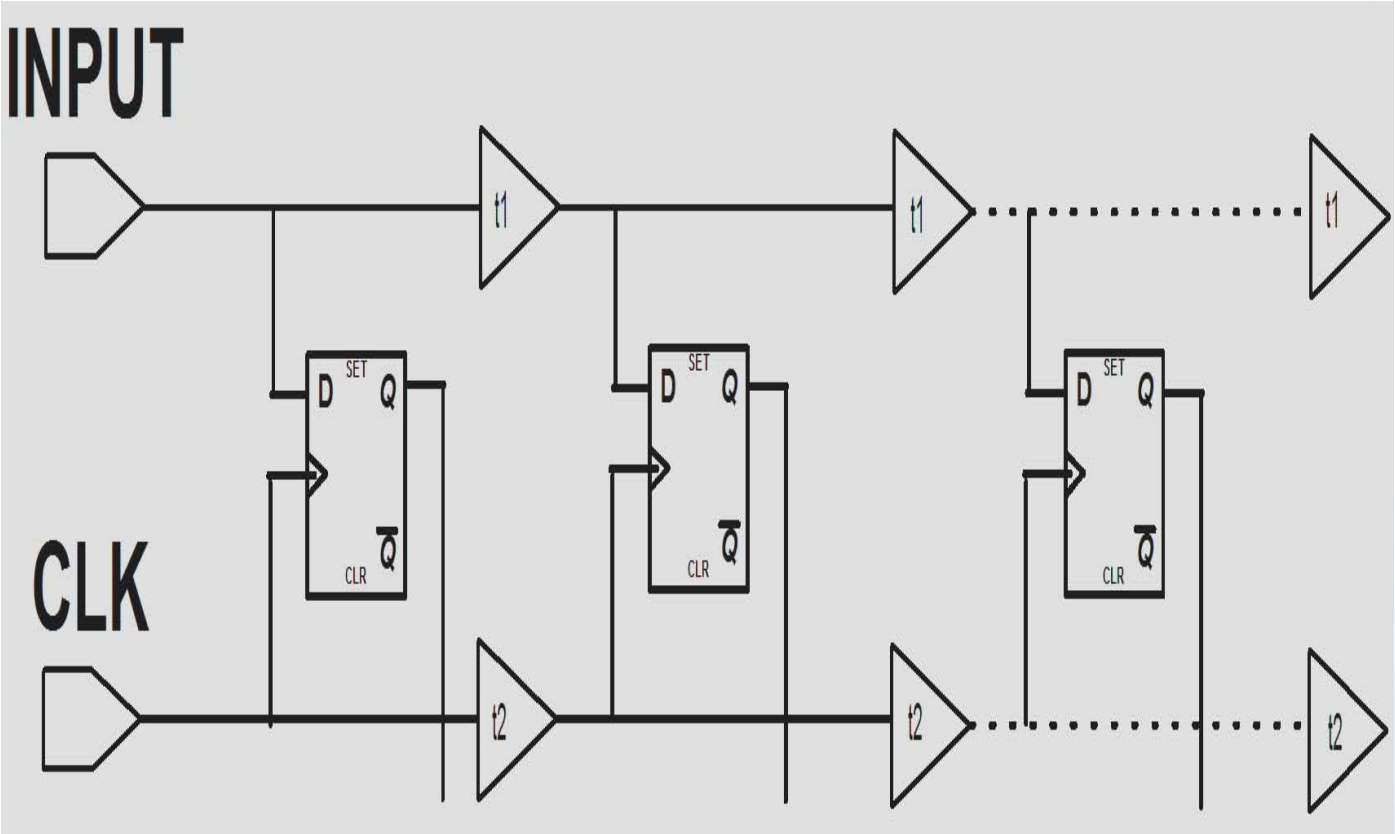
- Applications
- Architectures
  - Tapped delay line (TDL)
  - Vernier delay line (VDL)
  - Cyclic TDC
  - Two ring oscillator based self calibrating TDC
- Characteristics
- Implementation in FPGA
- Results
- Conclusion

TDC Architectures. Tapped Delay Line

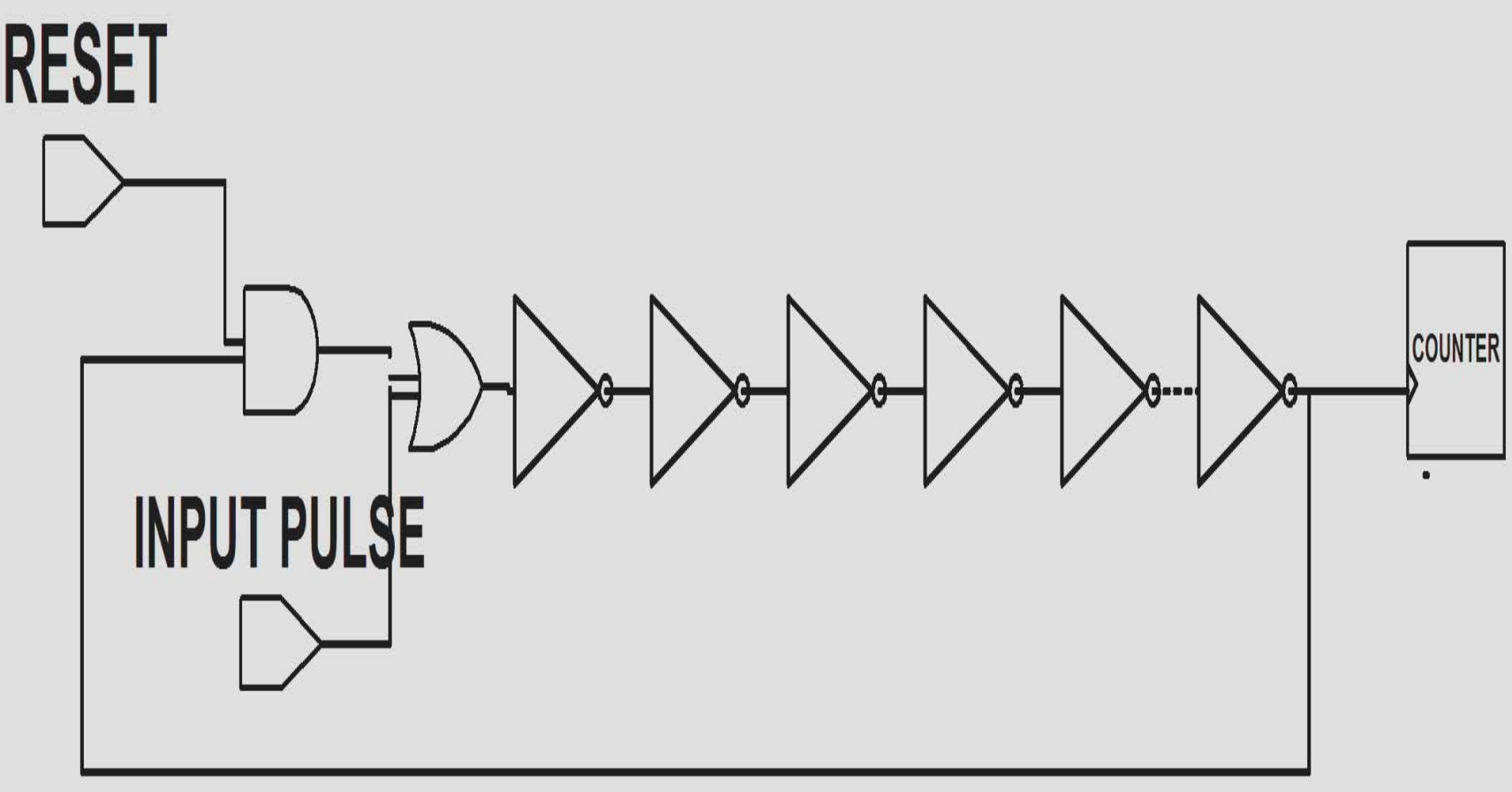




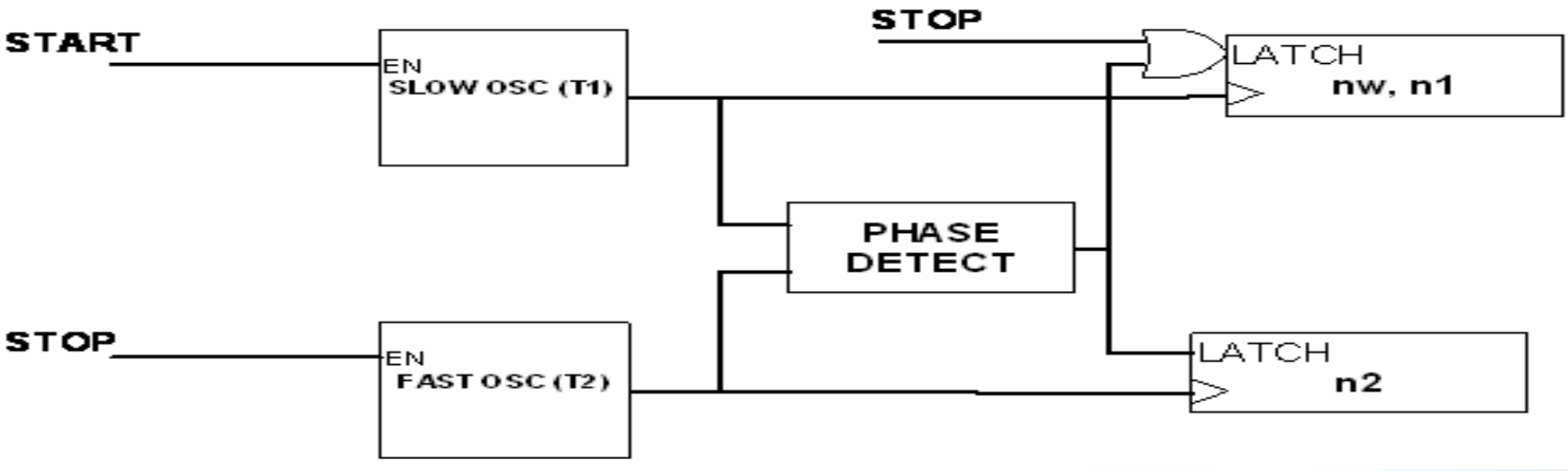
Vernier Delay Line

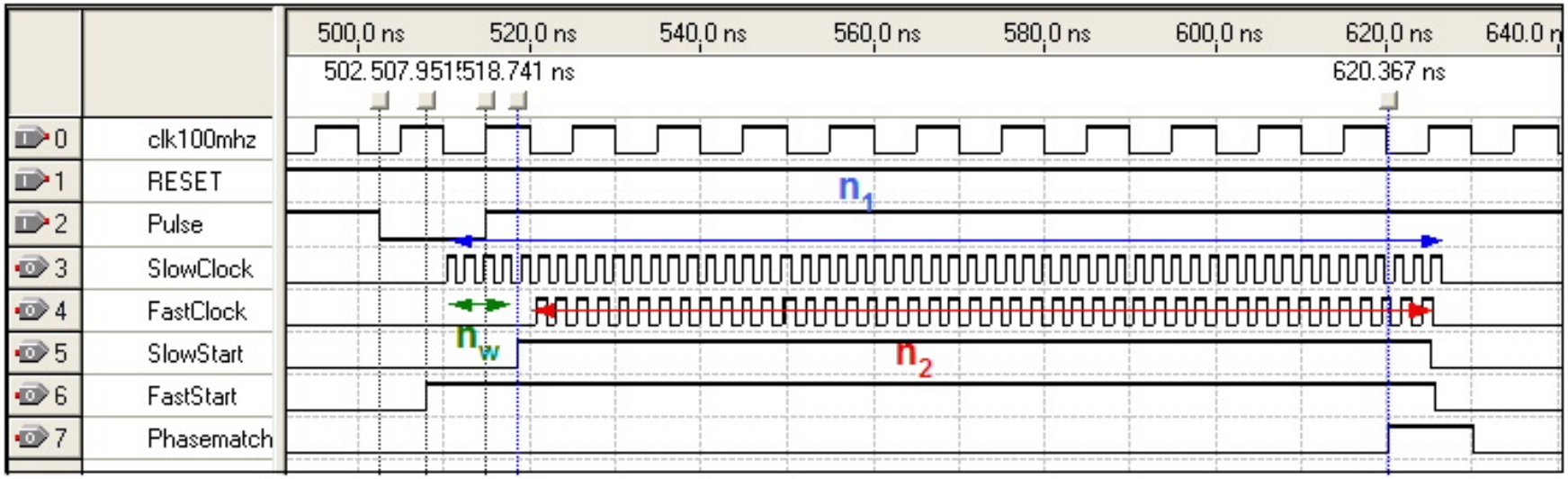


Cyclic TDC



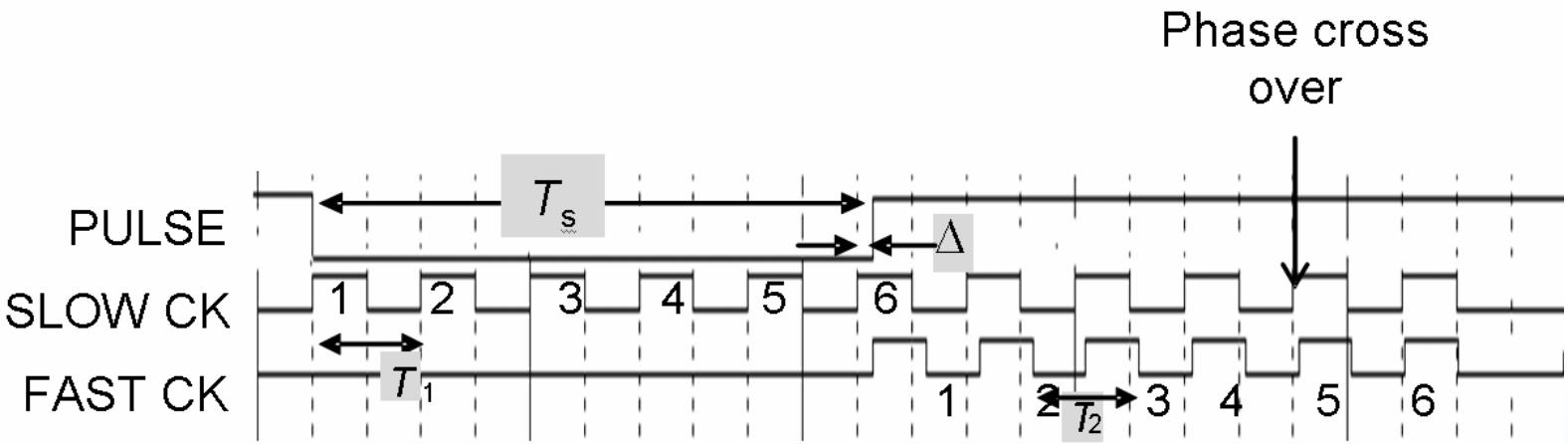
Two Ring Oscillator Topology





Self Calibration Scheme

Two Ring Oscillator Topology



$$T_S = n_w T_1 + \Delta$$

$$\Delta = n_2 (T_1 - T_2)$$

$$T_1 = \frac{2T_{Slarge}}{n_{1large} - n_{2large} + n_{wlarge}}$$

$$T_2 = \frac{n_{1small} T_1 - T_{Ssmall}}{n_{2small}}$$

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TDC Characteristics

$$DNL = T_W(Q_{m+1}) - T_W(Q_m) - 1LSB$$

$$b_m = 2^m + \varepsilon_m$$

Non-ideal weighting of the mth bit where ε_m is the error of the mth bit

$$INL = \Delta_{N-1} = \frac{2^{N-1}}{2^N - 1}\sum_{m=0}^{N-1}\varepsilon_m - \varepsilon_{N-1}$$

$$SNR = 6.02N + 1.76dB$$

PLASSCHE, R.,V-DE.,2003

Causes:

Cell to Cell Delay Variations

Routing Delay Variations

Clock Jitter

TDC Characteristics, Analytical expressions

$$T_{out} = T_{in}\left(1 + INL(LSB)\right)$$

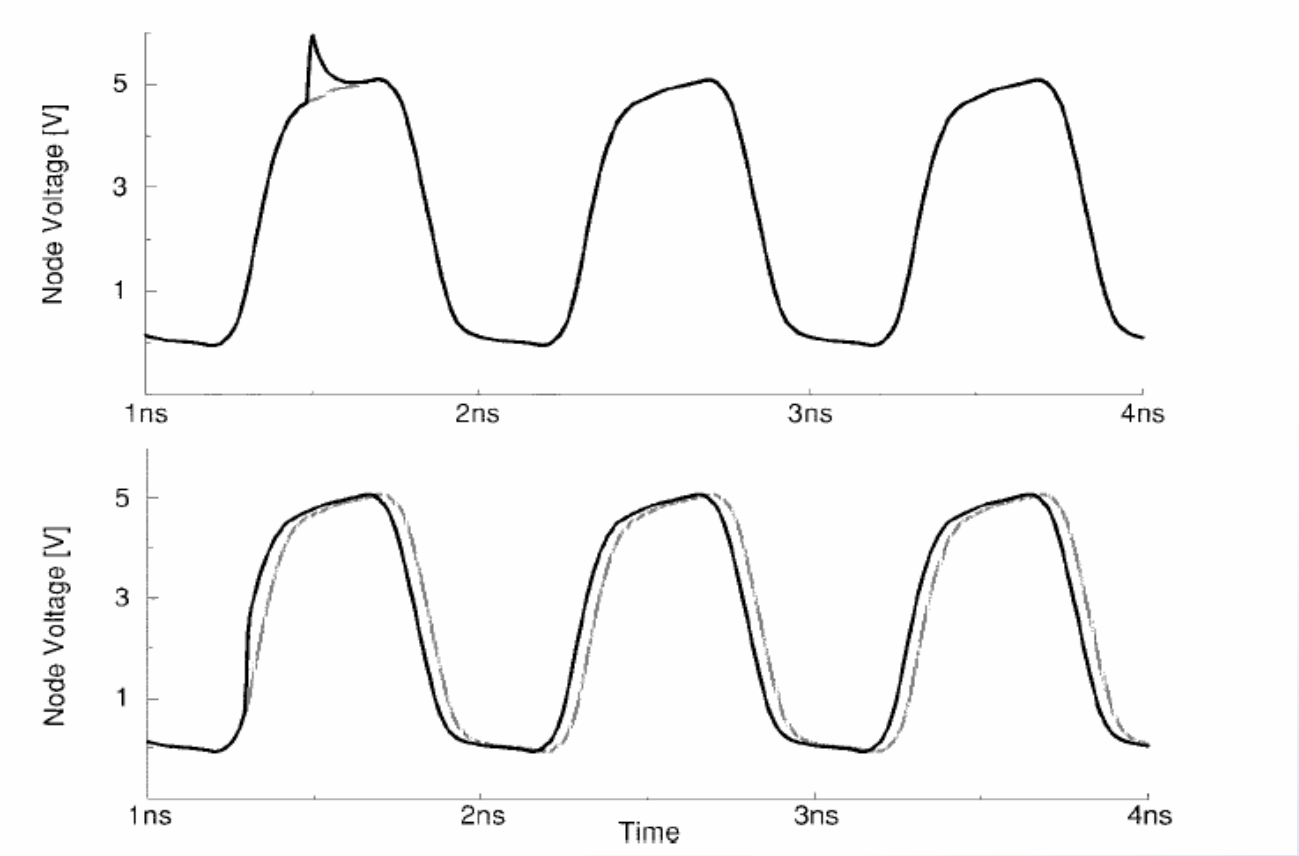
$$n_{reduction} = \left(\frac{\log(1 + 3 \times INL^2)}{2\log 2}\right)$$

$$ENOB = N - n_{reduction}$$

$$FOM_{TDC} = \frac{(P_{coarse} + P_{fine}).t_r}{2^{\left(ENOB_{fine} + N_{coarse}\right)}}$$

$$SINAD = \frac{P_S}{P_{NAD}} = \sqrt{1.5}(2^N)2^{-\frac{\log(1+3\times INL^2)}{2\log 2}}$$

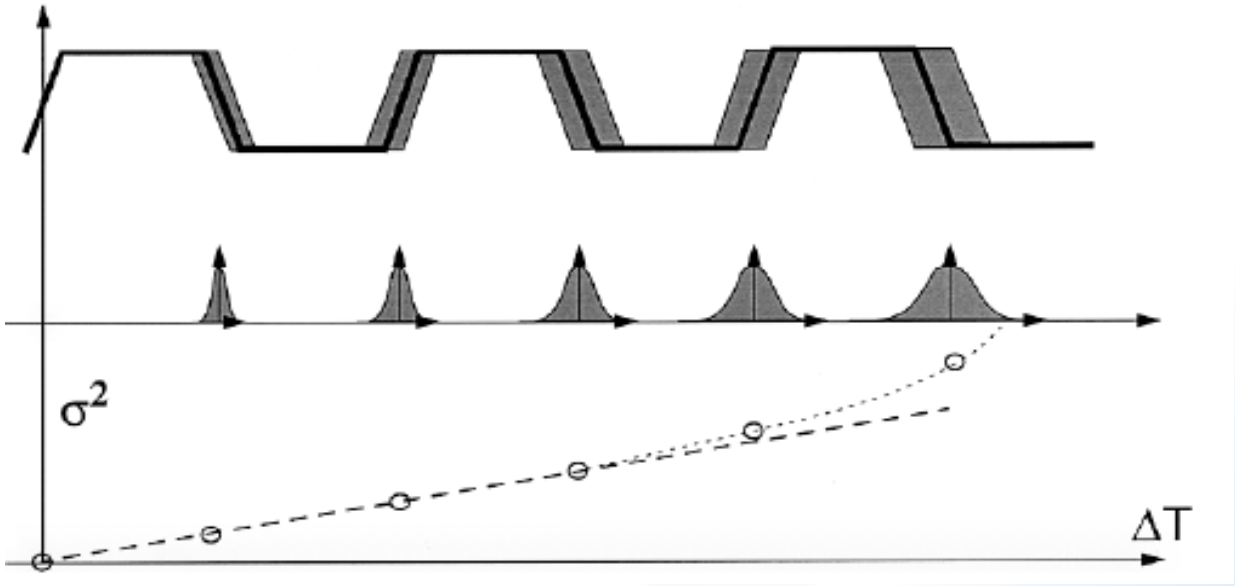
Effect of noise on ring oscillator



Ali Hajimiri et.al, IEEE journal of solid-state circuits, vol. 34, no. 6, june 1999

Analytical expression for phase noise/clock jitter in ring oscillators

$$\sigma_{\Delta\phi}^2 = \frac{\Gamma_{rms}^2 \bar{i}_n^2 / \Delta f}{2q_{\max}^2} \Delta T \qquad \Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^2}} \frac{1}{N^{1.5}}$$



Ali Hajimiri et.al, IEEE journal of solid-state circuits, vol. 34, no. 6, June 1999

Part I: TDC Circuits

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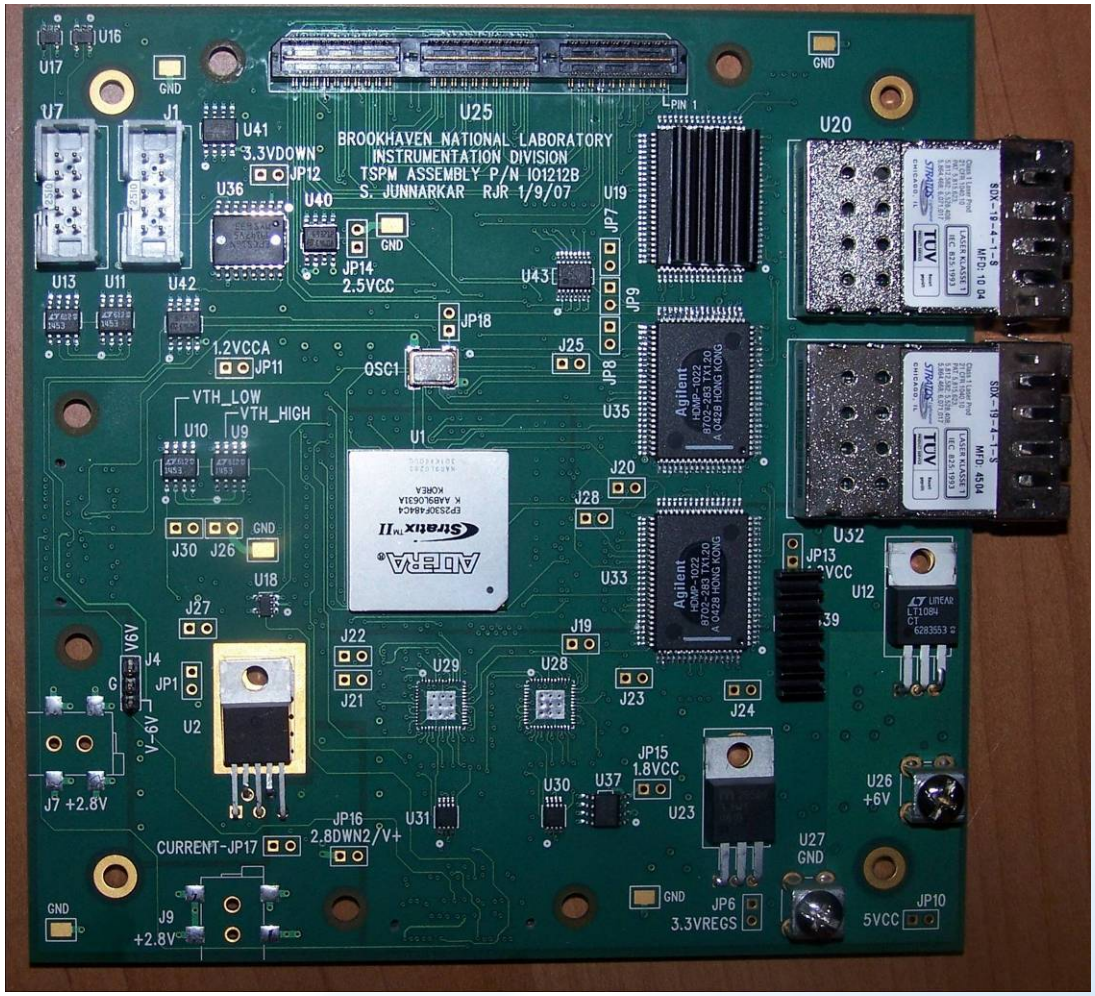
Why TDC implementation in FPGAs?

- Commercially available, cost effective
- Versatile with high speed digital logic and high density of programmable Logic Array Blocks (LAB)
- Low voltage differential signaling (LVDS) I/O provides high speed comparators for unconventional analog processing usage
- Ubiquitous in data acquisition chain for digital signal processing
- Faster turn around times from concept to design

FPGA based TDC and Signal Processing Module (TSPM)

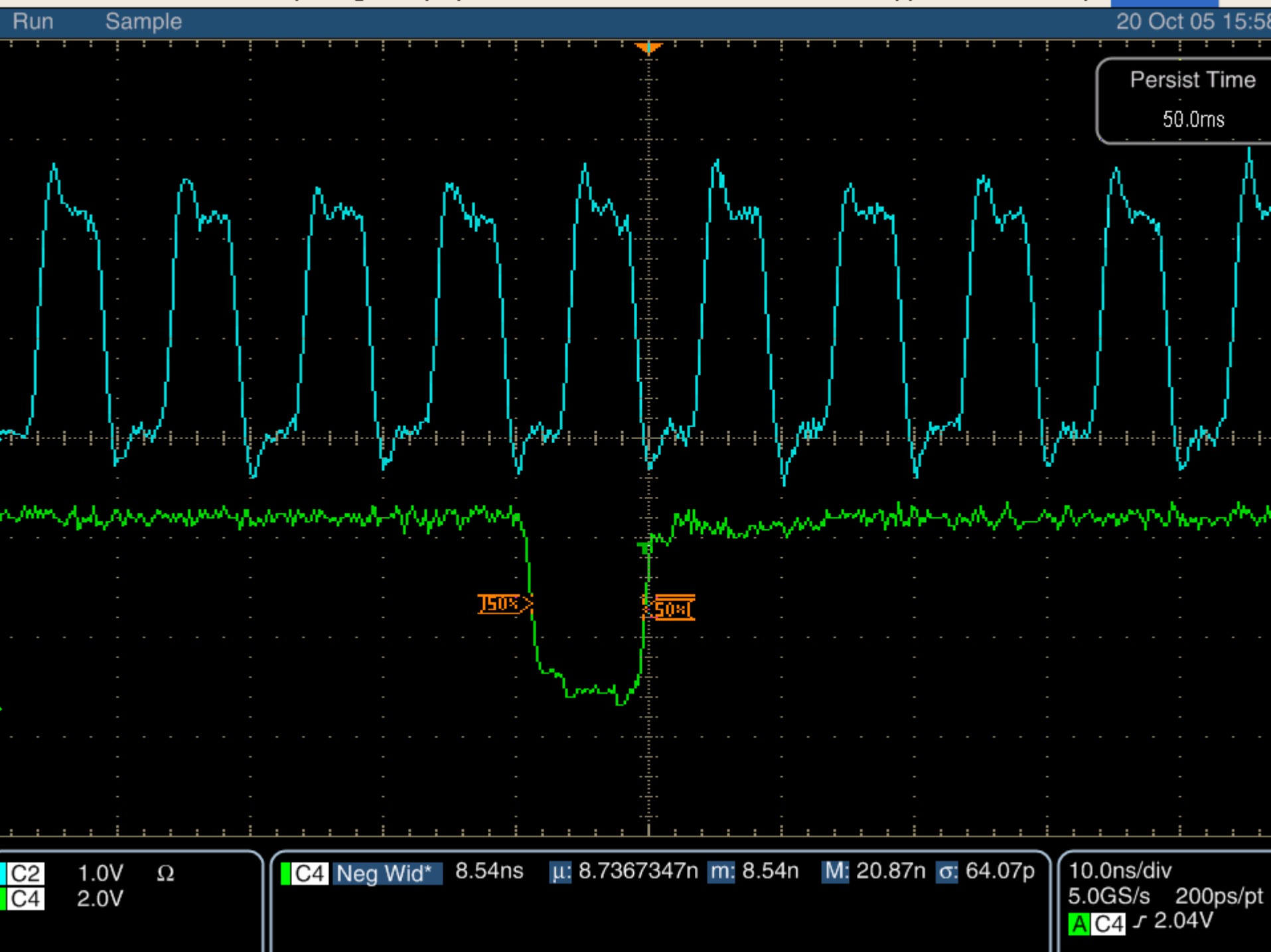
4.5”



4.5”

TSPM Specifications

- Serves upto 24 TDC/ADC channels and expandable
- 2 Gigabit/sec transmitter links
- 1 Gigabit/sec receiver link
- 24 Time to digital converters, with a very wide input dynamic range (limited only by the number of bits in a counter)
- Suitable for Time of Flight, Coincidence spectroscopy applications
- Virtually deadtime less with more than 1 Millions/sec singles rate with less than 1% deadtime
- Based on Altera Stratix II devices


Run
Sample
20 Oct 05 15:58
Persist Time
50.0ms
50%
50%
C2 1.0V Ω
C4 2.0V
C4 Neg Wid* 8.54ns μ: 8.7367347n m: 8.54n M: 20.87n σ: 64.07p
10.0ns/div
5.0GS/s 200ps/pt
A C4 2.04V

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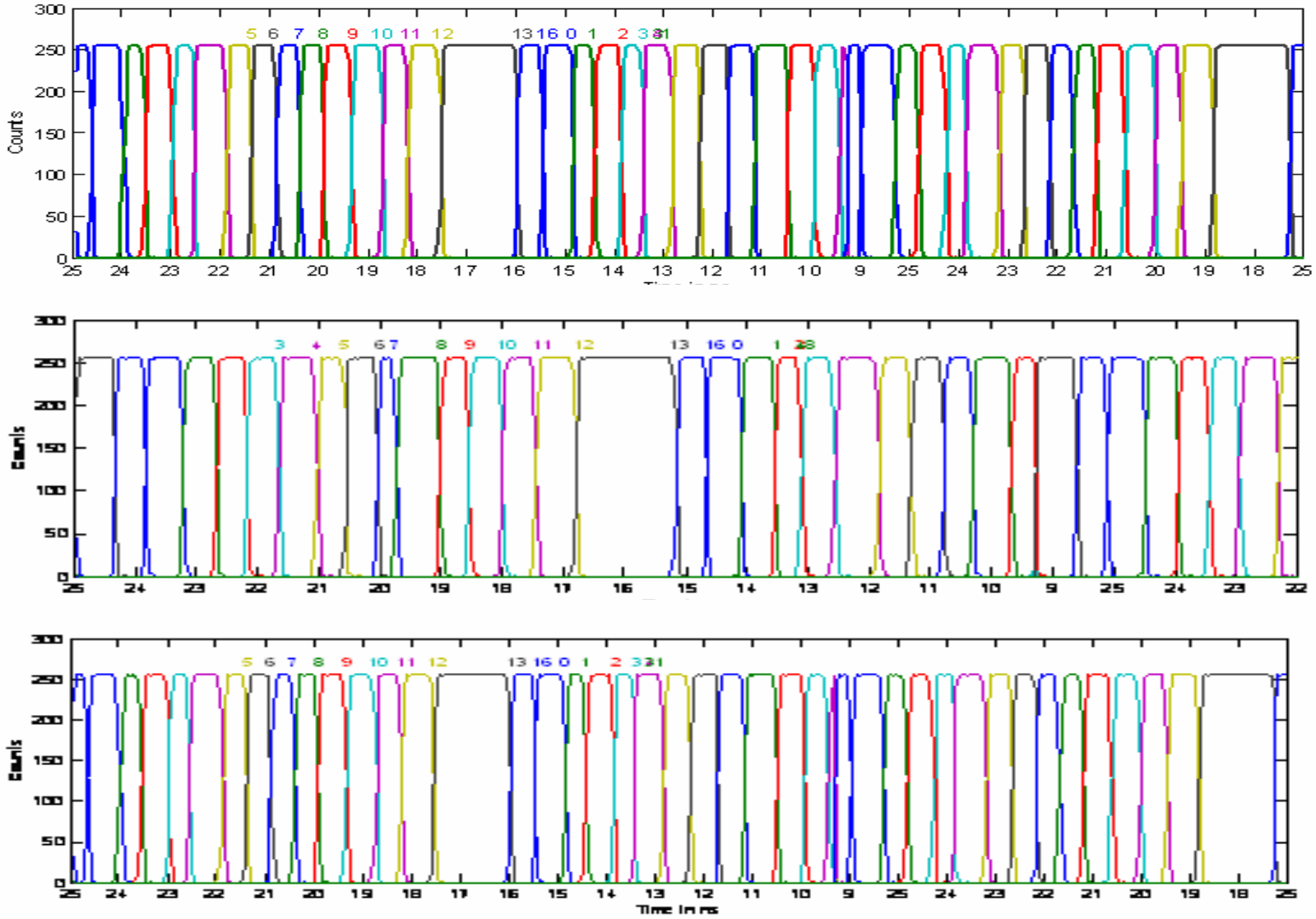
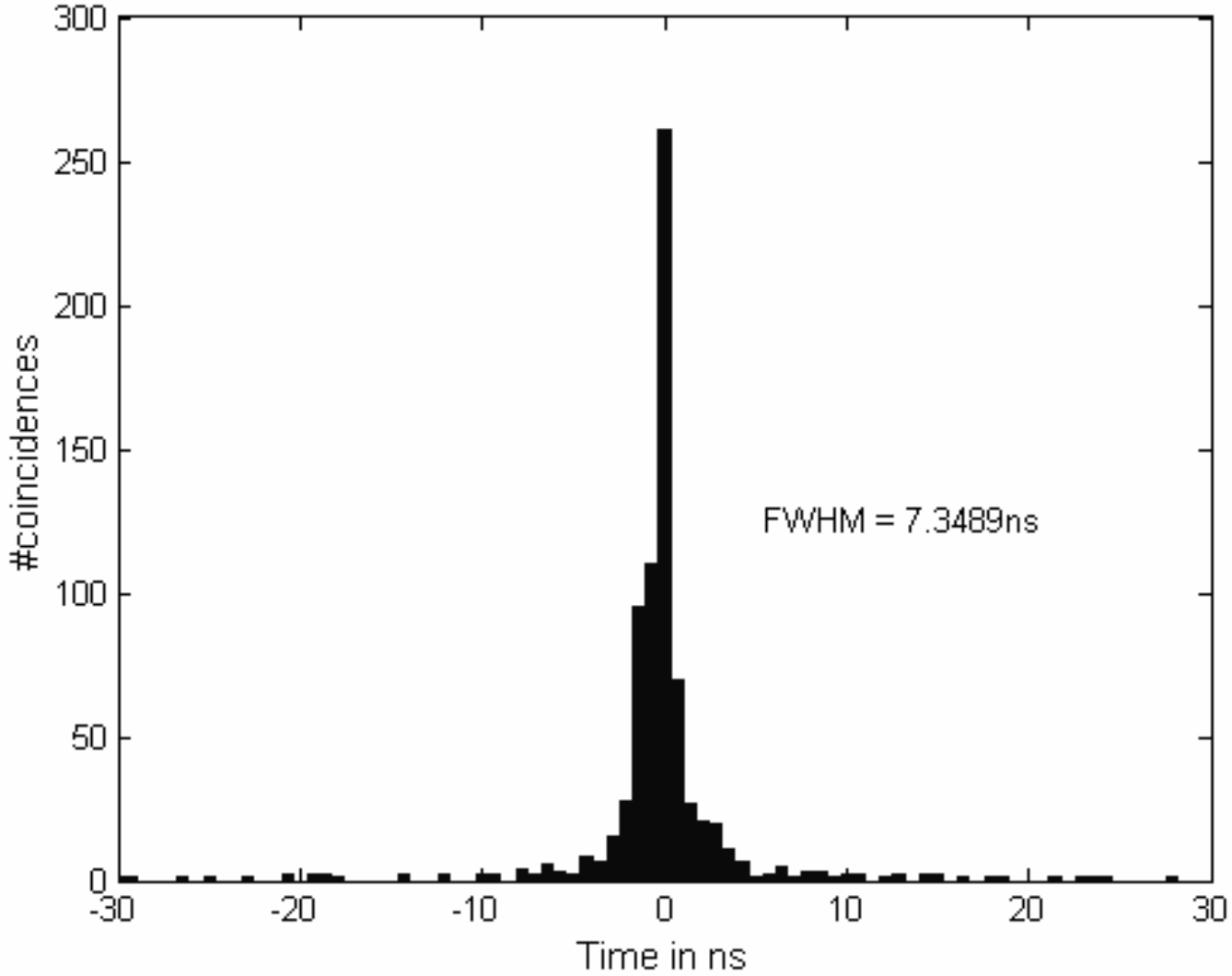
TDL-TDC Characterization Using Pulser. Reported resolution=625 ps



TDL based TDC in use in RatCAP: Coincidence timing spectrum for 1 RatCAP pair



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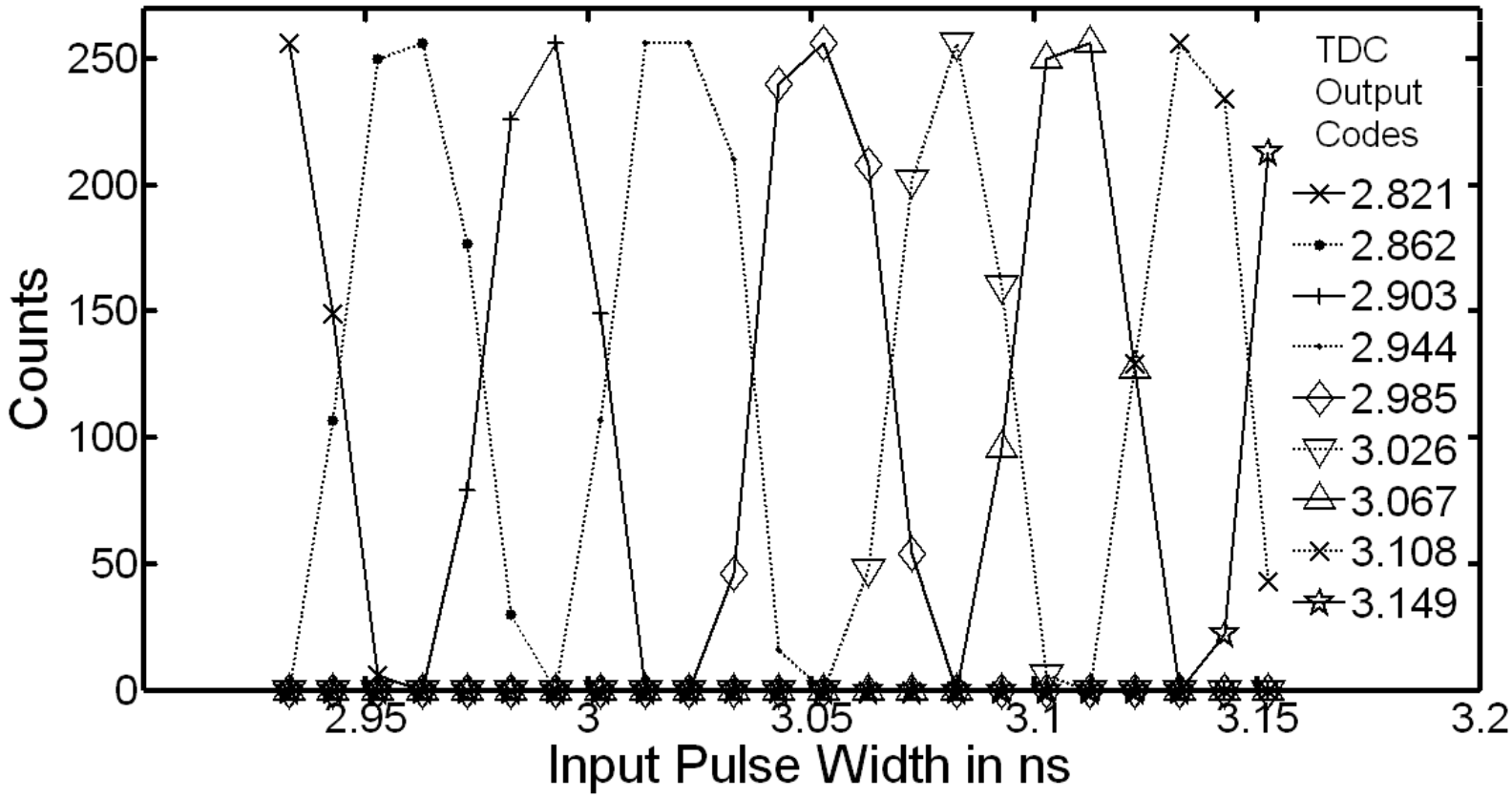
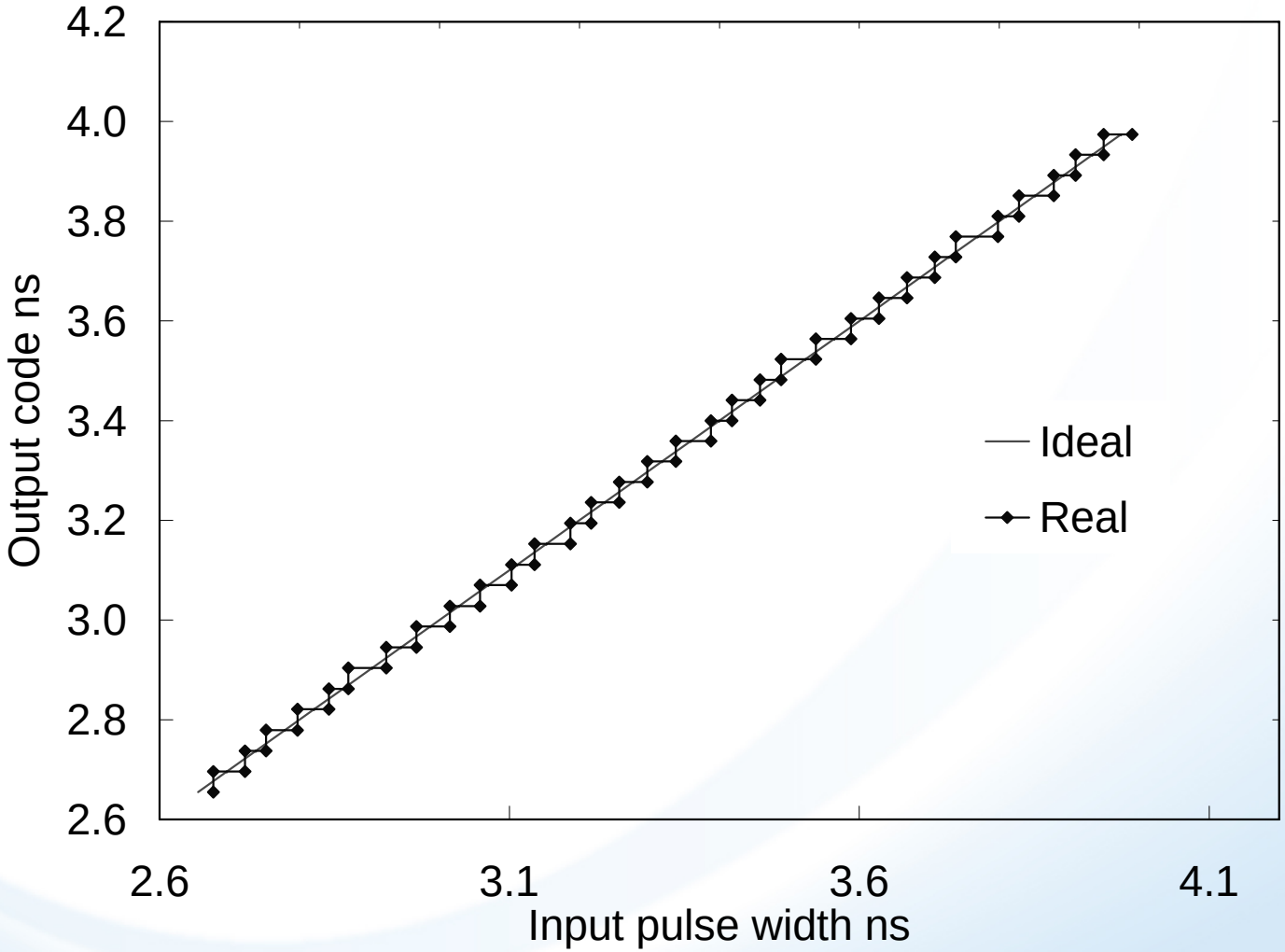
Calibration results

- T_{slarge} = 1 us
  - T_1 = 1.160 ns $\pm$ 0.1%
- T_{ssmall}= 3 ns
  - T_2 = 1.119 ns $\pm$ 0.1%
- $T_r = T_1 - T_2$ = 41 ps

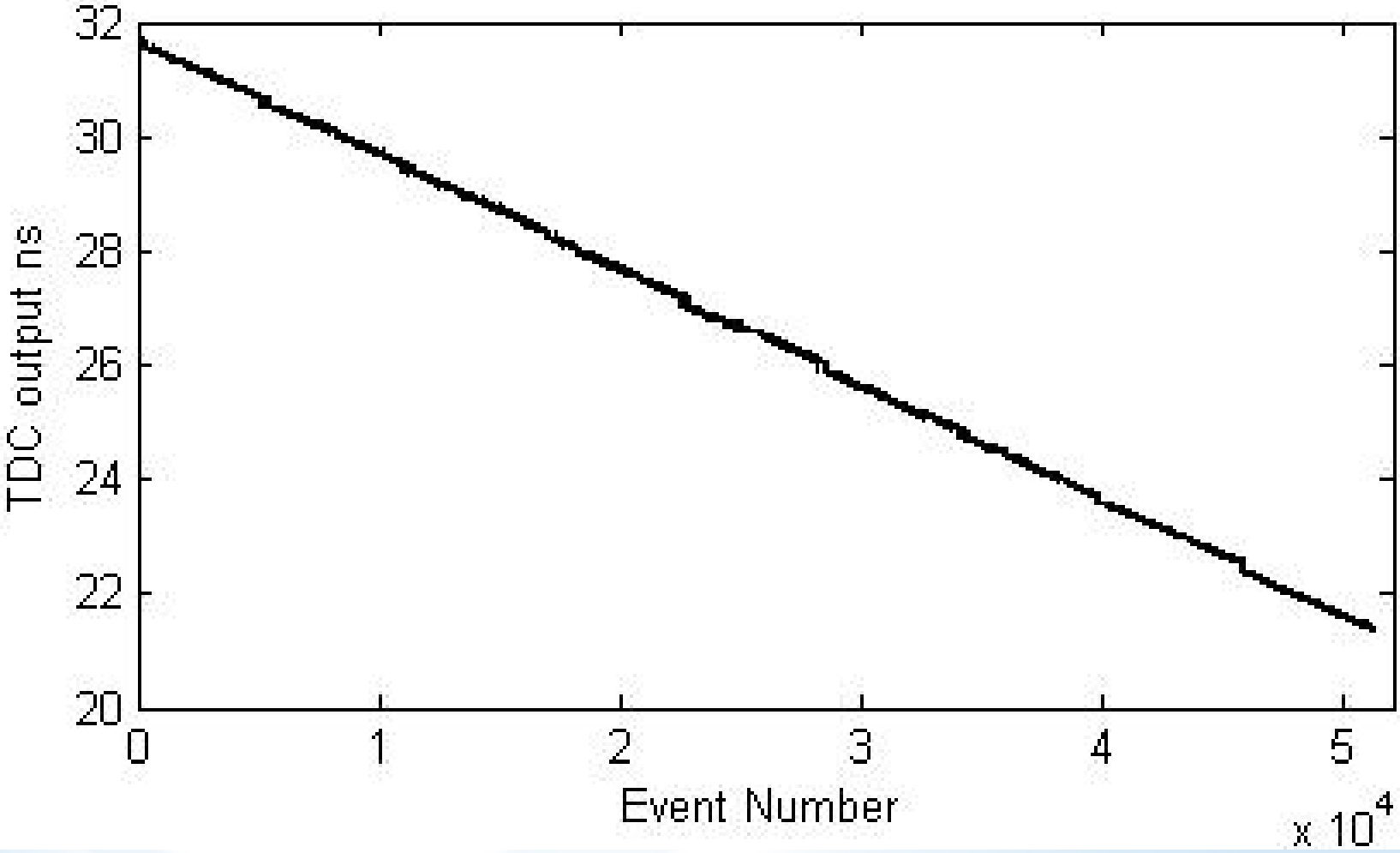
TDC output code histogram



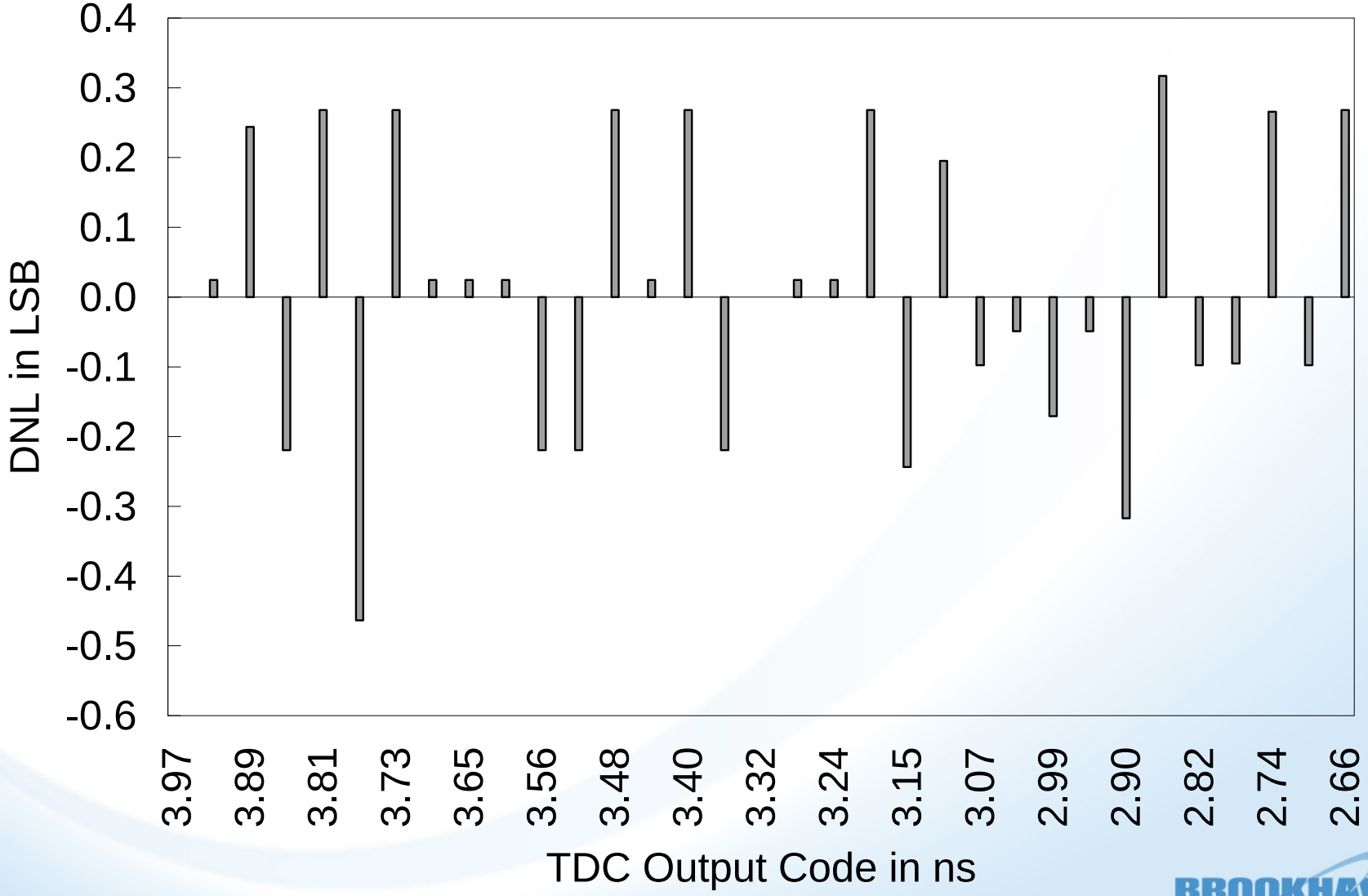
TDC Transfer Function



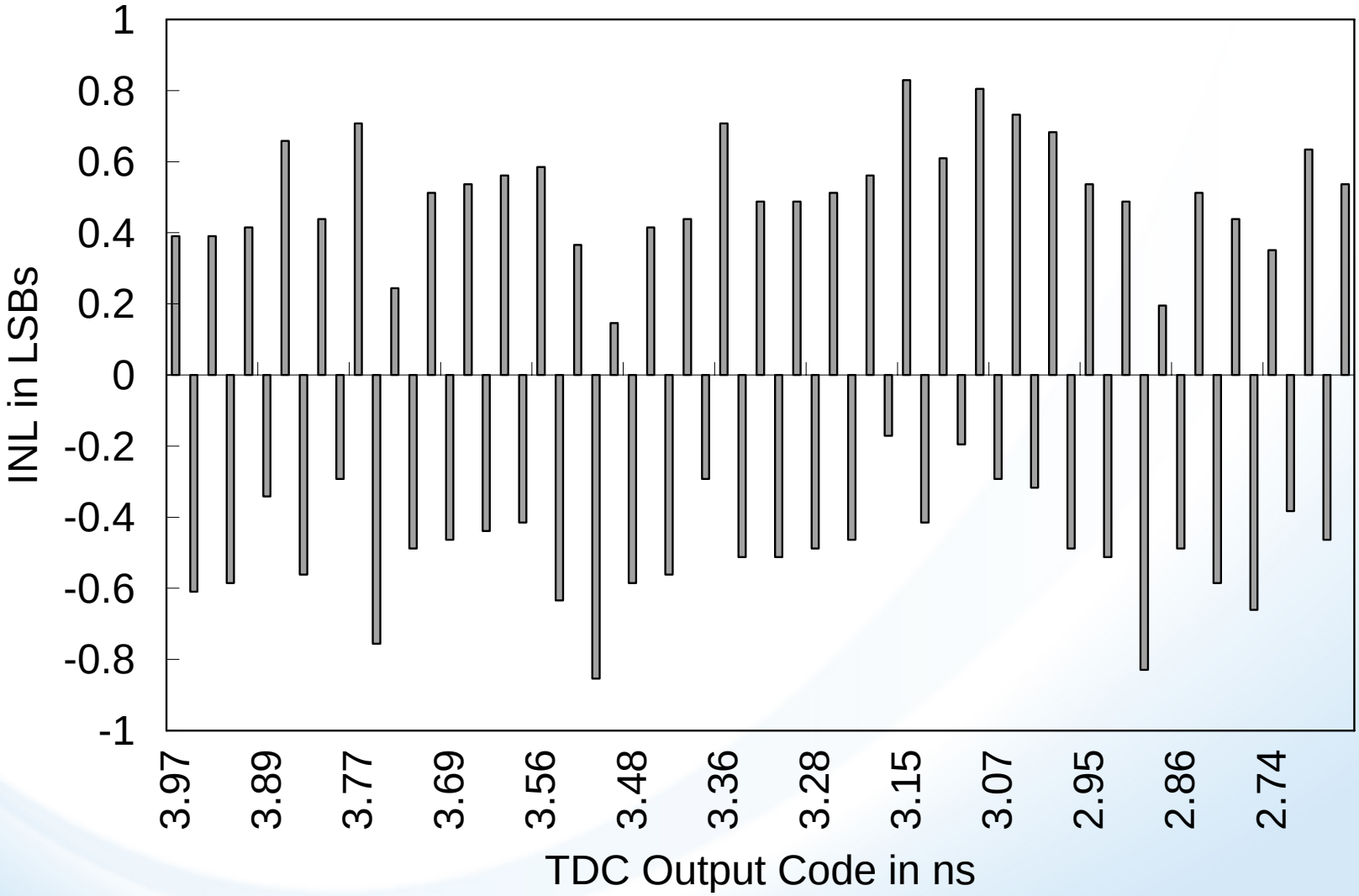
Clock transition nonlinearity corrected TDC output versus event



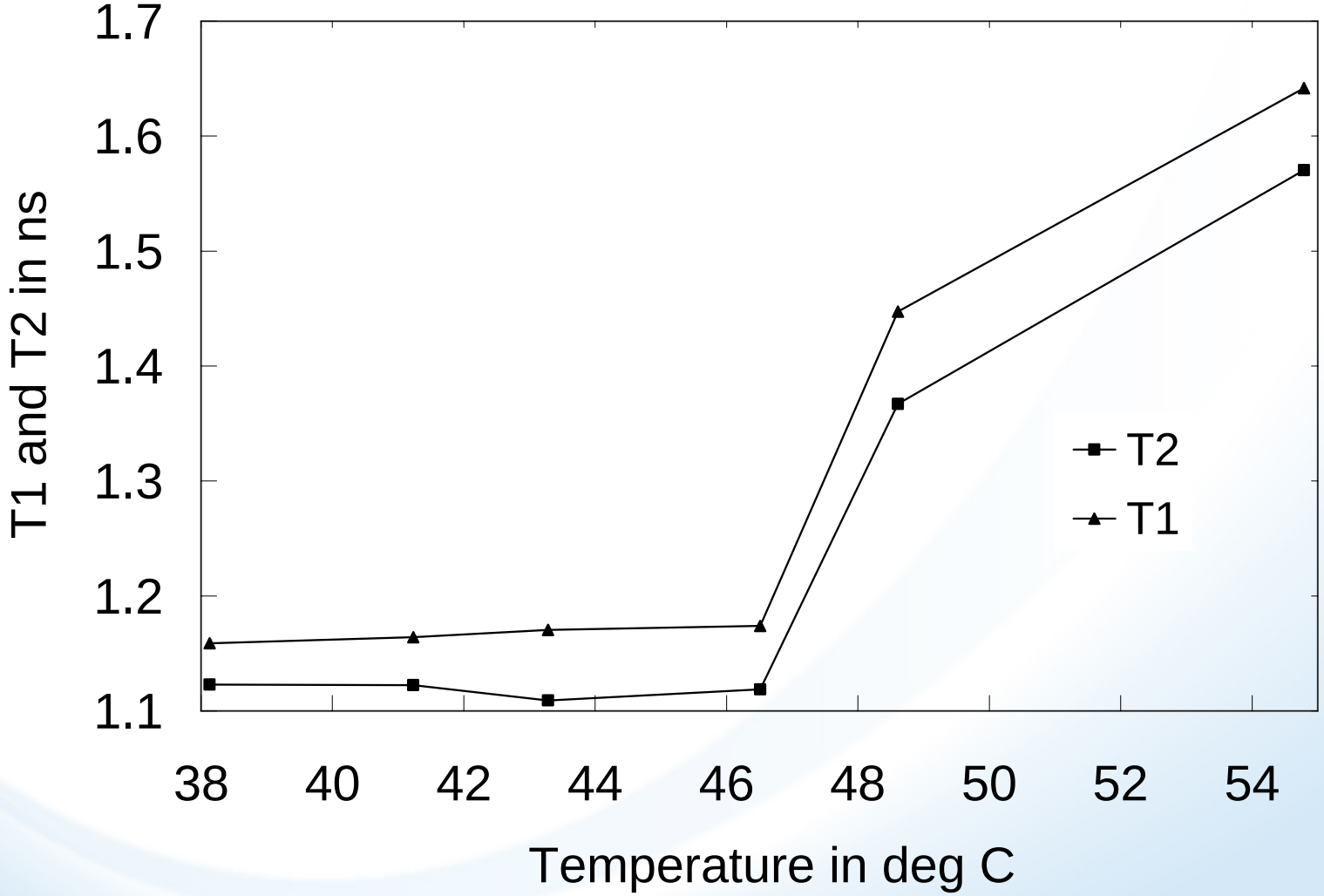
Differential Nonlinearity Error in TDC



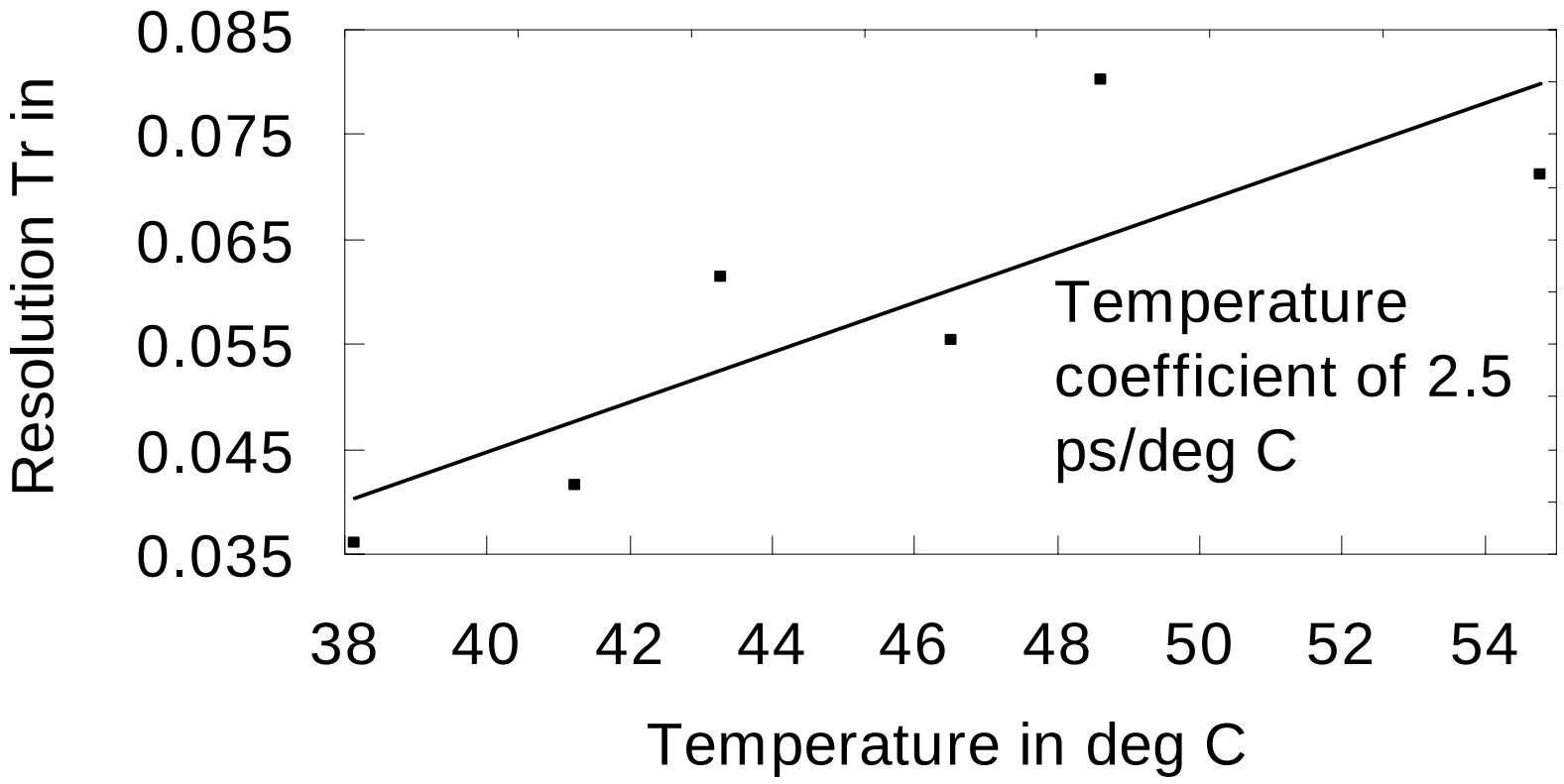
Integral Nonlinearity Error in TDC



Temperature Dependence of Ring oscillator Periods



Temperature Dependence of TDC resolution



Conclusion

- TDC resolutions of 625 ps and 40 ps are achieved using Altera Stratix II FPGAs
- INL < 1 LSB and DNL < 0.5 LSB is observed for both TDL and two ring oscillator technique
- Excellent linearity over wide dynamic range
- Vernier techniques achieve sub 100 ps resolution, and hits a limit at around 20-40 ps
- Sub 10 ps resolution regime should be explored in ASICs unless better control over FPGA design tools is available in near future

Part II: ADC circuits

- ADC state of the art
  - Effect of technology scaling
- Predominant ADC architectures
- TDC based ADC Architecture
- PMT pulse processing using TDC based ADC
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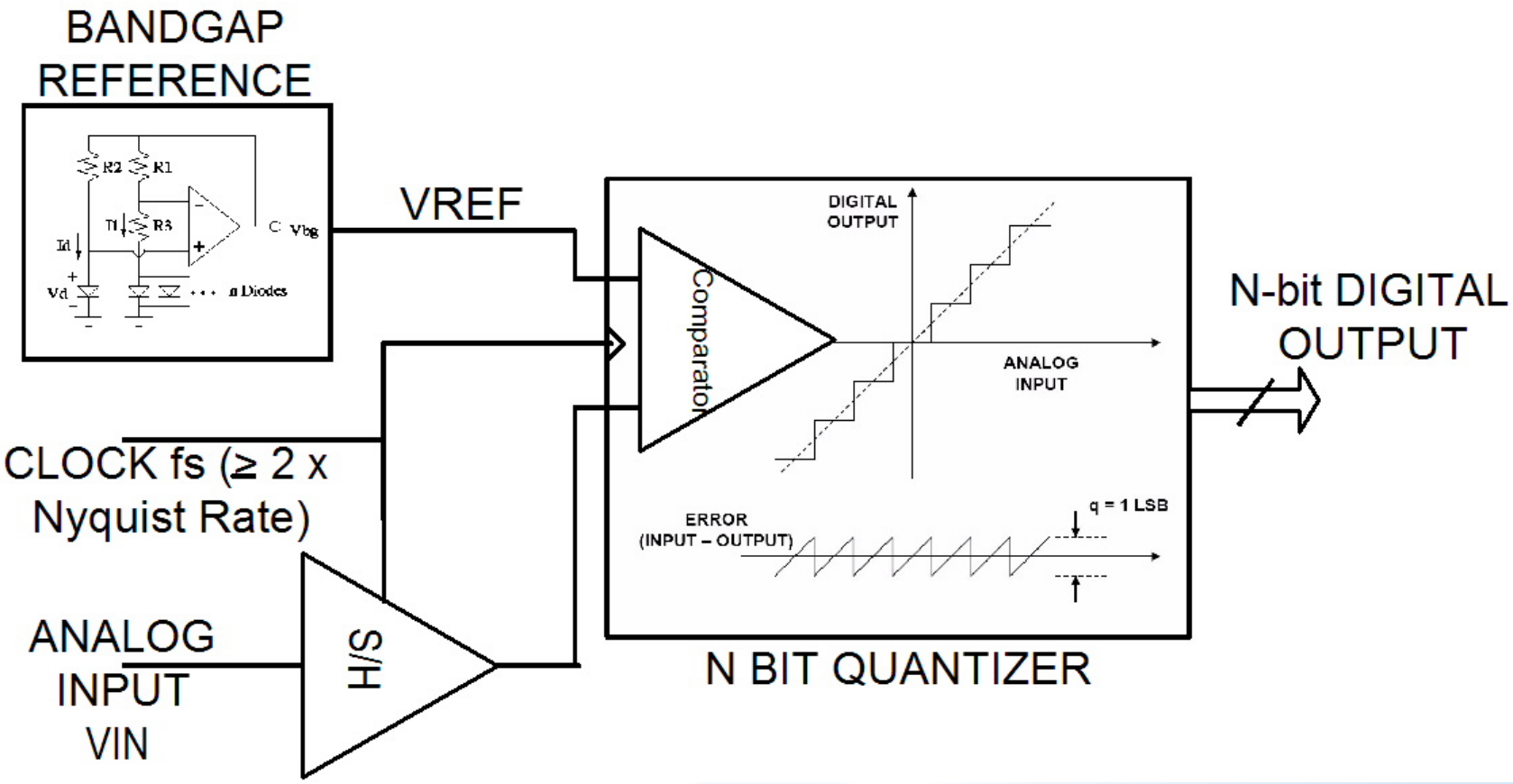
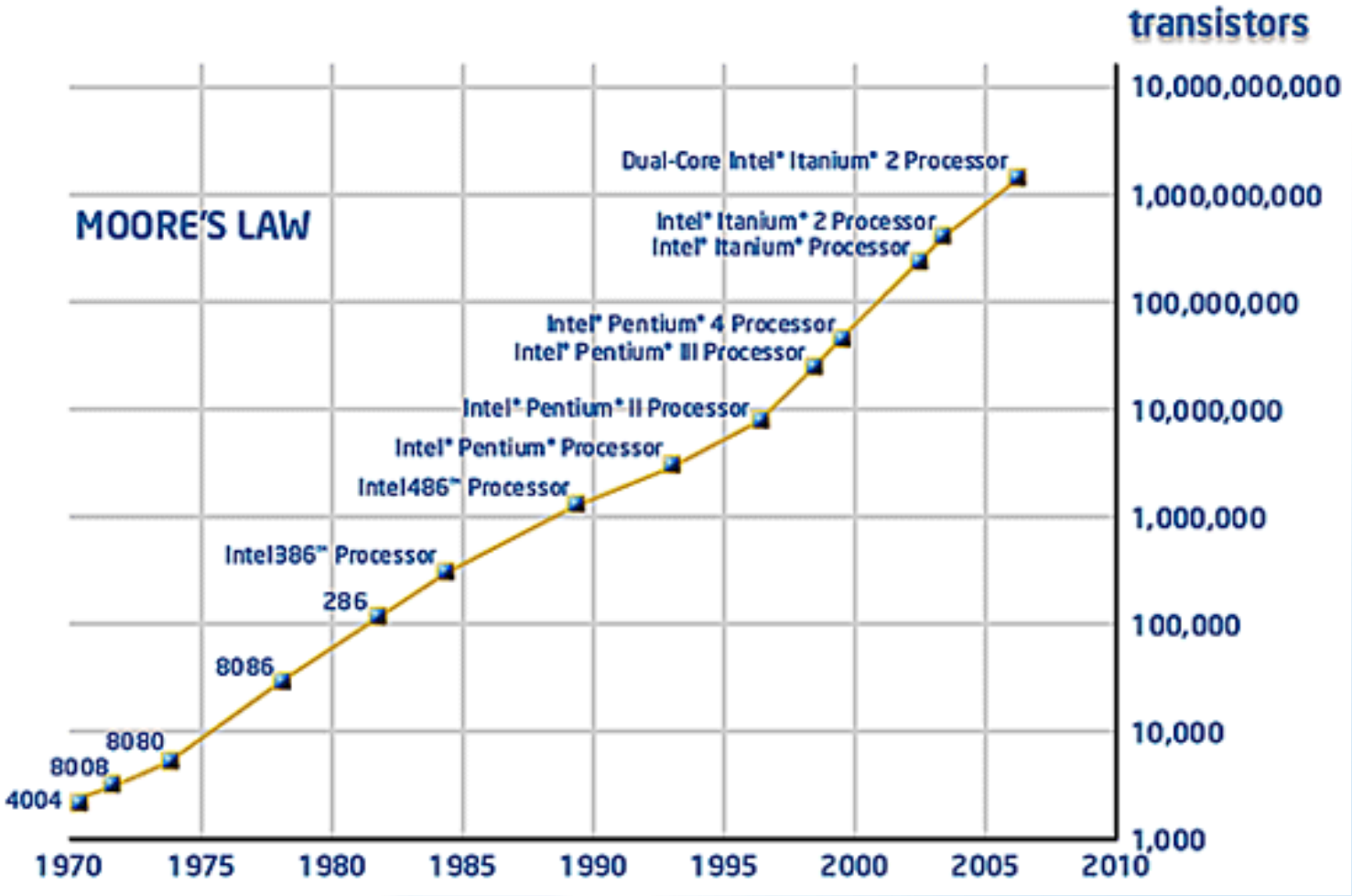
ADC Block Diagram

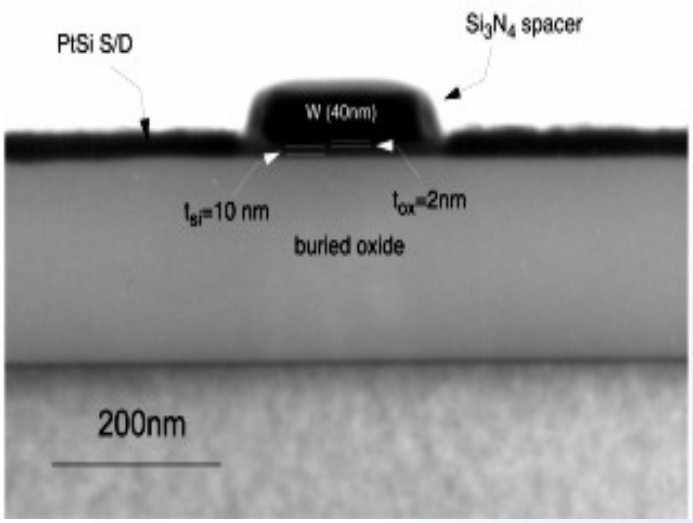


Moore's Law


transistors
MOORE'S LAW
Dual-Core Intel® Itanium® 2 Processor
Intel® Itanium® 2 Processor
Intel® Itanium® Processor
Intel® Pentium® 4 Processor
Intel® Pentium® III Processor
Intel® Pentium® II Processor
Intel® Pentium® Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
1970
1975
1980
1985
1990
1995
2000
2005
2010

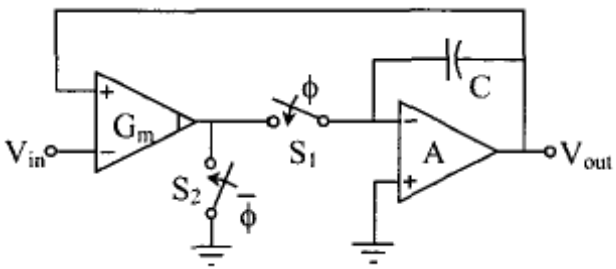
Technology Scaling Impact on Analog Design

- Gate oxide thickness ↓ =>Gate tunneling current ↑
- Early Voltage (VA) Reduction ↓
- Dynamic Range ↓



S/H Circuit

$$H_{OL} = \overbrace{\left(1 + \frac{1}{\underbrace{G_{OL}}_{Openloop-Gain} - 1}\right)}^{S/H-Error} \times \frac{1}{1 + p\frac{2\zeta}{\omega_n} + \frac{p^2}{\omega_n^2}}$$



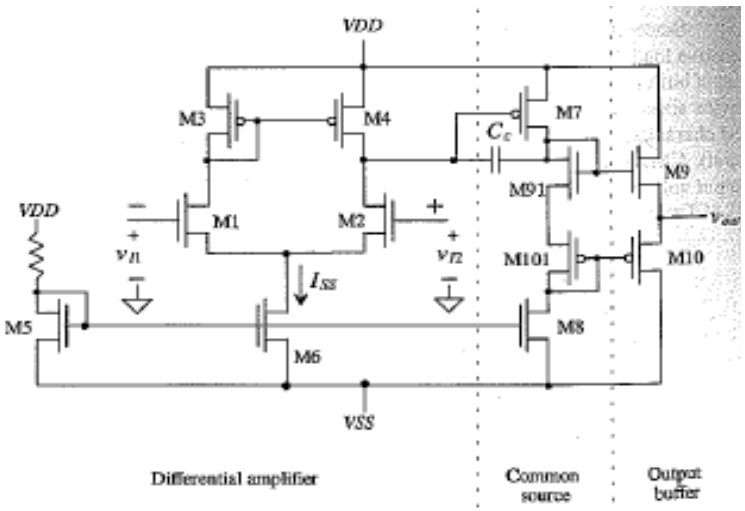
ζ is the S/H damping factor

ω_n is the S/H natural frequency

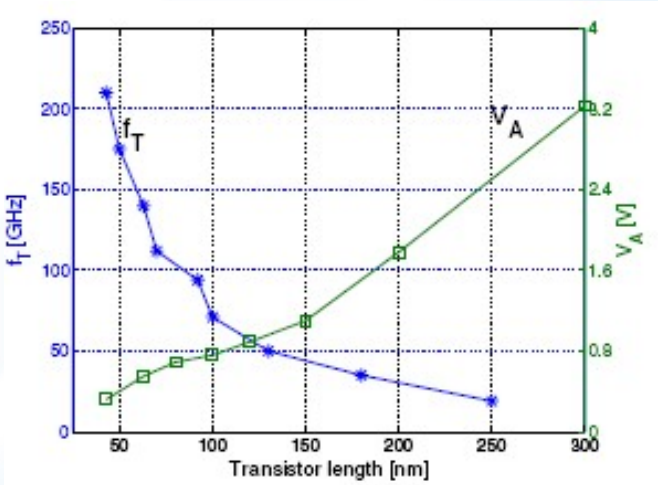
$G_{OL} = g_{m1}(r_{o2} \| r_{o4}) * (-gm_7(r_{o7} \| r_{o8}))$

$r_o \ \alpha \ 1/\lambda$

$r_o \ \alpha \ V_A$

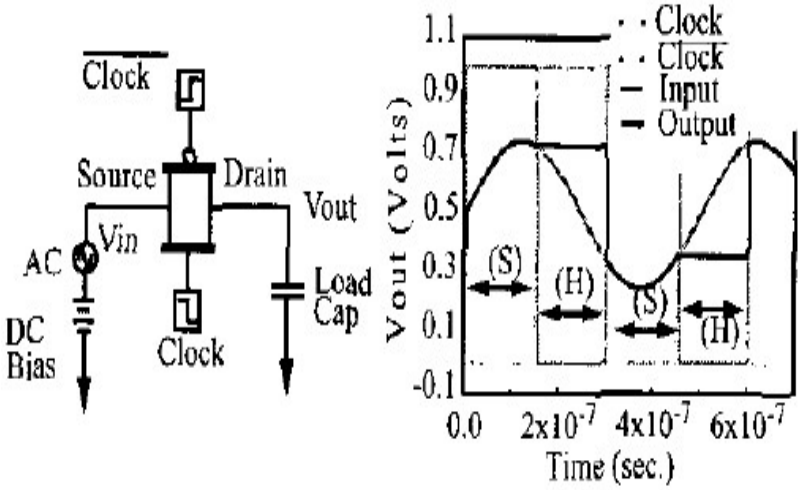


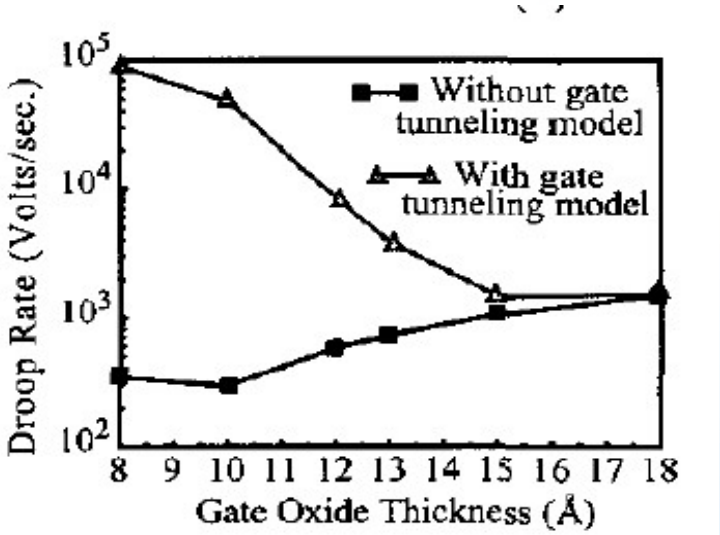
Operational Amplifier



NIELSEN, H.,J.,et al., 2005

Technology Dependence of Droop Rate





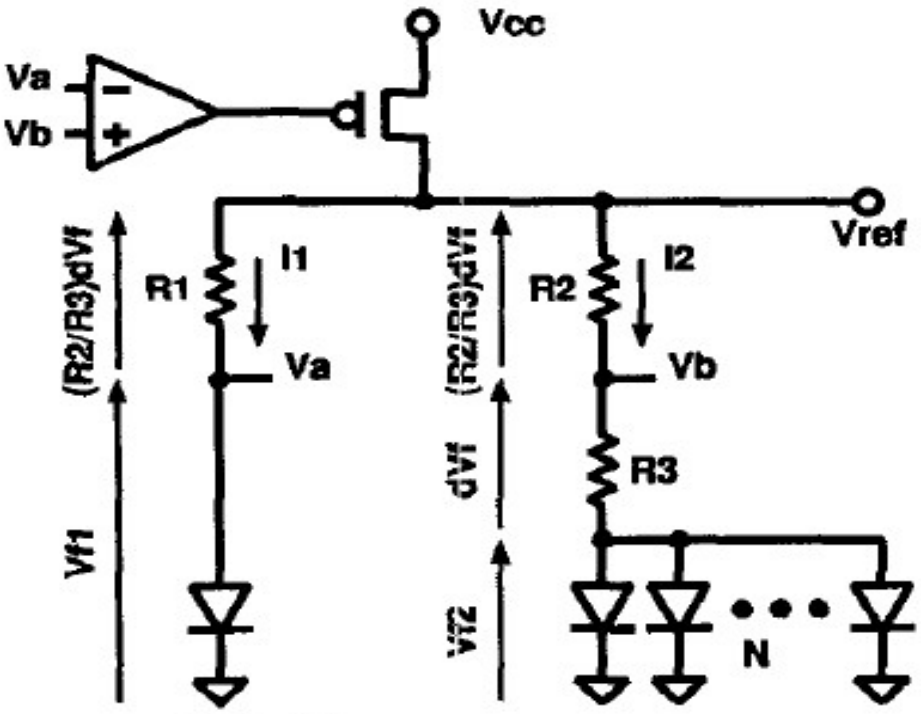
For 90 nm Technology, 1 V Dynamic Range, 13 Bit, 10 MSPS ADC, LSB = 0.12 mV

$$V_{droop} = 10^3 V/s \times 100ns$$

$$V_{droop} = 0.1mV$$

[Gupta, M., et al., Sept 2004]

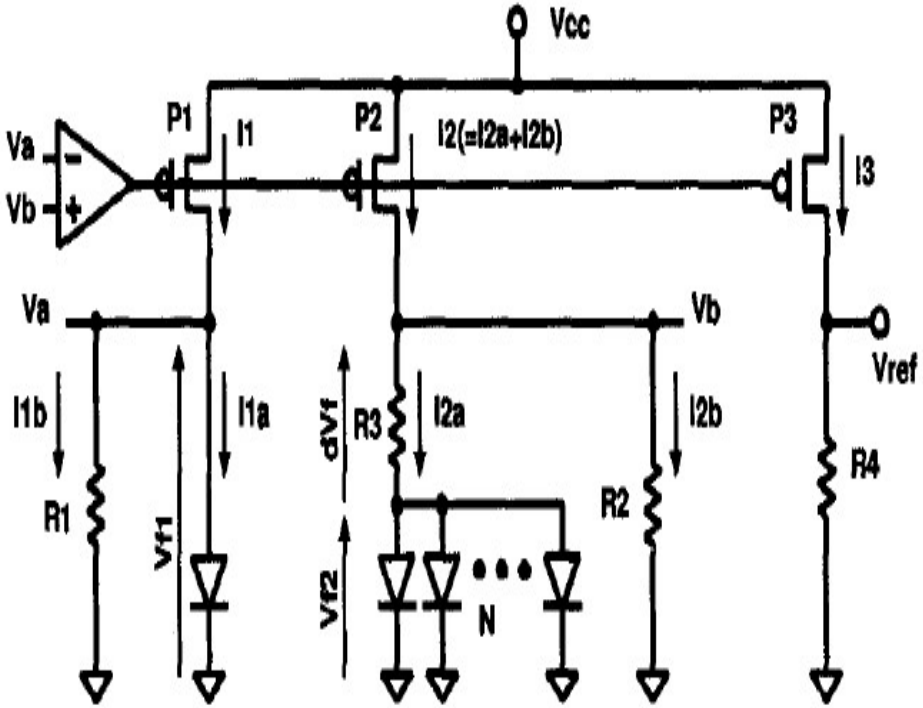
Bandgap Reference



VT=k ·T/q

dVf=VT · ln(N · Fl2/R1)

Vref=Vf1+(R2/Fl3)dVf



dVf=VT · ln N

Vref=R4(Vf1/R2+dVf/R3)

HÄNSLER, K., et al.,2003

Part II: ADC circuits

- ADC State of the art
- ADC Architectures
  - Comparison and suitability for deep submicron
- TDC based Analog to Digital Converter (ADC) Architecture
- PMT Pulse Processing using FPGAs
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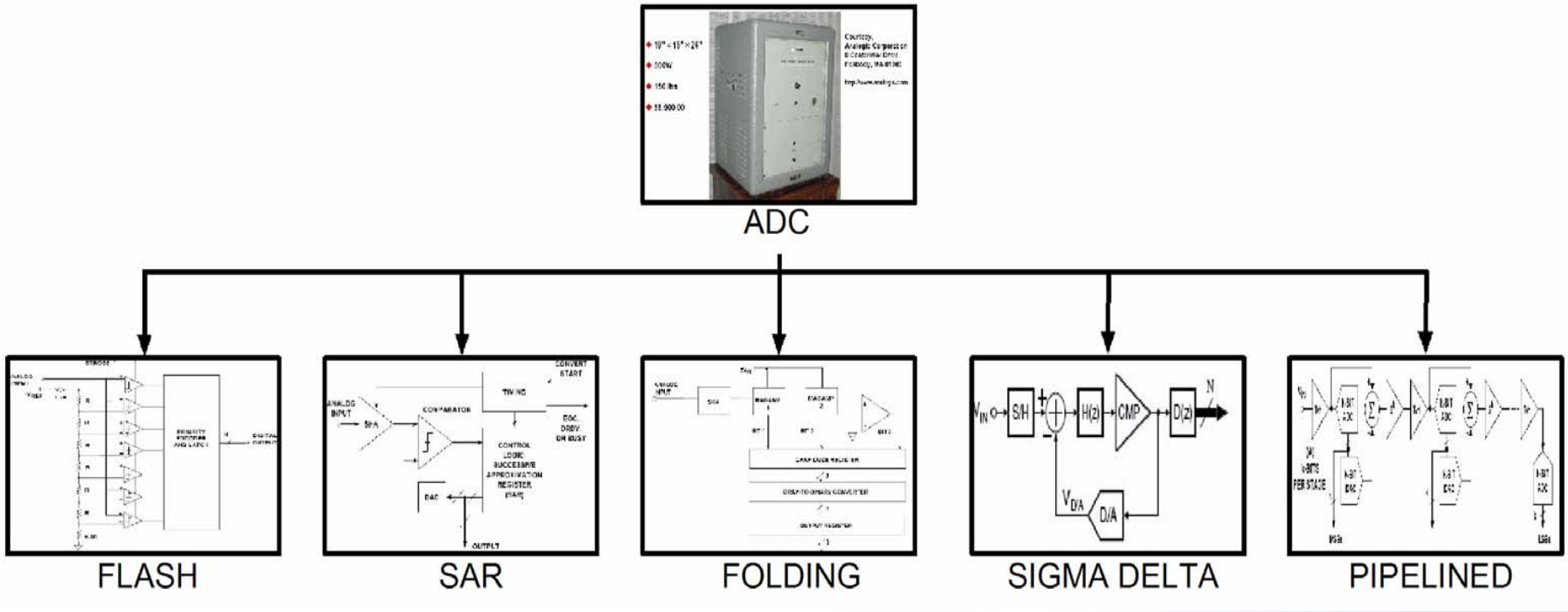
Predominant ADC Architectures



Comparison

Conversion	**FLASH** N bits - 2^N -1 Comparators, Resistors, Caps increase by a factor of 2 for each bit.	**SAR** Binary search algorithm, internal circuitry runs higher speed.	**Σ Δ** Oversampling ADC, Digital Decimation Filter
Encoding	Thermometer Code Encoding	Successive Approximation	Over-Sampling Modulator, Digital Decimation Filter
Disadva-ntages	Bubble codes / metastability, high power consumption, large size	May require anti-aliasing filter. Slow conversion	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC. Strict stability requirements. OTA in integrator stages and S/H

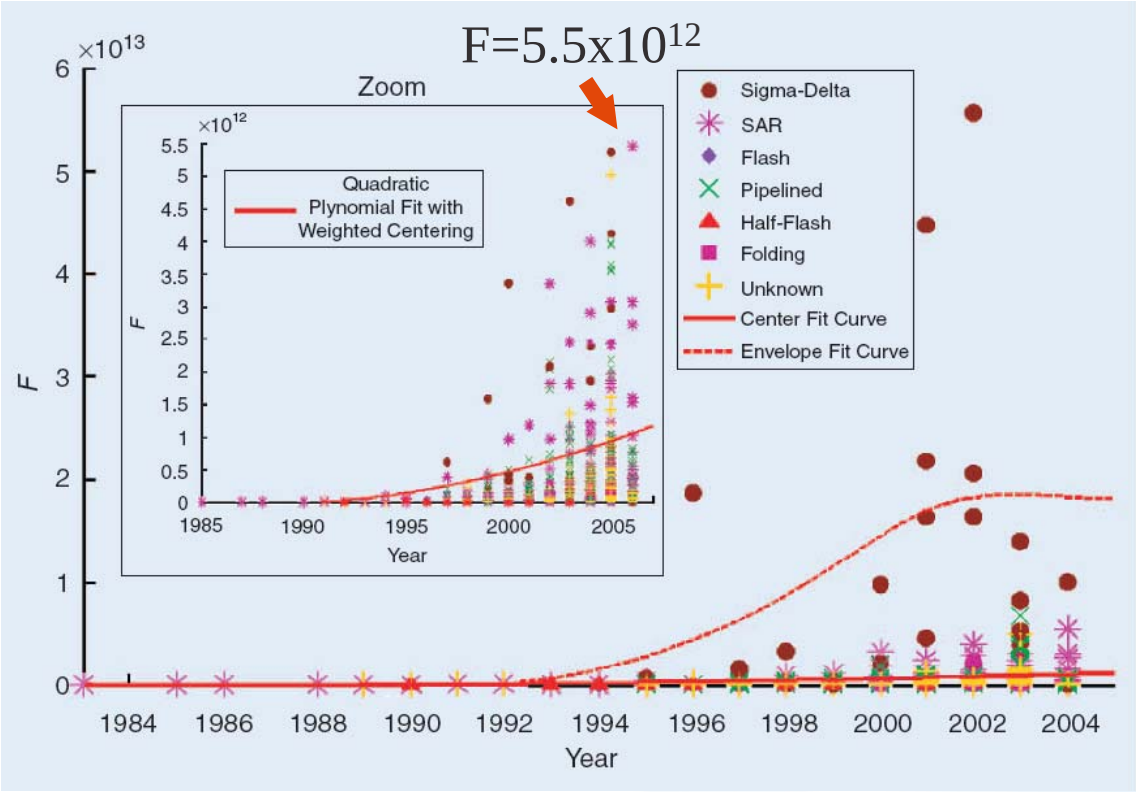
Conversion Time	**FLASH** High speed. Not dependant on N	**SAR** Increases linearly with increased resolution. Can be offset by using high speed clock in deep submicron	**Σ Δ** Tradeoff between data output rate and noise free resolution
Resolution	Limited to 8 bit maximum due to resistor matching, area and power concern. High N=> High cap=>Slow speed	Passive components matching better in deep submicron. Matching requirement double with every bit increase in N	Component matching requirements double with every bit increase in N
Size	2^N-1 comparators, power increases exponentially with N	Die increases linearly with increase in resolution.	Core die size will not change with increase in N

SAR: Choice for deep Sub Micron

- Ease of implementation
- Low power
- Reliance on passive component matching
- No OTA needed. S/H OTA can be combined in Charge Redistribution type DAC
- High clock speed can offset for N+1 cycle conversion time
- Stable BGR needed

ADC State of the art (F=1/Figure of Merit)

Best case
$F=5.5x10^{12}$



- BIN, L., et al., Nov. 2005, *Analog To Digital Converters, A Review Of Past, Present And Future,* IEEE Signal Processing Magazine, pages 69-77

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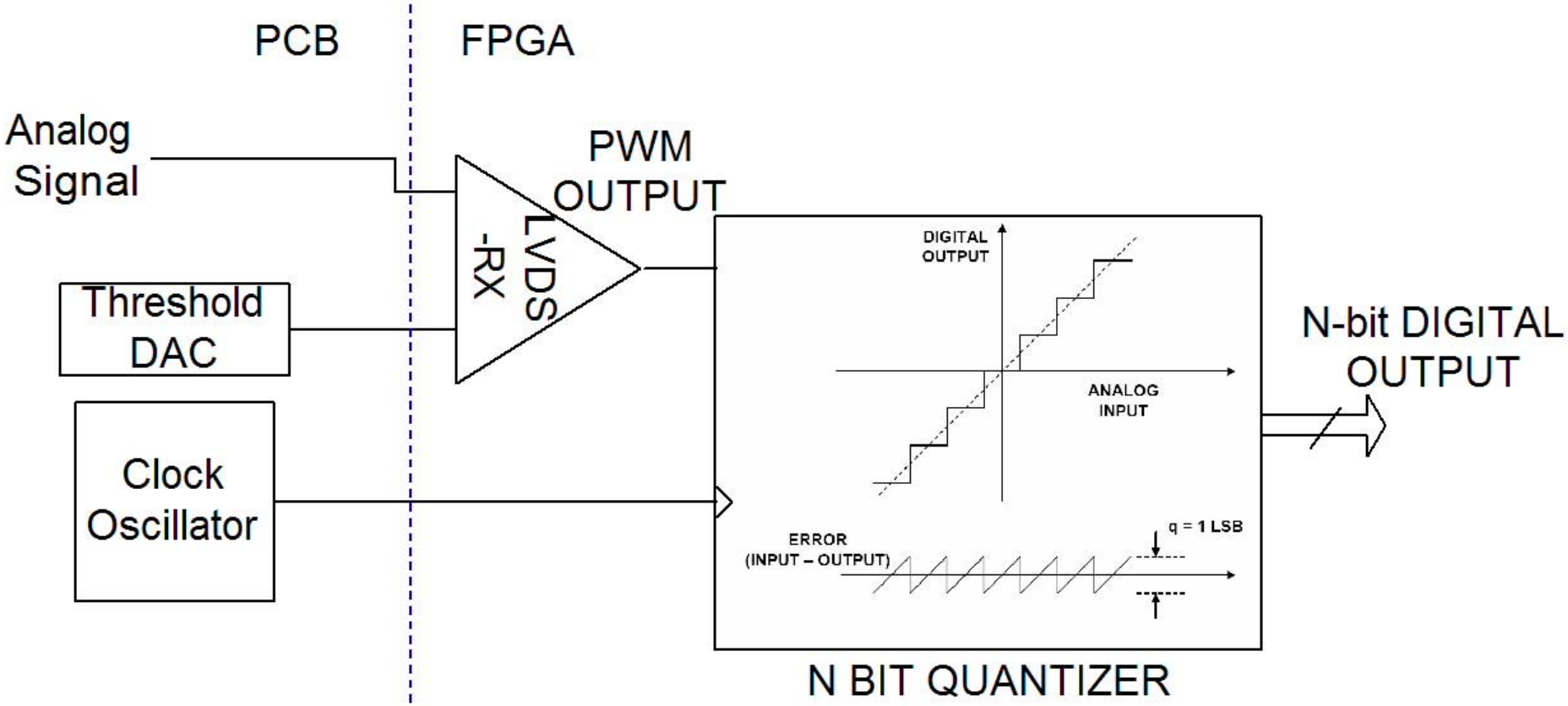
- Conclusion

TDC based ADC Topology



Nonlinearities: DNL and INL. SNR

$$DNL = A_{input}(Q_{m+1}) - A_{input}(Q_m) - 1LSB$$

$$INL = \Delta_{N-1} = \frac{2^{N-1}}{2^N - 1}\sum_{m=0}^{N-1}\varepsilon_m - \varepsilon_{N-1}$$

$$SNR = 6.02N + 1.76dB$$

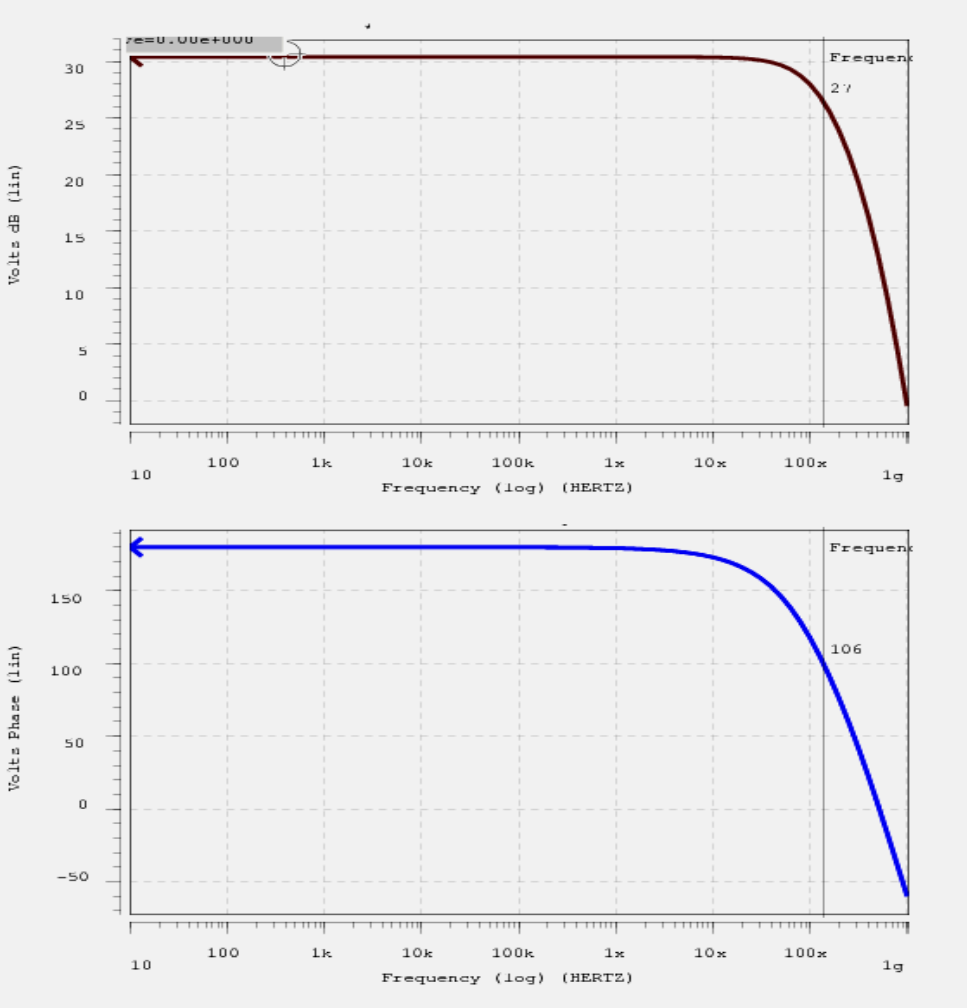
Causes:

Cell to Cell Delay Variations

Routing Delay Variations

Clock Jitter

Altera Cyclone family LVDS Comparator AC response



Quantizer (Comparator) performance

$$p_i = \frac{2V_L}{A_0 q} e^{-\frac{t}{\tau}} *$$

p_i is the probability that the comparator will yield ambiguous output.

V_L=Threshold for the digital gate at the comparator output=0.6

A_0=Open loop comparator gain≈32

q=Quantization step≈$2.5/2^{15}$

t=Comparison time≈10 ns

$\tau = 1/2\pi f_{3dB}$

f_{3dB}= 3dB bandwidth of the comparator≈100 MHz

Example case of Altera Cyclone device LVDS comparator

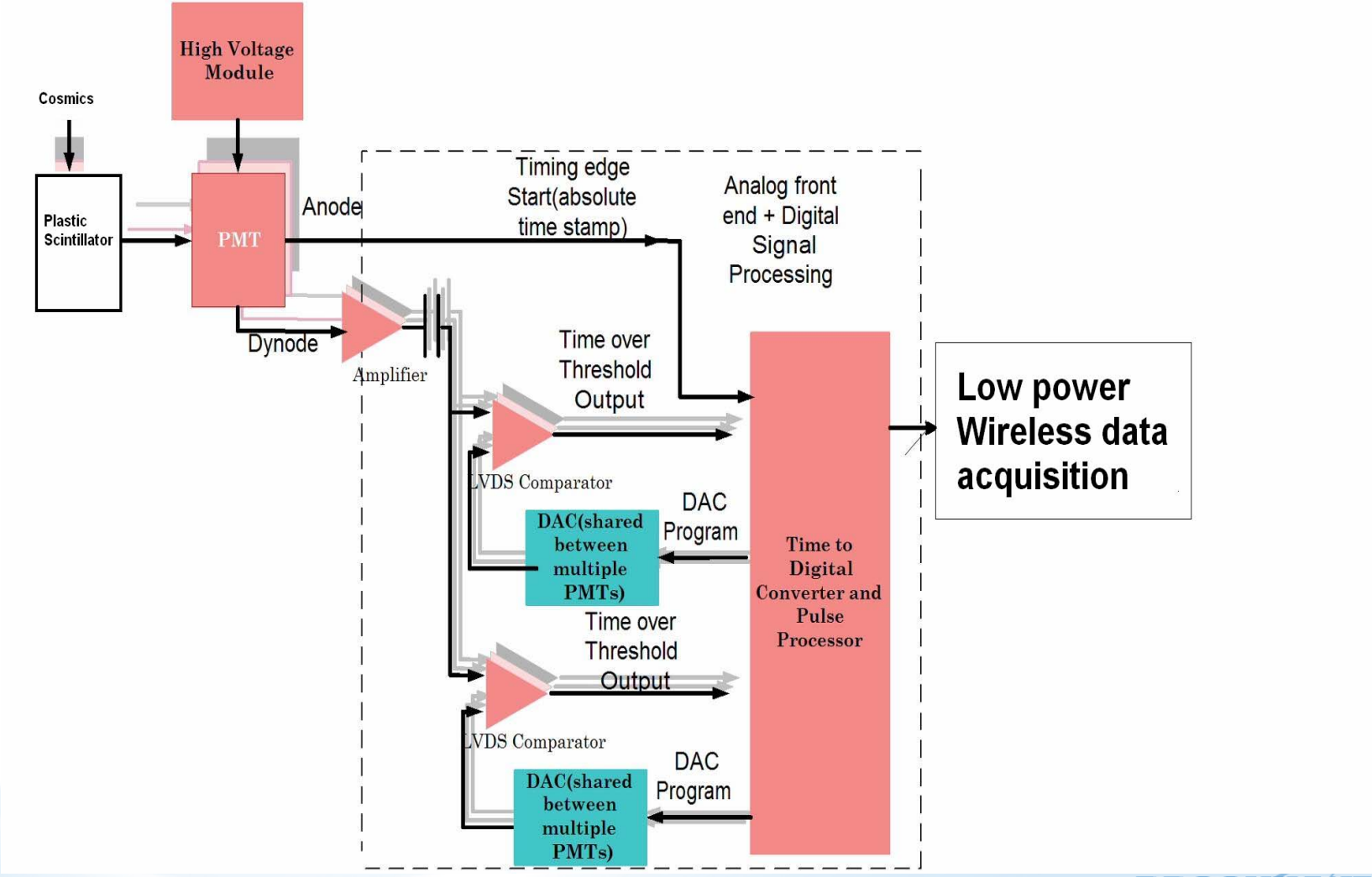
$p_i = 1.02 \times 10^{-6}$

* WOODWARD, C., et al., DEC 1975, *A Monolithic Voltage-Comparator Array for A/D Converters*, IEEE JOURNAL OF SOLID-STATE CIRCUITS,VOL. SC-10,NO. 6, pages 392-399

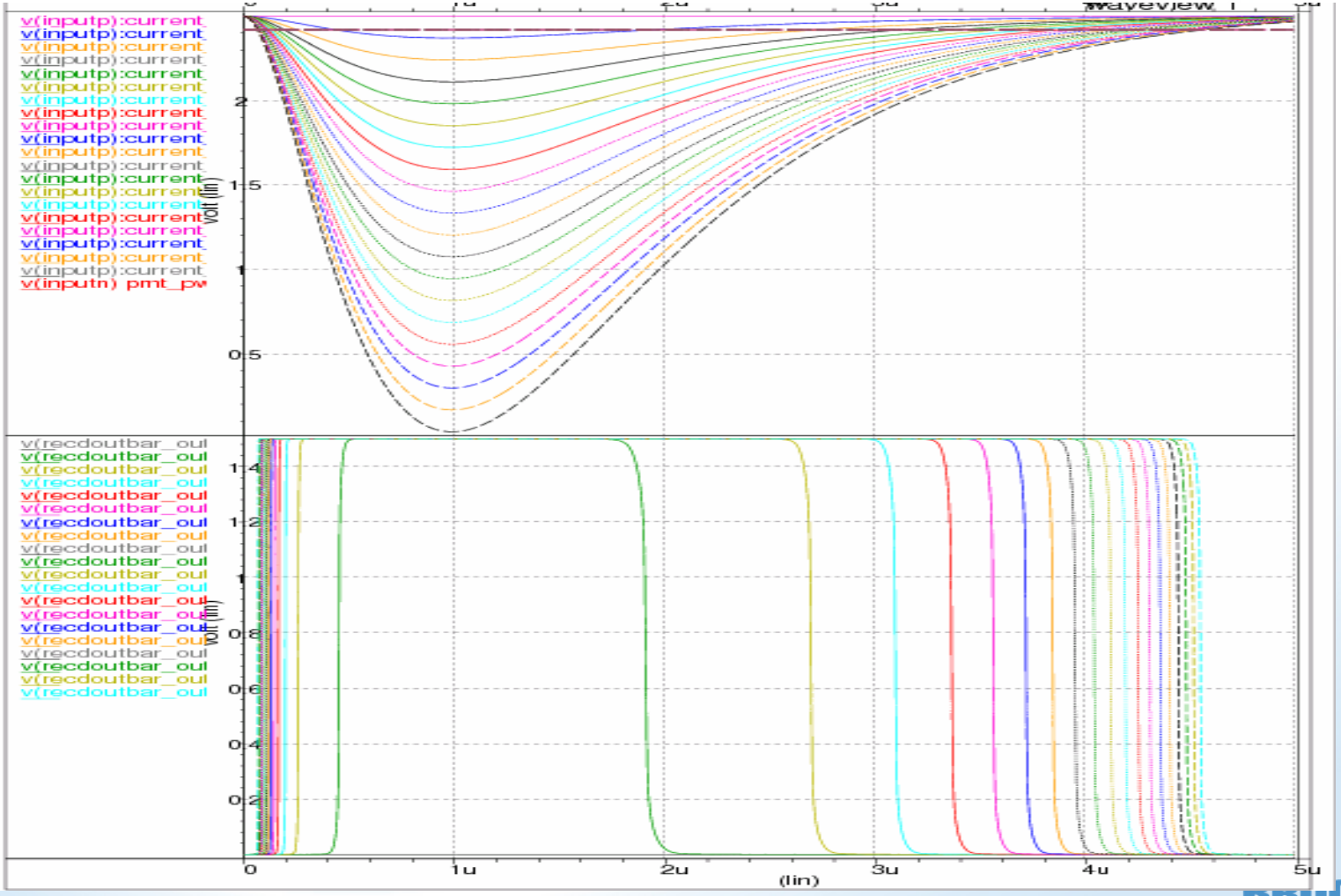
Part II: ADC circuits

- ADC State of the art
- ADC Architectures
- TDC based Analog to Digital Converter (ADC) Architecture
- Application: PMT Pulse Processing using FPGA
- Conclusion

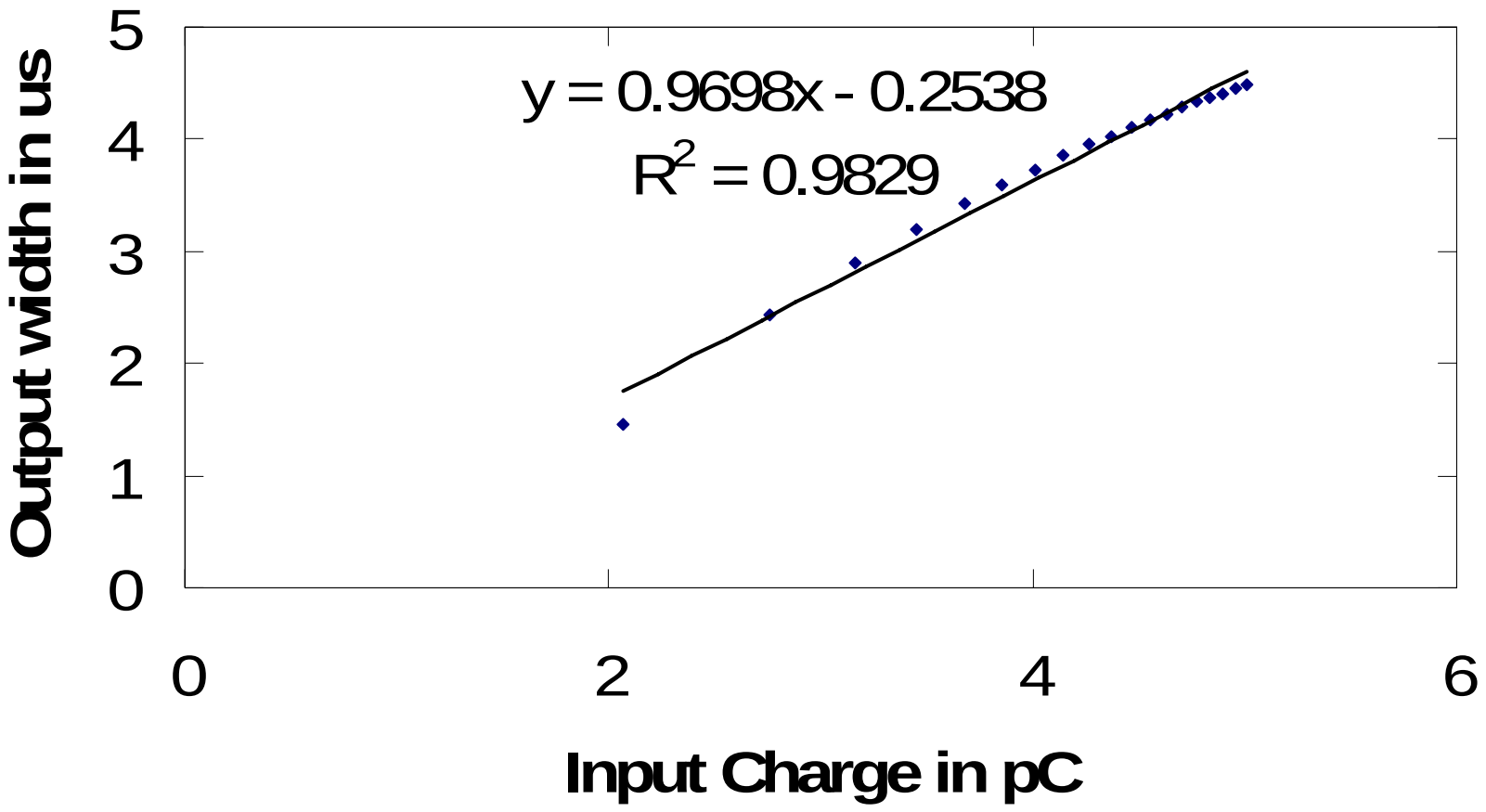
Battery operated, signal chain for PMT Pulse Processing using FPGA based TDC and ADC (MARIACHI experiment)



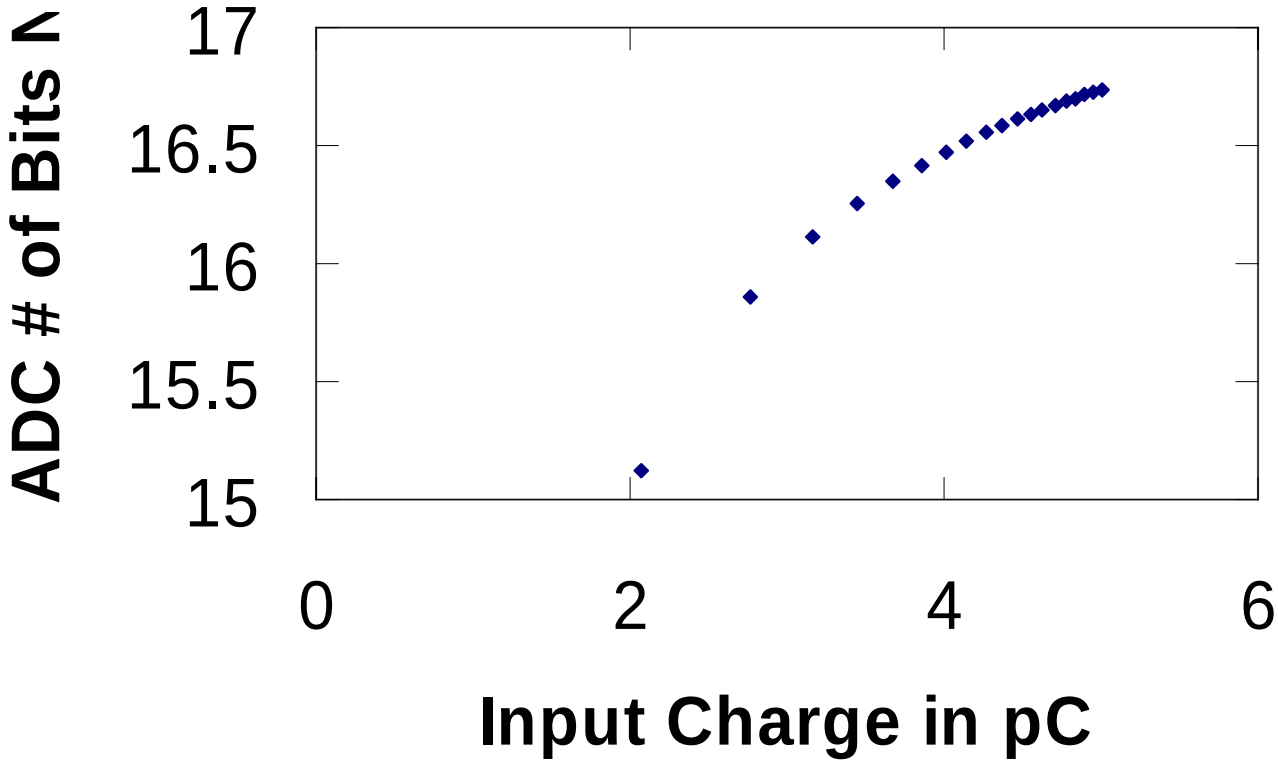
PMT Output and corresponding ToT comparator response



Simulated PMT output charge vs LVDS comparator output



ADC resolution vs input charge, Simulated



VTC based ADC power dissipation

$$P_{ADC} = P_{S/H} + P_{VTC} + P_{TDC}$$

Where P_{VTC} and P_{TDC} can be calculated from inverter power dissipation formula and number of inverter stages. For VTC, n=1 and for TDC $n=2^N$ where N=Number of bits

$$P_{VTC/TDC} = 2 \times n \times P_{inv} = 2(P_{dyn} + P_{dp} + P_{stat})$$

$$P_{dyn} = C_L V_{DD}^2 f_s$$

$$P_{dp} = V_{DD} I_{peak} \left(\frac{t_r + t_f}{2}\right) f_s$$

$$P_{stat} = V_{DD} I_{leak}$$

Example case TDC based ADC Figure of Merit

$$FOM_{ADC} = \frac{P_{ADC}}{2^{ENOB} \cdot f}$$

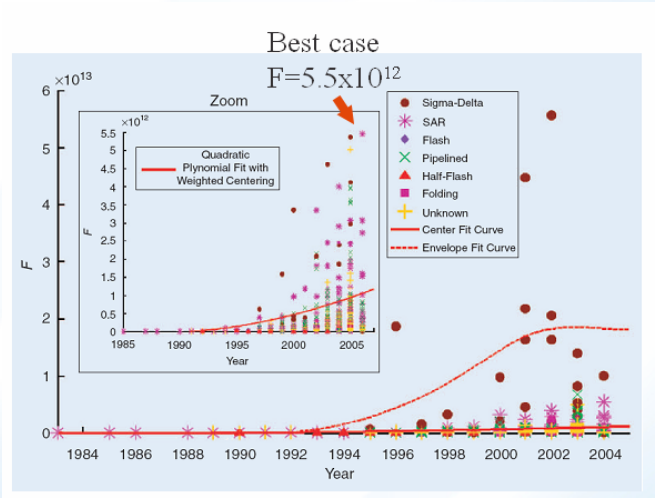
Example case of proposed ADC

ENOB≈15, f_s=1 MHz (using 20 ns TDC deadtime, multiple VTH),

C_L=10 fF, V_{DD}=1.8 V

FOM ≈ 0.048 pJ

1/FOM ≈ 21 x $10^{12} J^{-1}$



Conclusion

- TDC based ADC architecture is a way of the future ADC architectures as technology feature size shrinks
- FPGA based ADC architecture promises a resolution close to 15 bits using ToT method
- FOM for such ADC surpasses state of the art by an order of magnitude
- Future work involves detailed hardware implementation of ADC
- Real-time ToT PMT Pulse processing algorithms need to be developed for the architecture to be meaningful in practice

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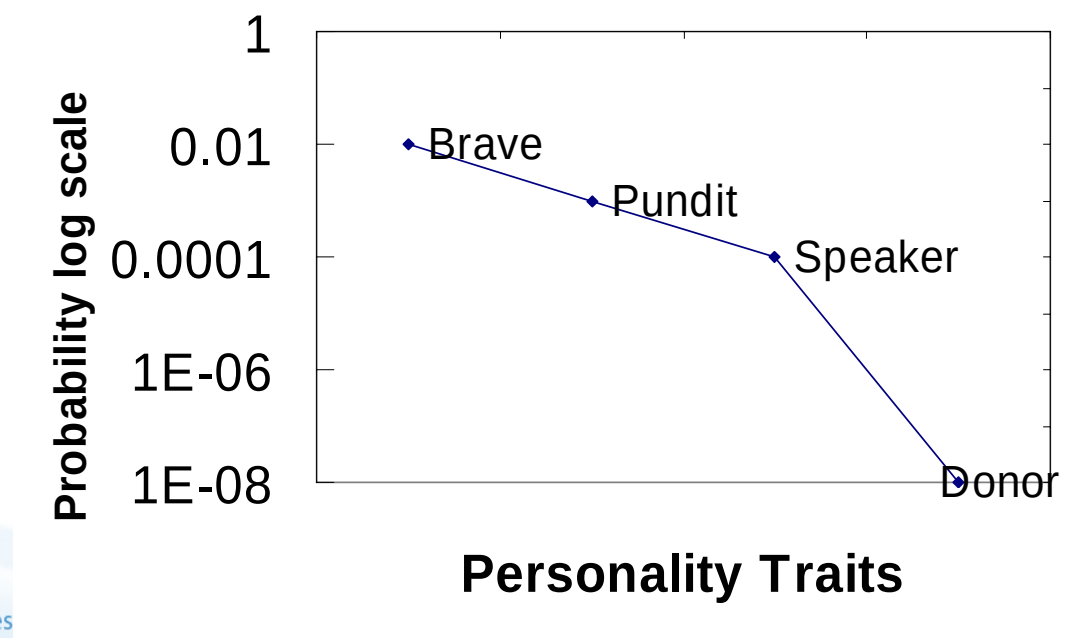
Excuse

शतेषु जायते शूरः सहस्रेषु च पंडितः।
वक्ता दशसहस्रेषु दाता भवति वानवा॥

Shateshu jaayate shoora(h) sahastreshu cha pundit (ah)|

Vakta dasha sahastreshu daata bhavati vanava ||

In hundreds one finds a brave; a pundit in thousands, a (good) speaker in ten thousands and seldom or never one finds a (generous) donor.



Thank You!