

Novel Charge Sensing Elements and Signal Processing on a CMOS Monolithic Active Pixel Sensors

Outline:

- Motivation for Monolithic Pixel Devices
- Operation Principle of MAPS for Particle Detection
- Simulation of Charge Collection ISE-TCAD
- First Prototypes - design summary
- Measurements - evaluation of basic parameters
- First Prototypes - summary of MIPs tracking performances
- Design and Performances of 3.5 cm², 1M Pixel Device
- Radiation Hardness
- CSE Optimised for VX Environment
- Summary

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Introduction **Why monolithic active pixel devices:**

- same unique substrate for detector and electronics:
 - thin device \Rightarrow reduced multiple scattering effect,
 - no complicated and expensive detector-electronics connection with bumps,
 - detector radiation hardness - no bulk charge transfer (CCDs).

 Why pixels CMOS:

- standard, well established CMOS industrial fabrication process:
 - access to the most advanced technologies,
 - convenient way of design - standard software tools, design kits and libraries,
 - good price and high yield !
 - low power consumption,
 - system-on-a-chip capability - integration of amplifiers, ADCs, signal processing units etc. on the detector, random pixel addressing,
 - very good spatial resolution ($\sim 1 \mu\text{m}$) - small pixel size, } *when submicron process used*
 - electronics radiation hardness (layout rules). } *process used*

1998 - IReS/LEPSI Strasbourg, R&D on CMOS MAPS for charged particle detection,

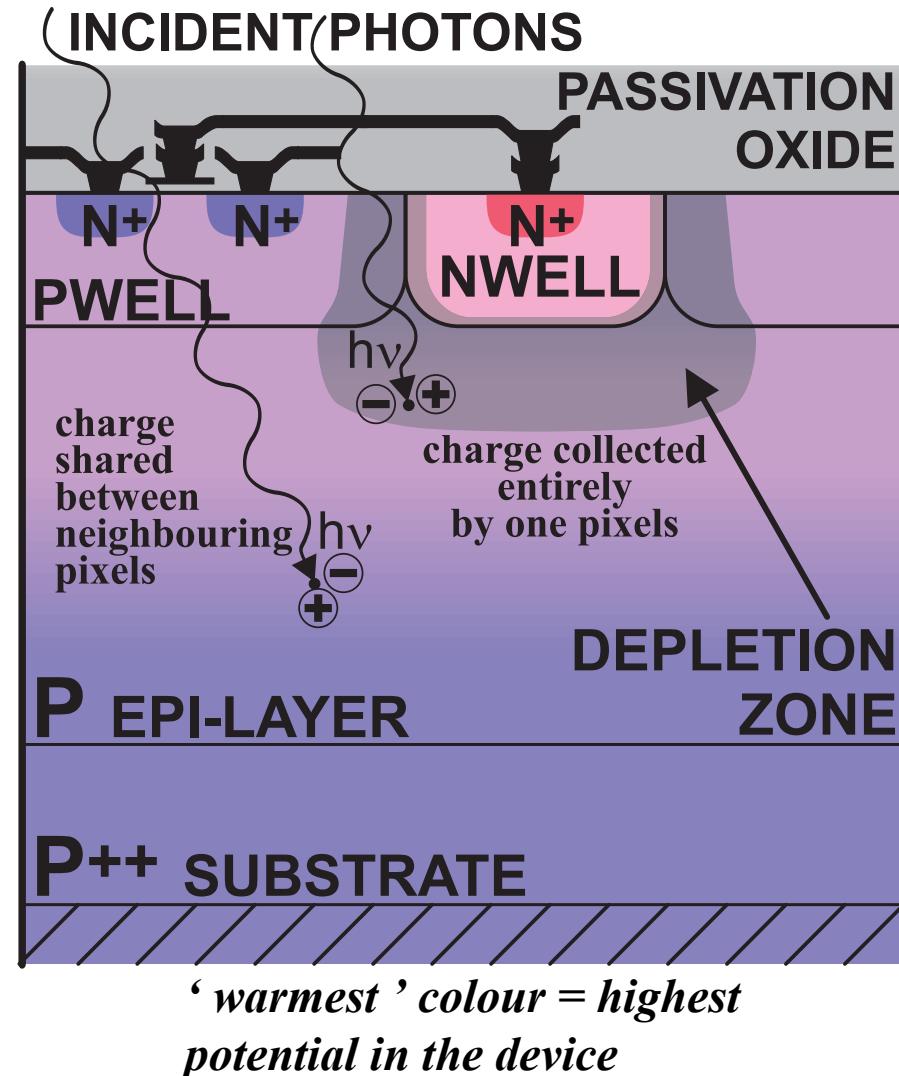
1999 - first small scale prototypes,

1999-2000 - first beam tests ($\sigma \sim 1.5 \mu\text{m}$, $\epsilon \sim 99\%$),

2001 - first large (10^6 pixels) scale prototype submitted,

Operation Principle of MAPS for Particle Detection

- Baseline architecture - similar to CMOS camera
- Twin-tub CMOS process on epitaxial wafer ...
- Typical epitaxial layer thickness ~ $10 \mu\text{m}$...
- Moderately doped epitaxial layer = long minority carrier lifetime ...
- Thin active volume = low signal expected ...



- Charges generated in non-depleted region collected through thermal diffusion (or they recombine...) ...
- Charge confined - potential barriers at layer interfaces - improving collection efficiency ...
- Active volume underneath the readout electronics \Rightarrow 100% fill factor; charge collected by deep n-well/p-epi diode.

Motivation for Monolithic Pixel Devices (I)**Motivation: Vertex Detector LC - TESLA****TESLA- 800×10^6 pixels**Charge Coupled Devices -

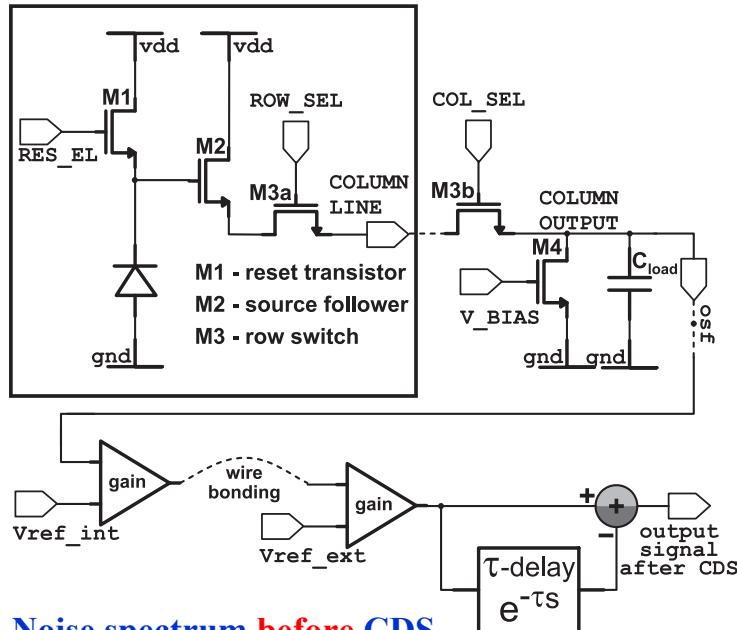
granularity ☺, material ☺ but RH ☹, speed ☹

Hybrid Pixels -

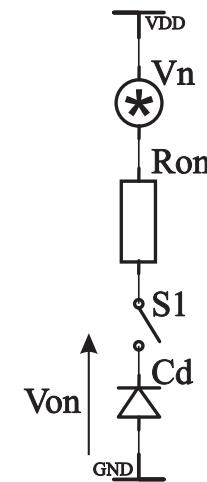
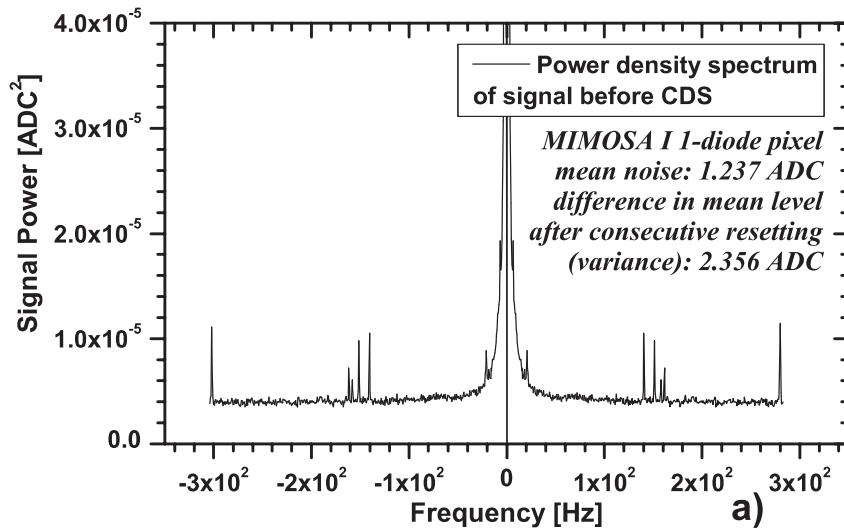
RH ☺, speed ☺ but granularity ☹, material ☹

Monolithic Active Pixel Sensors -
alternative combining good
features of both

CDS technique



Noise spectrum before CDS



① kTC noise suppressing

$$\sigma_{V_{on}}^2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(\omega)|^2 S_{Vn}(\omega) d\omega = \frac{kT}{C_d}$$

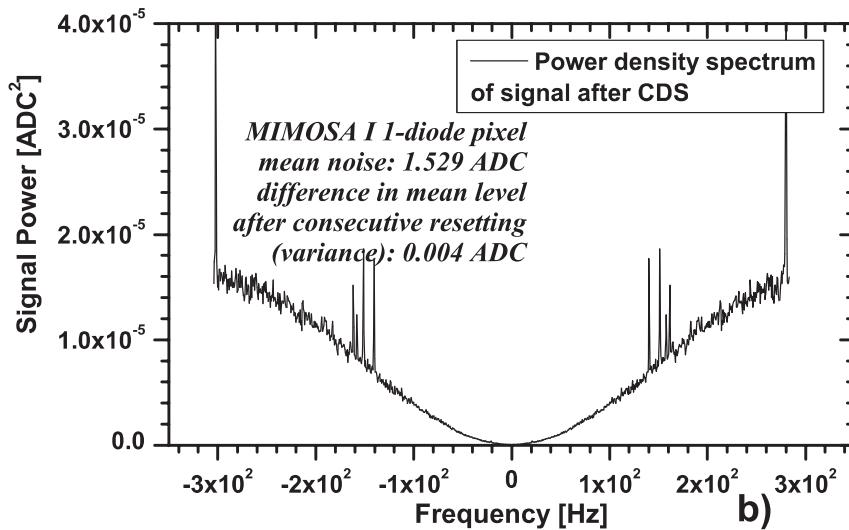
Noise kTC [V²]

② CDS processing transfer function

$$|H_{CDS}(f)|^2 = \frac{4f_{3dB}^2 \sin^2(\pi \tau f)}{f^2 + f_{3dB}^2}$$

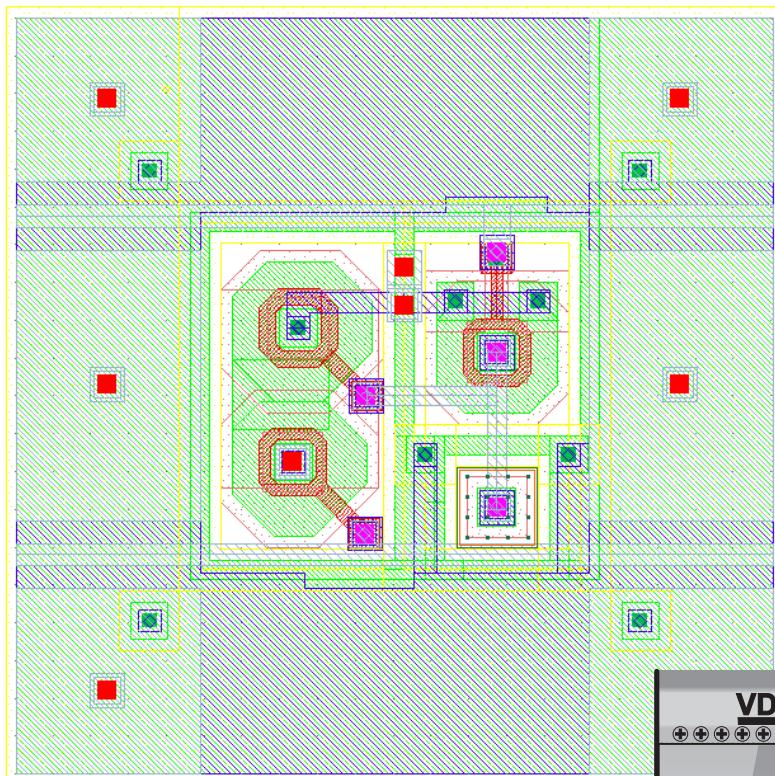
drops to 0 at f=0

Noise spectrum after CDS

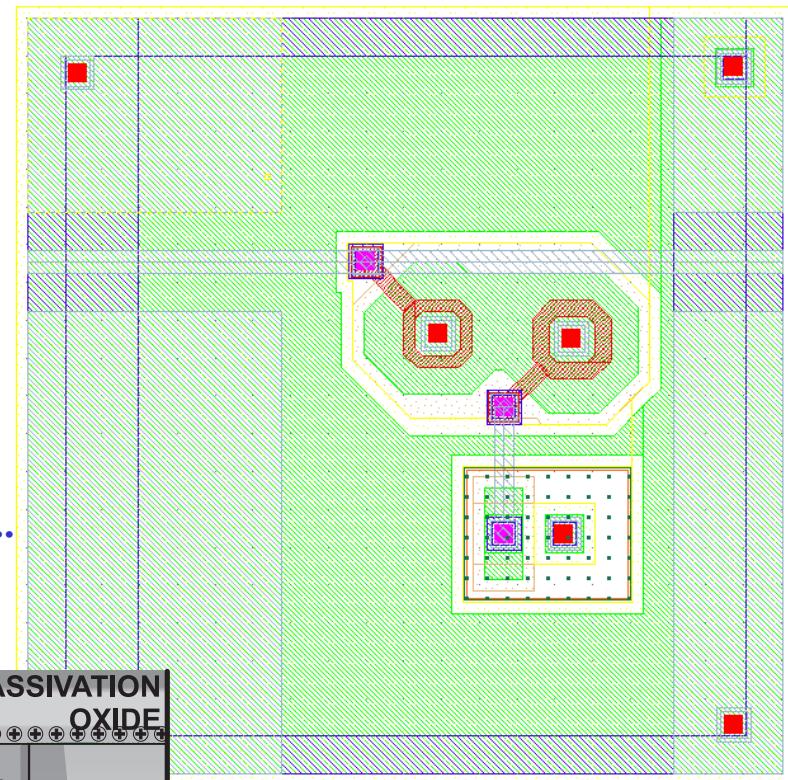


Radiation Hardness (III)

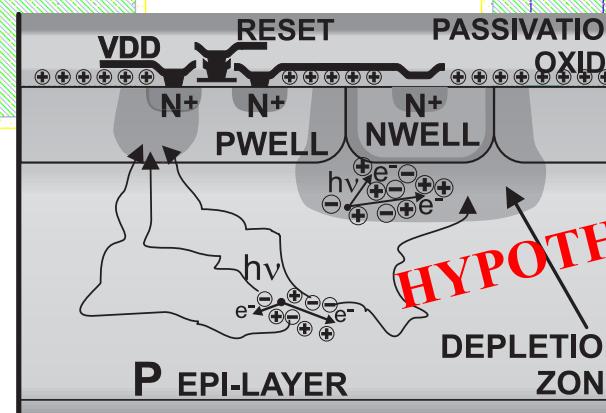
MIMOSA IV
pixel layout suffering from
poor charge collection



MIMOSA IV
pixel layout allowing good
charge collection

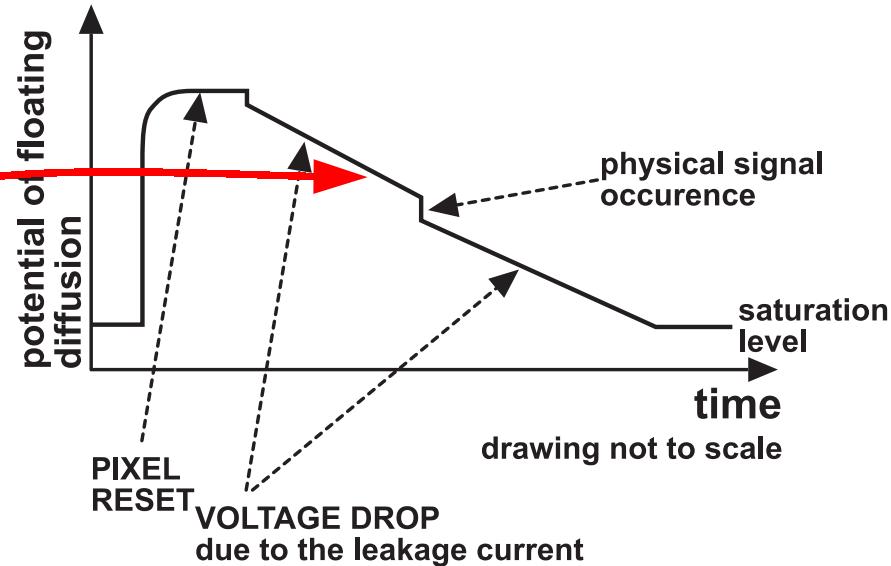
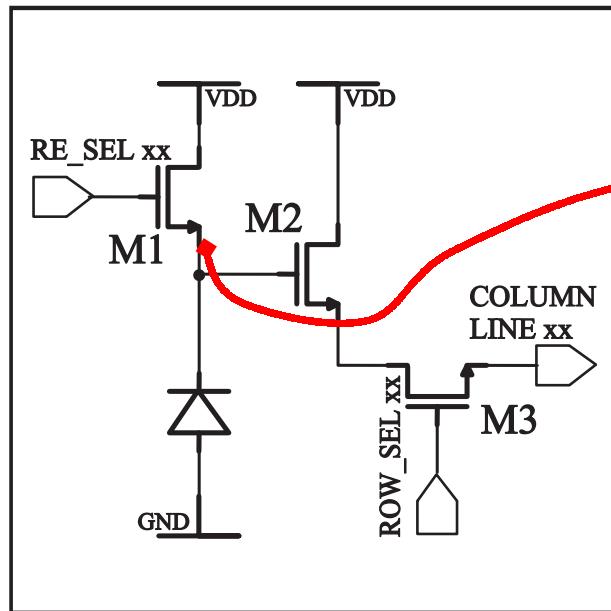


What is the
difference?
need for
thorough studies...



CSE* optimised for VXD environment (I) - self-reverse polarisation of diode

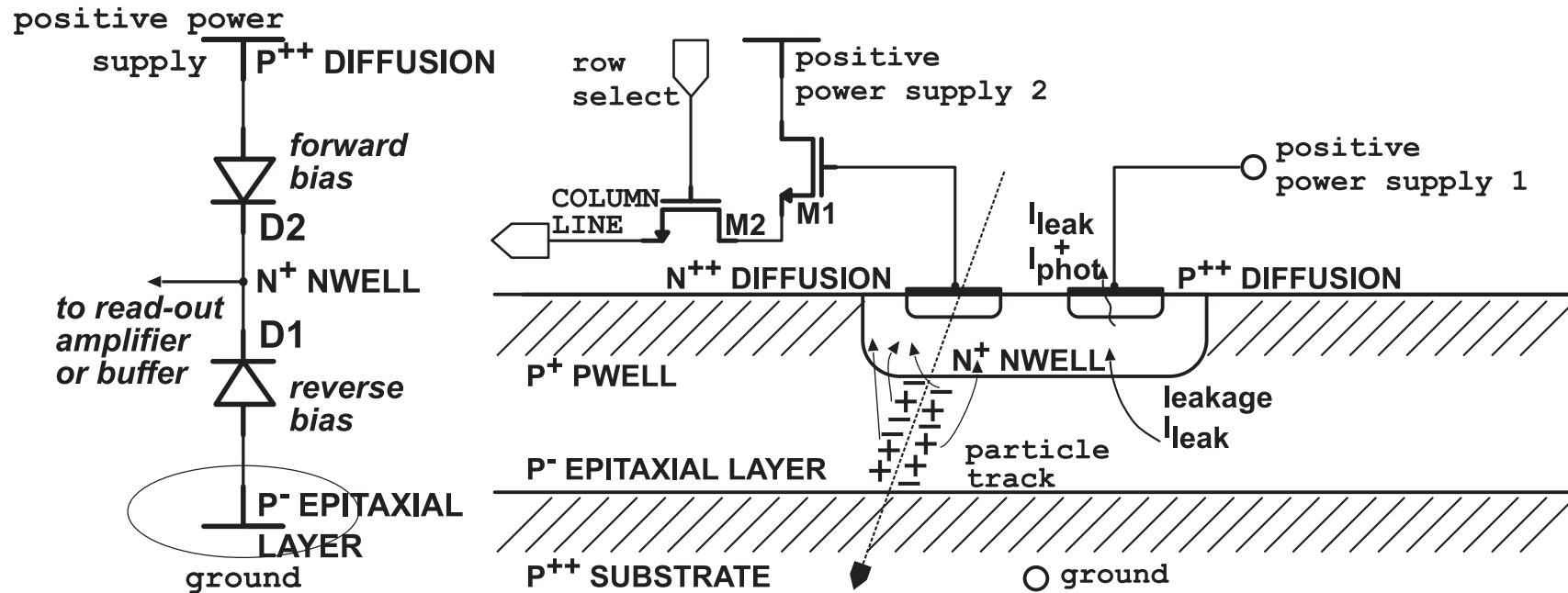
Classical 3T pixel design



- ◎ On-pixel amplification requires suppression of the leakage current effect - preserving charge integration!

CSE* optimised for VXD environment (II) - self-reverse polarisation

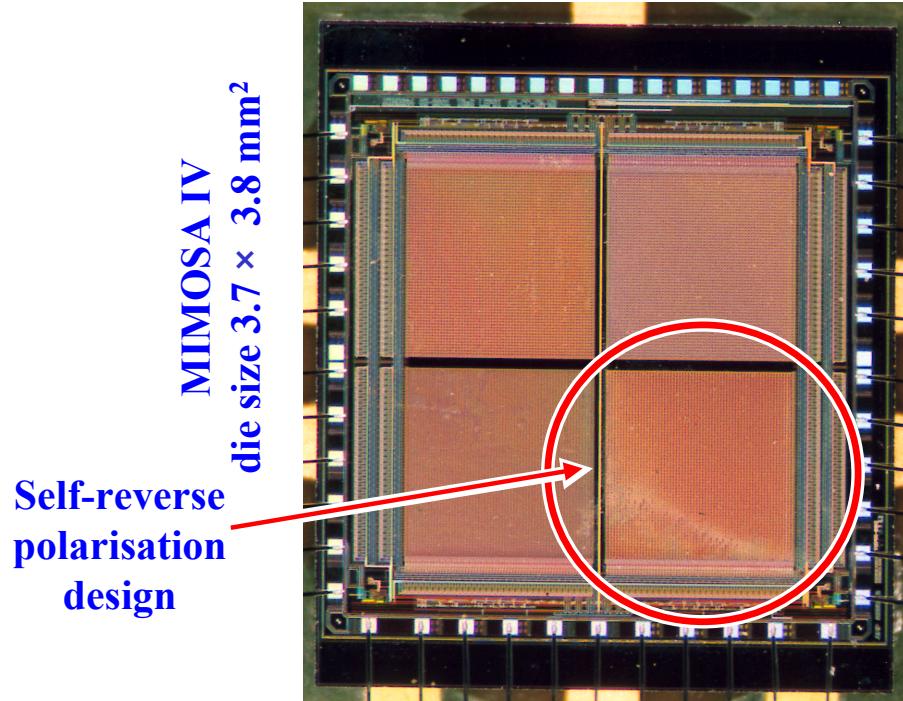
CSE Optimised for VX Environment



- ◎ Self-reverse polarisation of charge collecting diode,
- ◎ In darkness, the diodes D2 conveys only a small value leakage current, thus it represents very high value resistance ($10^9\text{-}10^{12}\ \Omega$).

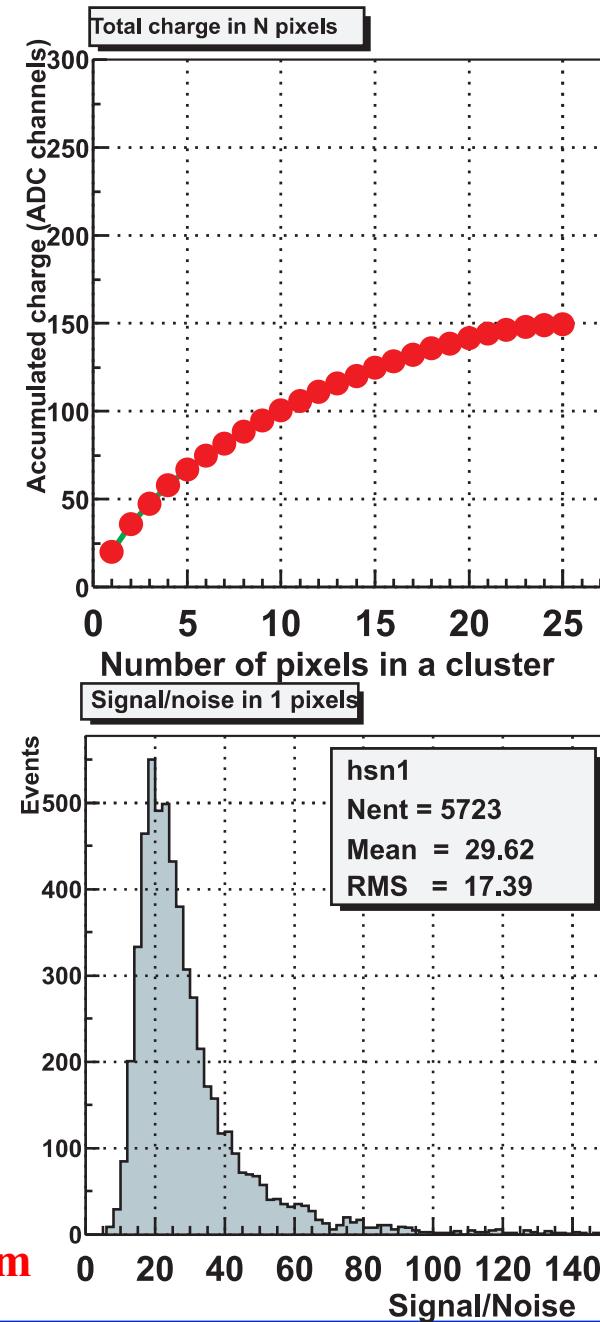
CSE Optimised for VX Environment
 - self-reverse polarisation design

- ◎ Charged particle detection performance,



- ◎ Charge Integration time $\sim 1\text{ms}$,
- ◎ Design particularity - non epitaxial substrate, but with low-doping level.

S/N ~ 30 but charge spread is wider and less peaked,
 $\varepsilon = \sim 99.7\%$, $\sigma = \sim 4\mu\text{m}$

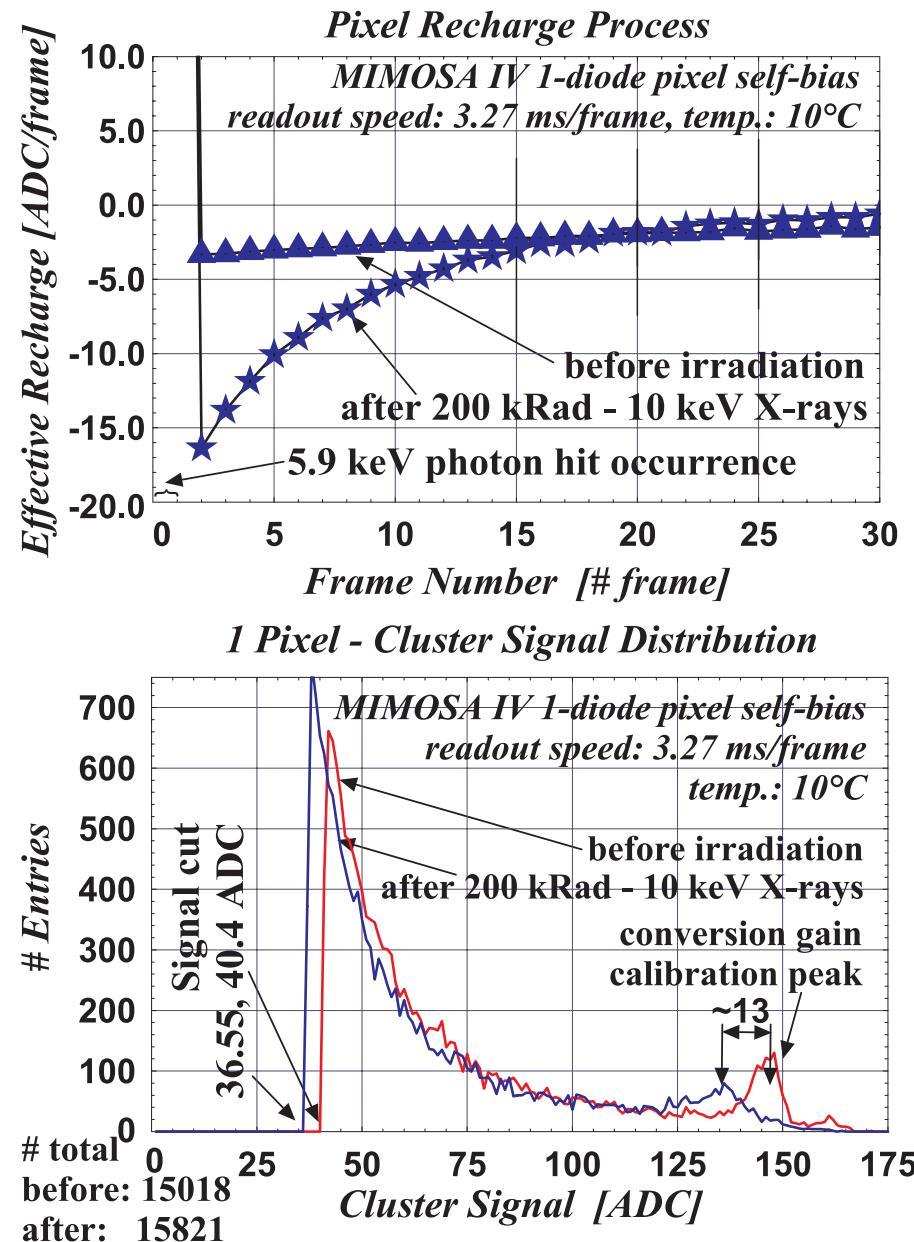


CSE Optimised for VX Environment - self-reverse polarisation design

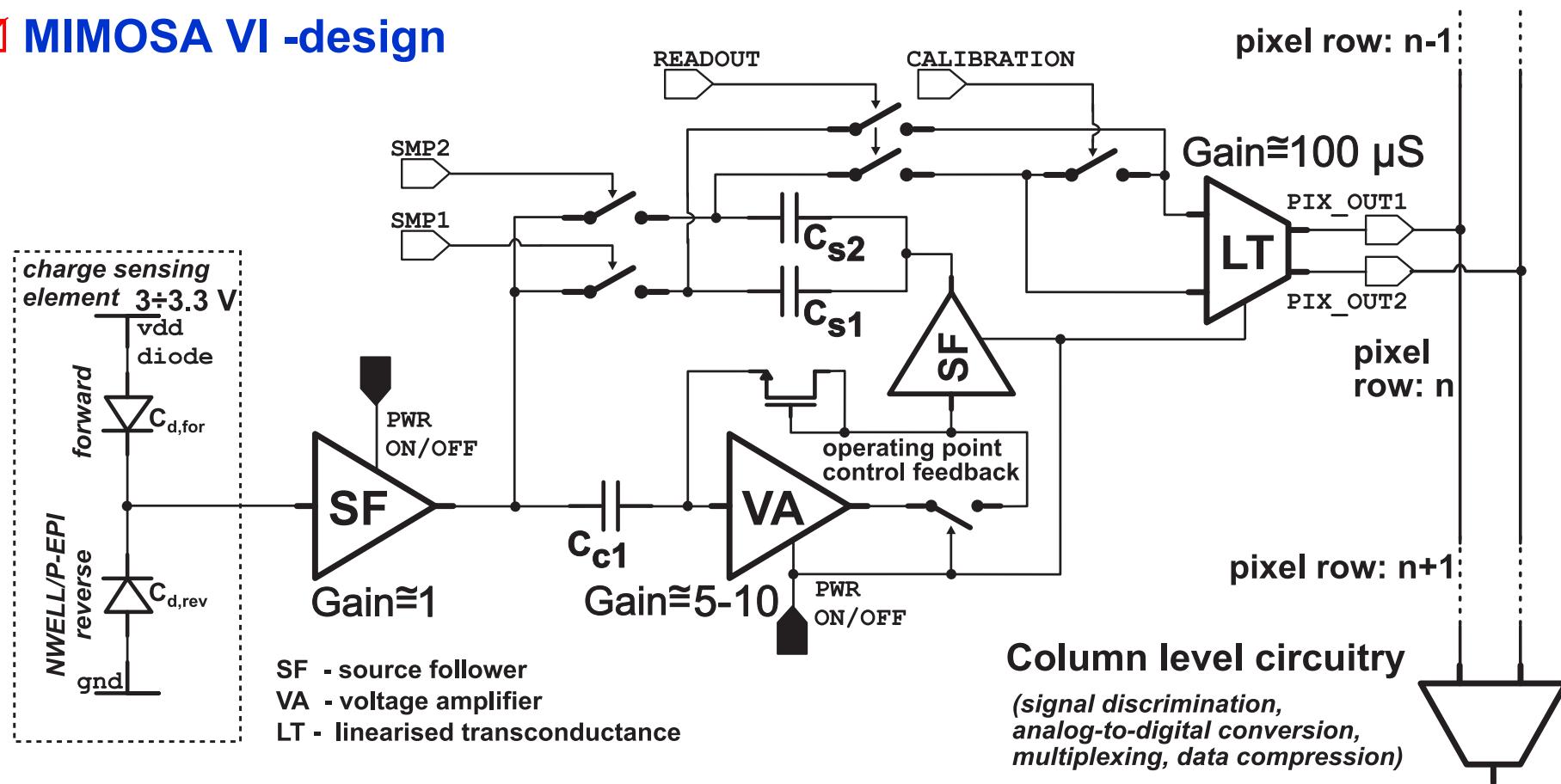
- ④ Efficiency of keeping reverse polarisation at high discharging resistance,

Speed of effective recharge of the charge sensing node after ^{55}Fe X-ray photon hit
 $>100\text{ADC}$.

Threshold correction in hit finding procedure for ^{55}Fe X-ray source.

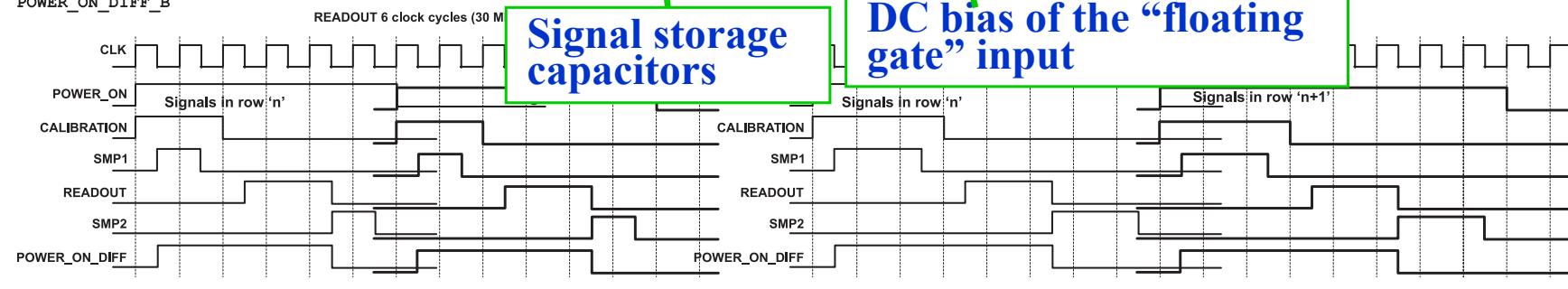
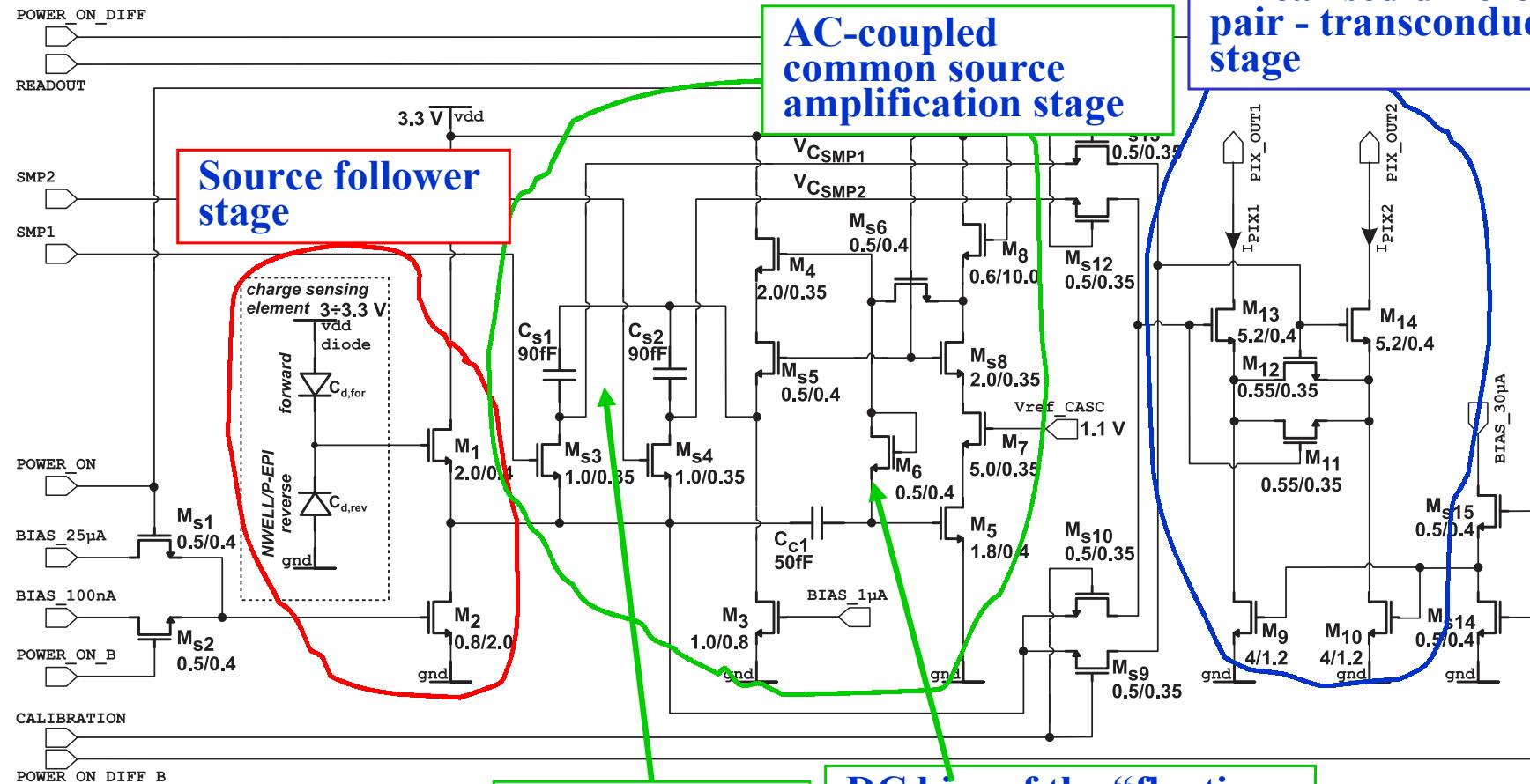


MIMOSA VI -design



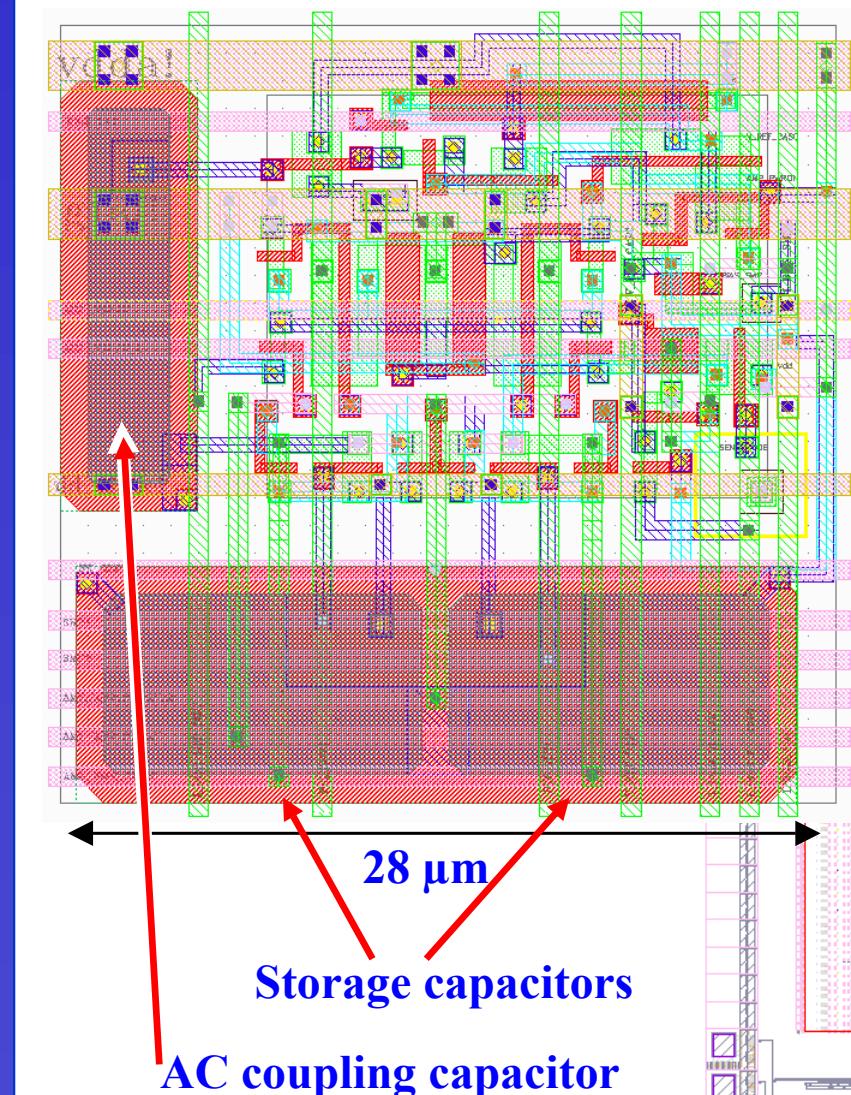
- ◎ Charge converted to voltage on diode cathodes; resulting voltage buffered by SF,
- ◎ Amplified voltage stored on first capacitor,
- ◎ Second capacitor stores amplified voltage from previous cycle,
- ◎ The signals are substracted on the transconduction stage, and currents sent for discrimination,
- ◎ Differential voltage gain $\sim 0.10 \text{ mV/e}^-$, differential current gain $\sim 9 \text{ nA/e}^-$.

MIMOSA VI - design



MIMOSA VI - design

Single pixel layout



◎ Pixel design features:

- only NMOS transistors, nwell/p-epi and pdiff/nwell diodes and poly1-to-poly2 capacitors.

◎ MIMOSA VI key design features

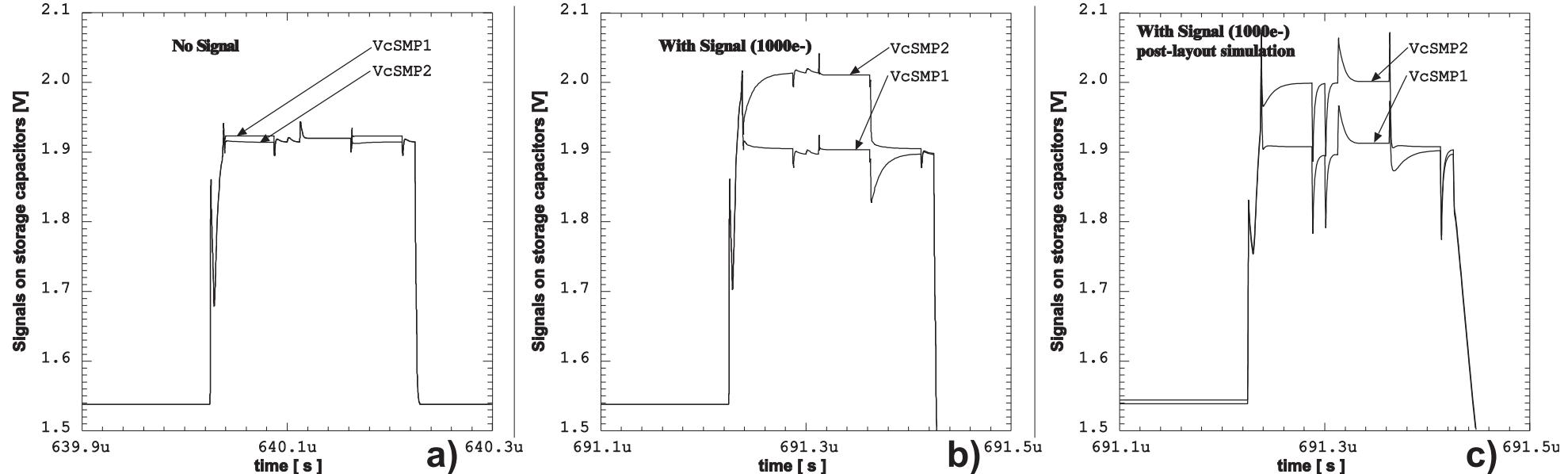
- **0.35 μm CMOS 4.2 μm thick EPI layer,**
- 1 array $(24+6) \times 128$ pixels, pitch $28 \times 28 \mu\text{m}^2$,
- 24 columns read-out in parallel,
- 30 MHz f_{clk} , 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size $4.0 \times 3.7 \mu\text{m}^2$ - 3.5 fF ,

MIMOSA VI chip layout (IReS-LEPSI/DAPNIA collaboration)



MIMOSA VI - simulation

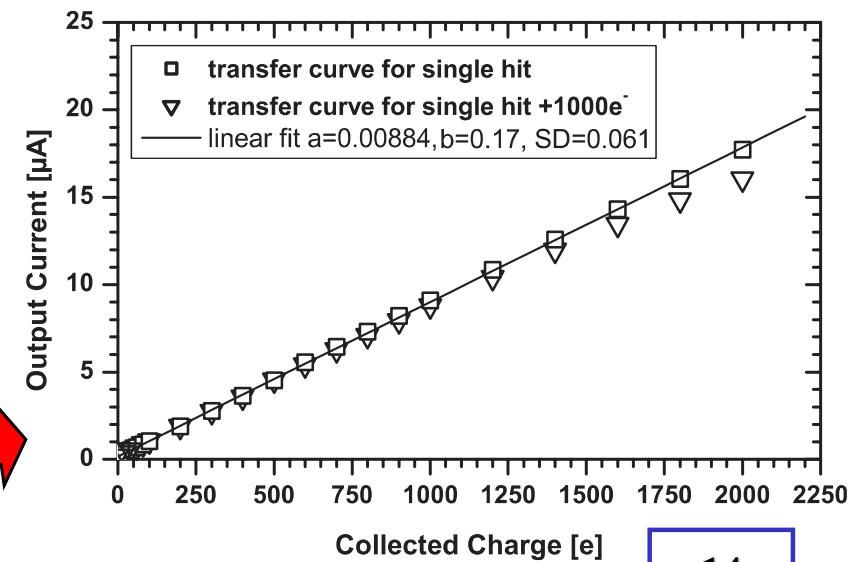
◎ SPICE simulation of pixel response



voltage on two storage capacitors:

- (a) in absence of any charge deposited,
- (b) for signal of 1000 e⁻ (schematic) $\sim 0.10 \text{ mV/e}^-$,
- (c) post layout simulation $\sim 0.09 \text{ mV/e}^-$.

Current gain of the pixel as function of charge acquired



MIMOSA VI - analogue part - preliminary results

Pixel readout phases

30-Mar-03

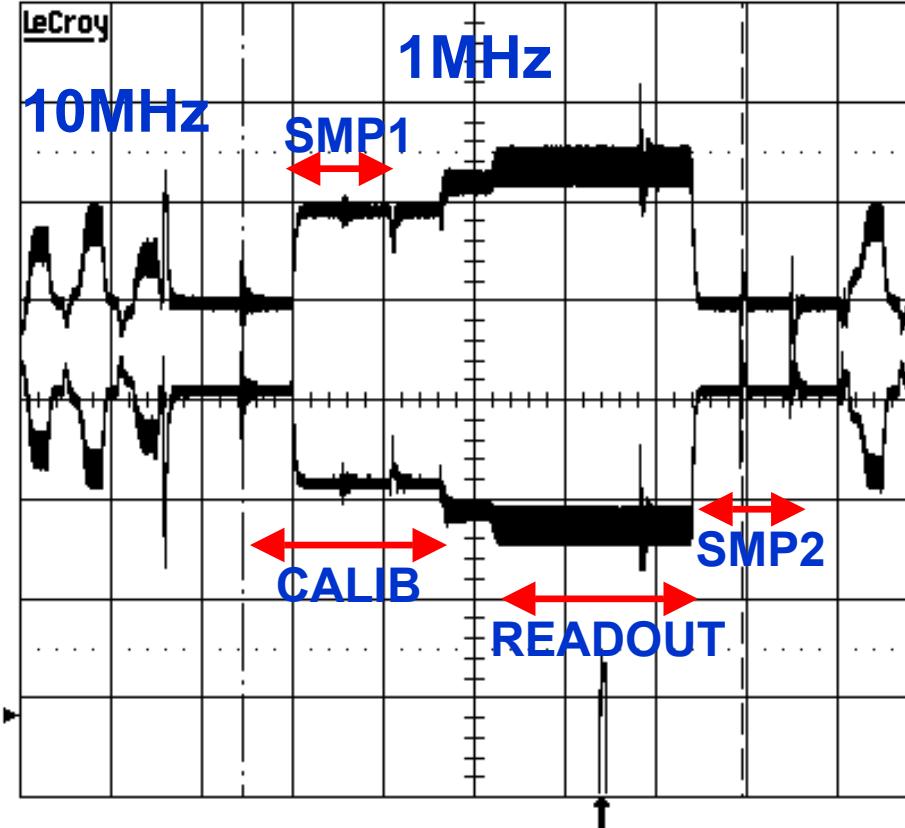
0:59:28

1
1 μ s
35.0mV
5.50 μ s
2744 swps

2
1 μ s
35.0mV
5.50 μ s
2744 swps

3
1 μ s
2.00 V
5.50 μ s
2744 swps

no source (analog persistane)



CHANNEL 1

Coupling

DC50 Ω
Grounded
DC1M Ω
Grounded
AC1M Ω

V/div OFFset

NORMAL
ECL TTL

BWL

OFF
20MHz 200MHz

Probe Atten-

x1
x2
x5
x10
x20

1 GS/s

■ NORMAL

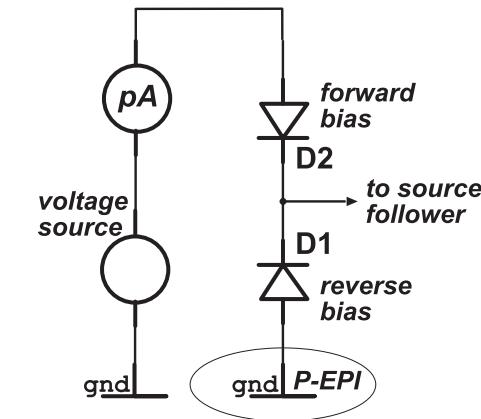
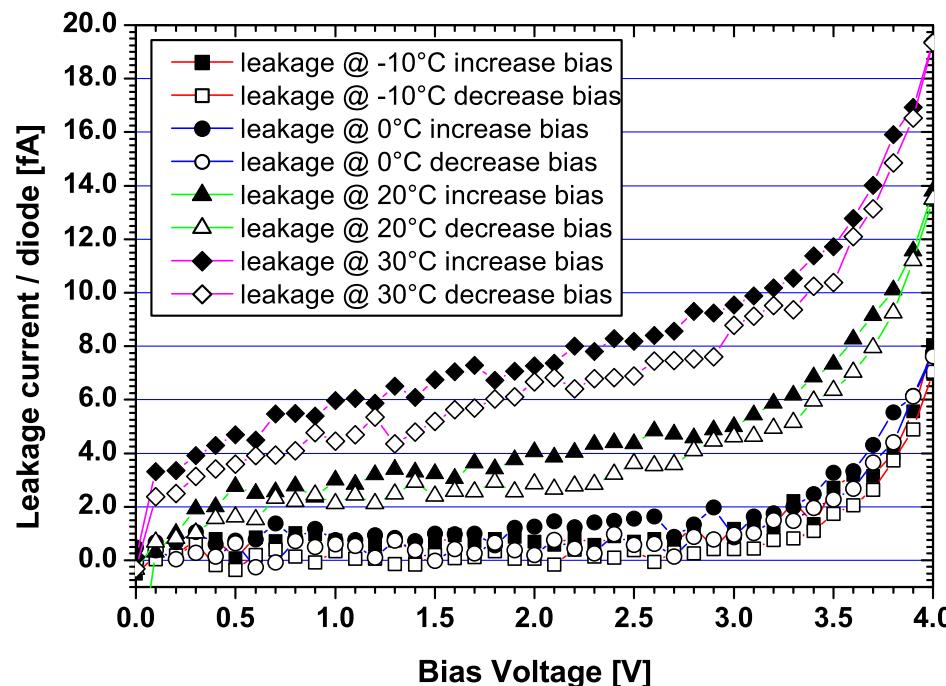
MIMOSA VI - analogue part - preliminary results

diode parameters ...

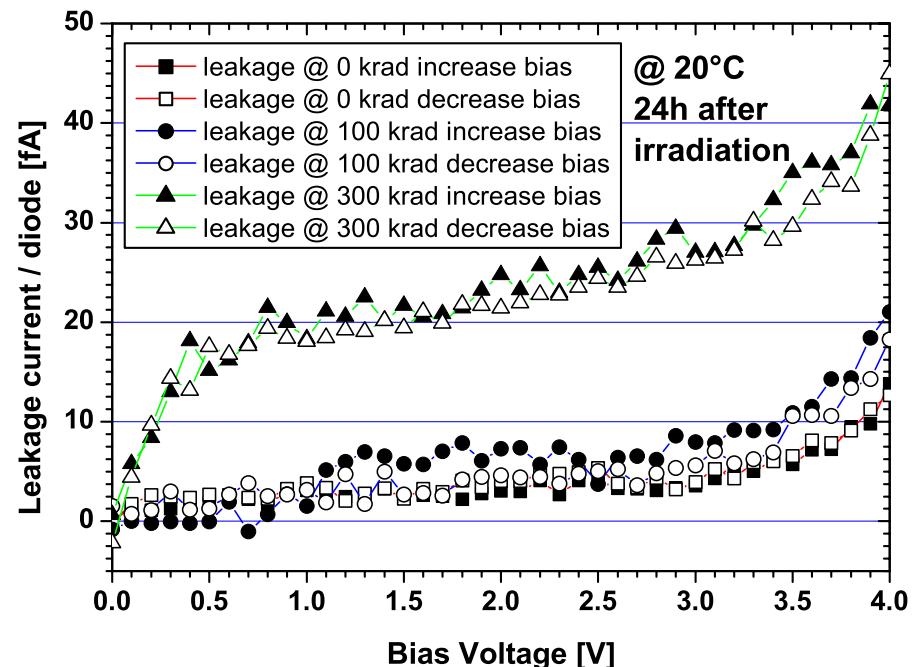
Leakage current measurements

$$I_{\text{diode}} = I_{\text{total}} / (30 \times 128)$$

T=-10°C, 0°C, 20°C



D=0 krad, 100 krad, 300 krad

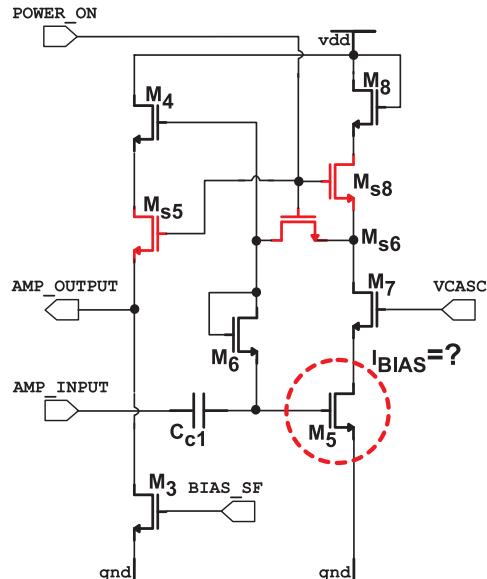


(unbiased)

MIMOSA VI - analogue part - preliminary results

Other results...

On-pixel amplifier bias current



Test procedure:

@ $f_{clk}=10MHz$

Analogue power supply current

$VCAS=1.1 V$

$I=15.1502 mA$

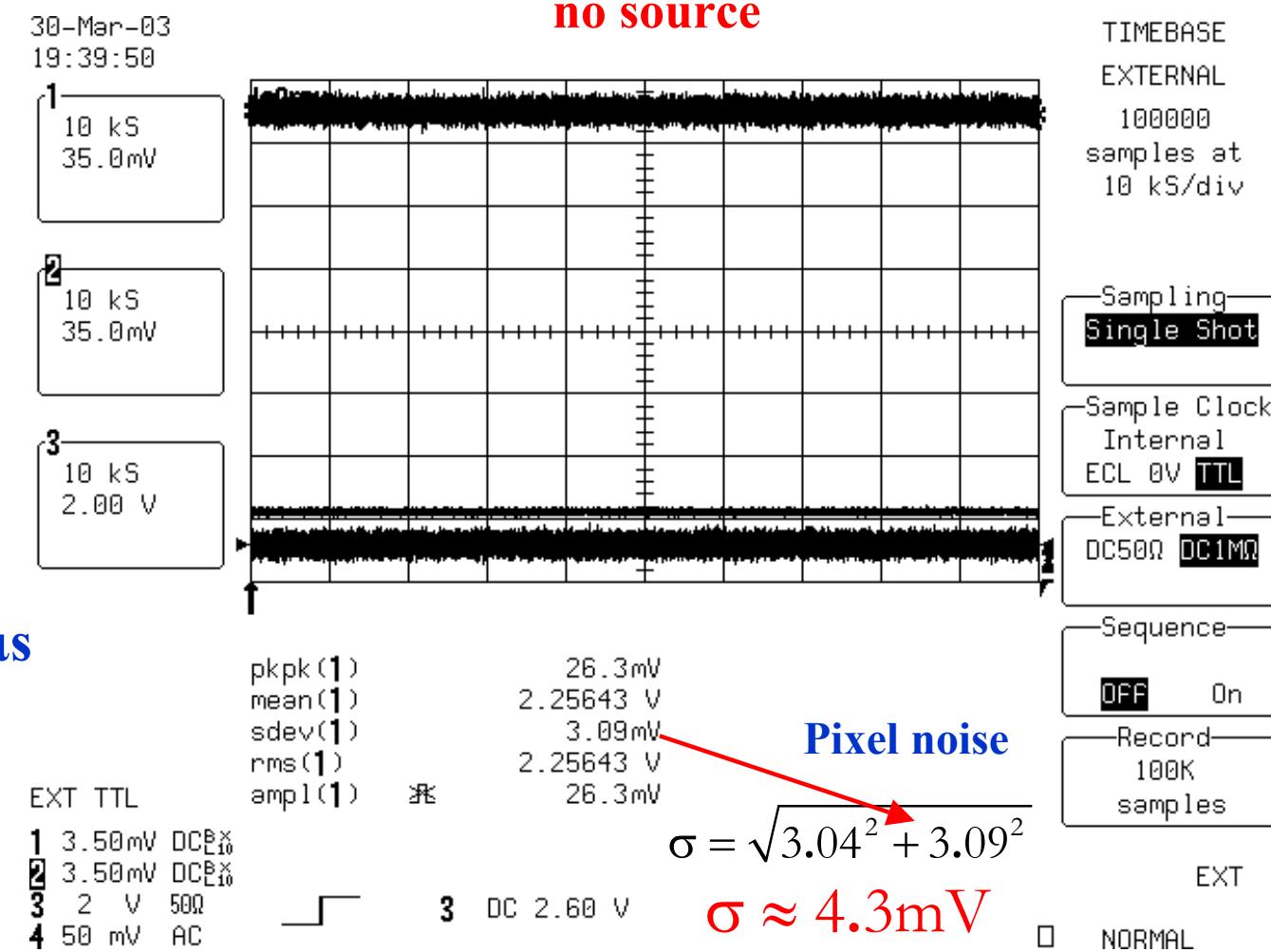
$VCAS= 0 V$

$I=14.9815 mA$

$$\Rightarrow I_{BIAS}=5.6 \mu A$$

MIMOSA VI - analogue part - preliminary results

Differential output sampled during READ_OUT phase



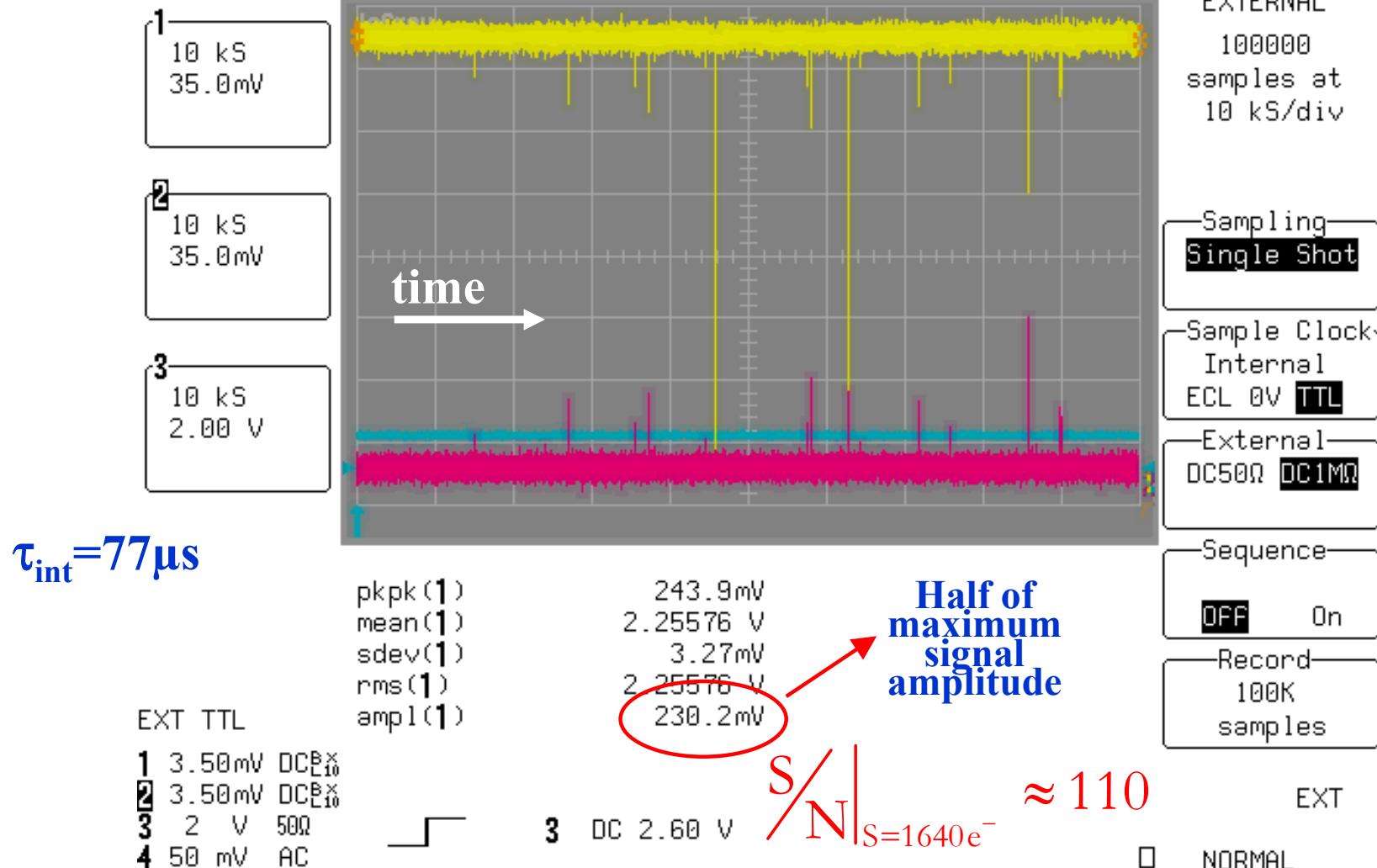
digital 8bit oscilloscope, single channel, external sample clock, 100k samples

MIMOSA VI - analogue part - preliminary results

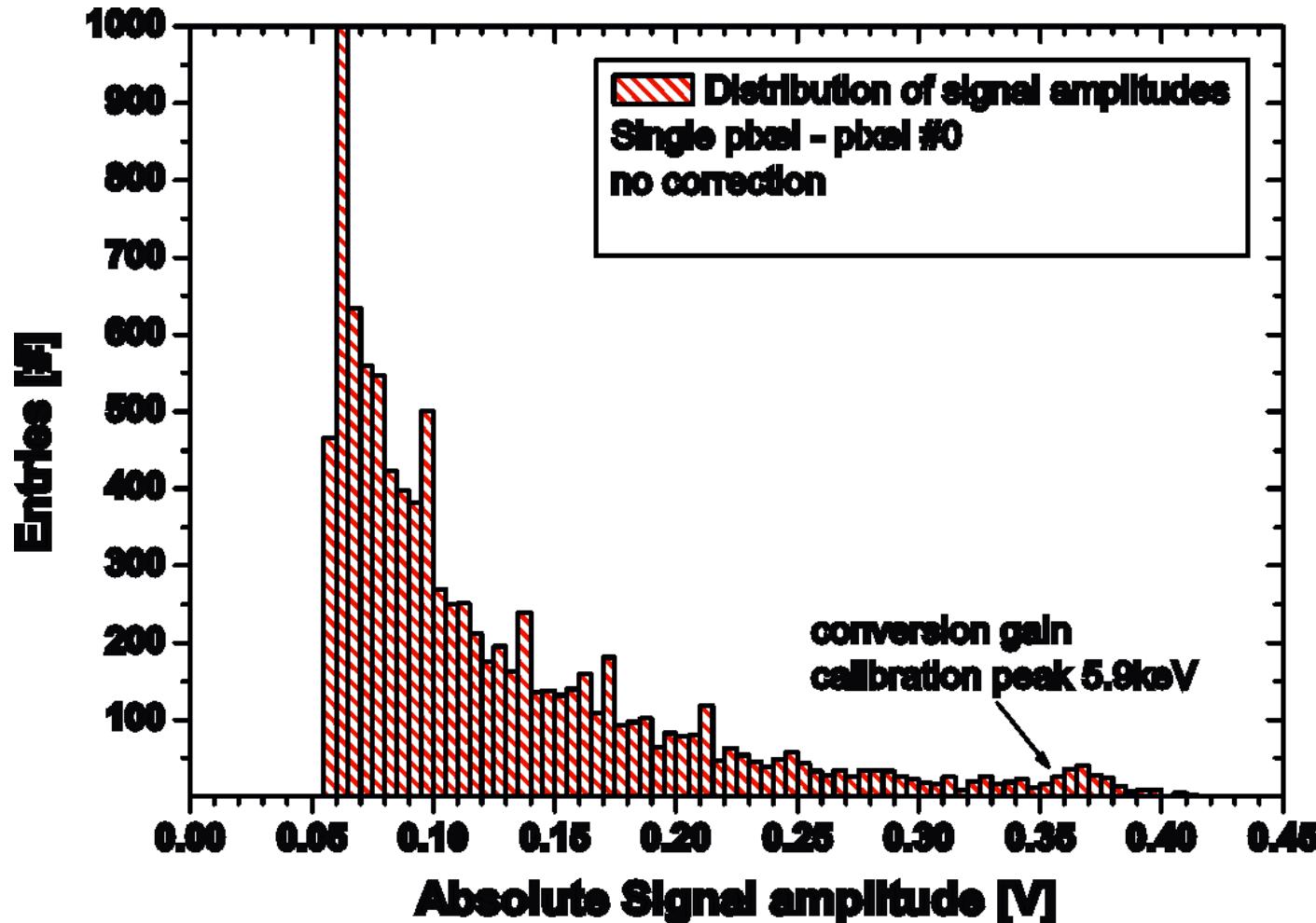
Differential output sampled during READ_OUT phase

30-Mar-03

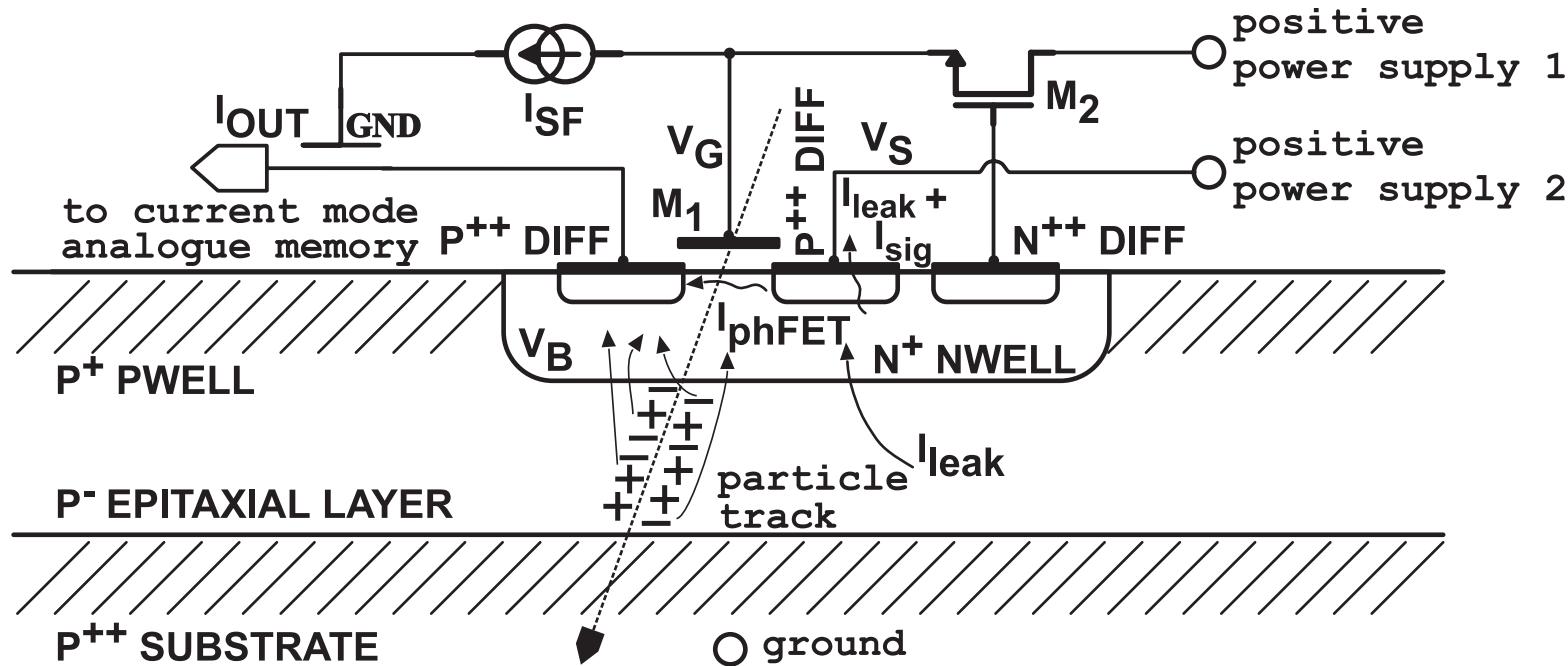
20:23:19

⁵⁵Fe source

digital 8bit oscilloscope, single channel, external sample clock, 100k samples

MIMOSA VI - analogue part - preliminary results Differential output sampled during READ_OUT phaseSingle pixel ^{55}Fe source spectrum (integration time = 77 μs)

Current mode CSE - *photofET*



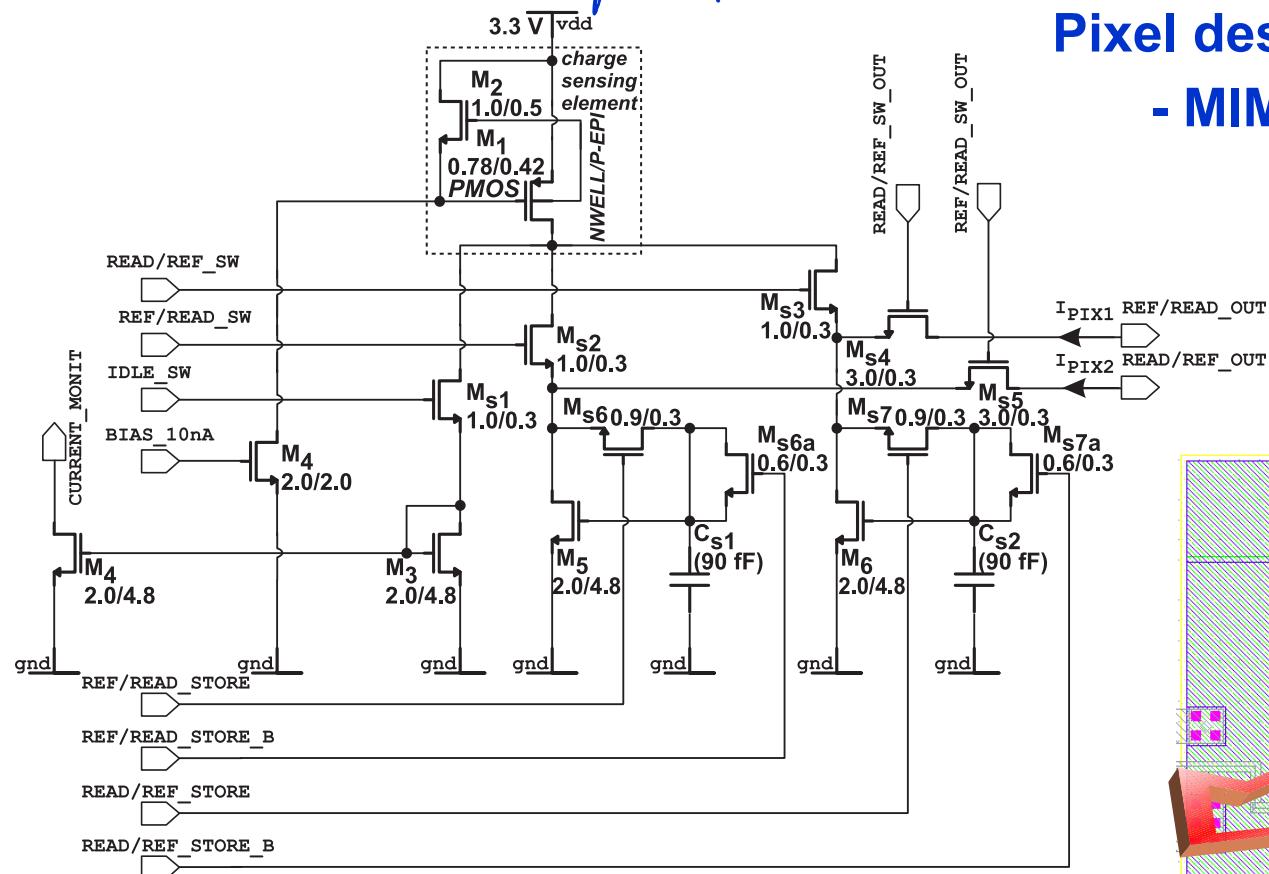
◎ DC bias photoFET current

$$I_{\text{OUT,strong}} = \frac{1}{2} \frac{W}{L} \mu C_{\text{ox}} (V_{GS}(I_{\text{SF}}) - V_{TH})^2, \quad \text{where } V_{TH} = V_{TH0} + \gamma \sqrt{2|\phi_F| - V_{BS}} - \sqrt{2|\phi_F|}$$

◎ Small-signal photoFET current

$$i_{\text{out}} = g_{mb,M_1} \cdot v_{bs,M_1} + \frac{g_{m,M_2}}{g_{m,M_2} + g_{mb,M_2}} \cdot g_{m,M_1} \cdot v_{bs,M_1}$$

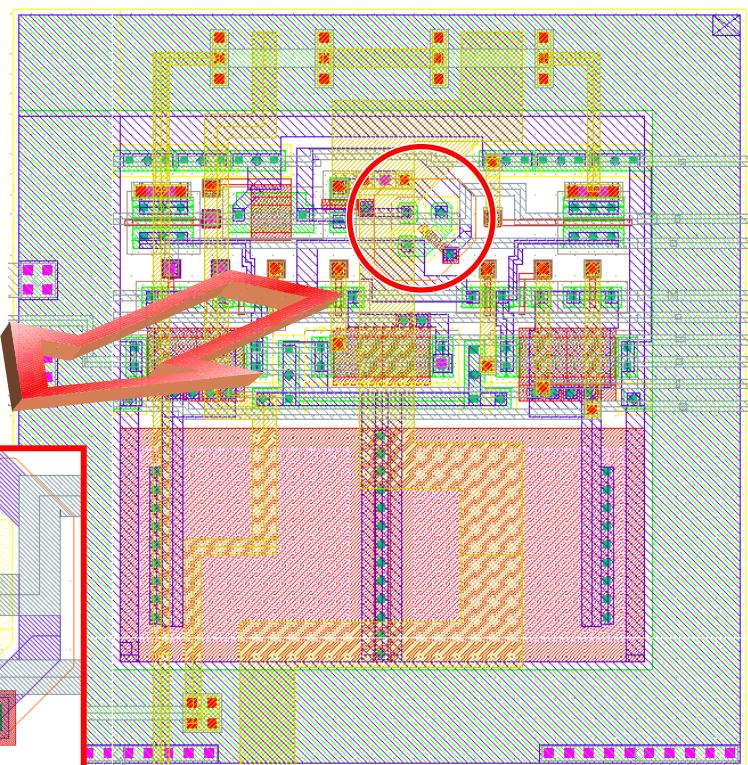
Current mode CSE - *photofET*



Pixel design with *photofET* element
- MIMOSA IV test structure

photofET layout
non-epi 0.35µm, MIV

26.00 µm



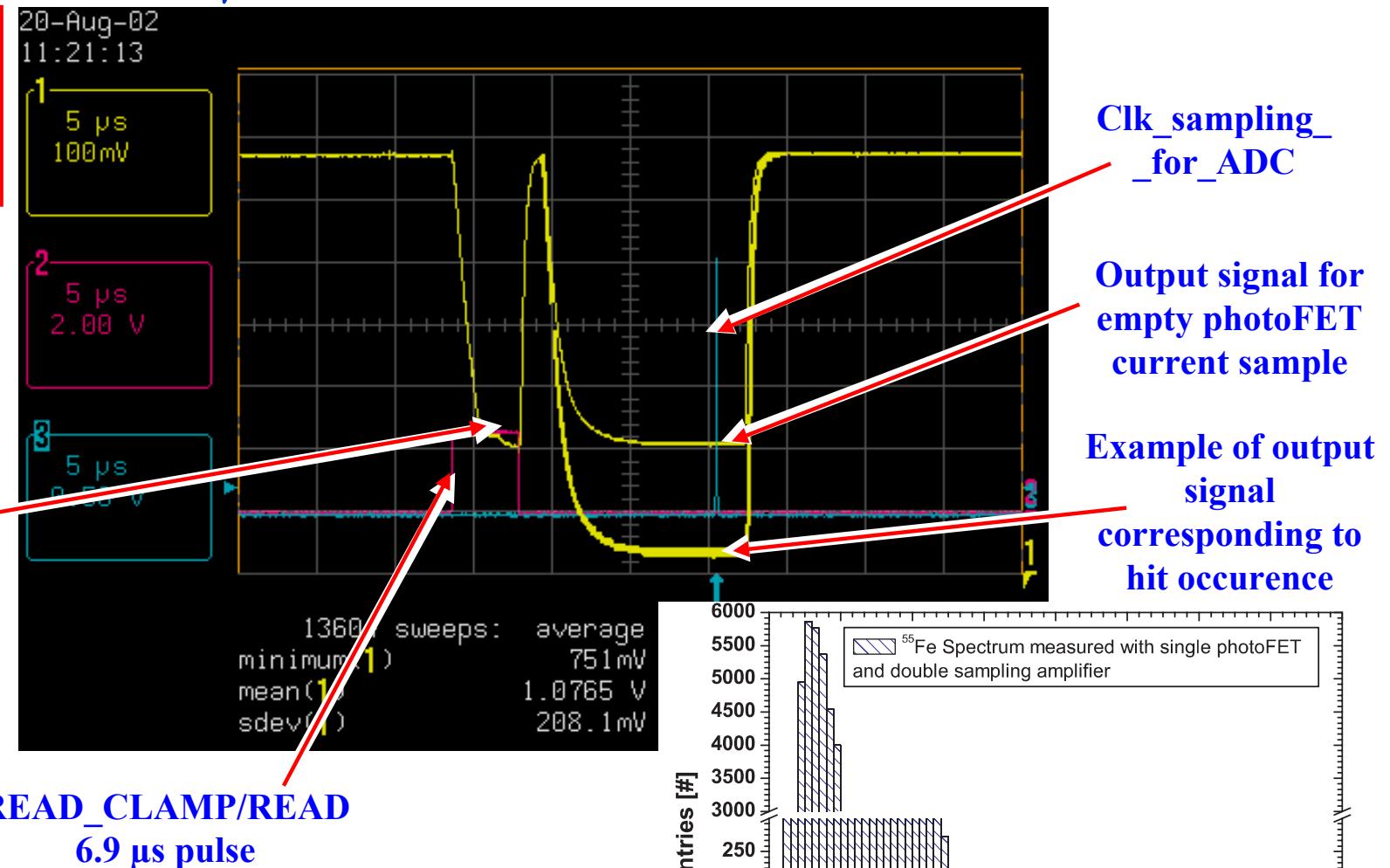
◎ ADVANTAGES of *photofET*:

- DC bias = high transconductance
- Easy current mode memory on pixel
- Continuous signal monitoring - wired OR

Current mode CSE - *photofET*

◎ Detection performance of ^{55}Fe X-ray photons

Readout of reference current and clamping output to V_CLAMP



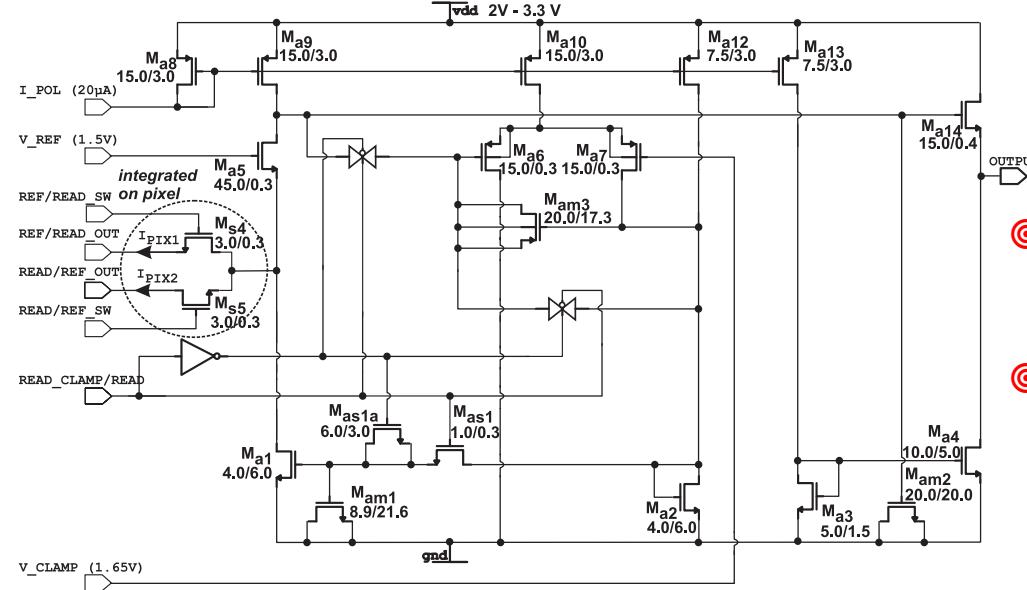
READ_CLAMP/READ
6.9 μs pulse

Clk_sampling_for_ADC

Output signal for empty photoFET current sample

Example of output signal corresponding to hit occurence

Current mode CSE - photoFET



◎ MIMOSA IV; Transimpedance chopper-stabilised amplifier with double sampling operation

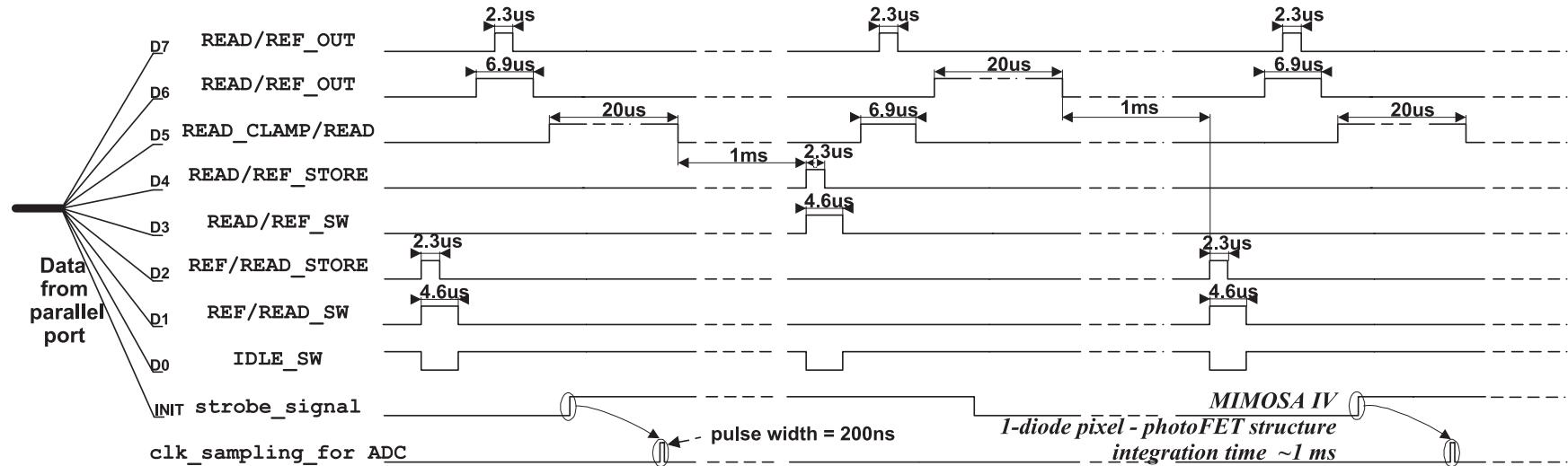
◎ DC output response

$$V_{\text{OUTPUT}} = V_{\text{CLAMP}} - V_{G_S, M_{a14}}$$

◎ Small-signal output response

$$V_{\text{OUTPUT}} = \frac{g_{m, M_{a14}}}{g_{m, M_{a14}} + g_{mb, M_{a14}}} \cdot \frac{1}{g_{ds, M_{a9}}} \left(i_{\text{REF/READ_OUT}} - i_{\text{READ/REF_OUT}} \right)$$

Timing for Read-out of photoFET Pixel and Transimpedance Double-Sampling Amplifier

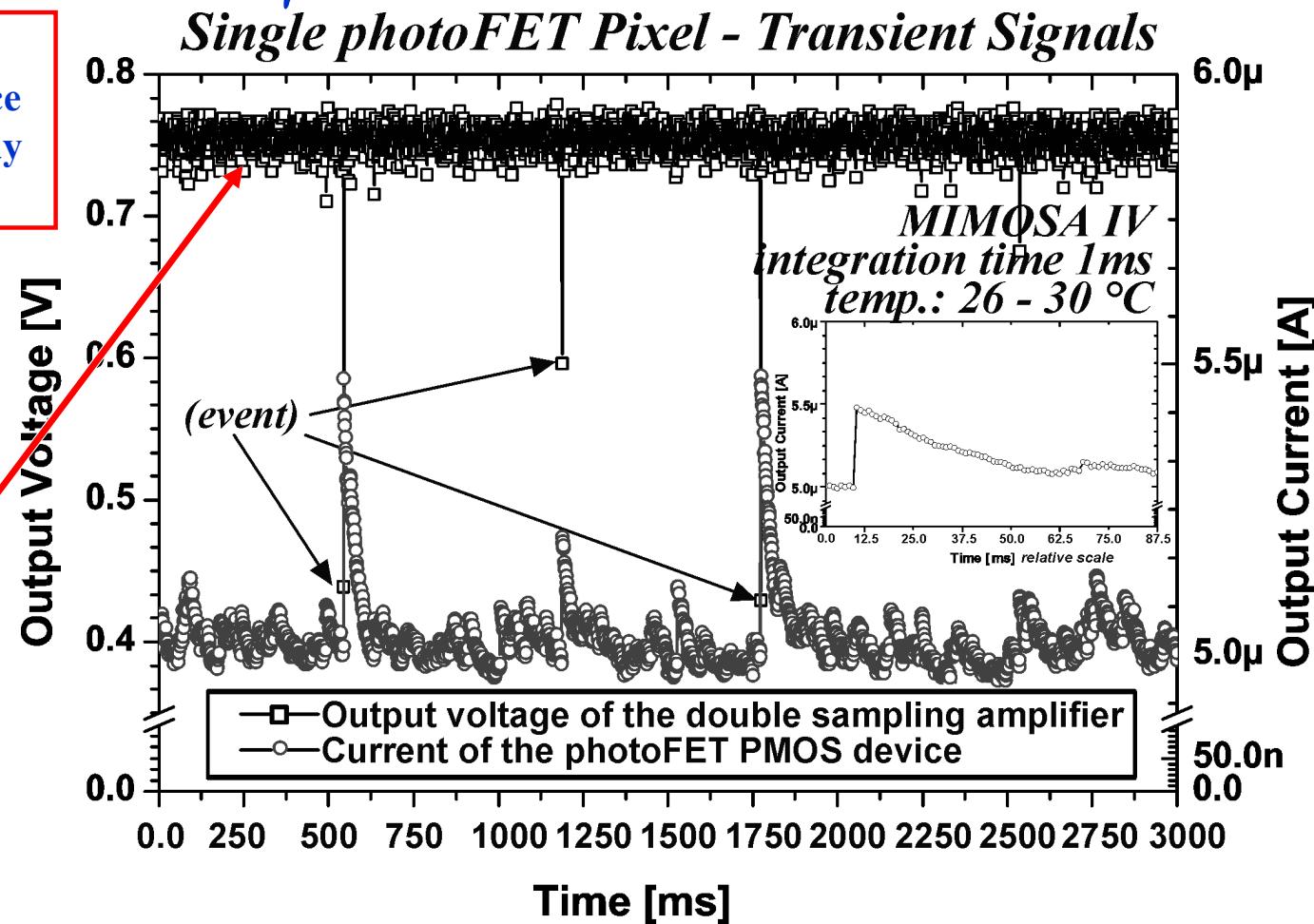


◎ Test performance - $r_{\text{transimp}} = 600 \text{ k}\Omega$

Current mode CSE - *photoFET*

- ◎ Detection performance of ^{55}Fe X-ray photons

- ◎ MIMOSA IV; Transimpedance chopper-stabilised amplifier with double sampling operation



- ◎ Summary of performances measured with single pixel prototype:

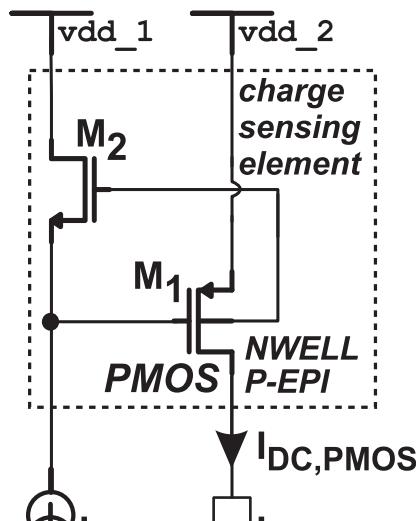
$$G_{q \rightarrow I} \approx 330 \frac{\text{pA}}{e^-} \quad \text{Noise} \quad \sigma = 1.4 \text{ nA} \div 2.7 \text{ nA}$$

$$G_{q \rightarrow V}^{\text{CDS}} \approx 183 \frac{\mu\text{V}}{e^-} \quad \text{Noise} \quad \sigma_{\text{output}}^{\text{CDS}} = 6 \text{ mV} \div 8 \text{ mV}$$

Current mode CSE - *photoFET*

Operation modes

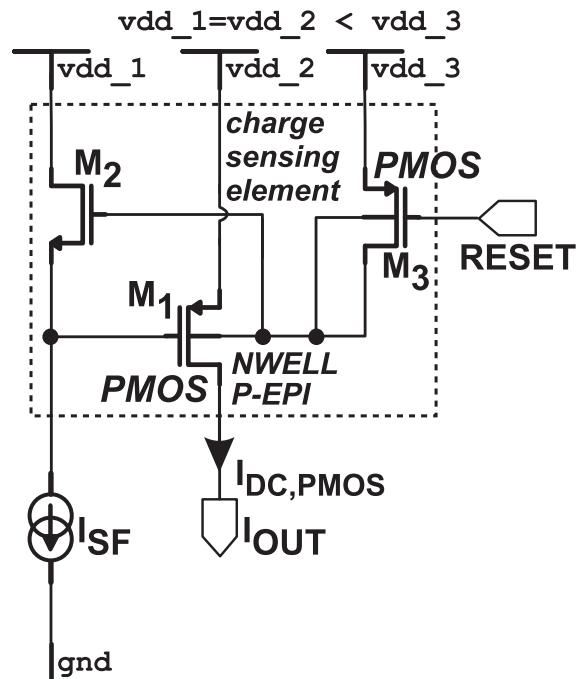
◎ Auto reverse polarisation



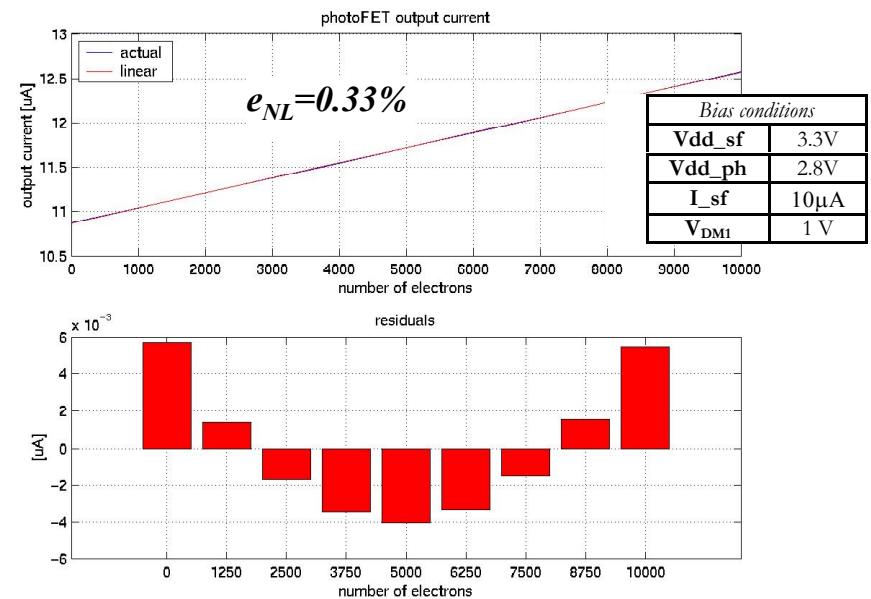
① weak inversion, I_{DC,PMOS}=low

$$V_{BS,M1} \propto \ln(\Phi + I_{leak}) \Rightarrow I_{DC,PMOS} \propto e^{(V_{BS,M1} + V_{GS,M2})}$$

◎ Charge integration with reset transistor



- Not easy analytical form ... but for integration mode ...



Paths for new chip design ...

"fast, high resolution, and macroscopic size MAPS detector"

◎ Use of linear sensor - 3T approach:

- Off-line CDS - « *no intelligence* » - (*MIMOSA V*),
- DDS - *kTC noise, column-level processing (sparsification)*.

◎ Use of self-reverse biased sensor:

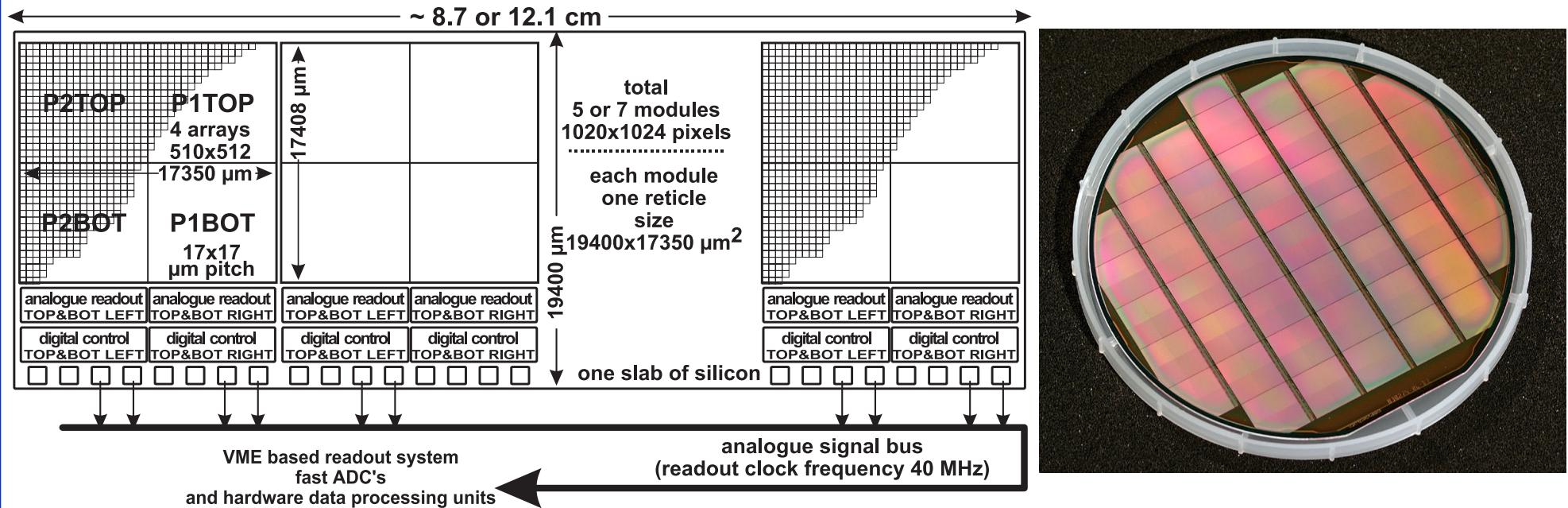
- Both readout modes as for linear sensors,

- On-pixel amplification {
- Voltage mode - charge-to-voltage conversion - *amplification, auto-zeroing, difference calculation, column-level processing (sparsification)* - (*MIMOSA VI*),
 - Current mode - charge-to-current conversion - *amplification, memory cells, column-level processing (sparsification)* - (*photoFET MIMOSA IV*).

Paths for new chip design ...

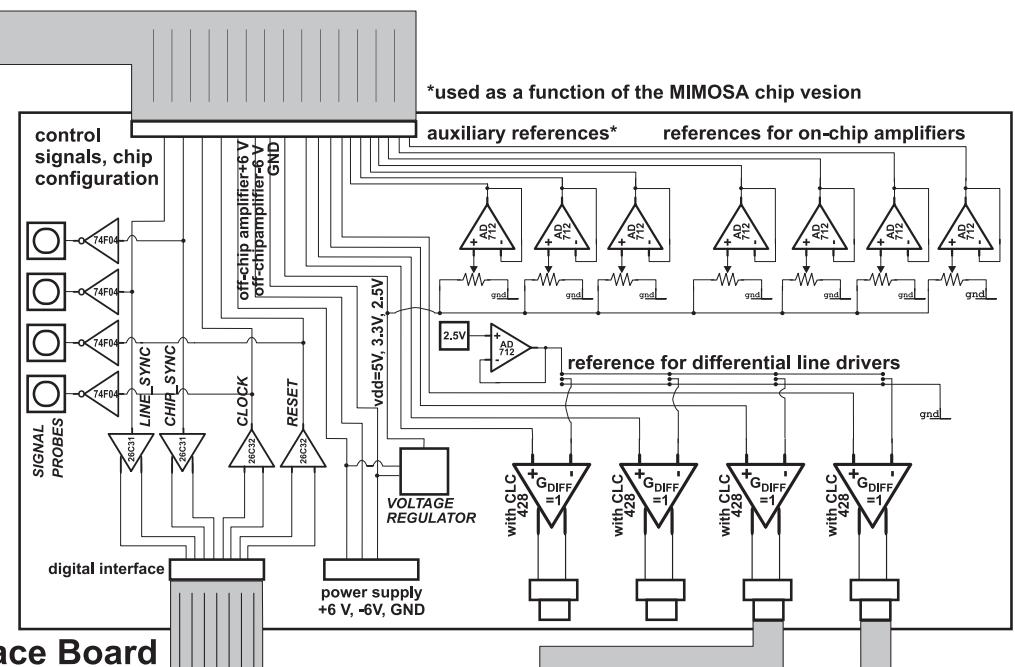
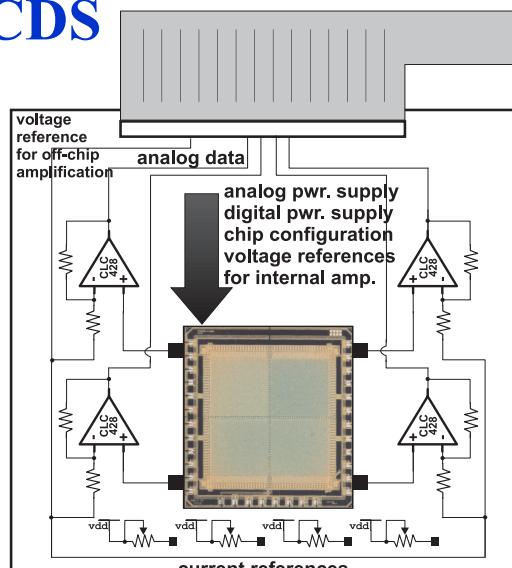
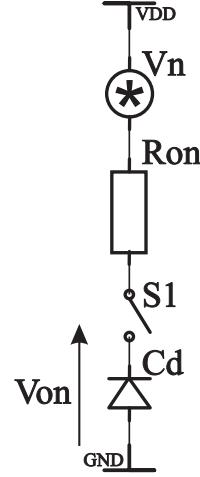
→ line represented by MIMOSA V:

- a) slow read-out (serialised pixel information),
- b) physical signal extraction with off-line CDS,
- c) non intelligent but slow read-out easily fits DAS,
- d) minimum **SNR ~10** for the seed pixel in order not to lose detection efficiency,
- e) parallelism in reading out information translates in practice to on chip data sparsification,
- f) Processing on-chip of CDS type (in non-aggressive way) requires **memory (digital)** - space??

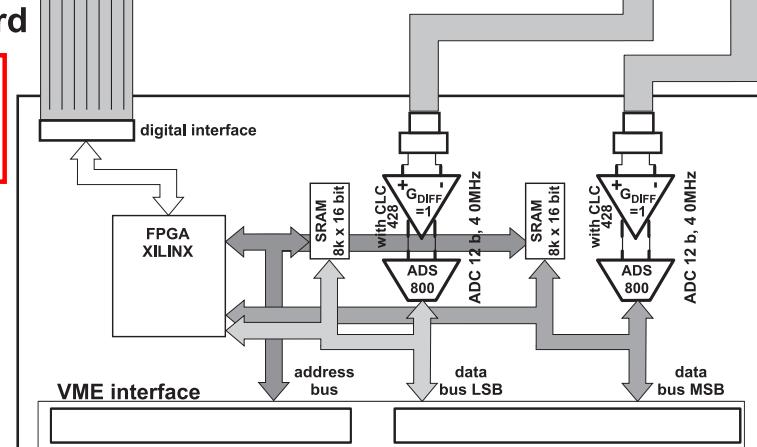
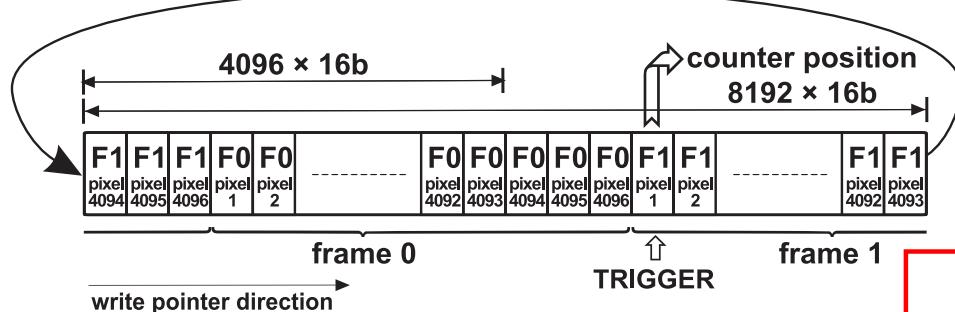


Paths for new chip design ...

- Off-line CDS

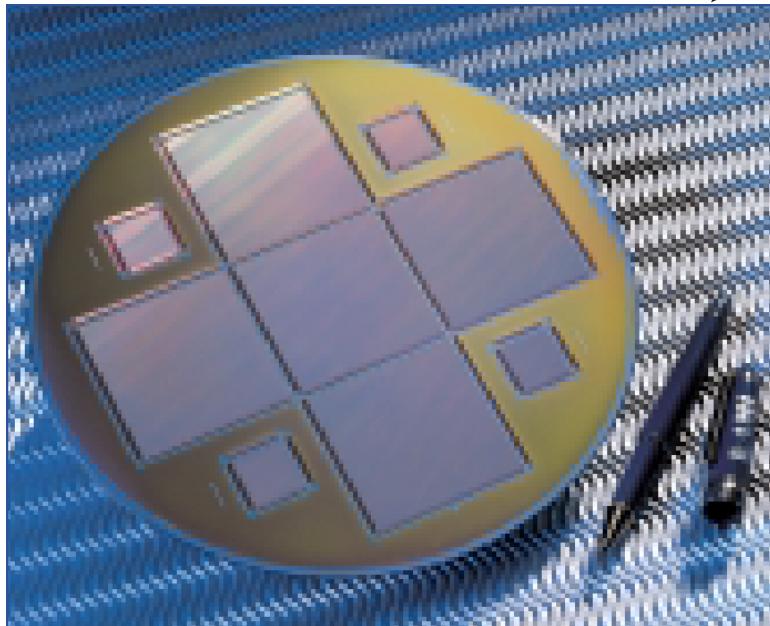
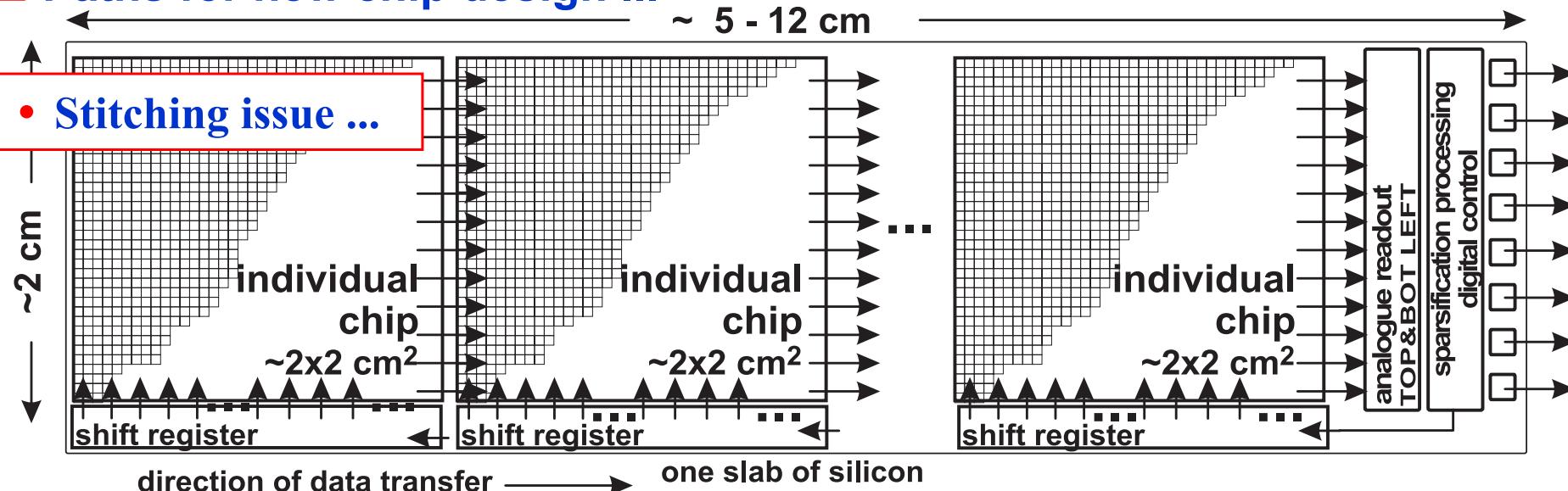


Readout with circular buffer memory architecture
allowing Correlated Double Sampling (CDS) (off-line)



In new version of DAQ cards (VME/USB2) CDS
(pedestals, noise etc.) values computed on -line ...

Paths for new chip design ...



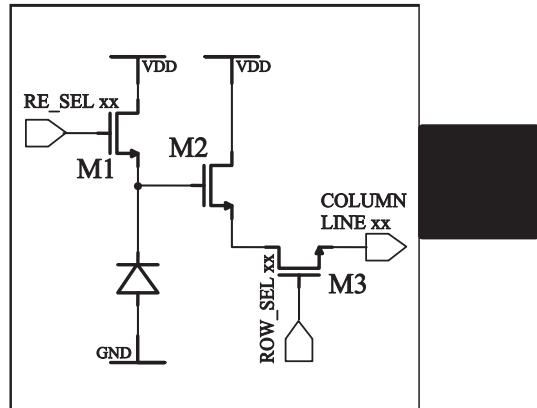
- Stitching technique - starting to be well established fabrication service at some foundries (AMI, Tower, etc.)
- Stitching offered in sub-micron processed on 8" wafers
- Available stitching precision ~0.1 μm !!!
- Stitched blocks must overlap
- Stitching design rules see US Pat. 6,225,013

2.1" x 2.1" Stitched Die on 8" wafer

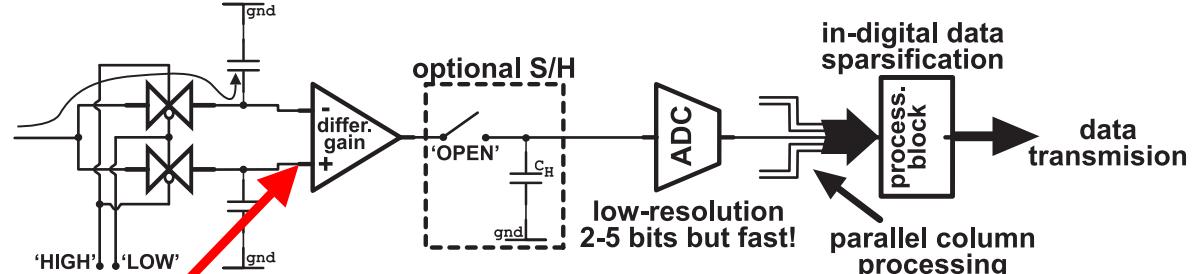
after American Microsystems, INC - www.amis.com

Paths for new chip design ...

- DDS - *signal readout → pixel reset → reference level readout*



1. readout of signal



2. reset of pixels in one row

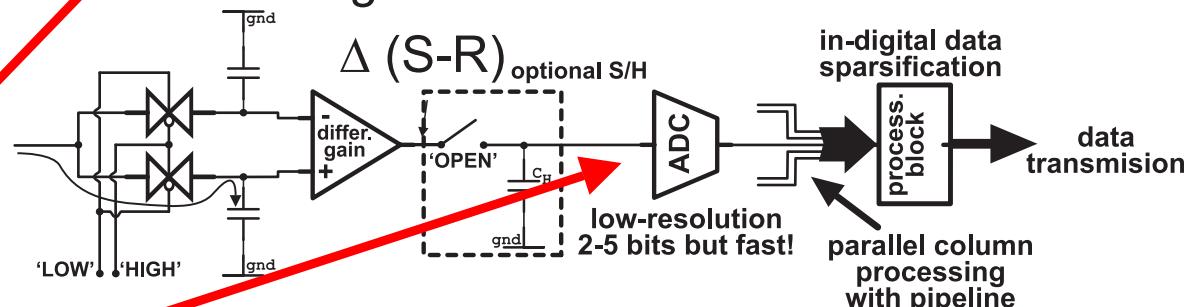
3. readout of signal after reset

- Task repartition between analogue and digital ...

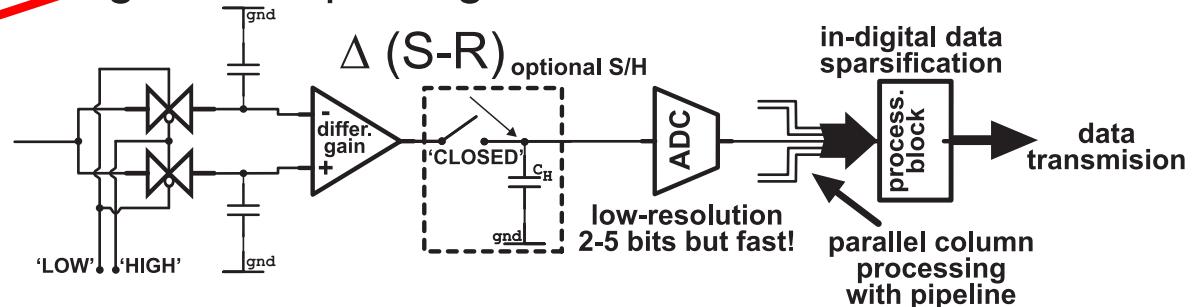
High resolution processing

Low resolution processing

*Design criteria:
power, space, speed,
practical feasibility*



4. signal multiplexing



→ each access to pixel requires at least 3 clock cycle.

Paths for new chip design ...

- DDS

→ no CDS instead DDS; penalty: decreased SNR w.r.t. CDS off-line:

$$\sigma_{\text{total}} = \sqrt{2} \cdot \sigma_{\text{kTC}} \oplus \text{non fully efficient reset} \oplus \text{noncancelled interferences}$$

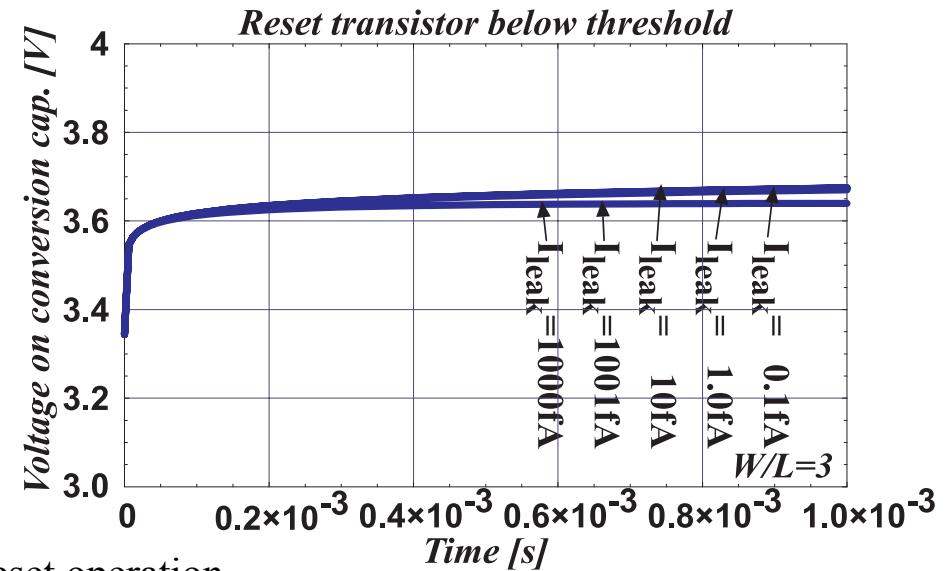
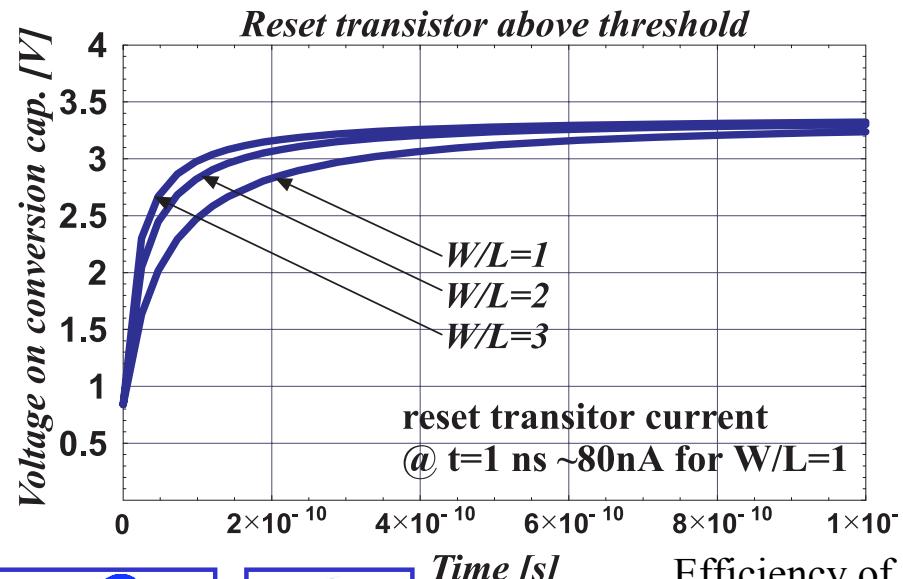
→ at current state of experience the only one method to satisfy:

a) column parallel readout, b) large size of matrix, c) fast read-out clock frequency.

→ necessary data processing on chip to:

a) accomodate to decreased SNR, b) fit data throughput to any DAS.

source of ‘noise’ - imperfection of reset operation - **use hard reset only!**

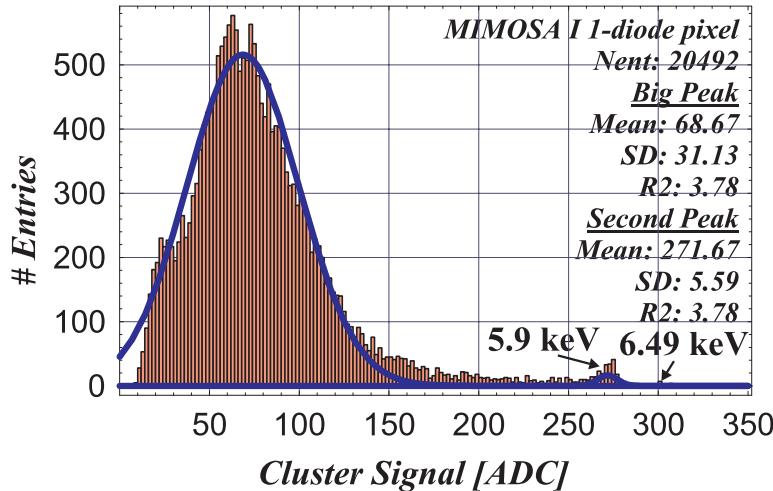


Efficiency of reset operation

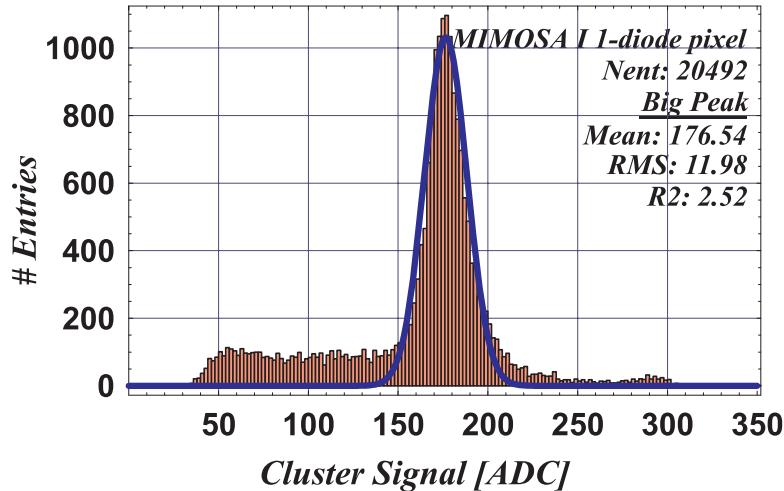
Paths for new chip design ...

Algorithm for on-line data sparsification - take into account charge spreading

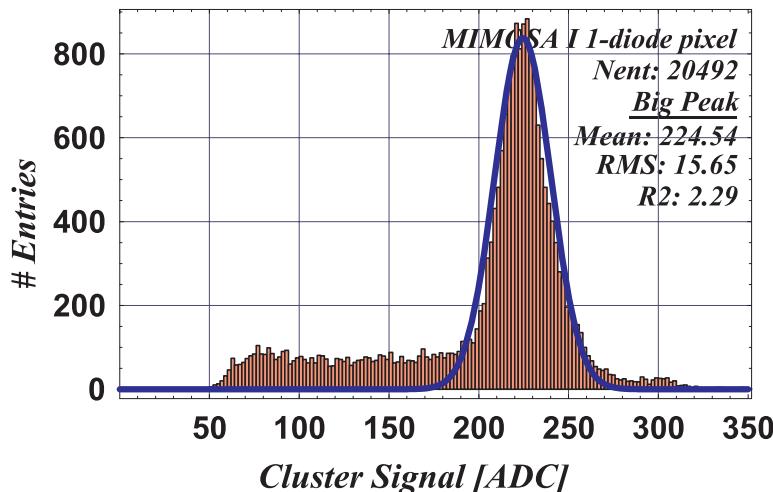
1 Pixel - Cluster Signal Distribution



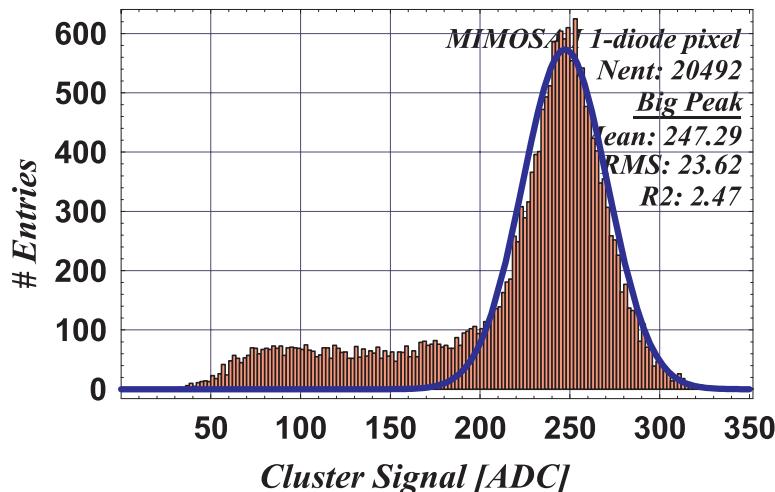
4 Pixel - Cluster Signal Distribution



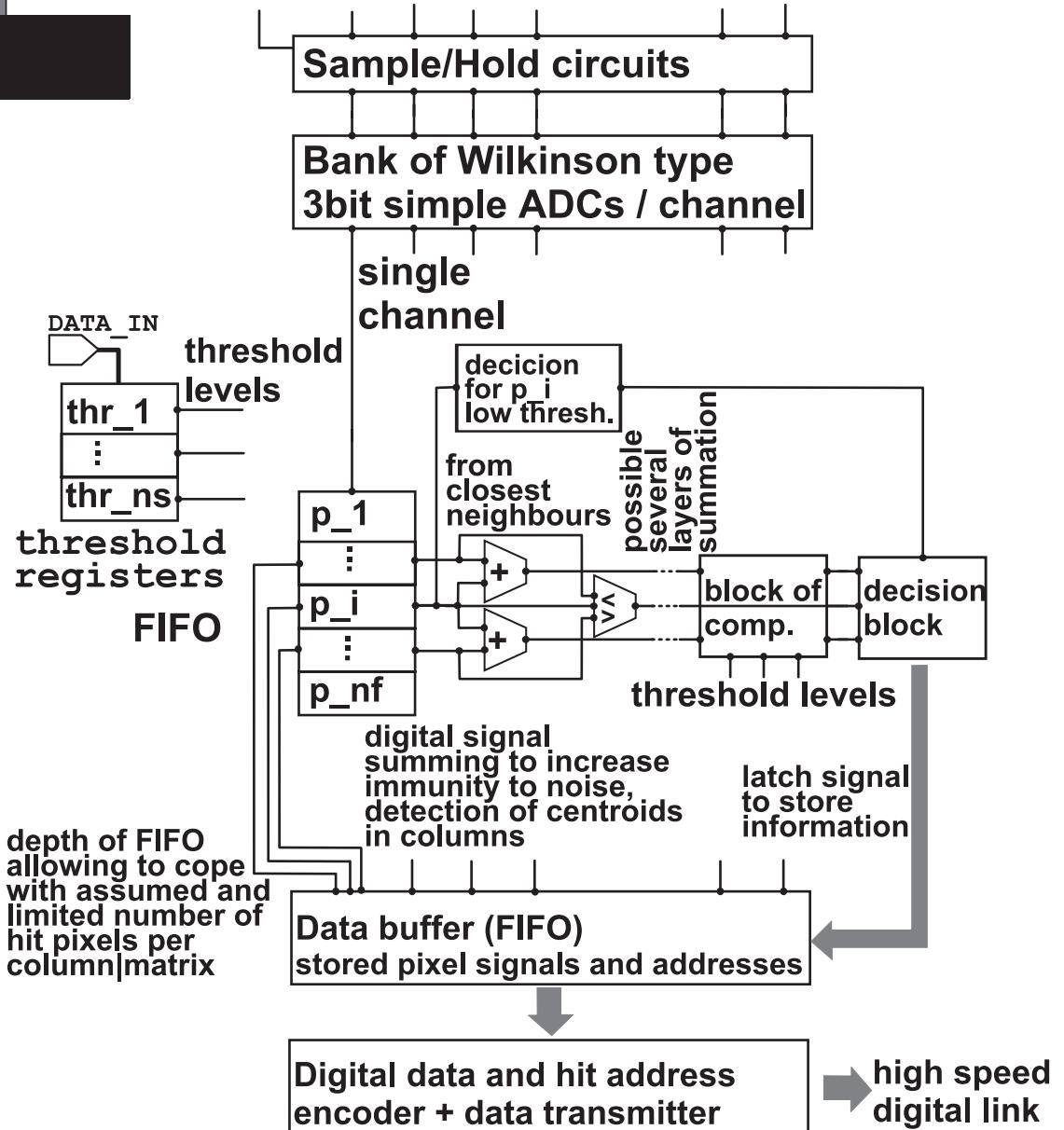
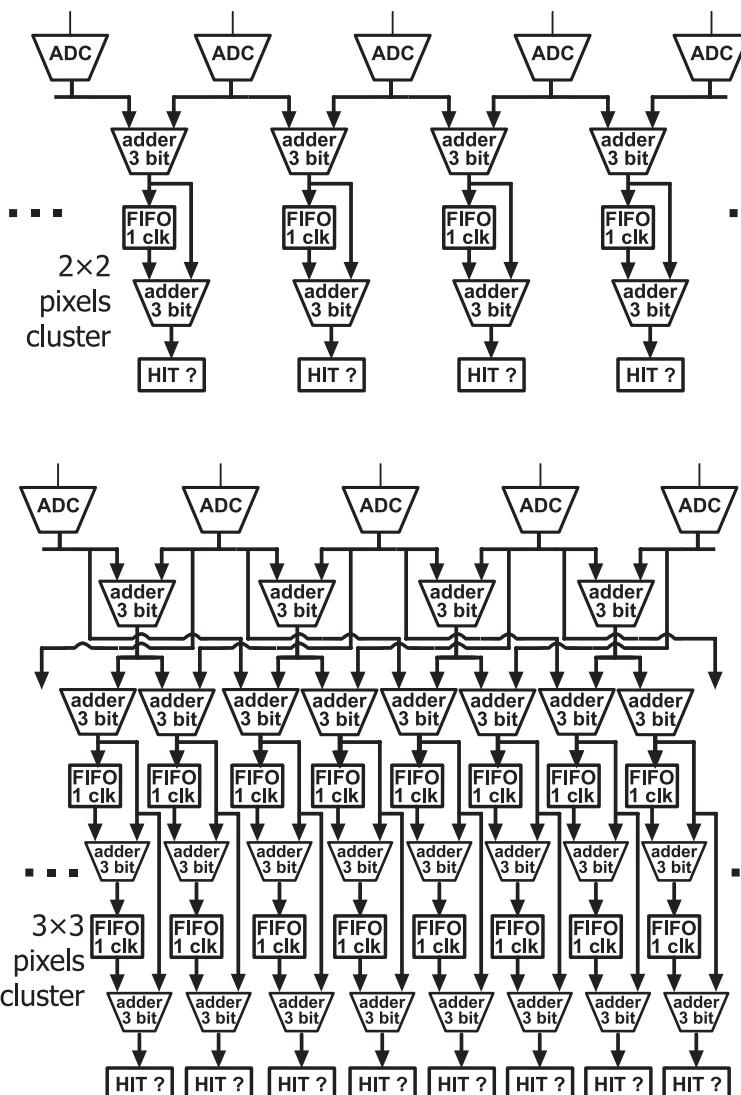
9 Pixel - Cluster Signal Distribution



25 Pixel - Cluster Signal Distribution



X-ray source - ^{55}Fe - 5.9 keV photons.



Paths for new chip design ...

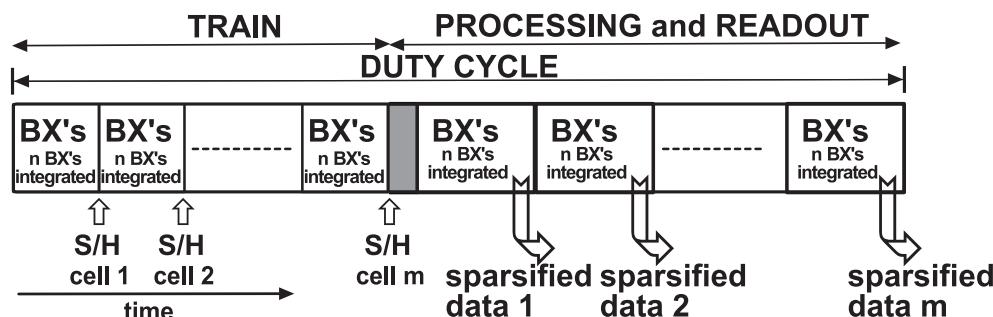
- Pixels with signal amplification

How to read data from vertex detector ???

What requires and constrains physics ...

What machine duty (timing) allows ...

*S/H in on-pixel memory cells...
Reading and processing
in dead time of the machine...*



TESLA:
rep. rate 4...5 Hz, BX/train 2820...4886, BX sep. 337...189 ns
⇒ dead time ~199 ms

100 fF “ncapfet” capacitor

0.35 μm CMOS - $4.67 \times 4.67 \mu\text{m}^2$

0.25 μm CMOS - $4.25 \times 4.25 \mu\text{m}^2$

*Continuous reading...
On-line, on-chip
data processing...*

*Fast readout clock
Increased power consumption
high system complexity*

*Example of MIMOSA VI based system:
~200 ns/pixel + 25 μs readout ⇒ 125 pixels
uncommitted force: rows in parallel*

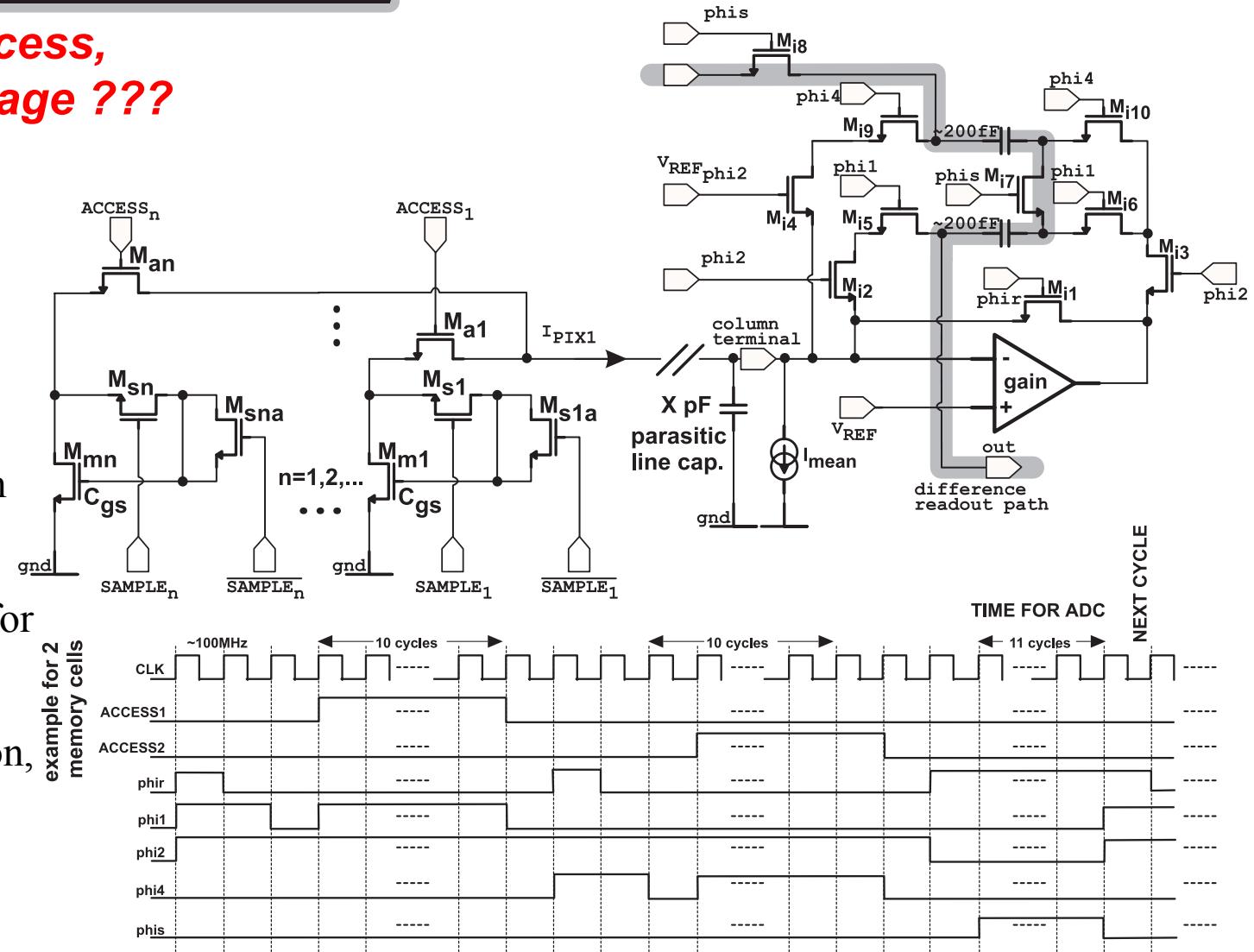
Paths for new chip design

*What to process,
current or voltage ???*

Imposed solution:

photofET CSE

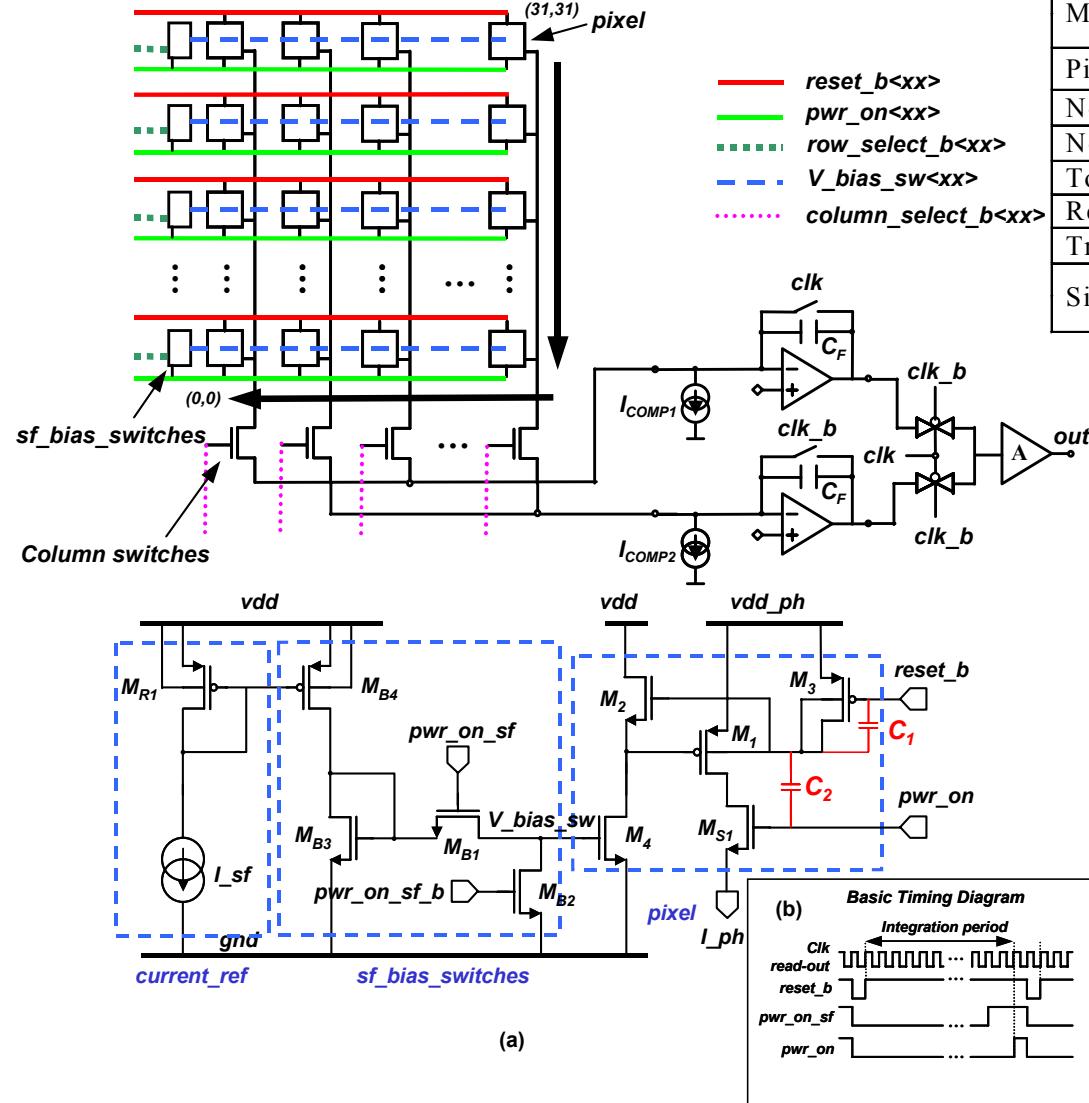
- efficient way for low noise pixel design,
- auto reverse biased nwell/psub junction,
- possible implementation of current mode memory cells on pixel,
- relatively easy method for signal extraction via implementing signal sampling and CDS function,
- similar in concept and performances to « DEPFET »! but... in monolithic approach!



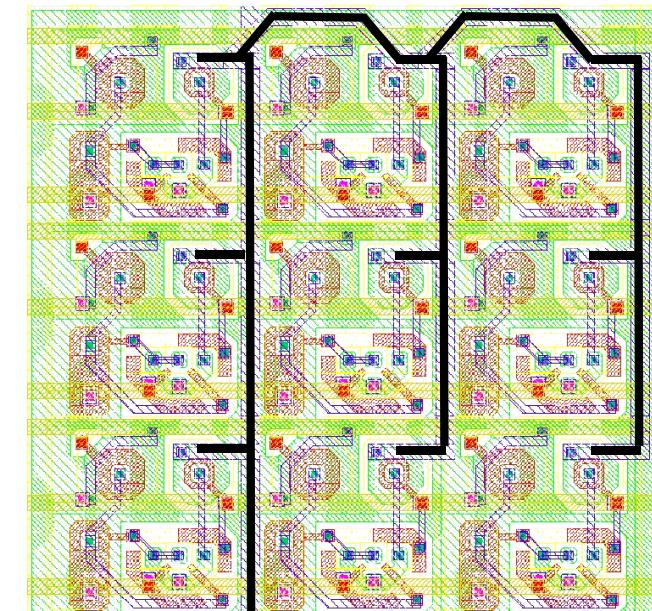
Current designs ...

SUCCESSOR*-2

photofET for dosimetry application



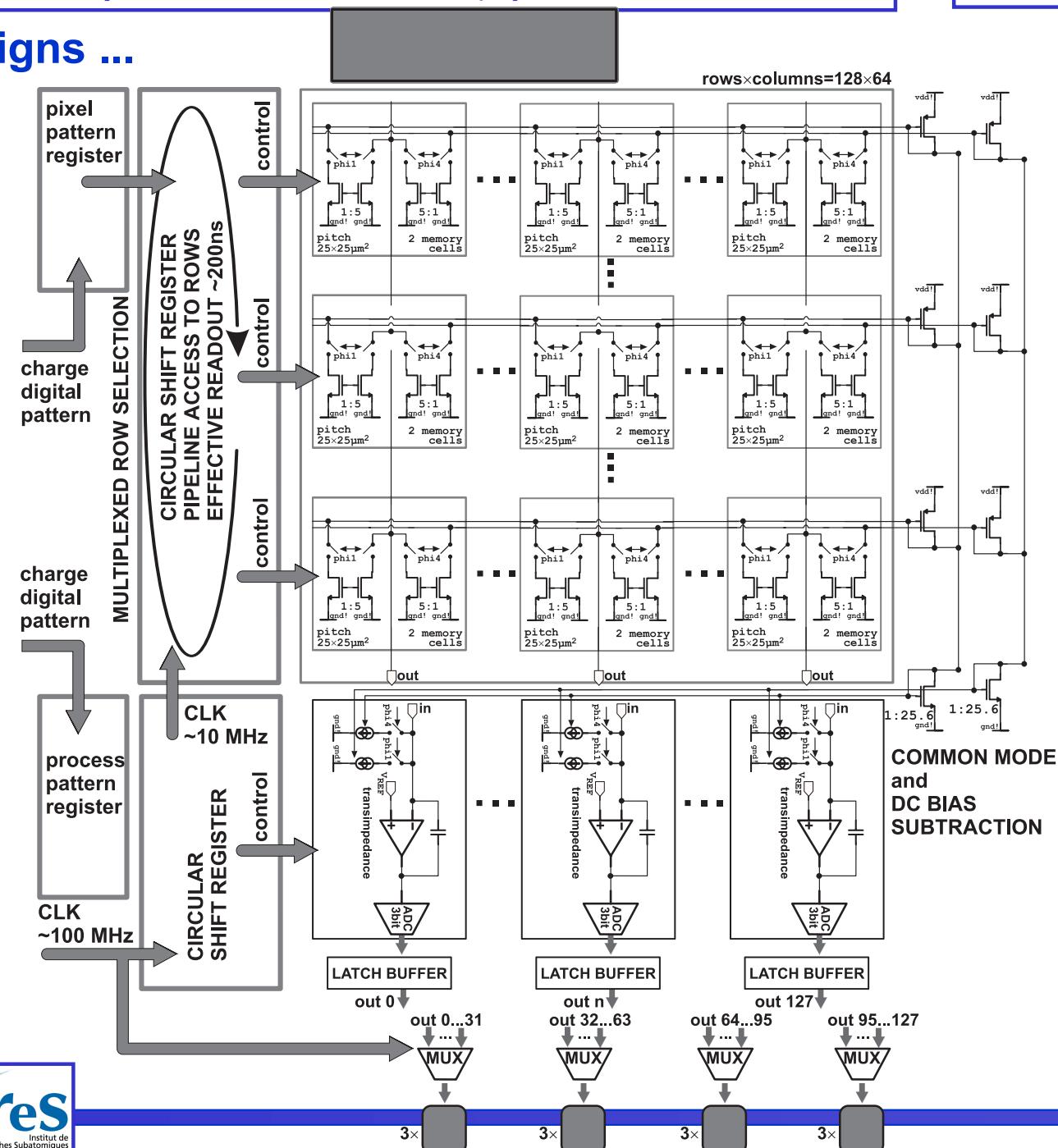
Matrix size	Matrix_single	32x32 pixels				
	Matrix_ganged	32x32 super-pixels (96x96 pixels)				
Pixel Size		$12.5 \times 12.5 \mu\text{m}^2$				
N-well area		$28.7 \mu\text{m}^2$				
N-well perimeter		$20 \mu\text{m}$				
Total n-well node capacitance		$\sim 30 \text{ fF} @ 3 \text{ V} (10 \times 10^3 \text{ e}^- \rightarrow 55 \text{ mV})$				
Read-out frequency		10 MHz				
Transimpedance Amp. Gain		$250 \text{ k}\Omega$				
Single Ended Input Amplifier		<table border="1"> <tr> <td>Gain</td><td>73 dB</td></tr> <tr> <td>ω_0</td><td>400 MHz w/ 2 pF col. load</td></tr> </table>	Gain	73 dB	ω_0	400 MHz w/ 2 pF col. load
Gain	73 dB					
ω_0	400 MHz w/ 2 pF col. load					



Ganged current

*SUCIMA CMOS Charge Sensor

Current designs ...



Summary

◎ Alternative approaches for pixel configurations - appealing:

- possible use of lightly doped non-epitaxial substrate,
- auto-reverse polarised CSE,
- current mode CSE photoFET,
 - ✓ test performances on array structure ⇐ **SUCCESSOR-2, MIMOSA VII.**
- design with amplification, double sampling, column parallel readout,
 - ✓ perform analysis on whole population of pixels ⇐ **DAQ ready.**
 - ✓ couple 24 analogue channels to discrimination stages ⇒ **test performance of discrimination.**
- analogue memory for on-pixel data storage,
 - ✓ current mode approach for memory and column readout.
- implementation of algorithm for on-chip data sparsification,
 - ✓ task repartition ⇐ pixel.

◎ Optimise granularity, on-pixel functionalities, readout method, readout speed, power + material budget to fit application needs.