Novel Charge Sensing Elements and Signal Processing on a CMOS Monolithic Active Pixel Sensors

Outline:

- Motivation for Monolithic Pixel Devices
- Operation Principle of MAPS for Particle Detection
- Simulation of Charge Collection ISE-TCAD
- First Prototypes - design summary
- Measurements - evaluation of basic parameters
- First Prototypes - summary of MIPs tracking performances
- Design and Performances of 3.5 cm², 1M Pixel Device
- Radiation Hardness
- CSE Optimised for VX Environment
- Summary

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Introduction

Why monolithic active pixel devices:
- same unique substrate for detector and electronics:
  - thin device $\Rightarrow$ reduced multiple scattering effect,
  - no complicated and expensive detector-electronics connection with bumps,
  - detector radiation hardness - no bulk charge transfer (CCDs).

Why pixels CMOS:
- standard, well established CMOS industrial fabrication process:
  - access to the most advanced technologies,
  - convenient way of design - standard software tools, design kits and libraries,
  - good price and high yield!
  - low power consumption,
  - system-on-a-chip capability - integration of amplifiers, ADCs, signal processing units etc. on the detector, random pixel addressing,
  - very good spatial resolution ($\sim 1 \, \mu m$) - small pixel size,
  - electronics radiation hardness (layout rules).

1998 - IReS/LEPSI Strasbourg, R&D on CMOS MAPS for charged particle detection,
1999 - first small scale prototypes,
1999-2000 - first beam tests ($\sigma \sim 1.5 \, \mu m$, $\varepsilon \sim 99\%$),
2001 - first large ($10^6$ pixels) scale prototype submitted,

CMOS MAPS – the option for the TESLA VD
Operation Principle of MAPS for Particle Detection

- Baseline architecture - similar to CMOS camera

- Twin-tub CMOS process on epitaxial wafer ...

- Typical epitaxial layer thickness \( \sim 10 \, \mu m \) ...

- Moderately doped epitaxial layer = long minority carrier lifetime ...

- Thin active volume = low signal expected ...

- Charges generated in non-depleted region collected through thermal diffusion (or they recombine...) ...

- Charge confined - potential barriers at layer interfaces - improving collection efficiency ...

- Active volume underneath the readout electronics \( \Rightarrow \) 100% fill factor; charge collected by deep n-well/p-epi diode.

\( \text{INCIDENT/PHOTONS} \)

\( \text{PASSIVATION OXIDE} \)

\( \text{N+} \)

\( \text{N+} \)

\( \text{N+} \)

\( \text{PWELL} \)

\( \text{NWELL} \)

\( \text{charge shared between neighbouring pixels} \)

\( \text{charge collected entirely by one pixels} \)

\( \text{DEPLETION ZONE} \)

\( \text{P EPI-LAYER} \)

\( \text{P++ SUBSTRATE} \)

\( \text{‘warmest’ colour = highest potential in the device} \)
Motivation for Monolithic Pixel Devices (I)

Motivation: Vertex Detector LC - TESLA

TESLA - 800×10⁶ pixels

Charge Coupled Devices -
granularity ☺, material ☺ but RH ☺, speed ☺

Hybrid Pixels -
RH ☺, speed ☺ but granularity ☹, material ☹

Monolithic Active Pixel Sensors -
alternative combining good features of both
**CDS technique**

- **kTC noise suppressing**

\[
\sigma_{V_{on}}^2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(\omega)|^2 S_{Vn}(\omega) d\omega = \frac{kT}{C_d}
\]

Noise kTC [V^2]

- **CDS processing transfer function**

\[
|H_{CDS}(f)|^2 = \frac{4f_{3dB}^2 \sin^2(\pi \tau f)}{f^2 + f_{3dB}^2}
\]

drops to 0 at f=0

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**Noise spectrum before CDS**

Power density spectrum of signal before CDS

MIMOSA 1 1-diode pixel mean noise: 1.237 ADC
difference in mean levels after consecutive resetting (variance): 2.356 ADC

**Noise spectrum after CDS**

Power density spectrum of signal after CDS

MIMOSA 1 1-diode pixel mean noise: 1.529 ADC
difference in mean levels after consecutive resetting (variance): 0.004 ADC
Radiation Hardness (III)

MIMOSA IV pixel layout suffering from poor charge collection

MIMOSA IV pixel layout allowing good charge collection

What is the difference? 
need for thorough studies...

HYPOTHESIS
CSE* optimised for VXD environment (I) - self-reverse polarisation of diode

Classical 3T pixel design

On-pixel amplification requires suppression of the leakage current effect - preserving charge integration!

*CSE - Charge Sensitive Element
CSE Optimised for VX Environment

- Self-reverse polarisation of charge collecting diode,
- In darkness, the diodes D2 conveys only a small value leakage current, thus it represents very high value resistance (10⁹-10¹² Ω).
CSE Optimised for VX Environment
- self-reverse polarisation design

- Charged particle detection performance,

- Charge Integration time ~1ms,

- Design particularity - non epitaxial substrate, but with low-doping level.

S/N ~30 but charge spread is wider and less peaked,

\[ \varepsilon = \sim 99.7\%, \sigma = \sim 4\mu m \]
CSE Optimised for VX Environment - self-reverse polarisation design

- Efficiency of keeping reverse polarisation at high discharging resistance,

Speed of effective recharge of the charge sensing node after $^{55}$Fe X-ray photon hit $>100$ADC.

Threshold correction in hit finding procedure for $^{55}$Fe X-ray source.
Charge converted to voltage on diode cathodes; resulting voltage buffered by SF,

- Amplified voltage stored on first capacitor,
- Second capacitor stores amplified voltage from previous cycle,
- The signals are subtracted on the transconduction stage, and currents sent for discrimination,
- Differential voltage gain \( \sim 0.10 \text{ mV/e}^- \), differential current gain \( \sim 9 \text{ nA/e}^- \).
MIMOSA VI - design

AC-coupled common source amplification stage
Source follower stage
Linearised differential pair - transconductance stage
Signal storage capacitors
DC bias of the “floating gate” input
MIMOSA VI - design

Pixel design features:
- only NMOS transistors, nwell/p-epi and pdiff/nwell diodes and poly1-to-poly2 capacitors.

MIMOSA VI key design features
- 0.35 µm CMOS 4.2 µm thick EPI layer,
- 1 array (24+6) × 128 pixels, pitch 28 × 28 µm²,
- 24 columns read-out in parallel,
- 30 MHz f_clk, 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size 4.0 × 3.7 µm² - 3.5 fF,
MIMOSA VI - simulation

SPICE simulation of pixel response

1. Voltage on two storage capacitors:
   a) in absence of any charge deposited,
   b) for signal of 1000 e⁻ (schematic) ~0.10 mV/e⁻,
   c) post layout simulation ~0.09 mV/e⁻.

Current gain of the pixel as function of charge acquired
MIMOSA VI - analogue part - preliminary results

Pixel readout phases

- No source (analog persistence)
- 10 MHz
- 1 MHz
- SMP1
- SMP2
- CALIB
- READOUT

Digital 8-bit oscilloscope, single channel, one pixel @1 MHz (for easy visualisation)
Leakage current measurements

\[ I_{\text{diode}} = \frac{I_{\text{total}}}{(30 \times 128)} \]

\( T = -10^\circ C, 0^\circ C, 20^\circ C \)

D=0 krad, 100 krad, 300 krad

@ 20°C
24h after irradiation
MIMOSA VI - analogue part - preliminary results

Other results...

On-pixel amplifier bias current

Test procedure:

@ $f_{\text{clk}}=10\text{MHz}$

Analogue power supply current

VCAS=1.1 V \quad I=15.1502 \text{ mA}

VCAS= 0 V \quad I=14.9815 \text{ mA}

⇒ \quad I_{\text{BIAS}}=5.6 \text{ µA}
MIMOSA VI - analogue part - preliminary results

Differential output sampled during READ_OUT phase

no source

Digital 8bit oscilloscope, single channel, external sample clock, 100k samples
MIMOSA VI - analogue part - preliminary results

Differential output sampled during READ_OUT phase

$^{55}$Fe source

\[ S = \frac{1640e^{-}}{N} \approx 110 \]

\[ \tau_{\text{int}} = 77 \mu s \]

Digital 8bit oscilloscope, single channel, external sample clock, 100k samples
MIMOSA VI - analogue part - preliminary results

Differential output sampled during READ_OUT phase

Single pixel $^{55}$Fe source spectrum (integration time = 77µs)

Conversion gain calibration peak 5.9keV
Current mode CSE - photoFET

\[ I_{OUT,\text{strong}} = \frac{1}{2} \frac{W}{L} \mu C_{\text{ox}} \left( V_{GS} (I_{SF}) - V_{TH} \right)^2, \quad \text{where } V_{TH} = V_{TH0} + \gamma \sqrt{2|\phi_F| - V_{bs} - \sqrt{2|\phi_F|}} \]

\[ i_{out} = g_{mb,M_1} \cdot V_{bs,M_1} + \frac{g_{m,M_2}}{g_{m,M_2} + g_{mb,M_2}} \cdot g_{m,M_1} \cdot V_{bs,M_1} \]
Current mode CSE - photoFET

Pixel design with photoFET element - MIMOSA IV test structure

ADVANTAGES of photoFET:

- DC bias = high transconductance
- Easy current mode memory on pixel
- Continuous signal monitoring - wired OR
**Current mode CSE - photoFET**

- Detection performance of $^{55}$Fe X-ray photons

- Readout of reference current and clamping output to V_CLAMP

- Example of output signal corresponding to hit occurrence

- Output signal for empty photoFET current sample

- Clk_sampling_for_ADC

- READ_CLAMP/READ 6.9 $\mu$s pulse
Current mode CSE - photofET

- MIMOSA IV; Transimpedance chopper-stabilised amplifier with double sampling operation
- DC output response
  \[ V_{\text{OUTPUT}} = V_{\text{CLAMP}} - V_{GS,M_{14}} \]
- Small-signal output response
  \[ V_{\text{OUTPUT}} = \frac{1}{g_{m,M_{14}} + g_{mb,M_{14}}} \left( i_{\text{REF/READ\_OUT}} - i_{\text{READ/REF\_OUT}} \right) \]

Test performance - \( r_{\text{transimp}} = 600 \, \text{k}\Omega \)
Detection performance of $^{55}$Fe X-ray photons

Summary of performances measured with single pixel prototype:

\[
G_{q\rightarrow 1} \approx 330 \quad pA/e^- \\
G_{q\rightarrow V}^{CDS} \approx 183 \quad \mu V/e^- \\
\sigma_{\text{noise}} = 1.4 \text{ nA} \div 2.7 \text{ nA} \\
\sigma_{\text{CDS output}} = 6 \text{ mV} \div 8 \text{ mV}
\]
Current mode CSE - photoFET

Operation modes

- Auto reverse polarisation

① weak inversion, \( I_{DC,PMOS} = \text{low} \)

\[
V_{BS,M1} \propto \ln (\Phi + I_{\text{leak}}) \\
I_{DC,PMOS} \propto e^{(V_{BS,M1} + V_{GS,M2})} \\
\Rightarrow \quad I_{DC,PMOS} \propto \Phi
\]

- Charge integration with reset transistor

\( V_{dd_1} = V_{dd_2} < V_{dd_3} \)

\( V_{dd_1} = V_{dd_2} = V_{dd_3} \)

\[ I_{SF} \]

\[ I_{OUT} \]

\[ I_{DC,PMOS} \]

\[ \text{ground} \]

\[ \text{PMOS} \]

\[ \text{NWELL P-EP} \]

\[ \text{charge sensing element} \]

\[ M_2 \]

\[ M_1 \]

\[ M_3 \]

\[ \text{RESET} \]

\[ \text{OUT} \]

\[ \text{ground} \]

\[ \text{Bias conditions:} \]

- \( V_{dd_{\text{sf}}} = 3.3V \)
- \( V_{dd_{\text{ph}}} = 2.8V \)
- \( I_{\text{sf}} = 10\mu A \)
- \( V_{\text{DML}} = 1V \)

\( e_{NL} = 0.33\% \)
Paths for new chip design ...

“fast, high resolution, and macroscopic size MAPS detector”

Use of linear sensor - 3T approach:
- Off-line CDS - « no intelligence » - (MIMOSA V),
- DDS - $kT$ noise, column-level processing (sparsification).

Use of self-reverse biased sensor:
- Both readout modes as for linear sensors,
  - Voltage mode - charge-to-voltage conversion - amplification, auto-zeroing, difference calculation, column-level processing (sparsification) - (MIMOSA VI),
  - Current mode - charge-to-current conversion - amplification, memory cells, column-level processing (sparsification) - (photoFET MIMOSA IV).
- Paths for new chip design ...

- line represented by MIMOSA V:
  a) slow read-out (serialised pixel information),
  b) physical signal extraction with off-line CDS,
  c) non intelligent but slow read-out easily fits DAS,
  d) minimum $\text{SNR} \approx 10$ for the seed pixel in order not to lose detection efficiency,
  e) parallelism in reading out information translates in practice to on chip data sparsification,
  f) Processing on-chip of CDS type (in non-aggressive way) requires memory (digital) - space??
Paths for new chip design ...

- Off-line CDS

Readout with circular buffer memory architecture allowing Correlated Double Sampling (CDS) (off-line)

In new version of DAQ cards (VME/USB2) CDS (pedestals, noise etc.) values computed on-line...
Paths for new chip design ...

- Stitching issue ...

- Stitching technique - starting to be well established fabrication service at some foundries (AMI, Tower, etc.)
- Stitching offered in sub-micron processed on 8” wafers
- Available stitching precision ~0.1 µm !!!
- Stitched blocks must overlap
- Stitching design rules see US Pat. 6,225,013

2.1” x 2.1” Stitched Die on 8” wafer

*after American Microsystemses, INC - www.amis.com*
Paths for new chip design ...

- DDS - signal readout → pixel reset → reference level readout

1. readout of signal

2. reset of pixels in one row

3. readout of signal after reset

4. signal multiplexing

- Task repartition between analogue and digital ...

High resolution processing

Low resolution processing

Design criteria: power, space, speed, practical feasibility

→ each access to pixel requires at least 3 clock cycle.
Paths for new chip design ...

- DDS
  - no CDS instead DDS; penalty: decreased SNR w.r.t. CDS off-line:

\[ \sigma_{\text{total}} = \sqrt{2} \cdot \sigma_{\text{kTC}} \oplus \text{non fully efficient reset} \oplus \text{noncancelled interferences} \]

- at current state of experience the only one method to satisfy:
  a) column parallel readout,  b) large size of matrix,  c) fast read-out clock frequency.
  - necessary data processing on chip to:
    a) accomodate to decreased SNR, b) fit data throughput to any DAS.

  source of ‘ noise ’ - imperfection of reset operation - **use hard reset only!**

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**Reset transistor above threshold**

**Reset transistor below threshold**

**Reset transistor current**

@ t=1 ns ~80nA for W/L=1

**Efficiency of reset operation**

- **Time [s]**
- **Voltage on conversion cap. [V]**
Paths for new chip design ...

Algorithm for on-line data sparsification - take into account charge spreading

X-ray source - $^{55}$Fe - 5.9 keV photons.
Sample/Hold circuits

Bank of Wilkinson type
3bit simple ADCs / channel

single channel

threshold levels

decision for \( p_i \) low thresh.

from closest neighbours

possible several layers of summation

block of decision block

threshold levels

digital signal summing to increase immunity to noise, detection of centroids in columns

latch signal to store information

Data buffer (FIFO)
stored pixel signals and addresses

Digital data and hit address
encoder + data transmitter

high speed digital link

2x2 pixels cluster

3x3 pixels cluster

ADC
adder
3 bit
FIFO
1 clk
HIT?

ADC
adder
3 bit
FIFO
1 clk
HIT?

ADC
adder
3 bit
FIFO
1 clk
HIT?

ADC
adder
3 bit
FIFO
1 clk
HIT?

ADC
adder
3 bit
FIFO
1 clk
HIT?
Paths for new chip design ...

- Pixels with signal amplification

How to read data from vertex detector ???

What requires and constrains physics ...

What machine duty (timing) allows ...

S/H in on-pixel memory cells...

Reading and processing in dead time of the machine...

Continuous reading...

On-line, on-chip data processing...

Fast readout clock

Increased power consumption

high system complexity

Example of MIMOSA VI based system:

~200 ns/pixel + 25 µs readout \Rightarrow 125 pixels

uncommitted force: rows in parallel

100 fF “ncapfet” capacitor

0.35 µm CMOS - 4.67 \times 4.67 \mu m^2

0.25 µm CMOS - 4.25 \times 4.25 \mu m^2
What to process, current or voltage ???

Imposed solution:

photoFET CSE

- efficient way for low noise pixel design,
- auto reverse biased nwell/psub junction,
- possible implementation of current mode memory cells on pixel,
- relatively easy method for signal extraction via implementing signal sampling and CDS function,
- similar in concept and performances to « DEPFET »! but... in monolithic approach!
Current designs ...

**SUCCESSOR*-2**

**photoFET for dosimetry application**

Matrix size
- Matrix_single 32×32 pixels
- Matrix_ganged 32×32 super-pixels (96×96 pixels)

Pixel Size
- Matrix_single 12.5×12.5 μm²
- Matrix_ganged 28.7 μm²

N-well area
- Matrix_single 20 μm²

N-well perimeter
- Matrix_single 20 μm

Total n-well node capacitance
- ~30 fF @ 3 V (10×10⁷ e⁻→55 mV)

Read-out frequency
- 10 MHz

Transimpedance Amp. Gain
- 250 KΩ

Single Ended Input Amplifier
- Gain 73 dB
- ω₀ 400 MHz w/ 2 pF col. load

**Matrix Single 32**
- 32 pixels

**Matrix Ganged 32**
- 32 super-pixels (96×96 pixels)

**Ganged current**

*SUcima Cmos ChargE SenSOR*
Current designs...
Summary

Alternative approaches for pixel configurations - appealing:

- possible use of lightly doped non-epitaxial substrate,
- auto-reverse polarised CSE,
- current mode CSE photoFET,
  - test performances on array structure ⇔ SUCCESSOR-2, MIMOSA VII.
- design with amplification, double sampling, column parallel readout,
  - perform analysis on whole population of pixels ⇐ DAQ ready.
  - couple 24 analogue channels to discrimination stages ⇒ test performance of discrimination.
- analogue memory for on-pixel data storage,
  - current mode approach for memory and column readout.
- implementation of algorithm for on-chip data sparsification,
  - task repartition ⇔ pixel.

Optimise granularity, on-pixel functionalities, readout method, readout speed, power + material budget to fit application needs.