Radiation-hard circuits in deep submicron CMOS technologies

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Outline

• Introduction and motivation
• Radiation effects on CMOS devices and circuits
• Scaling impact on the radiation tolerance
• A radiation tolerant layout approach
• The Enclosed Layout Transistor (ELT): special features
• One circuit example: a radiation tolerant analog memory
• Conclusions
CERN: above ground...
... and under ground
One of the 4 LHC experiments
Finding the Higgs boson...
Why rad-tolerant CMOS ICs?

High luminosity colliders generate a very harsh radiation environment, which requires radiation hard read-out ICs

Radiation hardened technologies represent a possible solution, but they are expensive and have several other problems

Can we use, with some tricks, a commercial, “inexpensive” CMOS technology for our circuits?
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• Introduction and motivation
• Radiation effects on CMOS devices and circuits
  ➢ Total Ionizing Dose (TID) Effects
  ➢ Single Event Effects (SEE)
• Scaling impact on the radiation tolerance
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• The Enclosed Layout Transistor (ELT): special features
• One circuit example: a radiation tolerant analog memory
• Conclusions
Ionizing particles through a MOST

Threshold voltage shift
Mobility degradation
Swing degradation

Other degradations:
• Transconductance
• Noise
• Matching

Contributions to the $V_T$ shift

<table>
<thead>
<tr>
<th></th>
<th>Oxide charges</th>
<th>Interface states</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td></td>
<td>$+$</td>
<td>$+$ or $-$</td>
</tr>
<tr>
<td>PMOS</td>
<td></td>
<td>$-$</td>
<td>$-$</td>
</tr>
</tbody>
</table>

- For deep submicron processes the sign of the $V_T$ shift for NMOS transistors tends to be positive.
- The bias conditions during irradiation have a great influence on the absolute value of the $V_T$ shift.
Transistor level leakage (NMOS)

Transistor level leakage

This is for LOCOS, what about STI? Things did not improve!

Transistor level leakage: example

NMOS - 0.7 µm technology - $t_{ox} = 17$ nm
Field oxide leakage

Radiation induced leakage between $V_{DD}$ and $V_{SS}$
The Field Oxide Transistor

Post-irradiation leakage currents depend on:

- n+ source
- n+ drain

Factors influencing leakage currents:
- Total Dose
- Bias conditions
- Gate Material
- Field oxide quality

Graphs showing:
- PRERAD
- After 1 Mrad

Graph parameters:
- ID [A]
- VGS [V]

Graphs comparison:
- Metal Gate
- Polysilicon Gate
Annealing (mainly in the oxide!)

- Trapped hole
- Thermally emitted electrons
- Electrons tunneling
- Oxide
- Silicon
- Gate
Single Event Latch-up (SEL)

Latch-up can be initiated by ionizing particles (SEL)
Single Event Upset (SEU)

Static RAM cell

Highly energetic particle

1 → 0
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    - Scaling impact on TID effects
    - Scaling impact on SEEs
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Total Dose damage and scaling

\[ \Delta V_{FB} \propto t_{OX}^2 \]

\[ \Delta D_{it} \propto t_{OX}^n \]

-10^{-3} - 10^3
-10^{-2} - 10^2
-10^{-1} - 10^1

1 \ 10 \ 100 \ t_{OX} \ [\text{nm}]$

Total Dose damage and scaling

Decreasing $t_{\text{ox}}$ we decrease the degradation of:

- Transconductance
- Subthreshold slope
- Noise
- And the threshold voltage shift for n-channel transistors might not be negative anymore...
$\Delta V_T$ and $t_{ox}$ scaling
SEL and scaling

Modern CMOS technologies have:

• Retrograde wells
• Thinner epitaxial layers
• Trench isolation
• \(V_{DD}\) reduced

All these issues help in preventing SEL, but they might not be always effective

SEU and scaling

- $V_{DD}$ reduced
- Node C reduced
  
  **BUT**
  
  - Charge collected reduced

The SEU problem may worsen with scaling

SEGR and scaling

SEGR in ULSI CMOS

SEGR is not a problem even in the most advanced CMOS processes

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  ➢ Total Ionizing Dose tolerance
  ➢ Enclosed Layout Transistors drawbacks (more later…)
  ➢ Single Event Effects tolerance
  ➢ Density and Speed considerations
• The Enclosed Layout Transistor (ELT): special features
• One circuit example: a radiation tolerant analog memory
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Enclosed Layout Transistor (ELT)

ELTs solve the leakage problem in the NMOS transistors
At the circuit level, guard rings are necessary
Effectiveness of ELTs

NMOS - 0.7 \( \mu \text{m} \) technology - \( t_{\text{ox}} = 17 \) nm

- Prerad
- After 1 Mrad
- After 1 Mrad (ELT)
ELT & deep submicron

NMOS - 0.25 μm technology - $t_{ox} = 5$ nm

Prerad and after 13 Mrad

No leakage
No $V_T$ shift
A radiation-hard inverter
Total ionizing dose tolerance

\[ \Delta V_{th} \propto t_{ox}^{n} + \text{ELT's and guard rings} = \text{TID Radiation Tolerance} \]

Deep sub-\(\mu\)m means also:
- speed
- low power
- VLSI
- low cost
- high yield
Drawbacks of ELTs

- Waste of area
- Increase in the parasitic gate and source/drain capacitances
- Modeling problems
- Lack of symmetry

\[ W = 8a + 4L \]
\[ W/L = 8a/L + 4 \]
\[ \text{Area} = 4(a+b+L)^2 \]

Another possible solution?
Single Event Effect tests

- **SEL**: The systematic use of guard rings is **ALSO** an effective tool against SEL. No latch-up observed up to 89 MeVcm^2mg^{-1}.

- **SEGR**: Never observed in our circuits.

- **SEU**: The higher gate capacitance of ELTs decreases the sensitivity.

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SEU: comparison with the trend

This static cell

Figure 5. Experimentally-measured and simulated upset thresholds in three Sandia SRAM technology generations (no feedback resistors). The 1- and 2-μm technologies are n-substrate, 5 V; the 0.5-μm technology is p-substrate, 3.3 V.

Density and speed

\[
\frac{\text{Area A}}{\text{Area C}} = 3.2 \\
\frac{\text{Area B}}{\text{Area D}} = 2.2
\]

A & B : 0.6 \( \mu \text{m standard} \)

C & D : 0.25 \( \mu \text{m rad-tol} \)

Inverter with F.O. = 1

<table>
<thead>
<tr>
<th></th>
<th>0.6 ( \mu \text{m} )</th>
<th>0.25 ( \mu \text{m} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} ) [V]</td>
<td>3.3</td>
<td>2</td>
</tr>
<tr>
<td>Delay [ps]</td>
<td>114</td>
<td>48</td>
</tr>
<tr>
<td>Pwr [( \mu \text{W/MHz} )]</td>
<td>1.34</td>
<td>0.14</td>
</tr>
<tr>
<td>Area [( \mu \text{m}^2 )]</td>
<td>162</td>
<td>50</td>
</tr>
</tbody>
</table>
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Aspect ratio modeling

\[
\frac{W}{L} = 4 \frac{2\alpha}{\ln \left( \frac{d'}{d' - 2\alpha L} \right)} + 2K \frac{1 - \alpha}{\frac{1}{2} \sqrt{\alpha^2 + 2\alpha + 5} \cdot \ln \frac{1}{\alpha}} + 3 \frac{d - d'}{2L}
\]

<table>
<thead>
<tr>
<th>L ((\mu m))</th>
<th>Calc. W/L</th>
<th>Extr. W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.28</td>
<td>14.8</td>
<td>15</td>
</tr>
<tr>
<td>0.36</td>
<td>11.3</td>
<td>11.2</td>
</tr>
<tr>
<td>0.5</td>
<td>8.3</td>
<td>8.3</td>
</tr>
<tr>
<td>1</td>
<td>5.1</td>
<td>5.2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3.2</td>
</tr>
<tr>
<td>5</td>
<td>2.6</td>
<td>2.6</td>
</tr>
</tbody>
</table>

Limitation in the W/L ratio values
Output conductance

\[ L = 0.28 \, \mu m \quad G_{Di} = 11.9 \, \mu S \quad G_{Do} = 9.6 \, \mu S \]

\[ \begin{array}{|c|c|}
\hline
L (\mu m) & \Delta G/G_{Di} \\
\hline
0.28 & 19 \% \\
0.36 & 23 \% \\
0.5 & 33 \% \\
1 & 53 \% \\
3 & 70 \% \\
5 & 75 \% \\
\hline
\end{array} \]
Matching of ELTs

\[
\sigma_{\Delta P}^2 = \left( \frac{A_P}{\sqrt{S_G}} \right)^2 + \sigma_0^2
\]

\[A_{Vth} = 5.4 \text{ mV} \cdot \mu\text{m}\]

\[\sigma_0 V_{th} = 0.95 \text{ mV}\]

\[A_\beta = 1.5 \% \cdot \mu\text{m}\]

\[\sigma_0 \beta = 0.33 \%\]
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Why an analog memory?

- Analog memories are often used in High Energy Physics applications
- Allows studying how to implement switched capacitor circuits in deep submicron CMOS processes
- Thin oxides (needed for radiation tolerance) requires low supply voltages, making difficult to have large dynamic ranges
- Allows to study the problems related to mixed signal circuits
Memory channel schematic

Digital Control Logic

IN

SW_W

V_{ref_w}

SW_R

SW_F

OUT

V_{ref_r}
Switch “on” conductance

\[ V_{DD} = 5 \text{ V} \]

\[ V_{DD} = 1 \text{ V} \]
Switch “on” resistance

Switch Resistance [kΩ] vs. Vin [V]

- Vdd = 2.5 V
- Vdd = 1.5 V
- Vdd = 1 V
Which capacitor for storage?

Structure 1: N+ poly - n well capacitor
Structure 2: NMOS capacitor
PMOS (S & D float.) P+ poly - N well
Shift register schematic

RES CK

FF (n-1)

D OUT

RES CK

FF (n)

D OUT

RES CK

FF (n+1)

D OUT

I_IN

VDDD

GND

OUT n

OUT n-1

Q n

Q n-1

Q

\overline{Q}

To cell n
Memory cell layout

- Cell area: $56.1 \times 11.1 \mu m^2$
- Minimum size edgeless transistors for the CMOS switches
- $C_{ox} \approx 5.5 \text{ fF/} \mu m^2$ $C = 600 \text{ fF}$
- Shielding
Test chip layout

- 0.25 µm CMOS Tech.
- Rad-Tol Layout
- area: 2 x 2 mm²
- 8 channels
- 8 x 128 cells
- 9300 transistors
- capacitors
  area: 0.11 mm²
- power consumption: 31.6 mW
I-O characteristic linearity

\[ V_{\text{out}} \ [ \text{V} ] \]

\[ V_{\text{in}} \ [ \text{V} ] \]
Deviation from linearity

\[ V_{\text{out}} - \text{LINFIT} \text{ [mV]} \]

\[ V_{\text{in}} \text{ [V]} \]
Pedestal variation

![Graph showing pedestals variation with cell numbers and voltage readings.]

- Vout [mV]
- Cell Number

- 1 mV variation

BNL, 21 April 2004
Giovanni Anelli
Performance summary

- Noise measured $\approx 0.8$ mV rms
- Pedestal variation $< 1$ mV peak-to-peak
- Dynamic Range $> 11$ bits
- Linearity $> 7.5$ bits over 2 V
- Cross talk $< 0.4\%$
Radiation test results

- Source: 10 KeV X-rays
- Dose rate: 31.6 Krad/min
- The memory is written and read continuously
- Total dose: 10 Mrad
- Vin = 1.5 V

<table>
<thead>
<tr>
<th>$V_{DDA}$ [V]</th>
<th>PWR pre [mW]</th>
<th>PWR after [mW]</th>
<th>$\Delta$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>30.95</td>
<td>30.5</td>
<td>1.45</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$V_{DDD}$ [V]</th>
<th>$f_W$ [MHz]</th>
<th>PWR pre [$\mu$W]</th>
<th>PWR after [$\mu$W]</th>
<th>$\Delta$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>25</td>
<td>390</td>
<td>377</td>
<td>3.3</td>
</tr>
<tr>
<td>2</td>
<td>25</td>
<td>216</td>
<td>212</td>
<td>1.8</td>
</tr>
<tr>
<td>2.5</td>
<td>50</td>
<td>707</td>
<td>685</td>
<td>3.2</td>
</tr>
<tr>
<td>2.5</td>
<td>12.5</td>
<td>225</td>
<td>215</td>
<td>4.4</td>
</tr>
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- Scaling is a general trend in CMOS, since it allows to have faster, denser and less power consuming integrated circuits. Generally it improves TID and SEL tolerance but it might worsen SEU.
- We have demonstrated that deep submicron technologies can stand very high radiation doses (30 Mrad) provided special layout rules are obeyed.
- Guard rings are effective against SEL, and there are special architectures to reduce SEU sensitivity.
- In this work we have developed the know-how necessary to design radiation tolerant ICs using ELTs: modeling, matching and noise issues have been characterized in detail.
- The validity of this approach has been demonstrated on several mixed-mode ICs which will be used in the LHC experiments.
- Due to the possibility of consistent costs reduction, many experiments decided and are deciding to adopt our approach to make the integrated circuits for detector read-out.
- To pursue this approach in the future, and therefore follow the CMOS technology down-scaling, many issues will have to be addresses:
  - Radiation effects in new materials (low and high K dielectrics)
  - New SEU-tolerant architectures
  - Low-voltage architectures
  - Modeling, matching, noise issues
  - Gate leakage current