FPGAs Operating in a Radiation Environment: Lessons Learned from FPGAs in Space

Brookhaven National Laboratory, May 8-9, 2012

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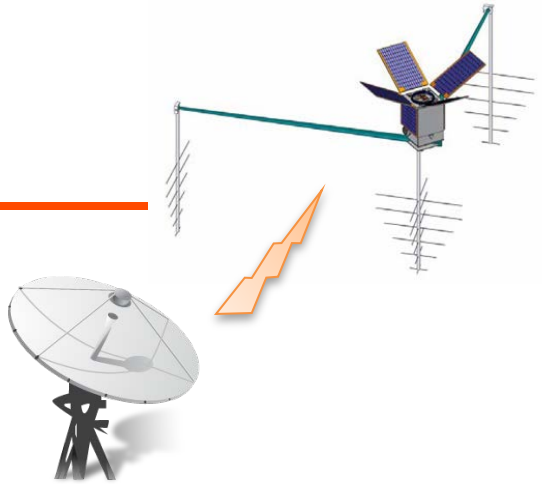

NSF Center for High-Performance Reconfigurable Computing

Presentation Outline

1) NSF CHREC Center
2) FPGAs in Space: Motivation and Examples
3) FPGA Single Event Effects and SEU Sensitivity
4) Emulating Single Event Upsets - Fault Injection
5) Single Event Mitigation Techniques
6) Case Study: LANL Cibola Flight Experiment
7) Summary

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What is CHREC?

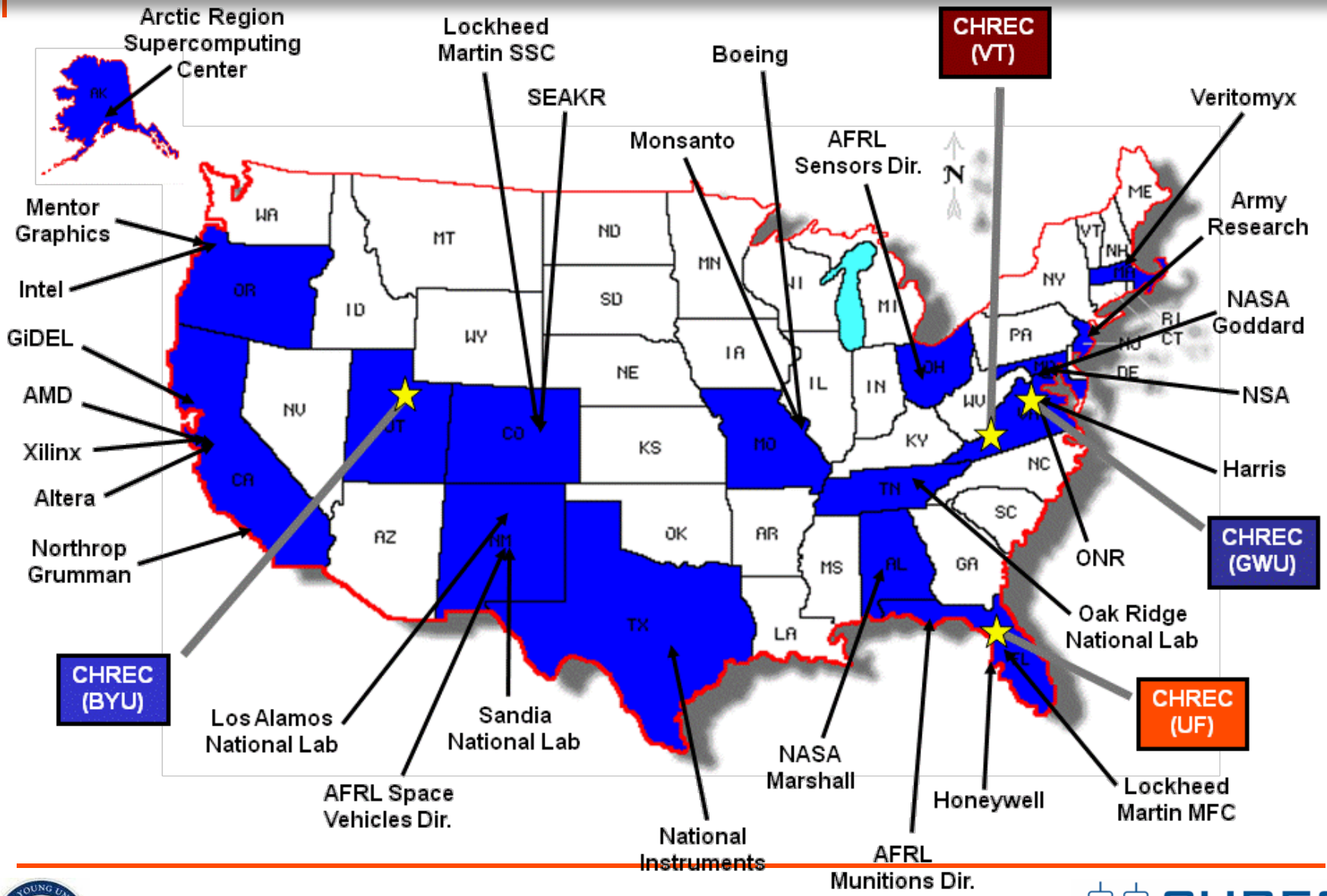
- NSF Center for High-Performance Reconfigurable Computing
  - Unique US national research center in this field, established Jan'07
  - Leading research groups in RC/HPC/HPEC @ four major universities
    - **University of Florida** (lead)
    - **Brigham Young University**
    - **George Washington University**
    - **Virginia Tech**
- Under auspices of I/UCRC Program at NSF
  - **Industry/University Cooperative Research Center**
    - CHREC is supported by CISE & Engineering Directorates @ NSF
  - CHREC is both a National Center and a Research Consortium
    - University groups serve as research base (faculty, students, staff)
    - Industry & government organizations are research partners, sponsors, collaborators, advisory board, & technology-transfer recipients

CHREC Members

1. AFRL Munitions Directorate (4)
2. AFRL Sensors Directorate
3. AFRL Space Vehicles Directorate (2)
4. Altera
5. AMD
6. Arctic Region Supercomputing Center (2)
7. Army RD&E Command
8. Boeing Research & Technology
9. GiDEL
10. Harris
11. Honeywell (2)
12. Intel
13. Lockheed Martin MFC
14. Lockheed Martin SSC
15. Lockheed Martin SVIL
16. Los Alamos National Laboratory (2)
17. Mentor Graphics
18. Monsanto
19. NASA Goddard Space Flight Center
20. NASA Marshall Space Flight Center
21. National Instruments (2)
22. National Security Agency (4)
23. Northrop-Grumman Aerospace Systems
24. Oak Ridge National Laboratory (2)
25. Office of Naval Research
26. Sandia National Laboratories
27. SEAKR Engineering
28. Veritomics
29. Xilinx (2)

42 memberships from 29 members in 2011

CHREC University, Industry, and Government Partners



2012 CHREC Projects

- **F1-12:** A Unified Design Stack for Productivity - from Modeling to Middleware
- **F2-12:** Rapid Application Design and Compilation for FPGAs
- **F3-12:** Application and Architecture Research for Scalable RC Systems
- **F4-12:** High-Level Framework & Tools for Partially Reconfigurable System Development
- **F5-12:** Device Analysis & Comparison - Metrics, Realizability, & Dependability
- **F6-12:** Adaptive Space Computing
- **B1-12:** Rapid FPGA Design Prototyping and Implementation
- **B6-12:** Reliable FPGA-Based Systems
- **G9-12:** GPU Virtualization for Heterogeneous Systems
- **V1-12:** Performance, Programmability, and Portability of Heterogeneous Computing
- **V2-12:** End-to-End Tool Flow for FPGA Productivity

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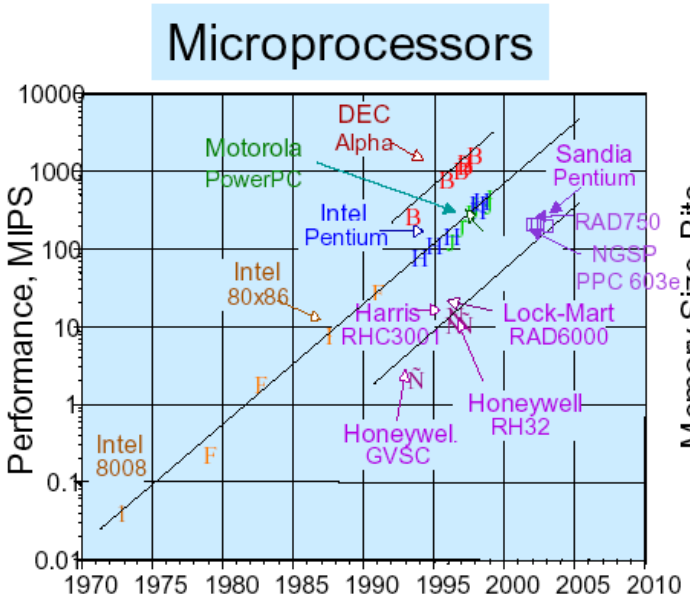
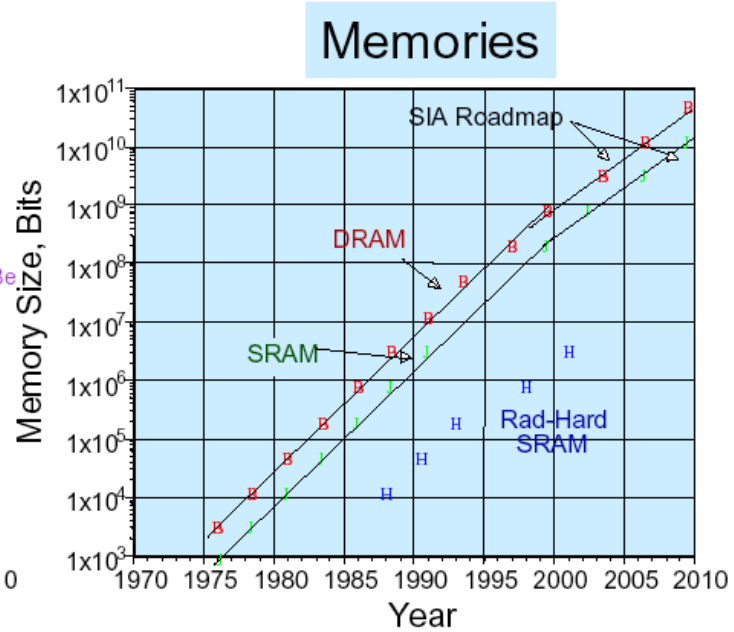
Limitations of Rad-Hard Semiconductors

- Rad-Hard semiconductors are a small fraction of market
- Few Rad-Hard foundries & low volume demand
- High cost for custom Rad-Hard ASIC fabrication
- Latest architectures/technology not available in Rad-Hard



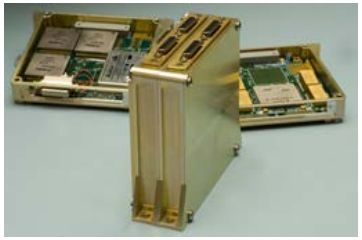


Rad-Hard Lags 2-3 Generations Behind Commercial

Benefits of FPGAs in Space

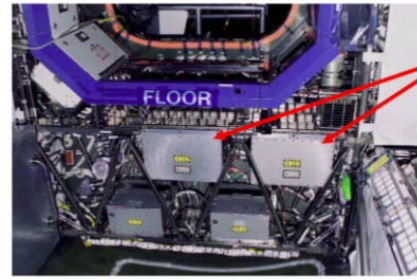
- Efficient Sensor Processing
  - High-throughput computation with dedicated logic
- Resource Multiplexing
  - Multiple Missions
  - Multiple Algorithms
- Improve Designs
  - Correct design flaws after launch
  - Improve design (timing, operation, etc.)
- Design Repair
  - Modify design to operate around device hard faults

SRAM FPGAs in Space: Examples



SpaceCube, NASA GSFC

MARS Rover, NASA JPL

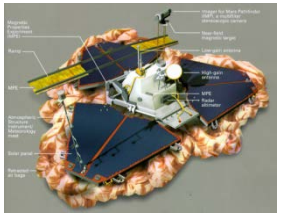


SEAKR
Inernational Space Station
APS

Venus Express, TU Braunschweig

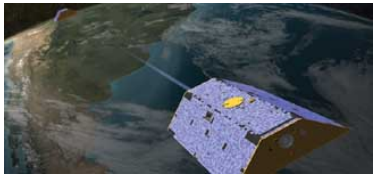
FedSat, Univ. South Australia

OPTUS-C1, Raytheon



MARS Lander, NASA GSFC

Cibola Flight Experiment (CFE), Los Alamos National Laboratory



GRACE, NASA GSFC

Photo courtesy of NASA

MISSE-8
Sandia NL

Many other classified missions using FPGAs

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Challenge: Ionizing Radiation

- Orbit conditions contain high-energy radiation
- Static RAM is sensitive to radiation
- SRAM FPGAs composed of a large amount of static memory

- Can SRAM FPGAs operate reliably in space?

Radiation Effects

- Total Ionizing Dose (TID)
  - Long-term ionizing damage to semiconductor device
  - Charge buildup within transistor gate oxide
  - Increases leakage current & modifies threshold voltage
- Single-Event Latchup (SEL)
  - Single-charged particle may trigger parasitic bi-polar NPN-PNP circuit in CMOS
  - Latchup currents can destroy the device
- Single-Event Upset (SEU)
  - Single-charged particle may transfer charge from one node to another
  - Circuits with feedback, switching of digital logic memory state
- Single-Event Transient (SET)
  - Temporary charge transfer within a node that is *not* a part of a state element
  - May temporarily affect timing or operation of logic, routing, or buffers
- Single-Event Functional Interrupt (SEFI)
  - Upset within a critical state element that interrupts the functionality of the device
  - Examples: configuration controller, global reset, etc.

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Destructive

- Single-Event Upset (SEU)
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- Single-Event Functional Interrupt (SEFI)
  - Upset within a critical state element that interrupts the functionality of the device
  - Examples: configuration controller, global reset, etc.

Non-Destructive

Xilinx Radiation Test Consortium (XRTC)

- Over 15 years of research and testing
- Very active community investigating FPGA radiation effects
  - Government organizations, industry, universities
- Collaboration and sharing of testing results
- Large amount of radiation and fault injection results
  - Effects of ionizing radiation on FPGAs is very well known

History Lesson

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010

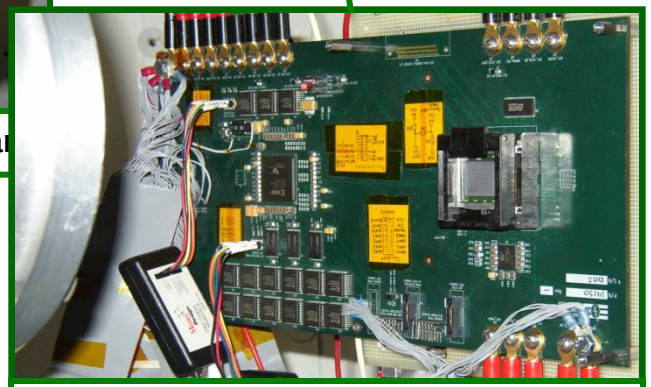
Virtex-2 | Virtex-IIpro | Virtex-4 | Virtex-5

JPL & Xilinx partner up

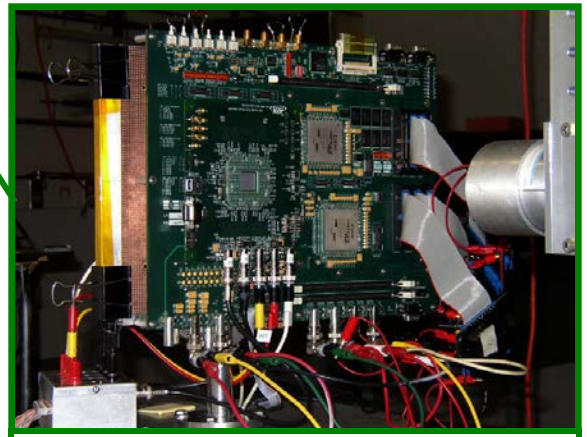
Consortium formation

1st Annual Meeting

0th generation motherboar



1st generation motherboard



2nd generation motherboard

??

3rd generation motherboard

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Radiation Tolerant Xilinx FPGAs

- Virtex QPro
  - 250 nm CMOS

- Virtex-II QV
  - 150 nm CMOS (8 layer)
  - Thin epitaxial layer (latch up resistance)
- Virtex-4 QV
  - 90 nm CMOS
  - Thin epitaxial layer (latch up resistance)

- Virtex-5 QV
  - 65 nm
  - Based on commercial Virtex 5 architecture
  - Radiation Hardened by design
    - Protect configuration cells and user flip-flops

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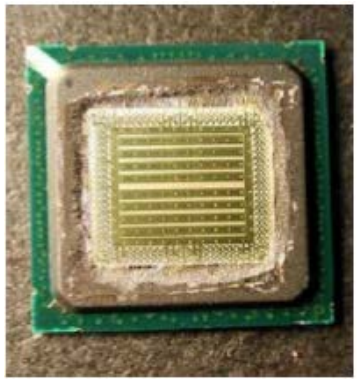
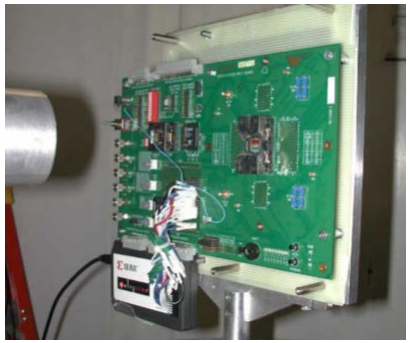
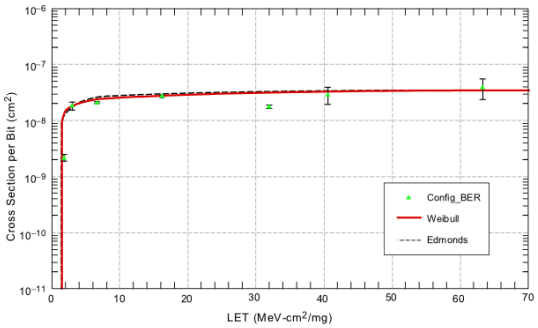
Typical FPGA Radiation Testing

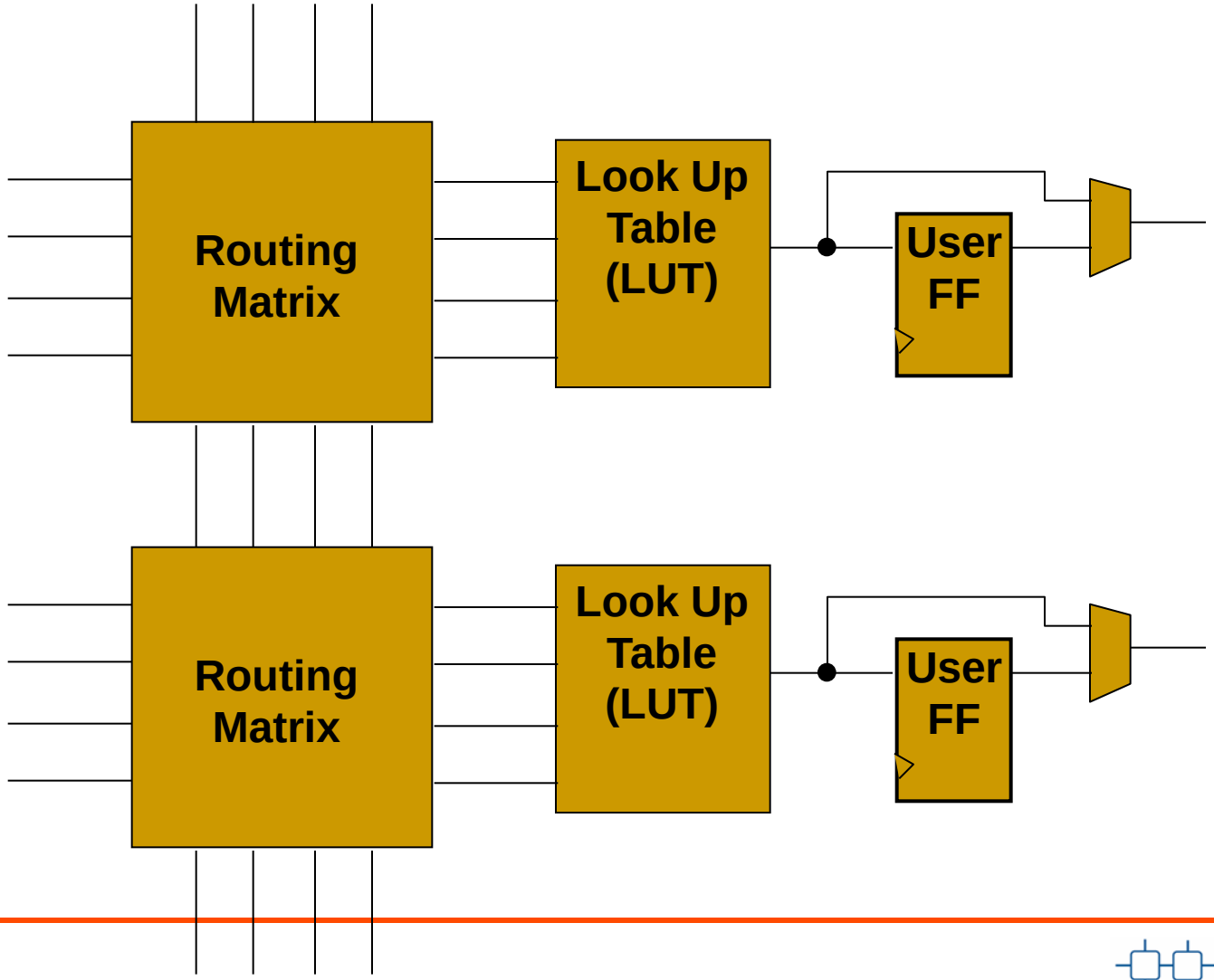
- Latch-up Testing
- Static SEU Testing
  - Identify saturation cross-section and threshold
    - Configuration Cells, BlockRAM cells, user Flip-Flops
  - Heavy Ion Testing and Proton Testing
- SEFI Testing
- Dynamic Testing
  - Application-specific behavior
  - Mitigation Approaches



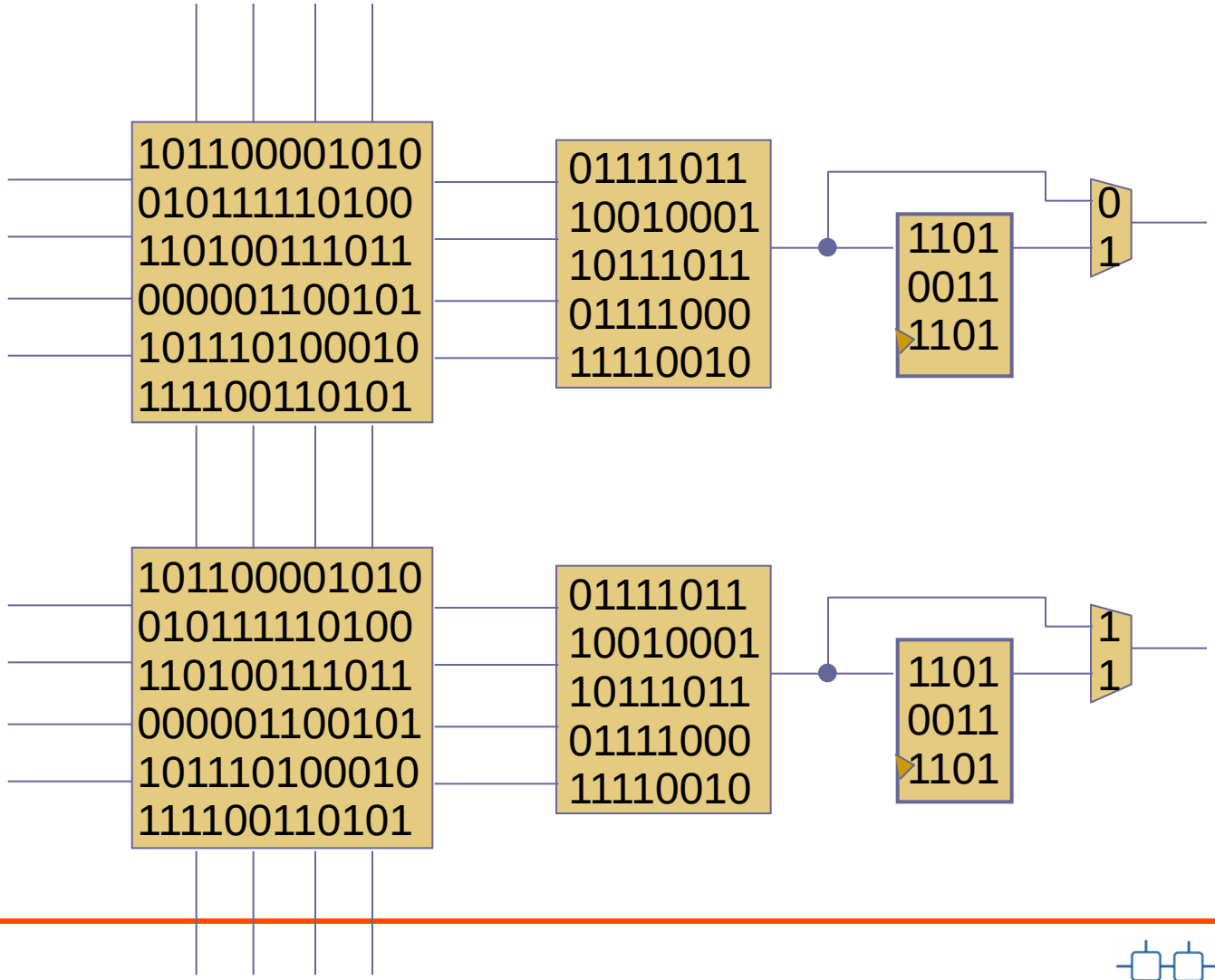




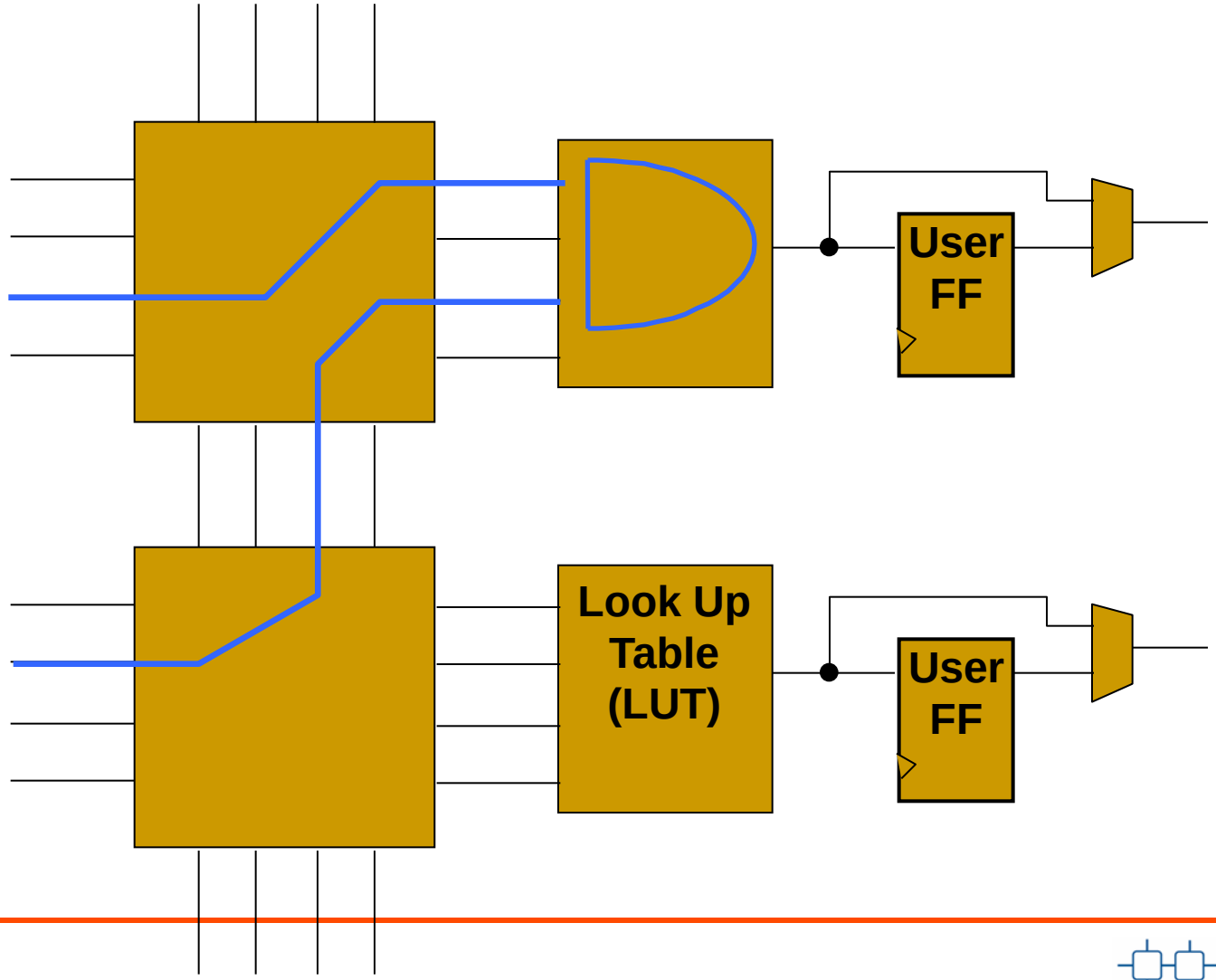
SRAM FPGA Architecture



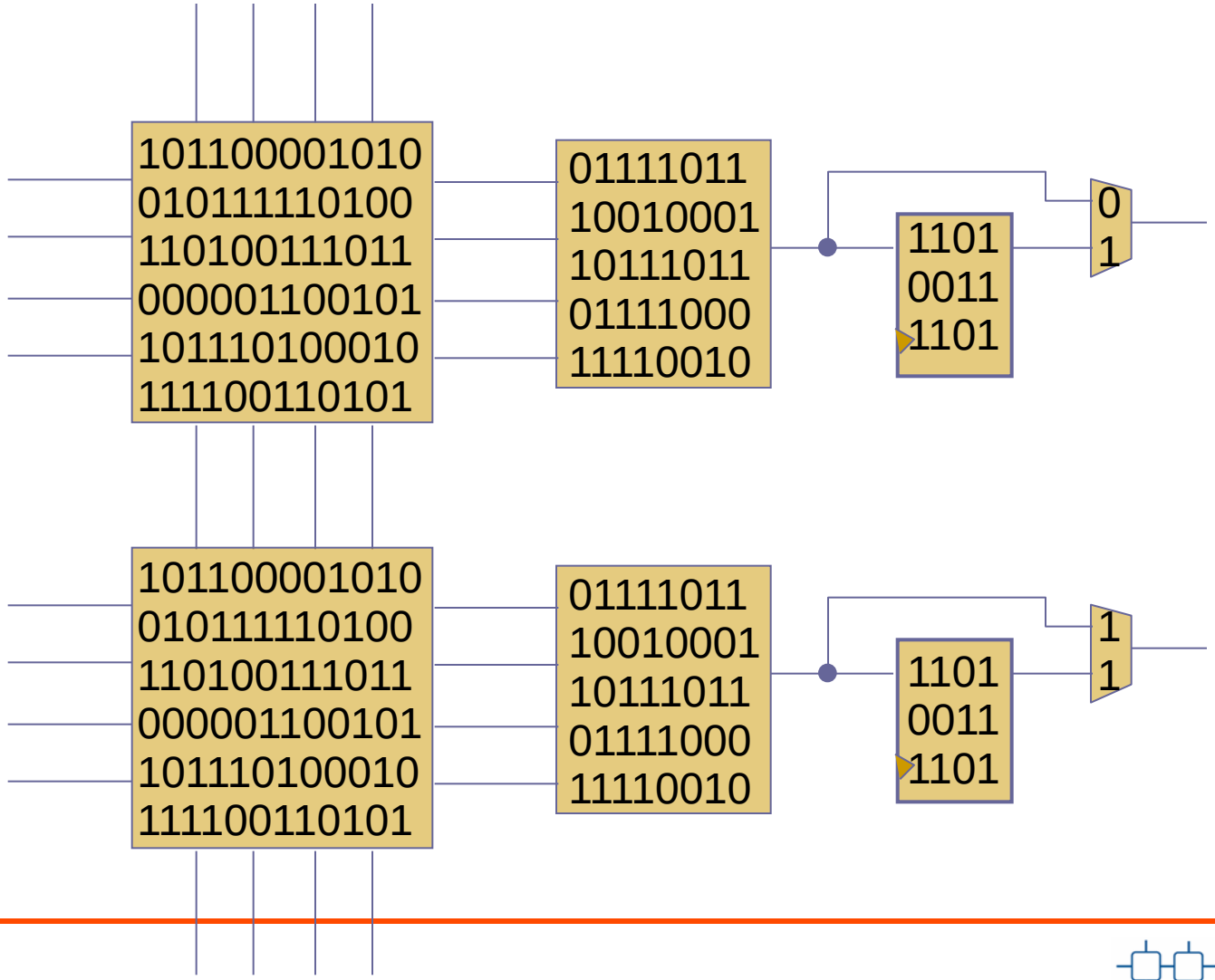
SRAM FPGA Configuration Bits



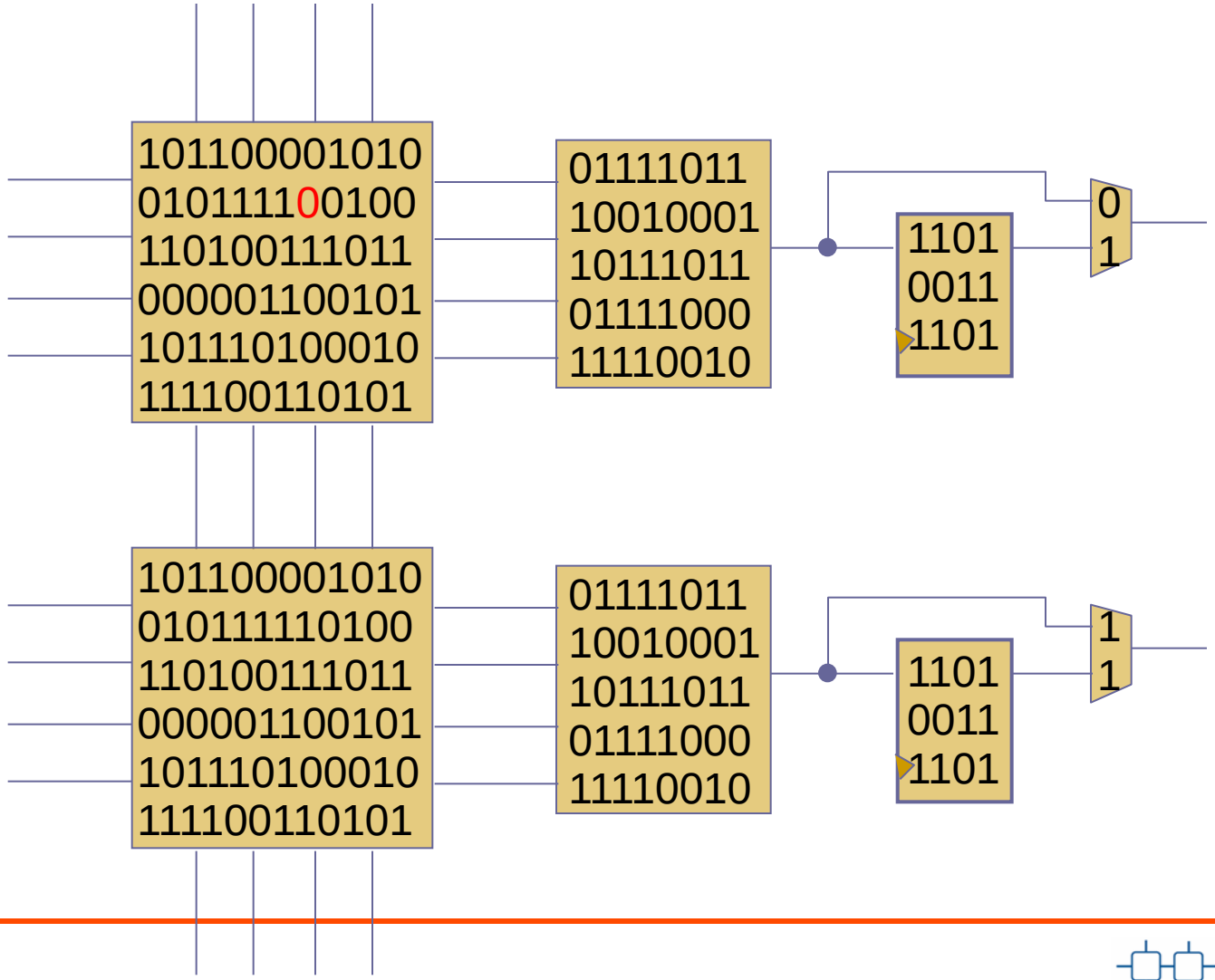
"Configured" FPGA Design



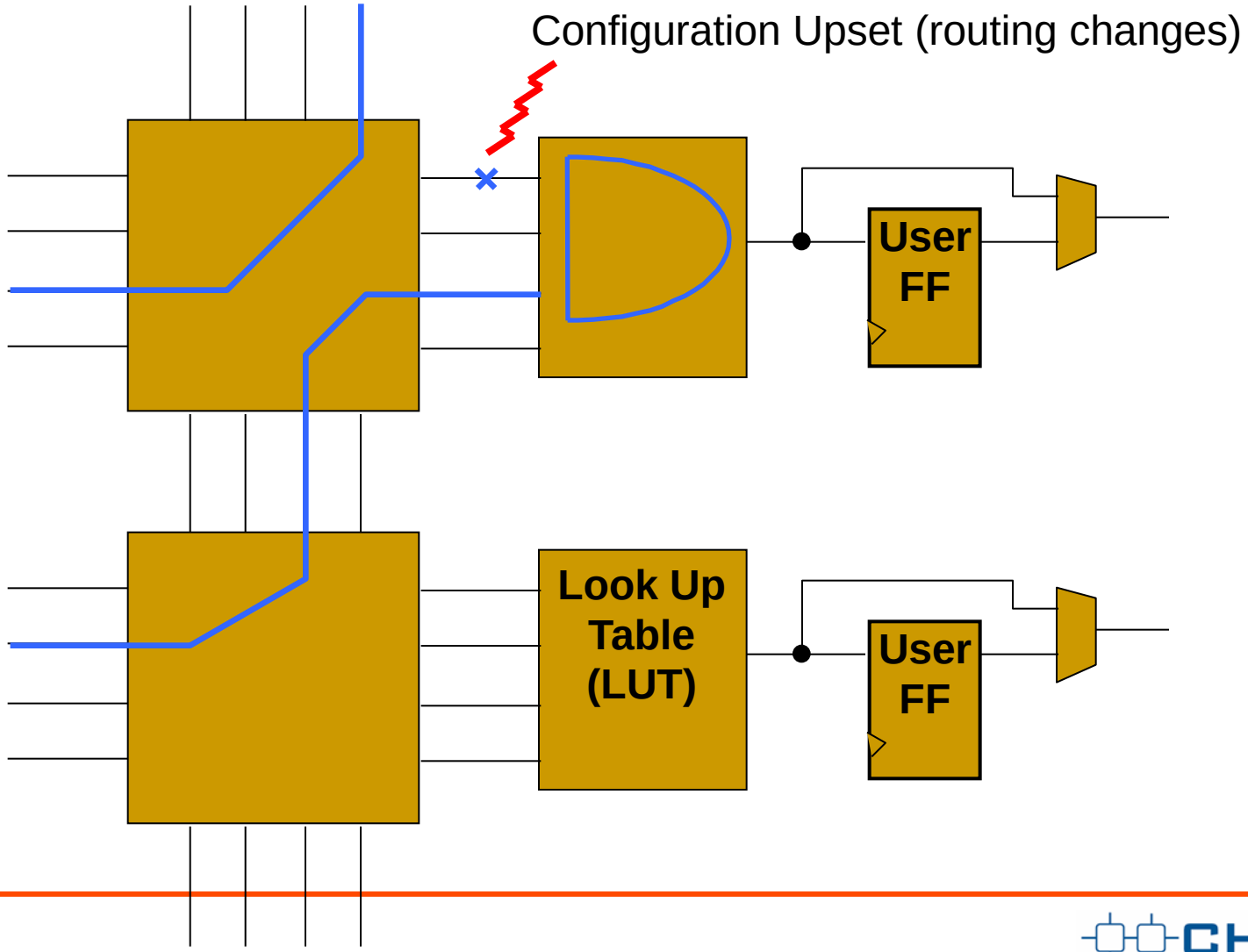
SRAM FPGA Configuration Bits



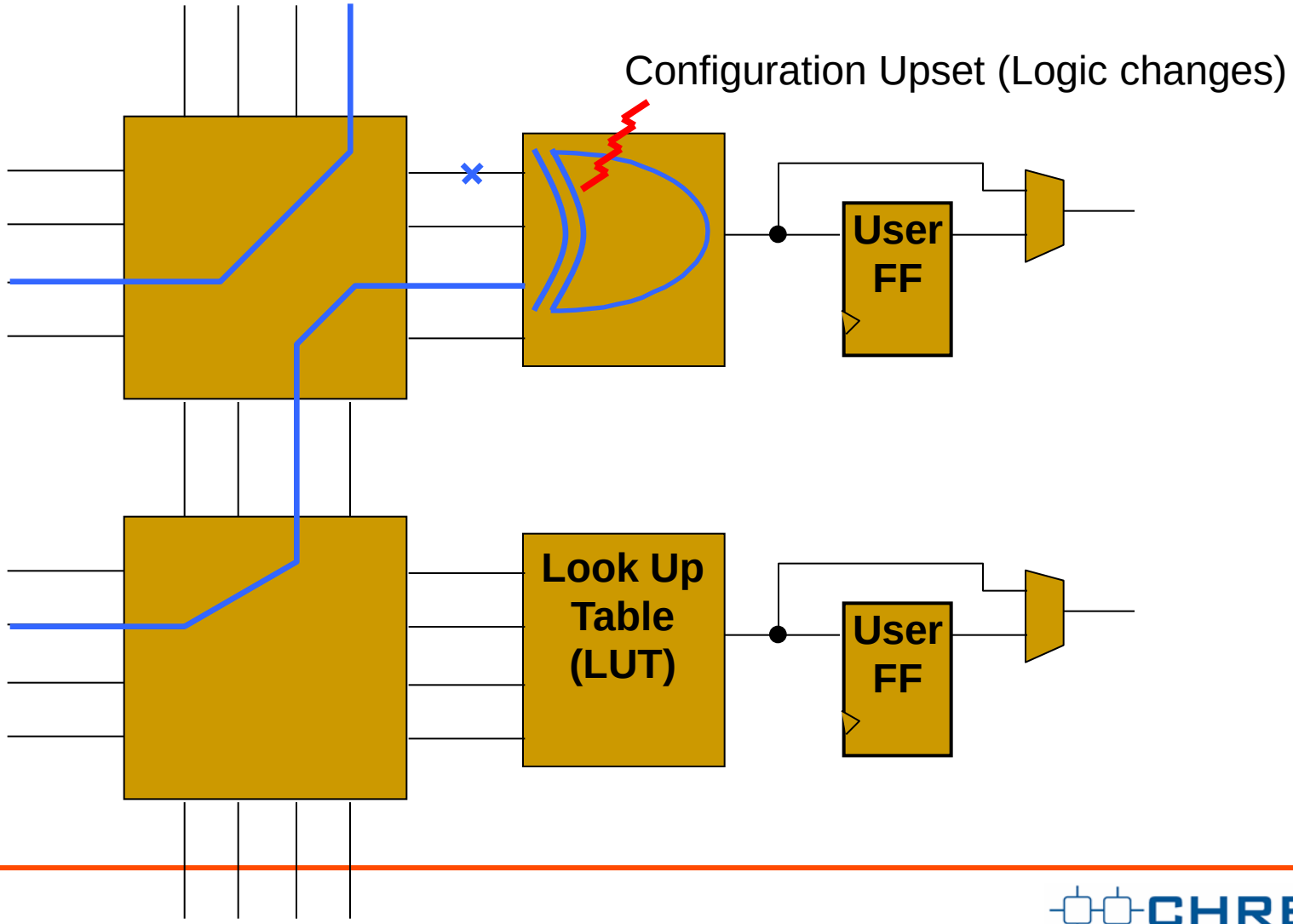
SRAM FPGA Configuration Bits



FPGA Design - Routing Upset



FPGA Design - Logic Upset



Xilinx Virtex5 LX110T Memory

- Vast majority of internal state is used for *configuration memory*

Configuration Bits		**31,119,600**	**92.4%**
User Flip-Flops	**160x54x4**	**276,480**	**0.8%**
LUT RAM	**160x54x4x16**	**1,105,920**	**3.3%**
BlockRAM	**64x1024x18**	**1,179,648**	**3.5%**
Internal Control State	**?**	**?**	**?**

Terrestrial Reliability (JEDEC89A)

Technology Node	Configuration Memory (FIT/Mb)	BRAM (FIT/Mb)	Config. Size (Largest Part of family)	Configuration Soft Failure Rate (FIT)
150 nm (Virtex II)	396	341	20.9 Mb	8,276
130 nm (Virtex IIP)	375	504	21.9 Mb	8,213
90 nm (Virtex 4)	240	353	40.8 Mb	9,792
65 nm (Virtex 5)	138	511	63.9 Mb	8,694

"Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits", Austin Lesea, White Paper 286 (WP286), March 10, 2008, Xilinx Corp.

"SEUs, Not Again!", Austin Lesea, PLD Blog, 10/30/2008, Xilinx Corp.

- Results from other methods are available
  - Atmospheric Testing (Rosetta)
  - QCRIT (simulation)

BYU BRIGHAM YOUNG UNIVERSITY FOUNDED 1875 PROVO, UTAH
CHREC NSF Center for High-Performance Reconfigurable Computing

Orbit Upset Rates

- Depends on many factors
  - Orbit (Apogee, Perigee, Inclination)
  - Solar conditions (Solar cycle, extreme solar events)

Orbit	Apogee (km)	Perigee (km)	Inclination (deg)	Solar Max	Worst Week	Worst Day	Peak 5-Minute
				(SEUs/Device/s)			
GEO	35786	35786	0	1.6E-5	1.7E-2	8.8E-2	3.3E-1
GPS	20200	20200	55	1.6E-5	1.5E-2	7.6E-2	2.9E-1
Molniya	39305	1507	63.2	7.9E-5	1.6E-2	8.2E-2	3.1E-1
Polar	833	833	98.7	5.9E-5	3.5E-3	2.1E-2	7.8E-2
LEO	560	560	35.0	2.5E-5	1.5E-6	1.1E-6	4.0E-6

Xilinx Virtex-4 XQR4VSX55 (22,702,848 config bits/device)

Orbit Upset Rates (FIT)

- Solar Max, GEO
  - FIT/device (configuration): 5.76×10^8
    - (5 orders of magnitude higher than atmospheric SEUs)

Orbit	Apogee (km)	Perigee (km)	Inclination (deg)	Solar Max	Worst Week	Worst Day	Peak 5-Minute
				(FIT/Mb)			
GEO	35786	35786	0	2.7E6	2.8E6	1.5E10	5.5E10
GPS	20200	20200	55	2.7E6	2.5E9	1.3E10	4.8E10
Molniya	39305	1507	63.2	1.3E7	2.7E9	1.4E10	5.2E10
Polar	833	833	98.7	9.8E6	5.8E8	3.5E9	1.3E10
LEO	560	560	35.0	4.2E6	2.5E5	1.8E5	6.7E10

Xilinx Virtex-4 XQR4VSX55 (22,702,848 config bits/device)

Table 9d. CREME96 Calculated Orbital Upset Rates

Configuration Memory Cells
Upsets/Device-Day
Quiet Solar Maximum Conditions

Orbit	**LEO**	**LEO**	**POLAR**	**CONST.**	**GEO**
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
XQR4VSX55	0.73	7.56	6.02	23.3	4.28
XQR4VFX60	0.69	7.12	5.67	21.9	4.03
XQR4VFX140	1.61	16.7	13.3	51.6	9.5
XQR4VLX200	2.03	21.1	16.8	65.1	11.9

Table 9b. CREME96 Calculated Orbital Upset Rates

Block Memory Cells
Upsets/Device-Day assuming all are used
Quiet Solar Maximum Conditions

Orbit	**LEO**	**LEO**	**POLAR**	**CONST.**	**GEO**
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
XQR4VSX55	0.72	4.05	4.00	13.3	4.49
XQR4VFX60	0.52	2.94	2.90	9.63	3.26
XQR4VFX140	1.24	6.99	6.90	22.9	7.75
XQR4VLX200	0.75	4.25	4.20	13.9	4.71

Table 9c. CREME96 Calculated Orbital Upset Rates

User Flip-Flops Cells
Upsets/Device-Day, assuming all are used, half storing zero
Quiet Solar Maximum Conditions

Orbit	**LEO**	**LEO**	**POLAR**	**CONST.**	**GEO**
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
XQR4VSX55	0.0066	0.0702	0.0568	0.223	0.0387
XQR4VFX60	0.0067	0.0722	0.0585	0.229	0.0398
XQR4VFX140	0.0169	0.180	0.146	0.573	0.0995
XQR4VLX200	0.0238	0.254	0.205	0.809	0.141

"VIRTEX-4QV STATIC SEU CHARACTERIZATION SUMMARY", JPL Publication 08-16 4/08

Single Event Functional Interrupt (SEFI)

- Single event that affects proper operation of the entire device
  - Requires reconfiguration of device (interrupt function)
- SEFI Types
  - Power-On Reset (POR)
    - Global reset of all internal storage
    - Loss of all program and state data
  - SelectMAP/JTAG
    - Inability to configure or readback configuration data
  - Readback/Scrub
    - Cannot correct some configuration upsets using readback/scrub
- SEFI cross section very small
  - Must be detected and repaired
- Well known methods to detect and repair SEFIs
  - Requires external configuration controller/scrubber

SEFI Orbital Upset Rates

Table 9a. CREME96 Calculated Orbital Upset Rates

Functional Interrupts (All Virtex-4QV)
Upsets/Device-Day
Quiet Solar Maximum Conditions

Orbit	**LEO**	**LEO**	**POLAR**	**CONST.**	**GEO**
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
POR	2.23×10^{-6}	2.73×10^{-5}	2.09×10^{-5}	8.40×10^{-5}	1.21×10^{-5}
SMAP	1.82×10^{-6}	2.46×10^{-5}	1.88×10^{-5}	7.81×10^{-5}	9.46×10^{-6}
GSIG	1.27×10^{-6}	2.41×10^{-5}	1.66×10^{-5}	7.31×10^{-5}	4.87×10^{-6}
	Device-**Years**/Event				
All SEFIs (Combined)	515	36	49	11	103

"VIRTEX-4QV STATIC SEU CHARACTERIZATION SUMMARY", JPL Publication 08-16 4/08

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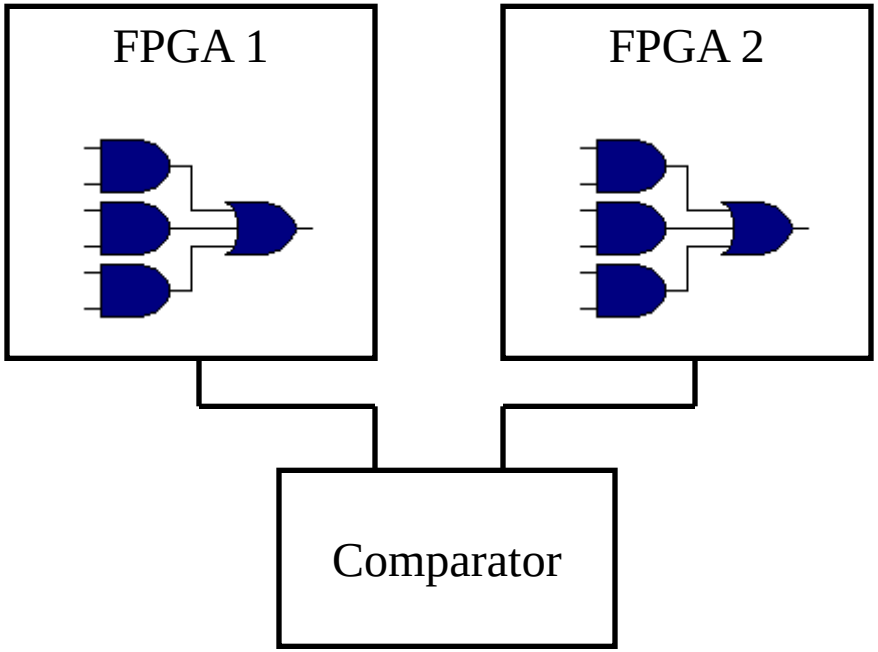
SEU Fault Injection

- What is the impact of SEUs within the FPGA configuration memory?
  - Does every configuration upset cause a design failure?
  - What types of design failures occur?

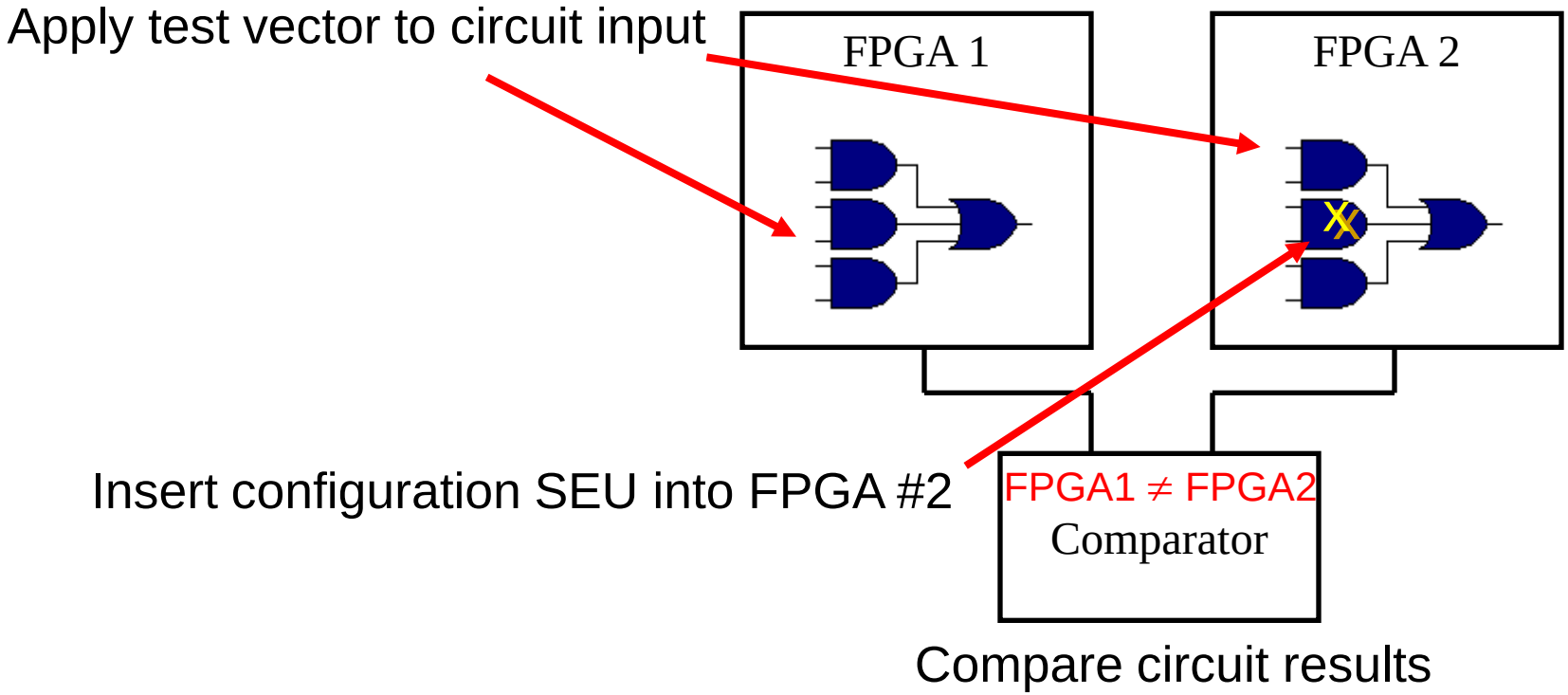
- Solution: emulate SEUs through fault injection
  - Artificially inject SEUs in the FPGA and observe behavior

BYU Fault Injection Simulator

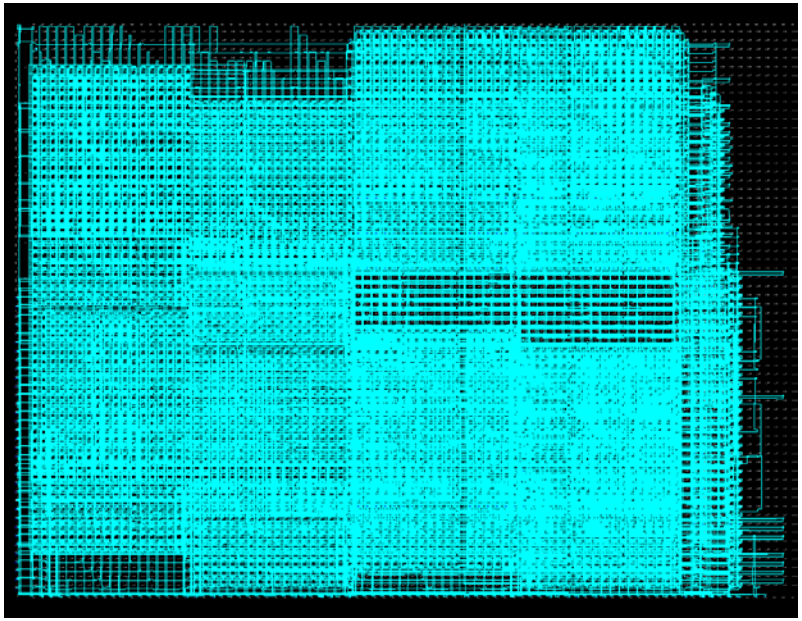
- Configure user design onto two identical FPGAs
- Compare results of two designs using Comparator FPGA
- Insert configuration SEUs into design under test (FPGA2) and compare results
- If discrepancies between FPGAs are found, record configuration error



SEU Insertion Example #1

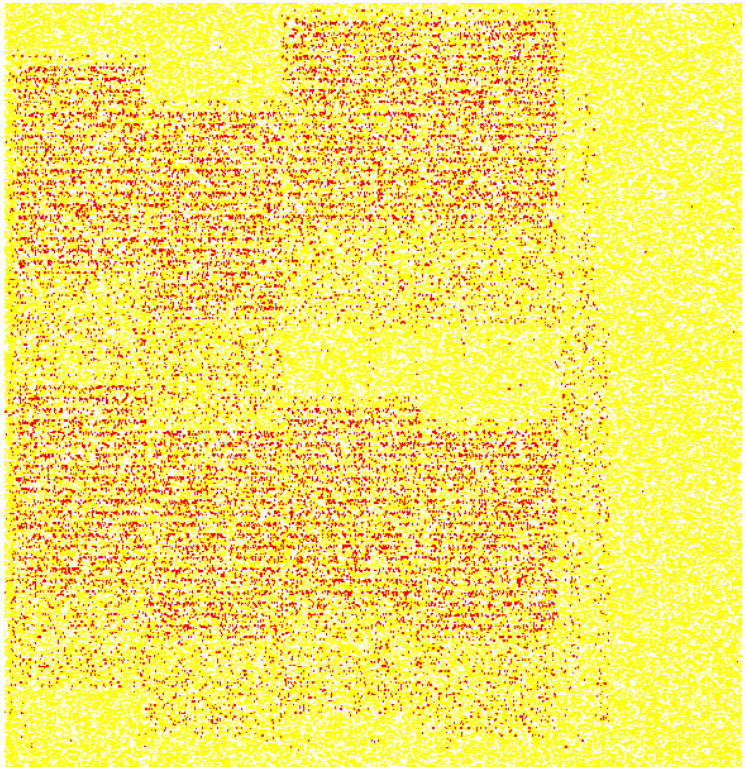


Configuration Upset Simulator



Design Layout (FPGA Editor)

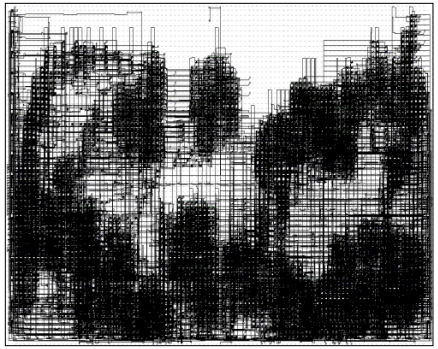
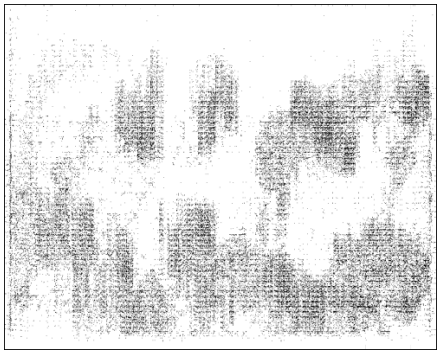
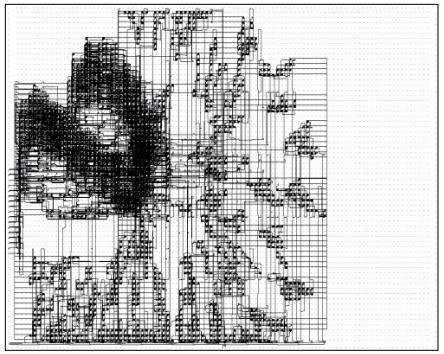
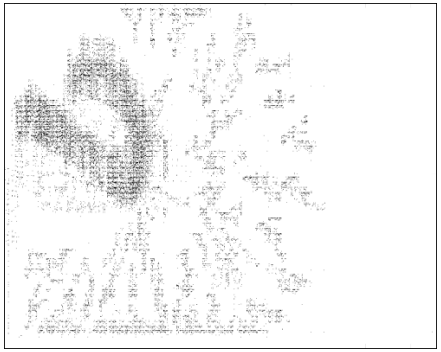
- Routing
- Logic
- Global resources



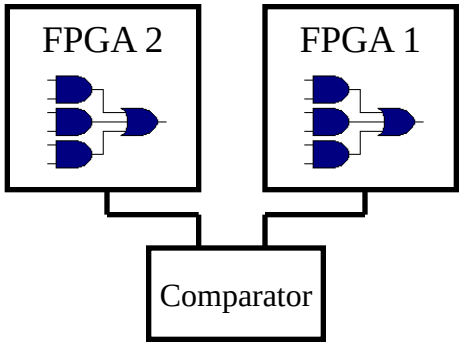
Configuration Fault Map

- **Highlights location of configuration faults causing errors**

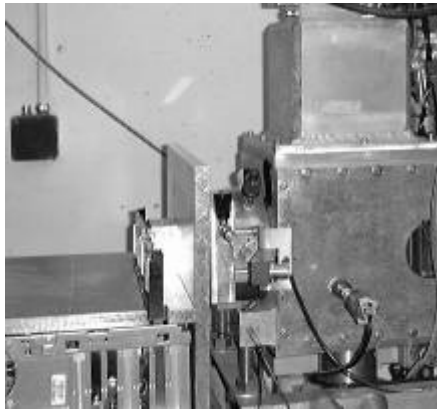
Sample Sensitivity Results

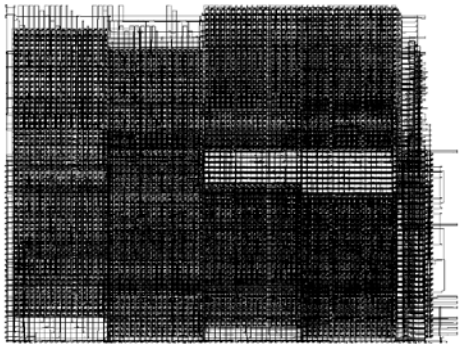
	FPGA Editor Layout	Sensitivity Map
DSP Kernel		
	5,746 slices (46%)	575,448 bits (9.9%)
Synthetic Design		
	2,538 slices (20%)	189,835 bits (3.3%)

SEU Fault Injection Simulator

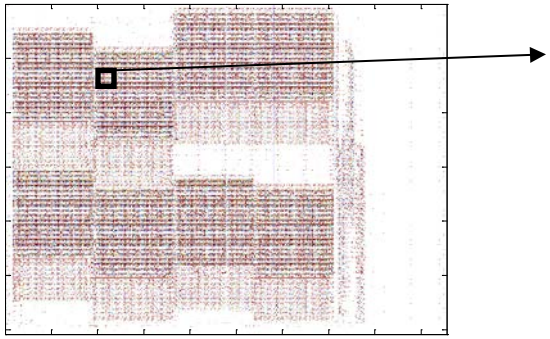


Measure configuration Sensitivity by artificially Inserting faults

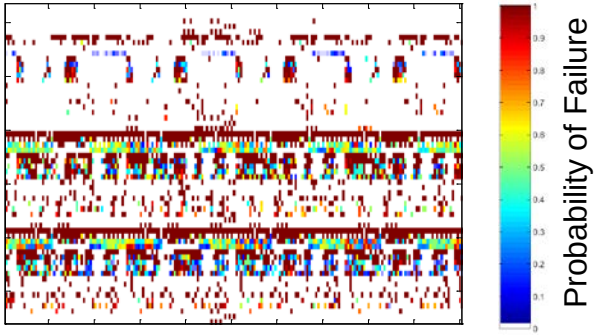




Original Circuit



Sensitivity Map



Zoom Sensitivity Map

Simulator Results

Design	Logic Slices	Percent of Device	Failures	Configuration Sensitivity	Normalized Sensitivity
LFSR 18	2178	15.8%	66797	1.15%	7.3%
LFSR 36	4356	31.5%	137861	2.37%	7.5%
LFSR 54	6534	47.3%	208536	3.59%	7.6%
LFSR 72	8712	63.0%	279450	4.81%	7.6%
VMULT 18	583	4.2%	60929	1.05%	24.9%
VMULT 36	2206	16.0%	232239	4.00%	25.0%
VMULT 54	4781	34.6%	520747	8.96%	25.9%
VMULT 72	8308	60.1%	856802	14.75%	24.5%
MULT 12	144	1.0%	13263	0.23%	21.9%
MULT 24	561	4.1%	52454	0.90%	22.2%
MULT 36	1249	9.0%	122657	2.11%	23.4%
MULT 48	2205	16.0%	220197	3.79%	23.8%

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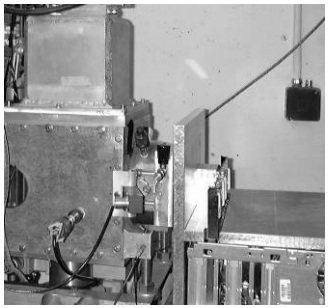
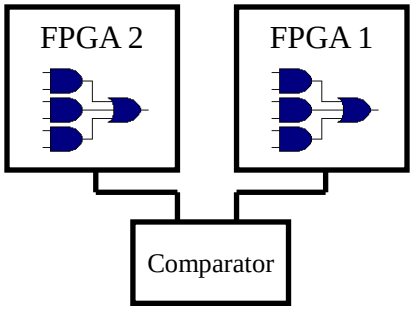
Model Validation



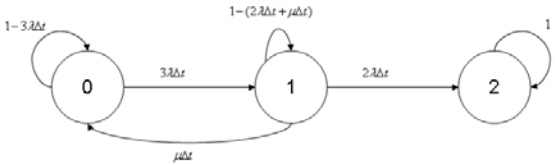
Proton Beam

Test Design Suite



Fault Injection

Compare and evaluate



Reliability Model

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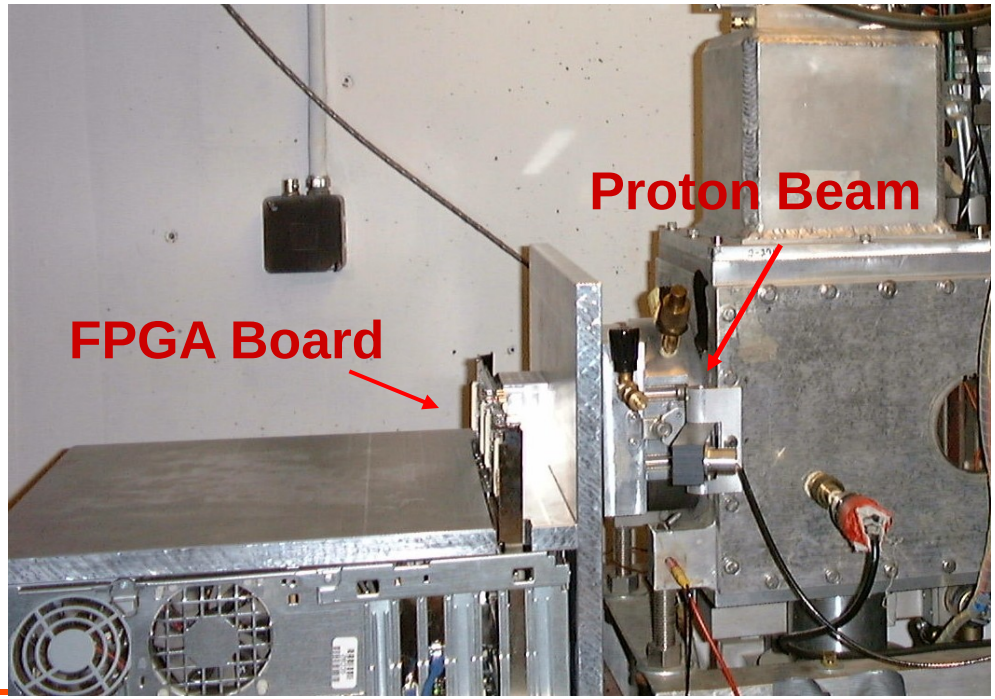
Simulator Verification

- Results from SEU simulator validated with a radiation source
  - Verify accuracy of artificial simulator
  - Identify upset in non-configuration state

UC Davis, Crocker Nuclear Laboratory
- Medium-energy particle accelerator (76-inch cyclotron)
- 63 MeV proton source
- Flux: 1e7 particles/cm^2/second: (~1 upset/second)
- 16 hour test (~25,000 upsets)

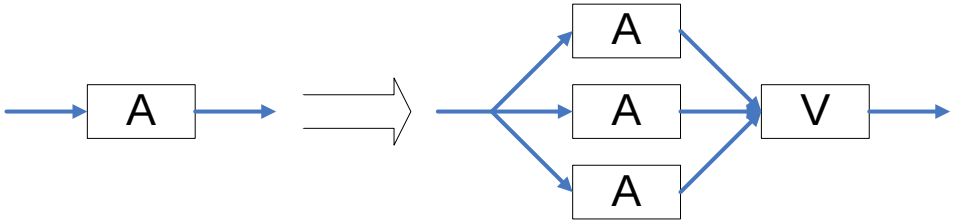


Presentation Outline

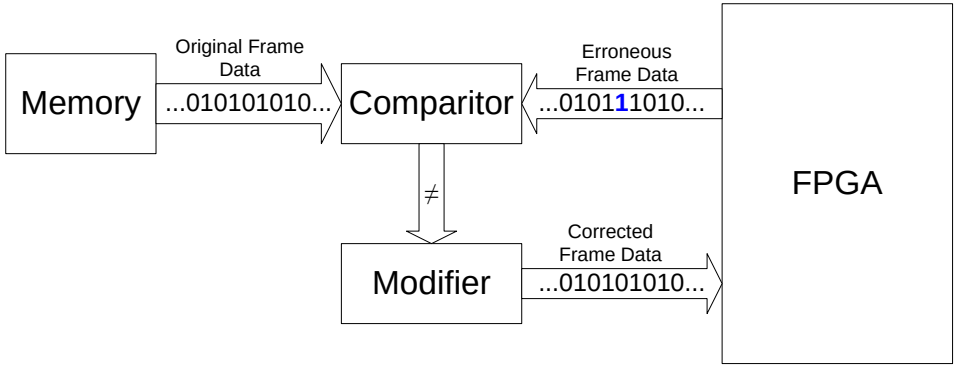
1) NSF CHREC Center
2) FPGAs in Space: Motivation and Examples
3) FPGA Single Event Effects and SEU Sensitivity
4) Emulating Single Event Upsets - Fault Injection
5) Single Event Mitigation Techniques
6) Case Study: LANL Cibola Flight Experiment
7) Summary

FPGA Fault Tolerant Strategy

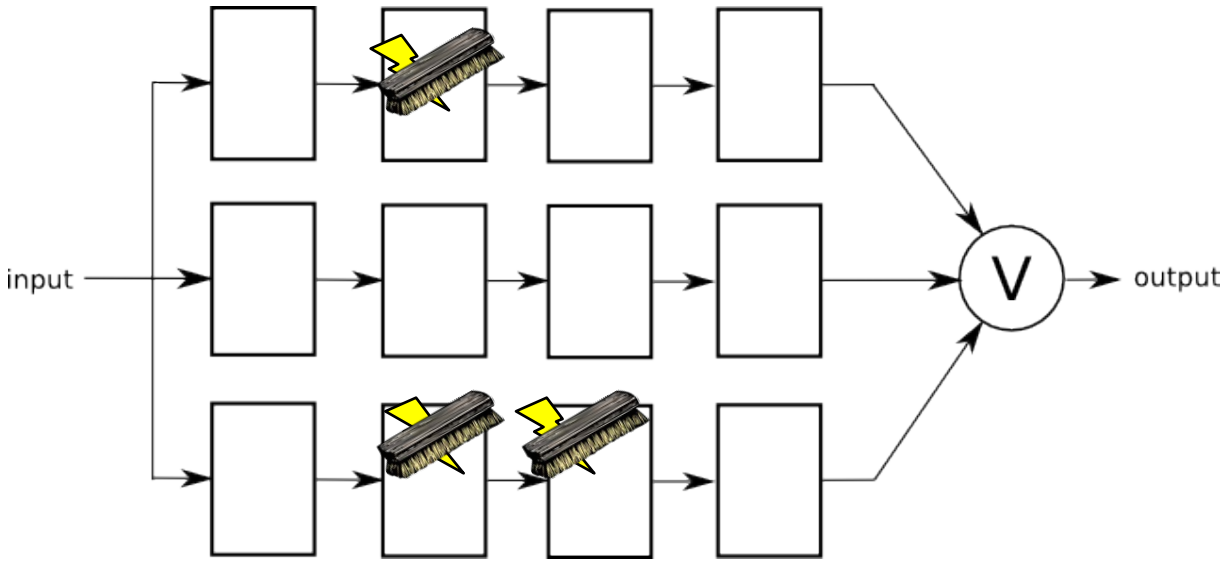
- FPGAs provide SEU mitigation through redundancy and scrubbing
- Triple Modular Redundancy (TMR)
  - Triplicate module to introduce redundancy
  - Vote on outputs of triplicated module
  - Use greatest common result



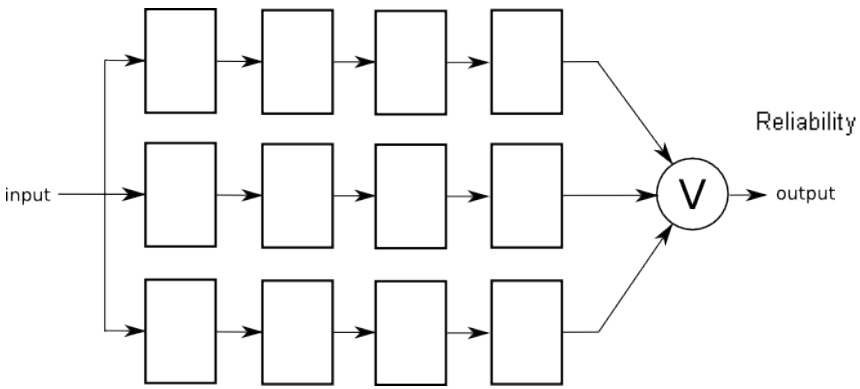
- Configuration Scrubbing
  - Readback frame data
  - Compare frame to original
  - Correct erroneous bits in frame
  - Writeback frame to FPGA

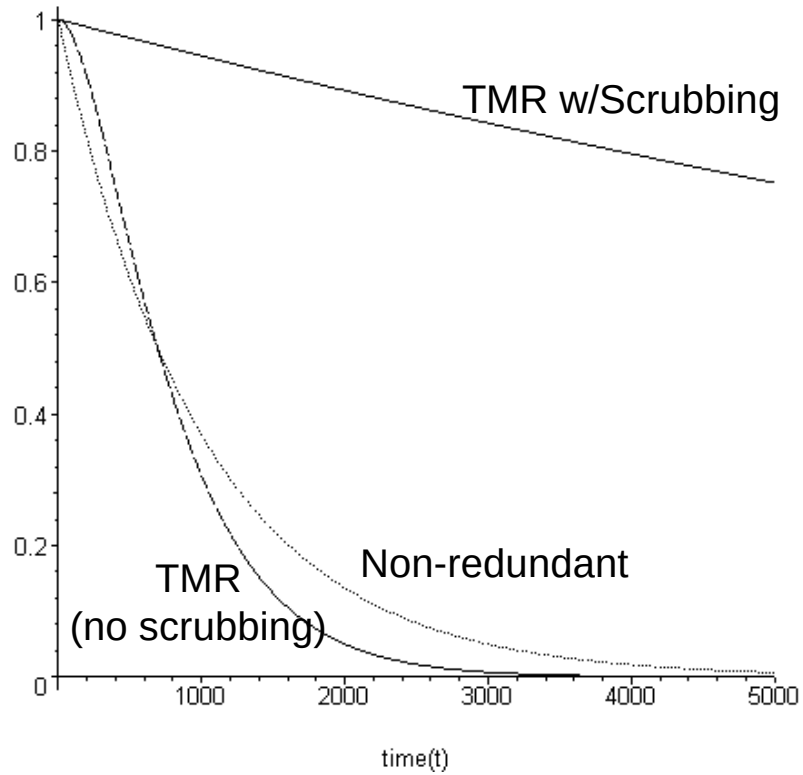


TMR & Scrubbing Example

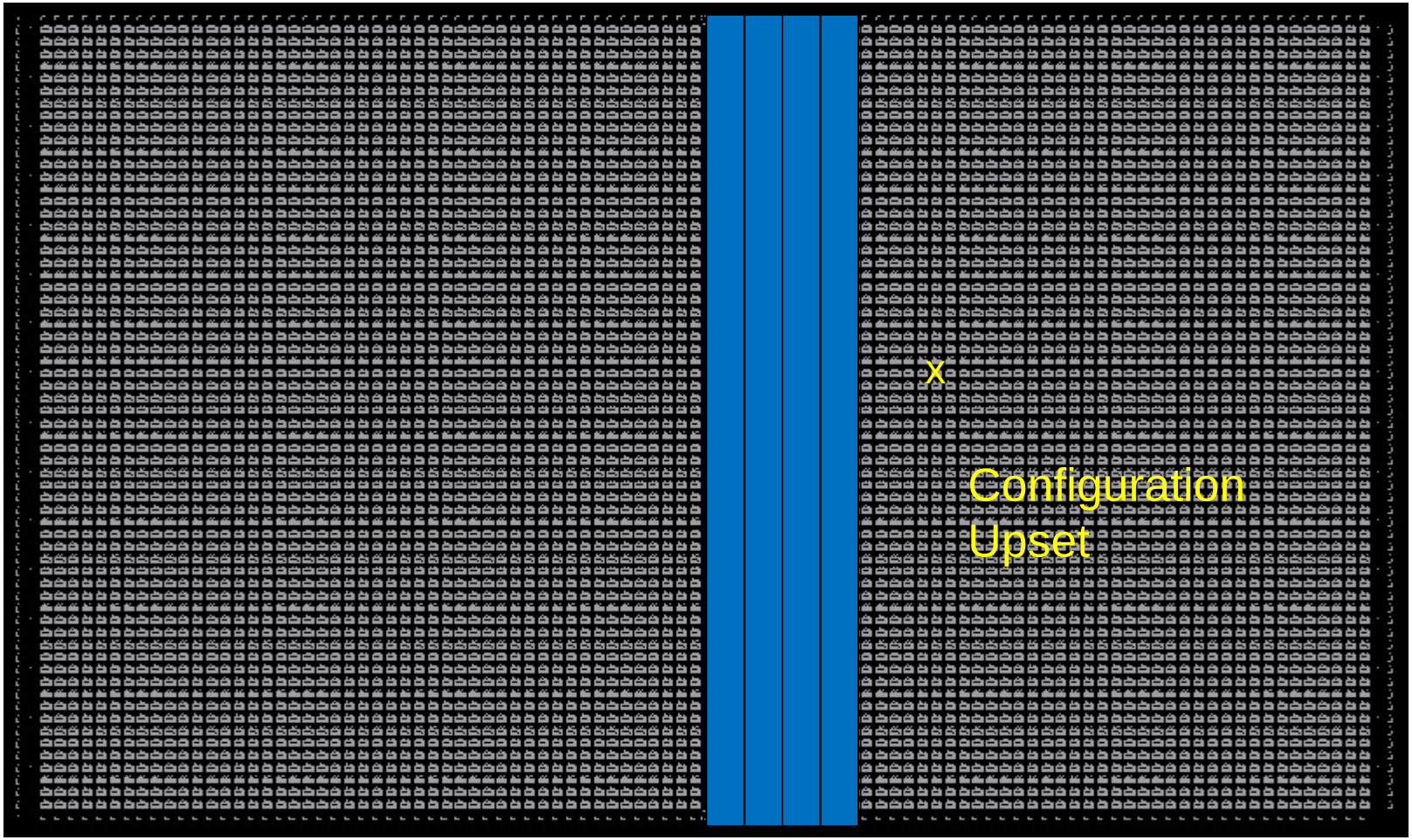


TMR & Scrubbing Reliability

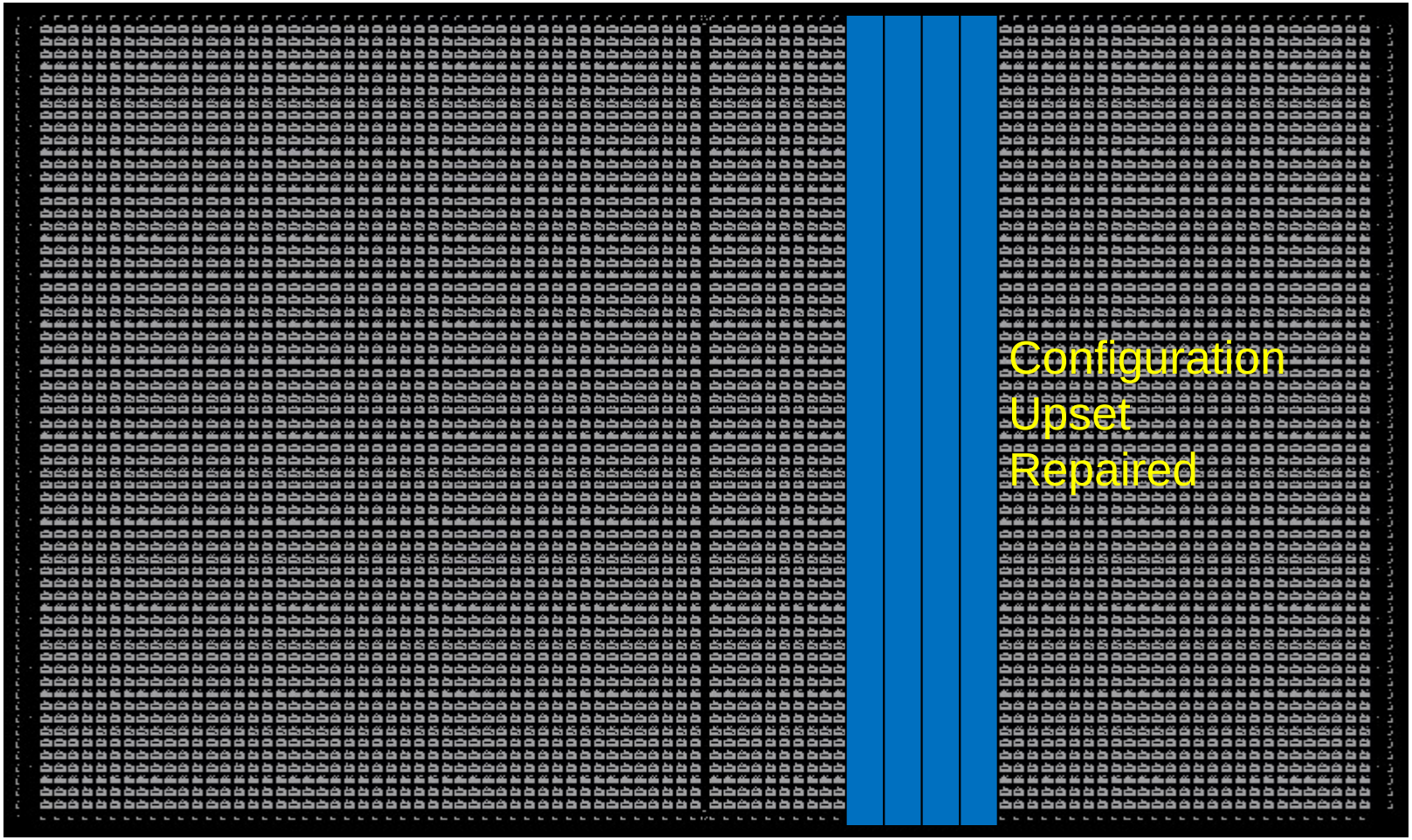




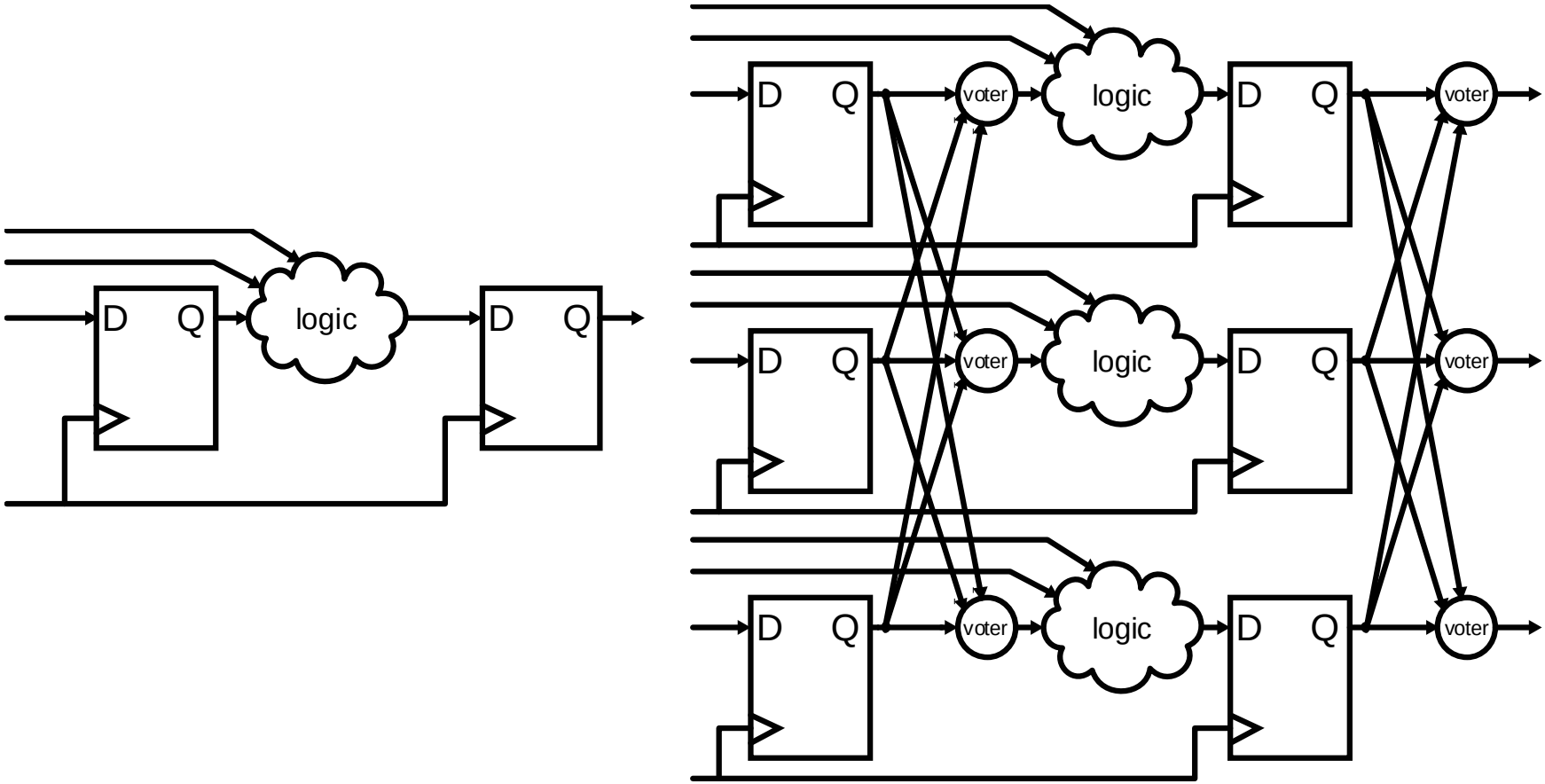
Configuration Scrubbing Example



Configuration Scrubbing Example



Triple Modular Redundancy (TMR)



BL-TMR (BYU/LANL TMR)

- EDIF data structure & API
  - Parse, represent, and manipulate EDIF
- Available tools:
  - EDIF parser
  - Half-latch removal
  - SRL replacement
  - Feedback cutset tool
  - Full and partial TMR
  - Detection circuitry insertion
  - EDIF output
- Project size
  - ~50 Java packages
  - 350+ Java classes
  - 478,401 lines of code
  - Includes contributions from CHREC member LANL

```
[brian@tiger:test] java -cp ~/jars/BLTmr.jar
byucc.edif.tools.tmr.FlattenTMR ../no_tmr/synth/counters80.edf --
removeHL --full_tmr --technology virtex -p xcv1000fg680 --log
counters80.log

BLTmr Tool version 0.2.3, 12 Oct 2006
Search for EDIF files in these directories: [.]
Parsing file ../no_tmr/synth/counters80.edf
Removing half-latches...
Flattening
            Flattened circuit contains 3451 primitives, 3461
nets, and 13692 net connections
Processing: ASUF 1.0

Forcing triplication of instance safeConstantCell_zero

Analyzing design . . .
            Full TMR requested.
Triplicating design . . .
domainreport=BLTmr_domain_report.txt
            Added 1931 voters.
            3431 instances out of 3451 cells triplicated (99%
coverage)
            6862 new instances added to design.
            3431 nets triplicated (6862 new nets added).
            0 ports triplicated.
```

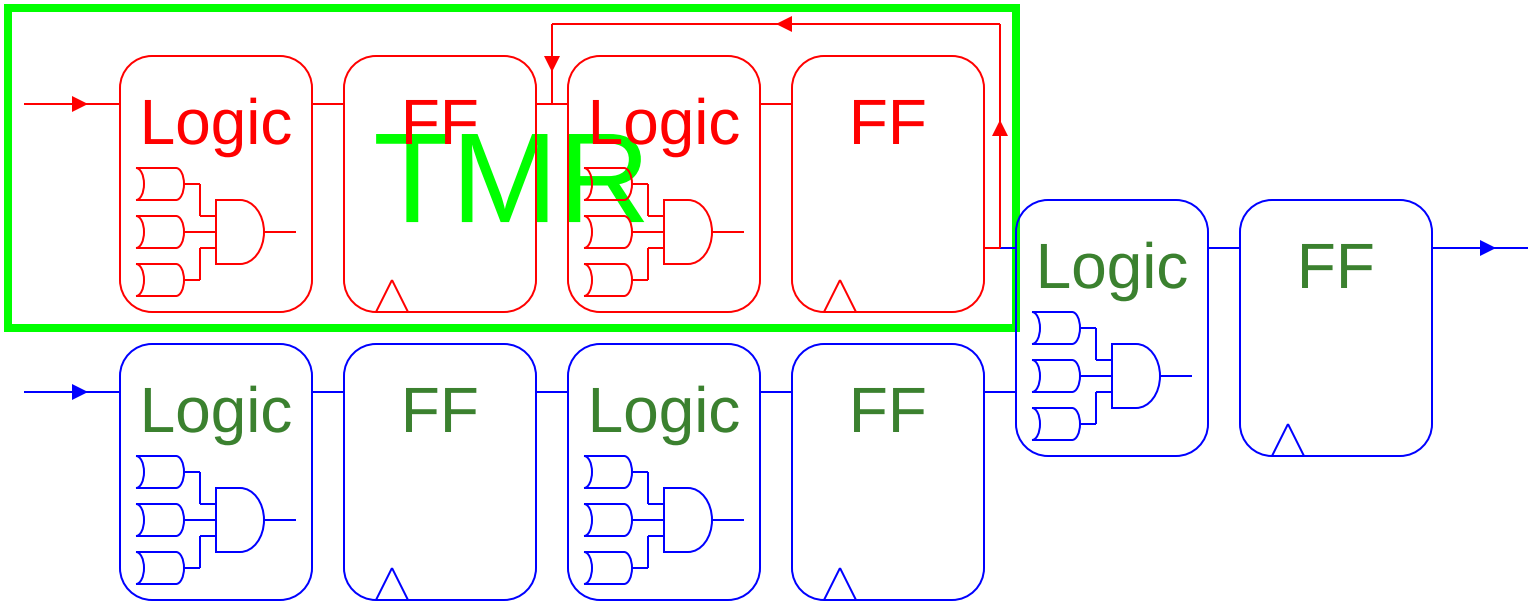
Tools and code available at: http://sourceforge.net/projects/byuediftools/

CHREC NSF Center for High-Performance Reconfigurable Computing

Cost of TMR

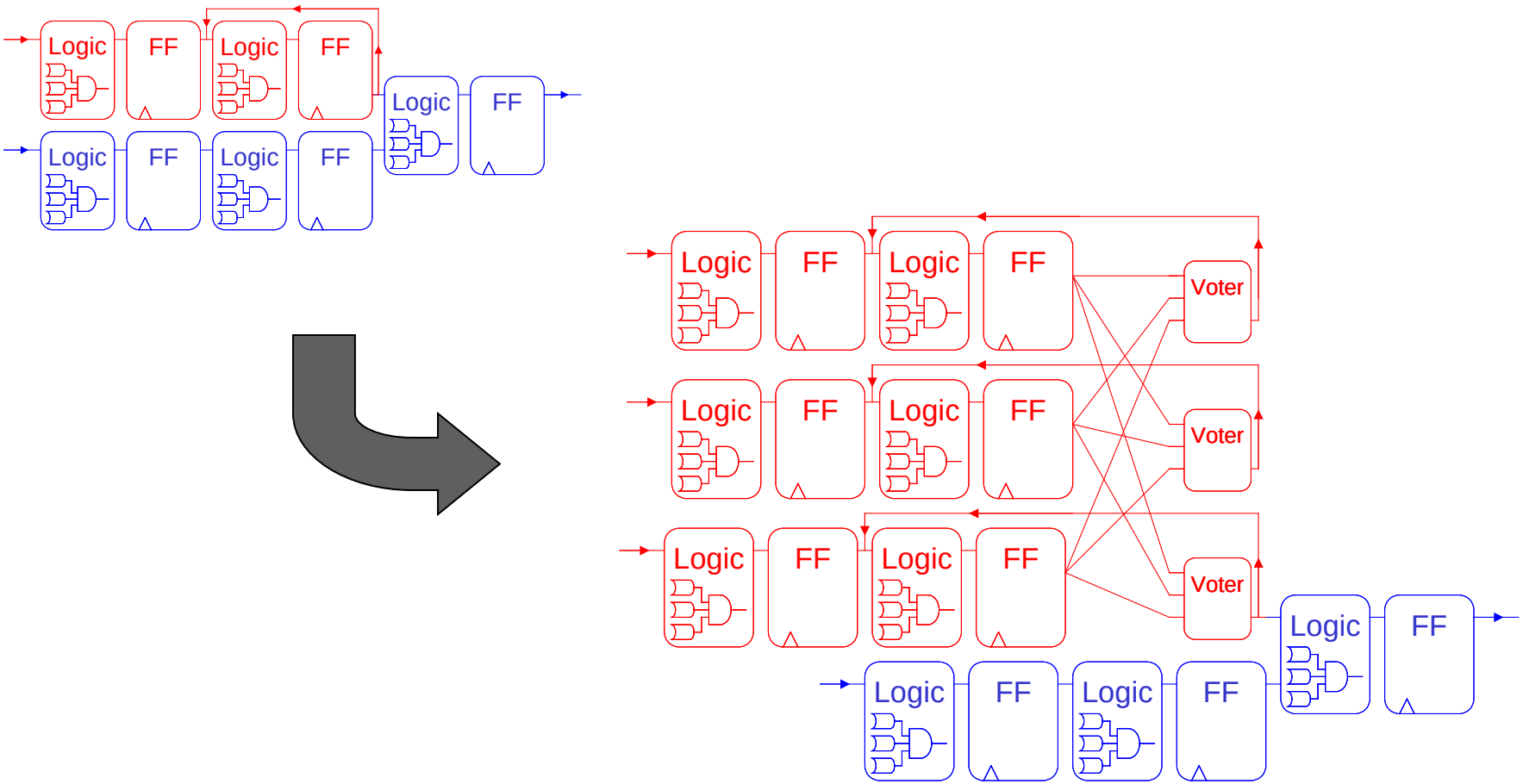
	Size Increase	Critical Path Before TMR	Critical Path After TMR	% Increase in Critical Path
blowfish	3.1X	28.3 ns	31.7 ns	12.0%
des3	3.4X	11.1 ns	13.6 ns	22.5%
qpsk	3.1X	80.0 ns	83.9 ns	4.9%
free6502	3.3X	29.6 ns	33.1 ns	11.8%
T80	3.3X	27.8 ns	33.7 ns	21.2%
macfir	3.9X	14.4 ns	19.5 ns	35.4%
serial_divide	4.1X	9.2 ns	12.2 ns	32.6%
planet	3.1X	10.9 ns	12.6 ns	15.6%
s1488	3.1X	9.9 ns	12.0 ns	21.2%
s1494	3.1X	10.4 ns	12.2 ns	17.3%
s298	3.1X	15.8 ns	19.1 ns	20.9%
tbk	3.9X	10.3 ns	12.9 ns	25.2%
synthetic	4.0X	9.9 ns	10.4 ns	5.1%
lfsrs	6.3X	9.0 ns	12.7 ns	41.1%
ssra_core	3.5X	6.1 ns	7.2 ns	18.0%
mean	**3.6X**	**8.17 ns**	**12.08 ns**	**16.0%**

Persistent Circuit Structures

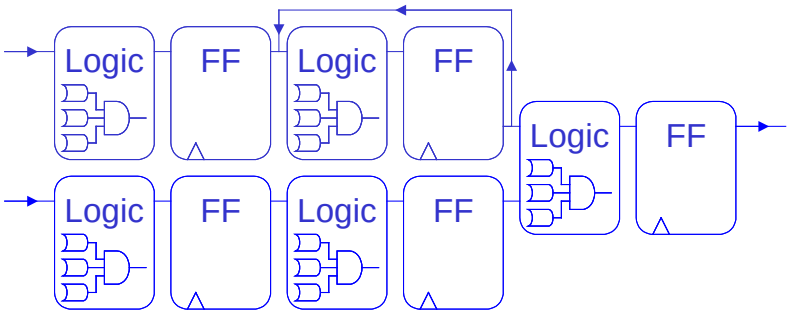


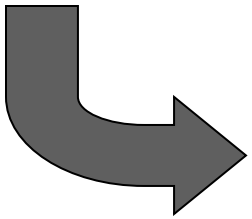
- Non-Persistent Structure – Feed-forward
- Persistent Structures – Contribute to feedback
- Partial TMR – Priority given to persistent structures

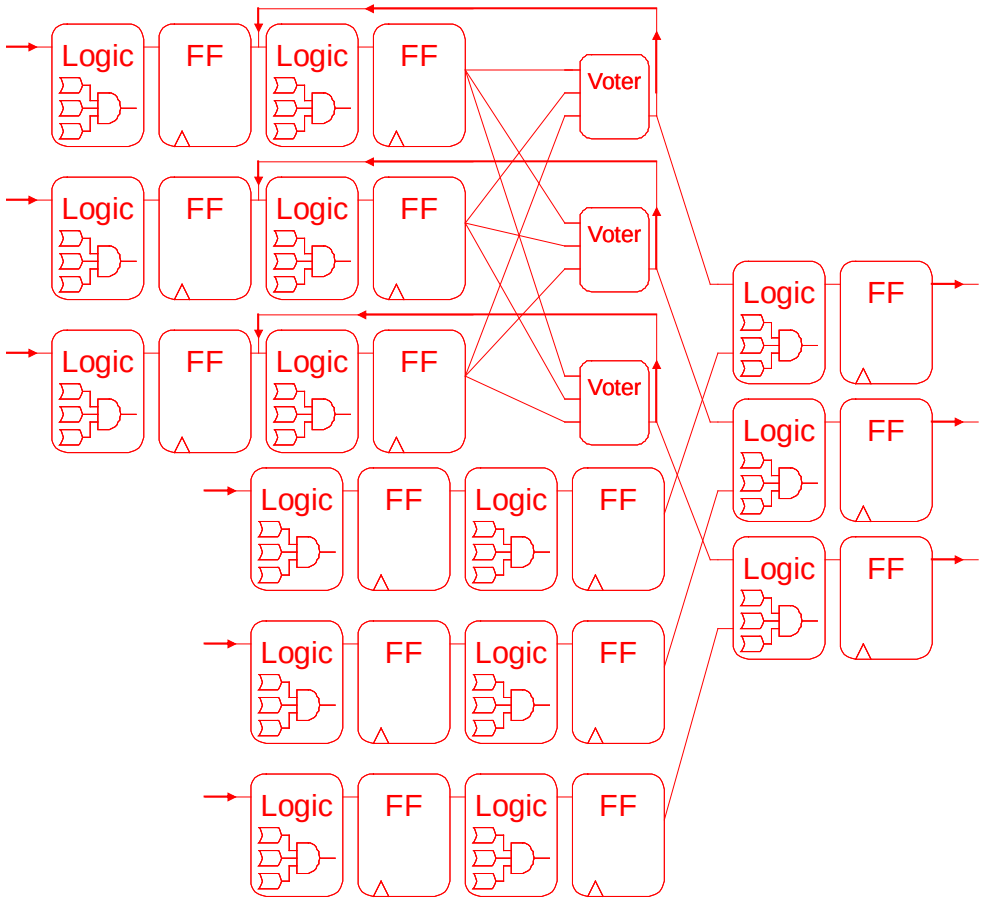
Partial TMR


Logic
FF
Logic
FF
Logic
FF
Logic
FF
Logic
FF
Logic
FF
Logic
FF
Logic
FF
Voter
Voter
Voter
Logic
FF
Logic
FF

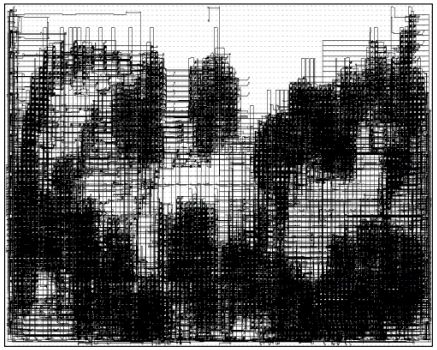
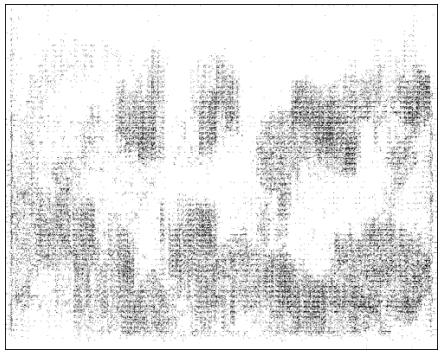
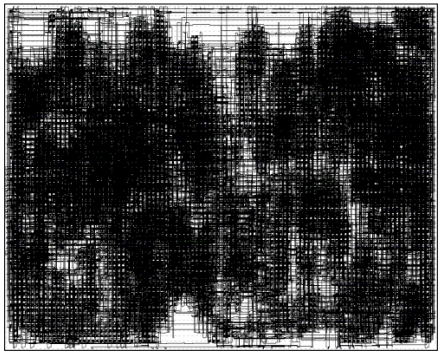
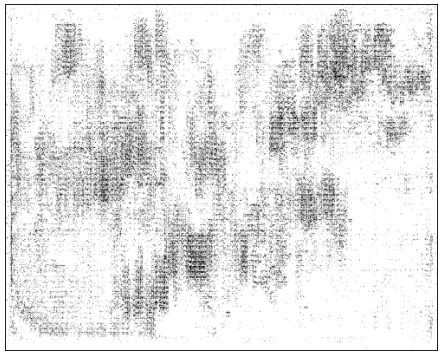
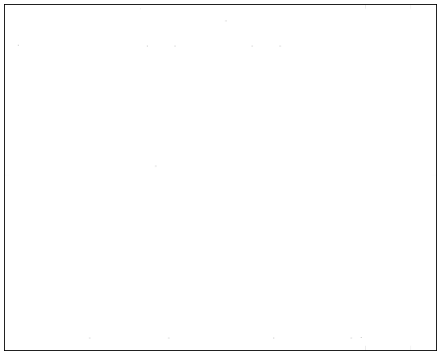
Triple Modular Redundancy



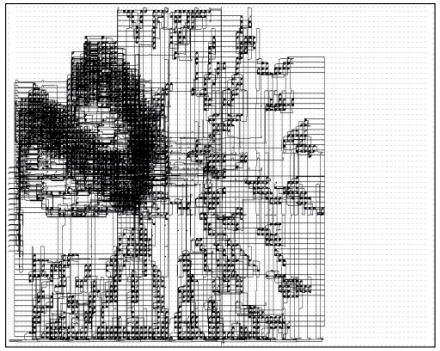
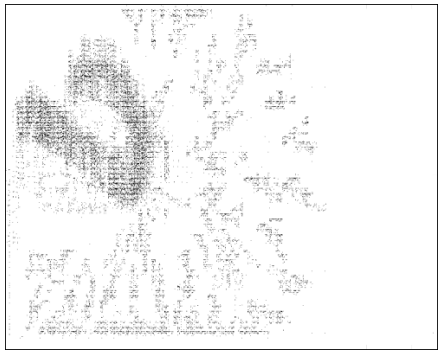
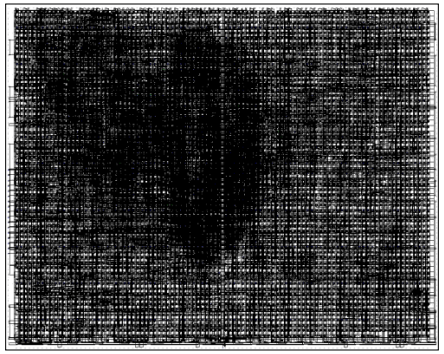
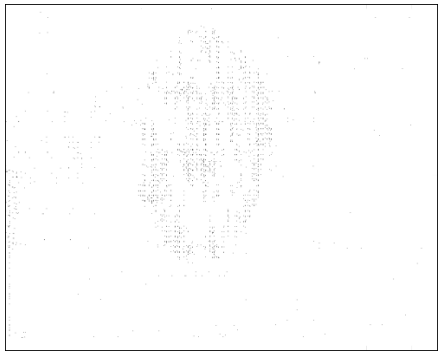
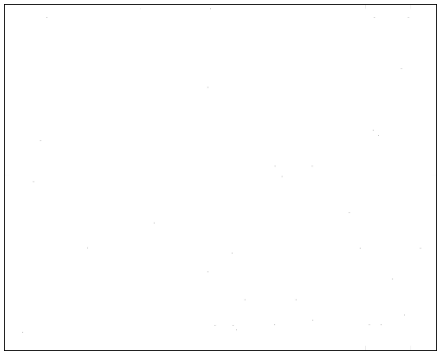




Experimental Results – Design #1
DSP Kernel

	FPGA Editor Layout	Sensitivity Map	Persistence Map
Unmitigated			
	5,746 slices (46%)	575,448 (9.90%)	13,841 (0.24%)
Partial TMR applied to persistent sections			
	8,036 slices (65%)	569,700 (9.81%)	152 (0.0026%)

Experimental Results – Design #2
Synthetic (LFSR/Mult)

	FPGA Editor Layout	Sensitivity Map	Persistence Map
Unmitigated			
	3,005 slices (24%)	254,840 (4.39%)	46,368 (0.80%)
Full TMR Applied			
	12,165 slices (99%)	2,395 (0.041%)	671 (0.005%)

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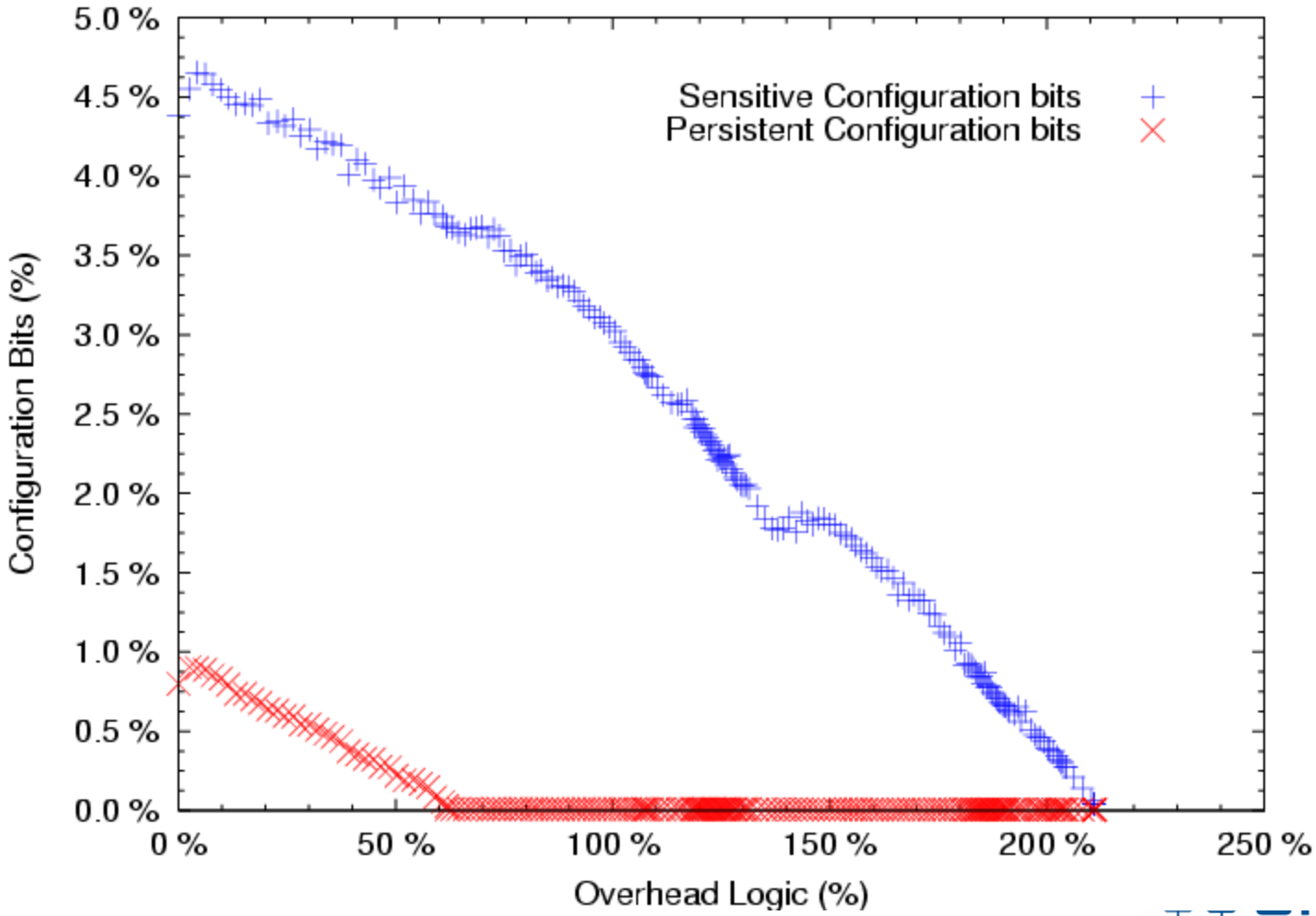
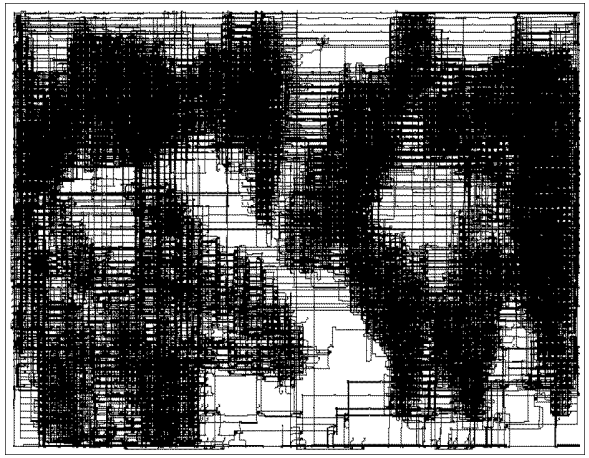
BL-TMR Incremental Results

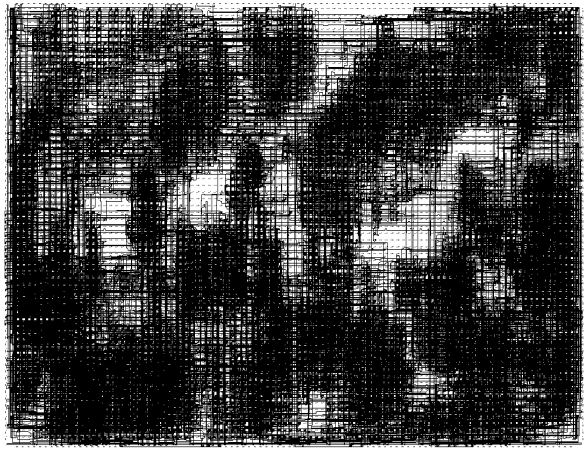


LANL DSP Kernel – Selective Mitigation



Original DSP Kernel

Original DSP Kernel Sensitivity

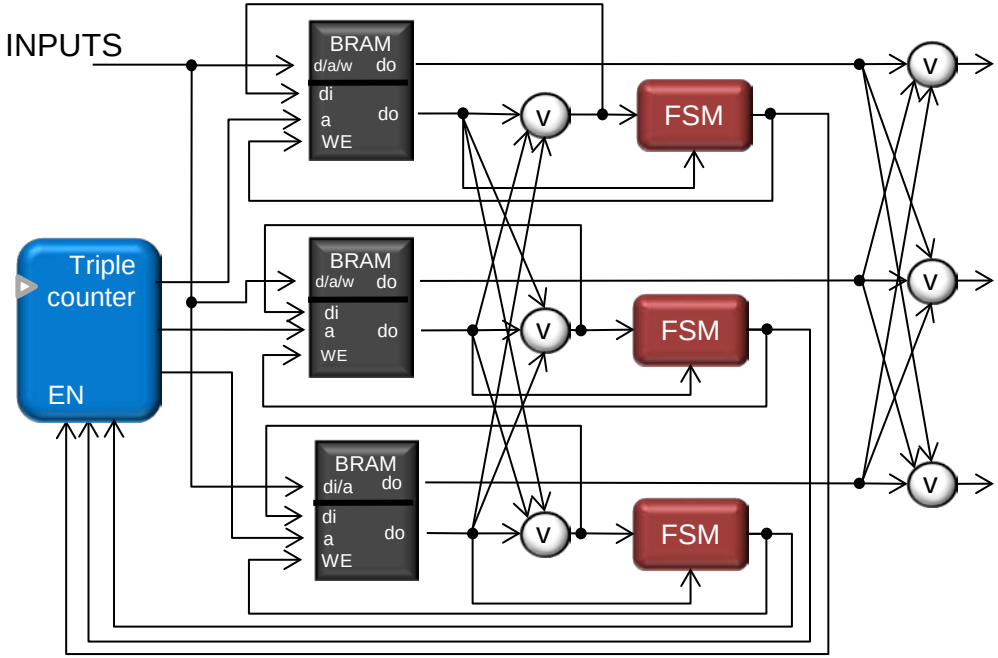


DSP Kernel – Selective Mitigation

Partial Mitigation Sensitivity

BRAM Mitigation: TMR + Scrubbing

- Triplicate Memories:
  - Information redundancy
- Active Memory Scrubbing:
  - Memory repair



SEFI Detection

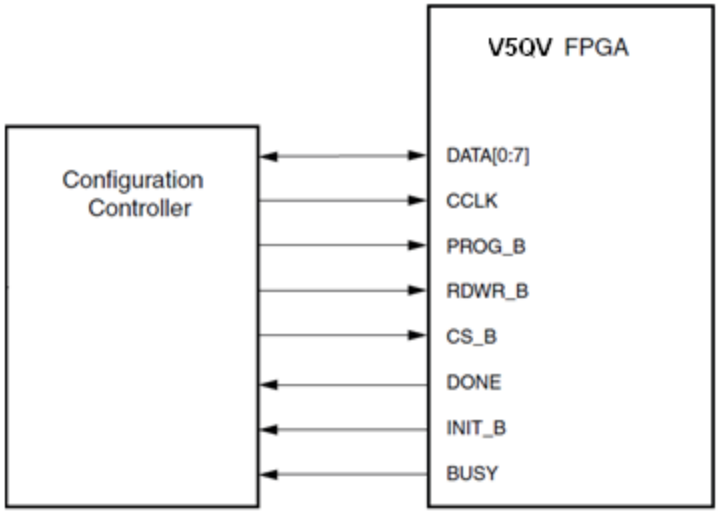
- SEFI Detection must be a part of an FPGA mitigation strategy
  - External configuration controller
  - Well known protocol to detect SEFI

Block diagram illustrating the SelectMAP interface between the Configuration Controller and the DUT V5QV.

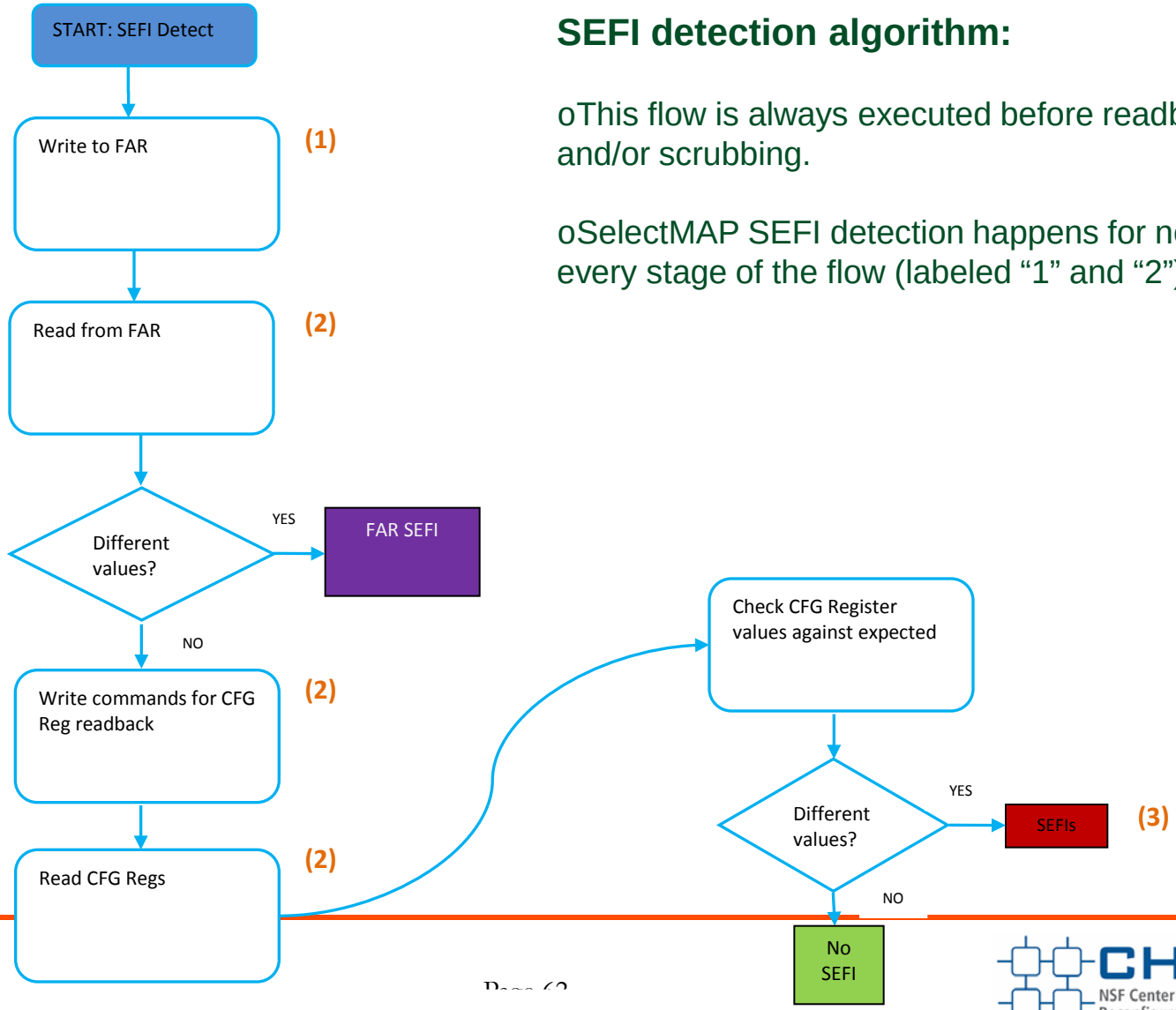
1.Commands are sent from the Configuration Controller to the DUT V5QV FPGA.

2.Readback is performed from the DUT via the SelectMAP interface.

3.DONE and BUSY are also monitored for SEFI detection.



SEFI Detection, Cont'd

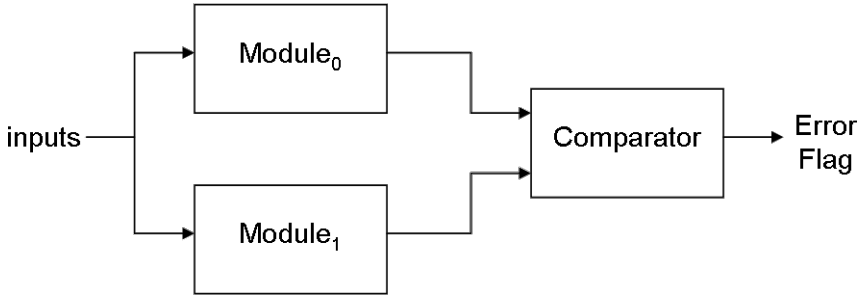


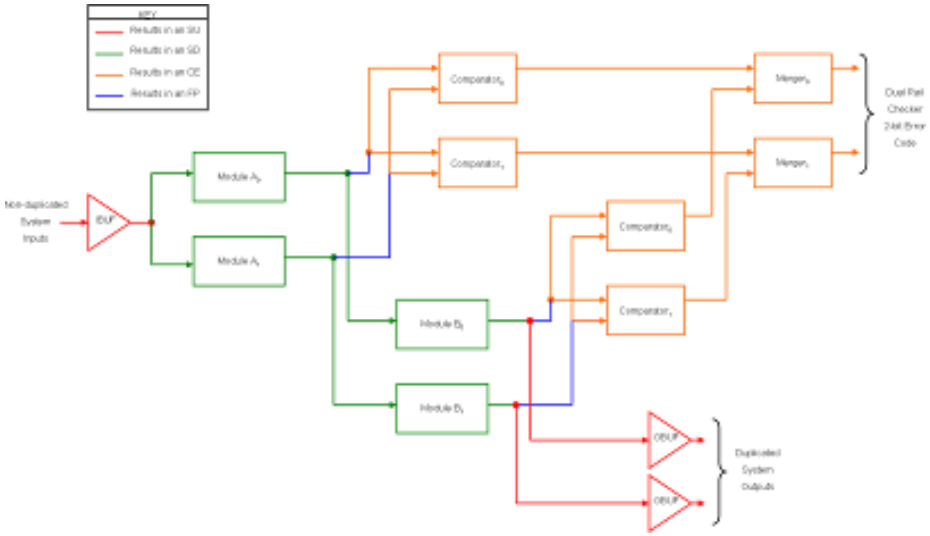
SEFI detection algorithm:

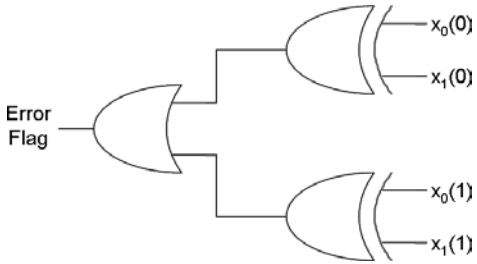
oThis flow is always executed before readback and/or scrubbing.

oSelectMAP SEFI detection happens for nearly every stage of the flow (labeled "1" and "2").

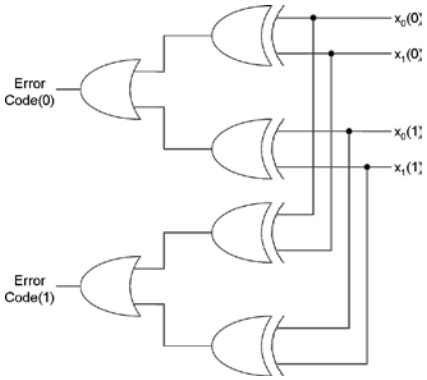
Duplication with Compare (DWC)







Single Bit Comparator



Dual Rail Comparator

Coverage and Size of DWC

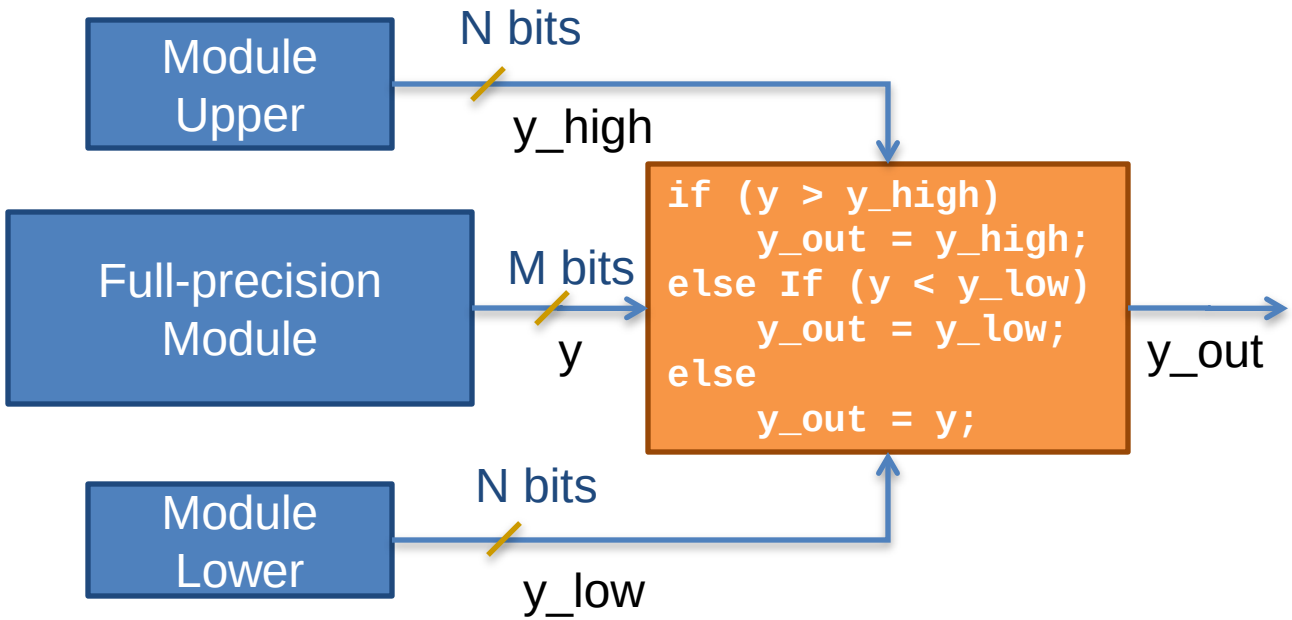
Design	Coverage (%)
Counters200	99.75%
Synthetic	99.73%
QPSK Demodulator	99.32%
Triple DES	99.77%

Design	Implementation	Slices	% Increase
Counters200	BLDwc	2,171	102%
	original	1,076	0%
Synthetic	BLDwc	9,343	210%
	original	3,012	0%
QPSK Demodulator	BLDwc	2,248	114%
	original	1,049	0%
Triple DES	BLDwc	12,286	128%
	original	5,387	0%

Average Coverage of all Designs = 99.64%

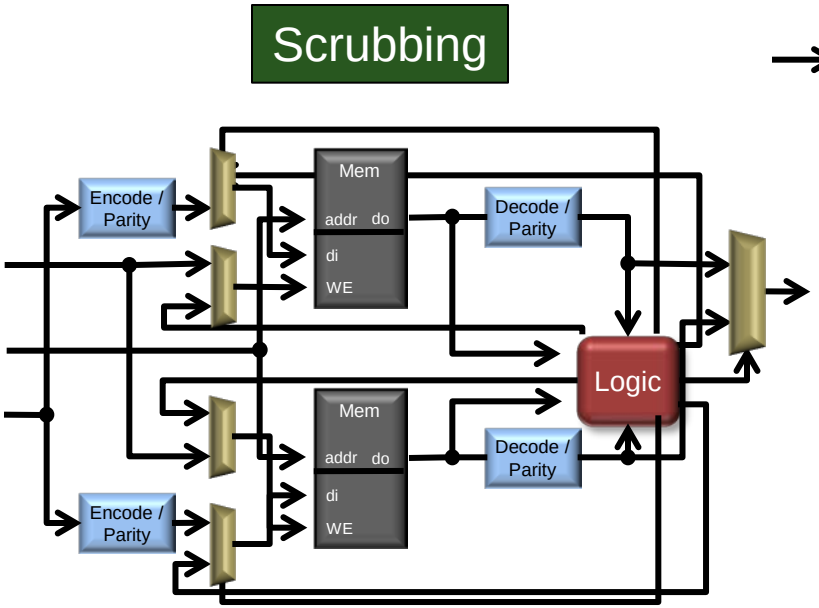
Reduced-Precision Redundancy (RPR)

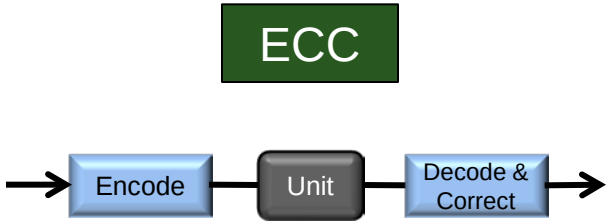
- Reduced-cost alternative to TMR
- Concentrates mitigation on upper bits of computation

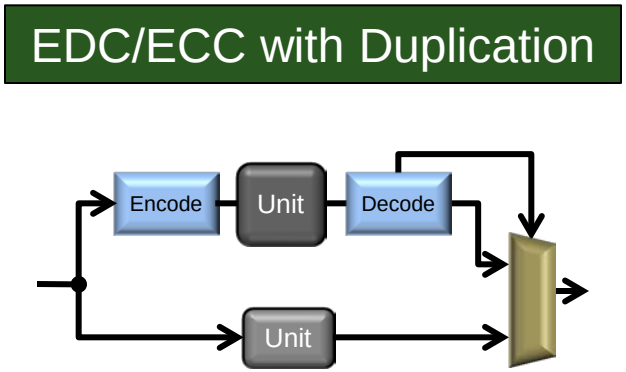


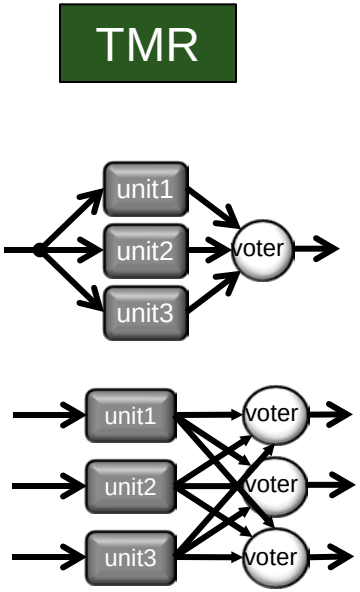
Memory Techniques

- Test FPGA logic and ASIC memory fault-tolerant techniques
  - Add scrubbing to each technique – to eliminate critical failures
  - Compare techniques with unprotected memory and against each other
  - Apply to BRAM, LUTRAM, SRL



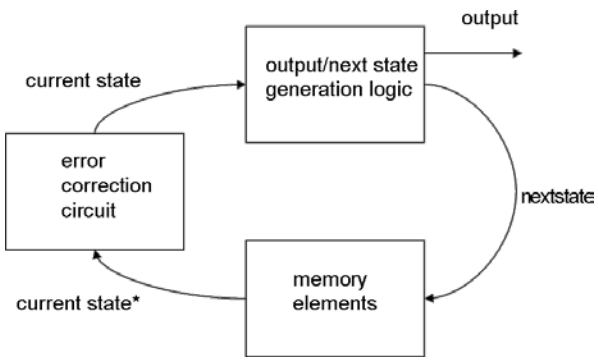




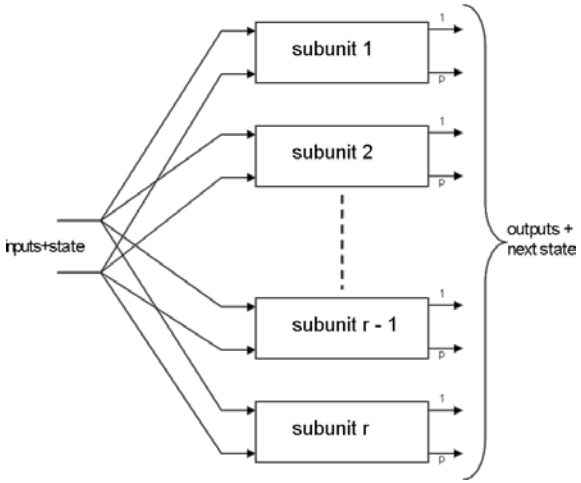


State Machine Encoding

- Apply conventional signal encoding techniques on state variables
  - Explicit error correction
  - Implicit error correction
  - Armstrong's method



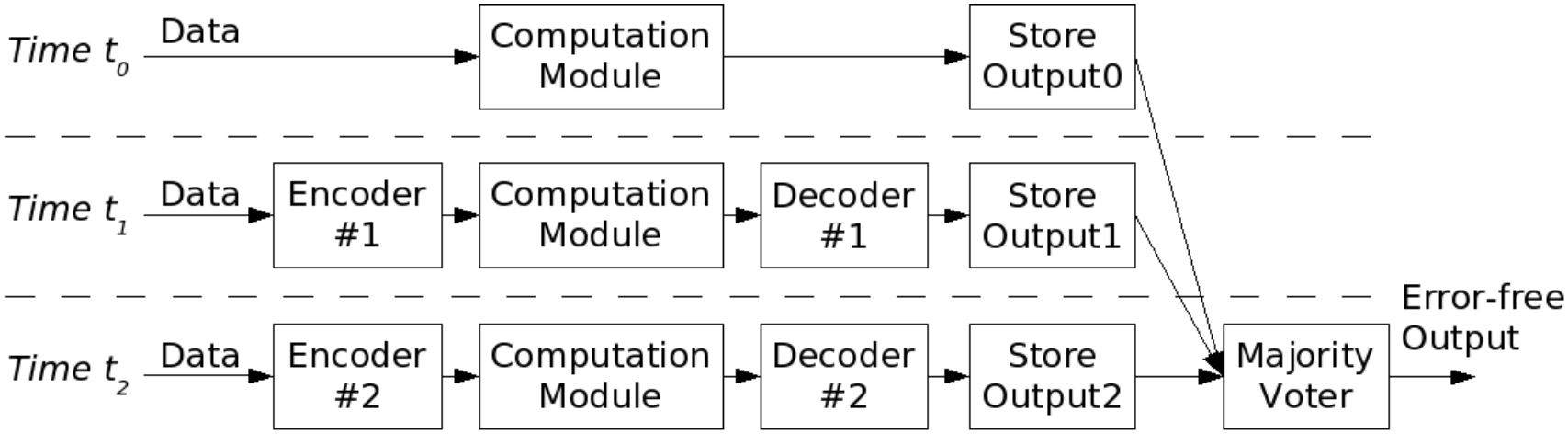
Explicit Error Correction



Armstrong's Method

Temporal Redundancy

- Perform three computations sequentially in time
- Use encoder/decoder to insure detection of all permanent errors
  - Difficult to design for non-trivial modules
- Low area overhead since modules are reused
- High Latency cost (3x or more)



Other Design Mitigation Techniques

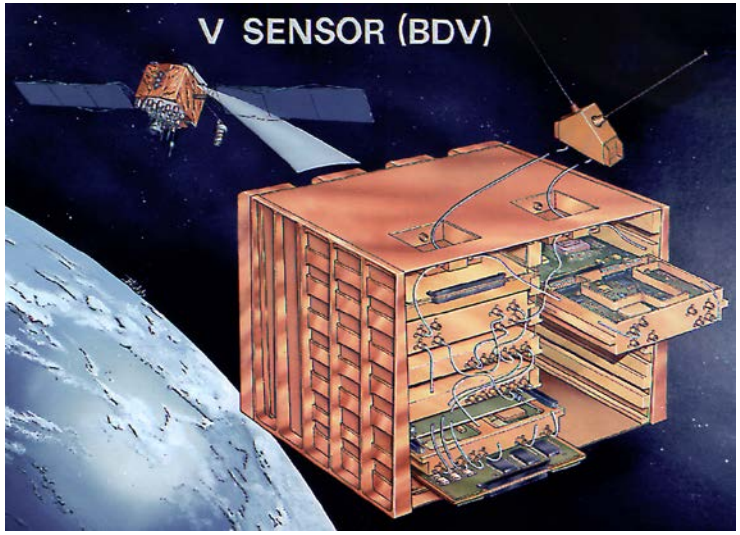
- Non-redundant fault avoidance
- Alternative logic systems
  - Dual rail
  - Arithmetic encoding
  - Logic error correction codes
- Distributed checking
  - Totally self checking
  - Partially self-checking
- Masking logic
- Boolean difference fault masking
- Duplication with parity (hot swap)
- Dynamic redundancy

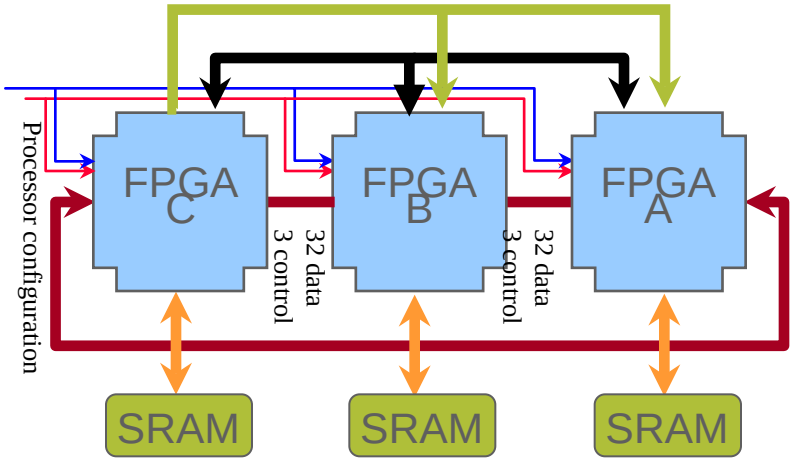
Presentation Outline

1) NSF CHREC Center
2) FPGAs in Space: Motivation and Examples
3) FPGA Single Event Effects and SEU Sensitivity
4) Emulating Single Event Upsets - Fault Injection
5) Single Event Mitigation Techniques
6) Case Study: LANL Cibola Flight Experiment
7) Summary

Los Alamos Cibola Flight Experiment

- Reconfigurable RF Payload (Wide-band RF processing)
- Uses 9 Virtex V1000 FPGAs
  - Over 9 million logic gates
  - 150 KByte internal memory
- 1000 km orbit
- Target 2.4 Gbit/sec continuous processing
  - 2 12-bit 100 MHz ADCs
- Launch: March 7, 2007

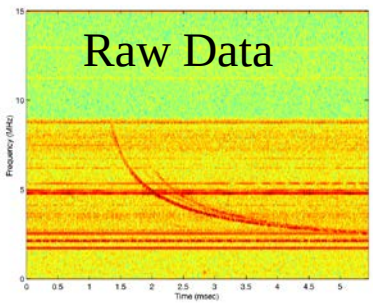


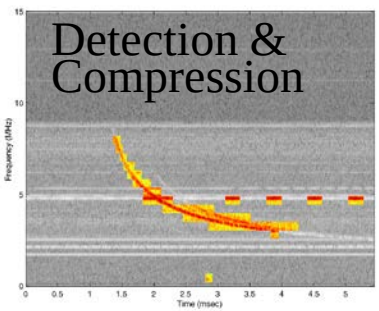


Michael Caffrey, "*A Space-Based Reconfigurable Radio*", Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), pp. 49-53, June 2002.

CFE Objectives

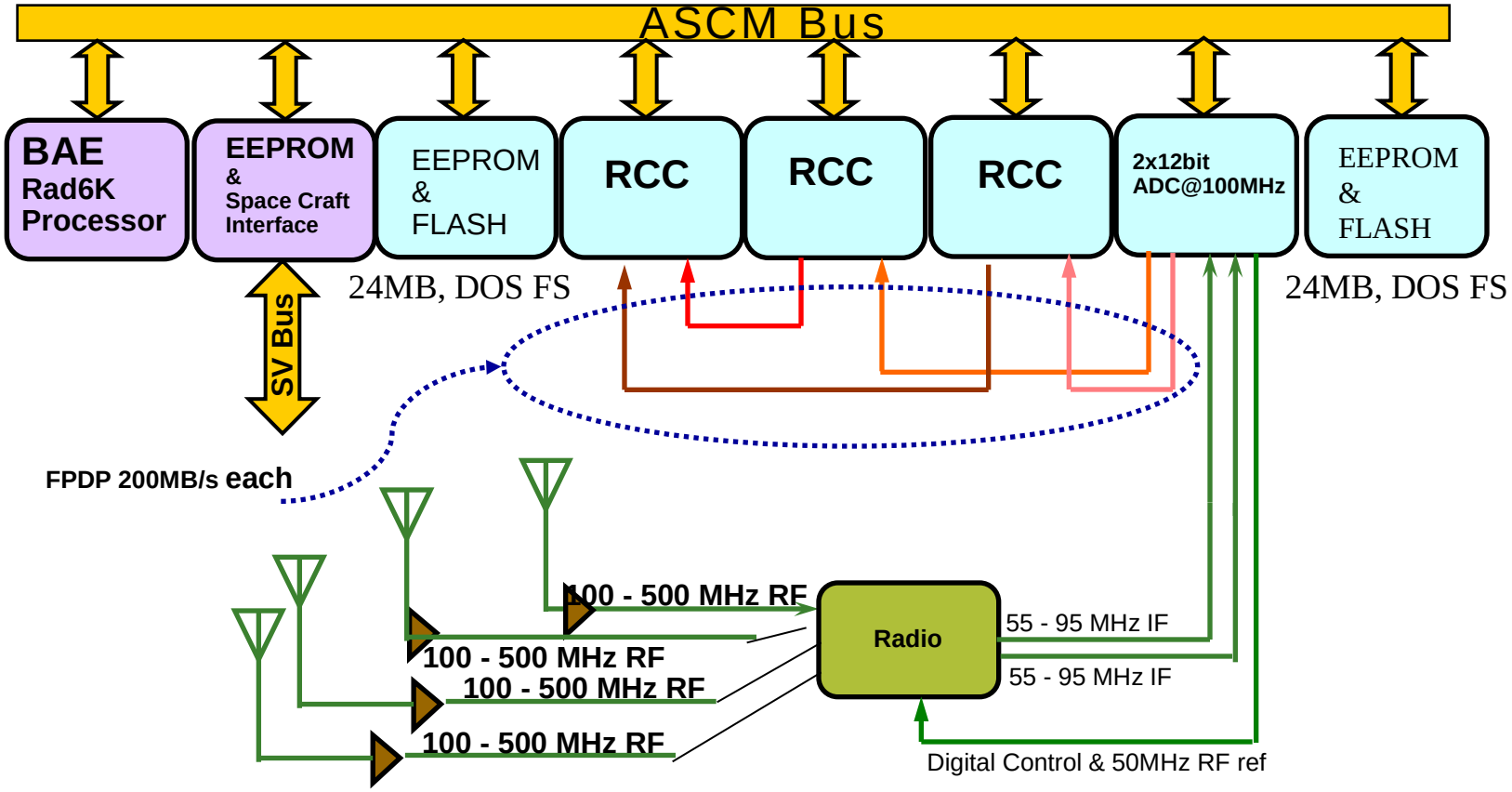
- Demonstrate use of SRAM FPGAs for real-time sensor processing
  - Provide greater computational performance than RAD-Hard alternatives
  - Reduce design time
  - Provide on-board hardware programmability
  - Demonstrate reduced cost using COTS
- Challenges
  - Single-Event Upset (SEU) mitigation
  - Power density, thermal management, and packaging
  - Matching application needs to architecture





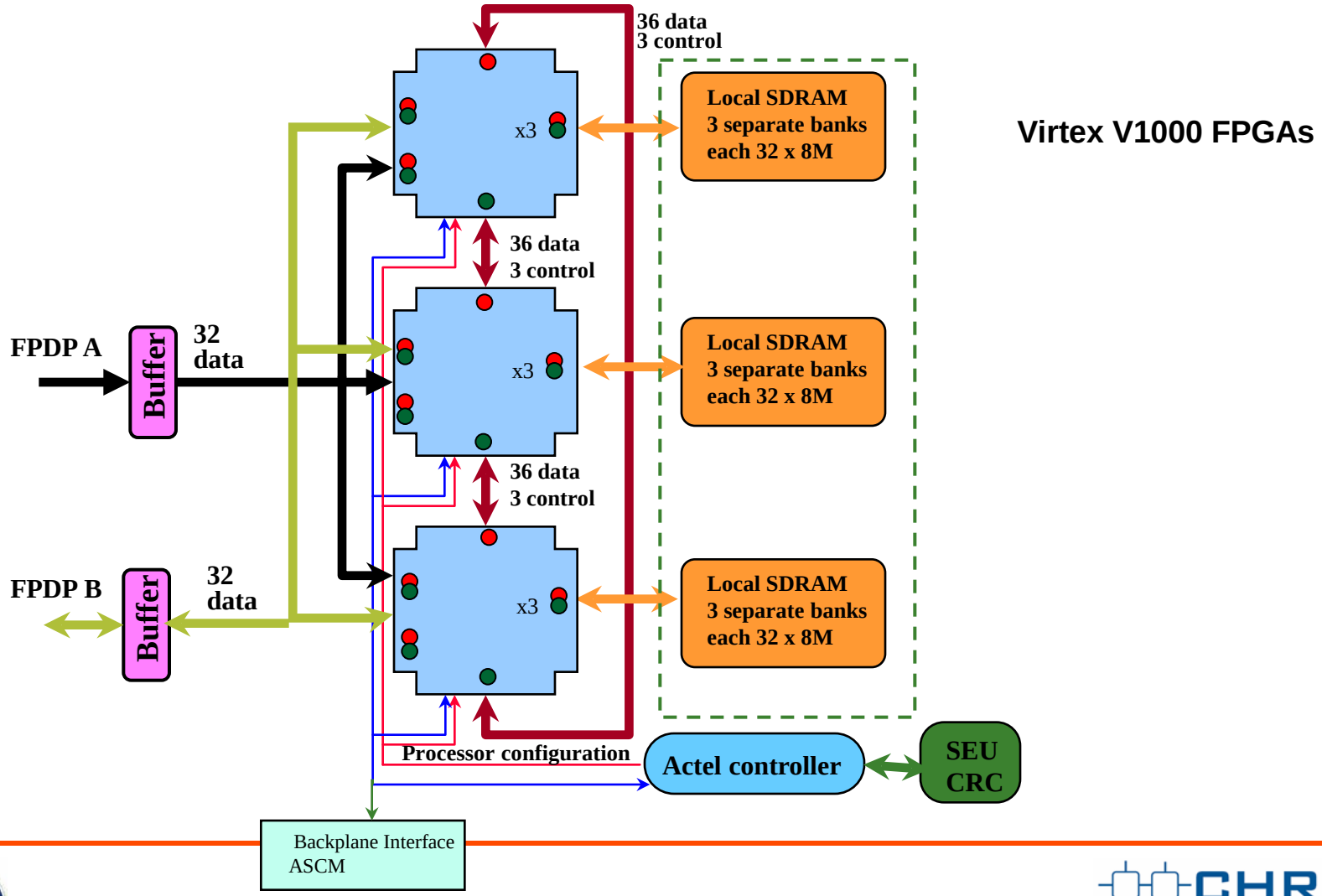
Continuous, full bandwidth real-time signal processing

CFE Payload Block Diagram

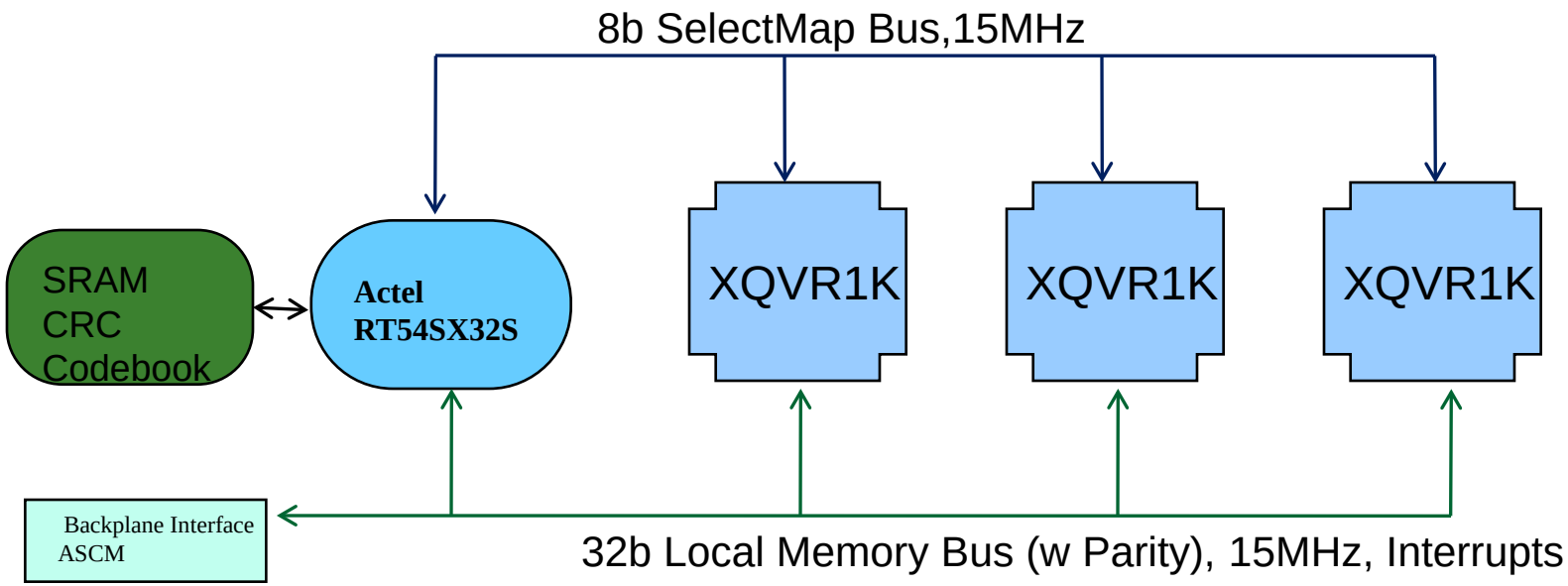


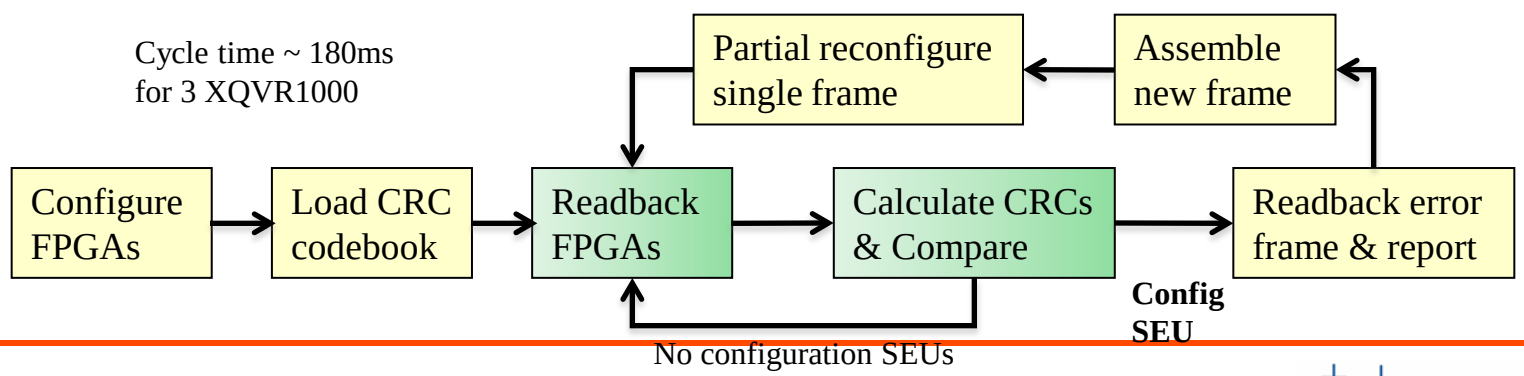
four 20MHz wide radio channels, gang tuned
2 channels combined into each 50MHz RCC input

RCC Payload Block Diagram



SEU Detection and Mitigation via Scrubbing





CFE Launch, March 8, 2007

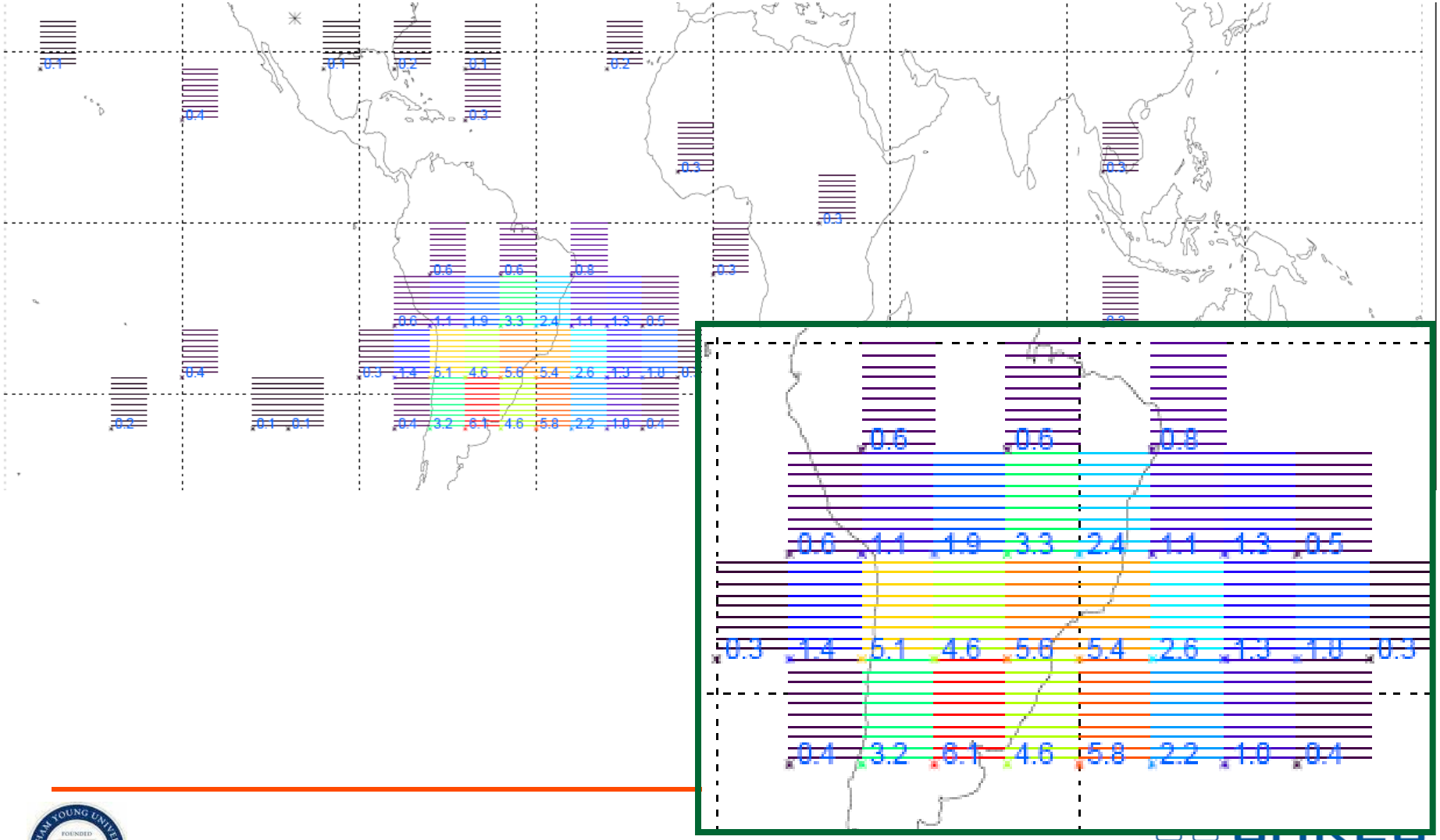
CFE Mated to Launch Adapter

Lockheed Atlas-5 (STP1)

Orbit: 560 km, 35.4 inclination

Location of CFE can be found at: http://www.n2yo.com/?s=30777

SEU Events



NSF Center for High-Performance Reconfigurable Computing

SEU Results

	Device Days	Config. SEUs	SEUs/ Device Day	BRAM Upsets	BRAM Upsets/ DD	SDRAM Upsets	SDRAM Upsets/ DD
SEU1	455.3	216	.47	N/A	N/A	N/A	N/A
SEU2	97.2	46	.47	N/A	N/A	N/A	N/A
SEU3	1101.2	305	.28	32	.029	N/A	N/A
SEU4	1162.8	326	.28	19	.016	N/A	N/A
SEU5	100.3	46	.46	0	.000	223	.74
SEU6	201.6	80	.40	6	.030	456	.75

Measured: 1019 SEUs / 3118 device days = .33 upsets/device day

Operating in orbit as expected

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Summary

- Great interest in using SRAM FPGAs in space
  - In “field” reconfigurability
  - High density and computational resources
- Radiation effects on FPGAs are well known
  - Large amount of radiation test data on several FPGA families
  - Susceptible to single event effects
  - Effects of SEU well understood (fault injection)
- Proven SEU mitigation techniques
  - Configuration Scrubbing
  - TMR
  - Memory error protection/detection
- FPGAs have been successfully used in space