SiGe BiCMOS 16-channel 12-bit Wilkinson ADC

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Outline

- Wilkinson ADC architecture
- Design Blocks
  - Auto-zero Comparator
  - Ramp Generator
  - Gray Code Counter
  - Radiation Aware Power Management System (RAPM)
- Test Setup and Results
  - Test Board
  - Measurement Results
- Conclusion

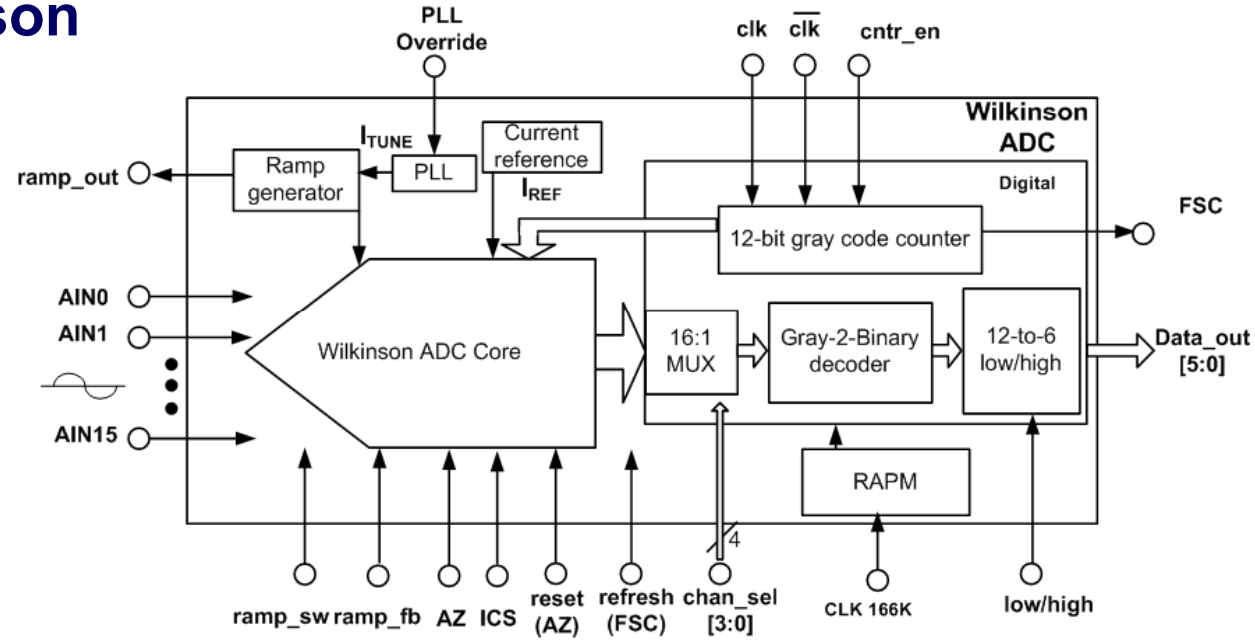
Wilkinson ADC Specifications

Specifications of ADC

- 20-KSps sampling rate
- 12-bit accuracy
- Input range of 0 to 1.2 V
- Operation over a wide temperature range of −180°C to 125°C
- Required to operate in a lunar surface environment.
- Clock frequency of 85 MHz to operate Gray code counter
- Shared ramp generator and counter lower power consumption
- 16 input channels supported (parallel operation w/ simultaneous sampling)

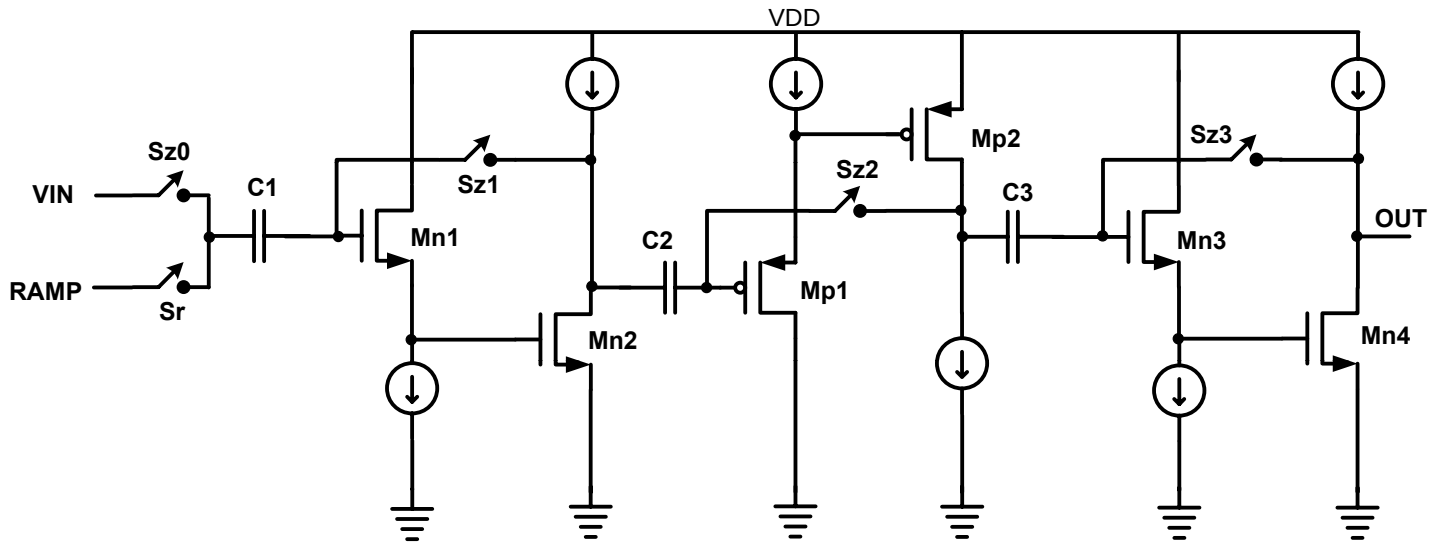
Wilkinson ADC Architecture & Operation

- **Design blocks of Wilkinson ADC**
  - Ramp generator
  - AZ comparators (16)
  - Counter
  - Current Reference
  - 2.5-V regulator (RAPM)
  - Digital Section



- **ADC operation:**
  - Phase 1:
    - Comparators sample the input and ramp generator resets.
  - Phase 2:
    - Ramp changes from 0 to 1.2 V.
    - Counter counts from 0 to 4096 (e.g., 12 bit).
    - Channel comparator changes state, storing value of count.

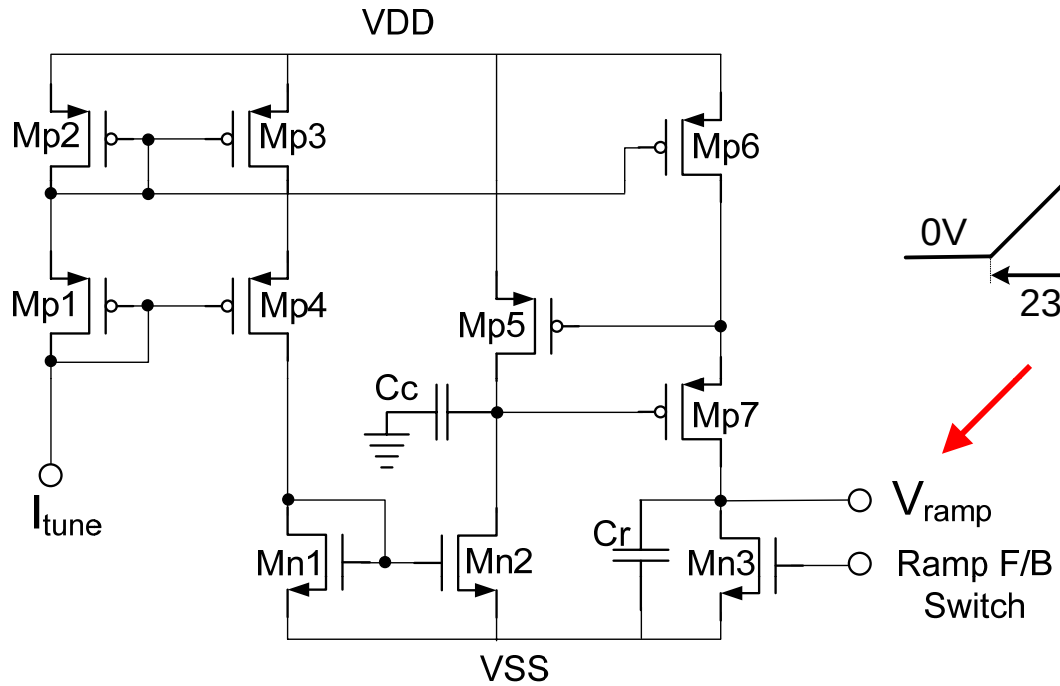
Low-Power Auto-Zeroed Comparator

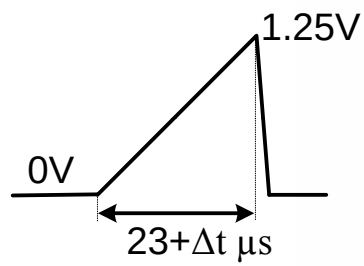


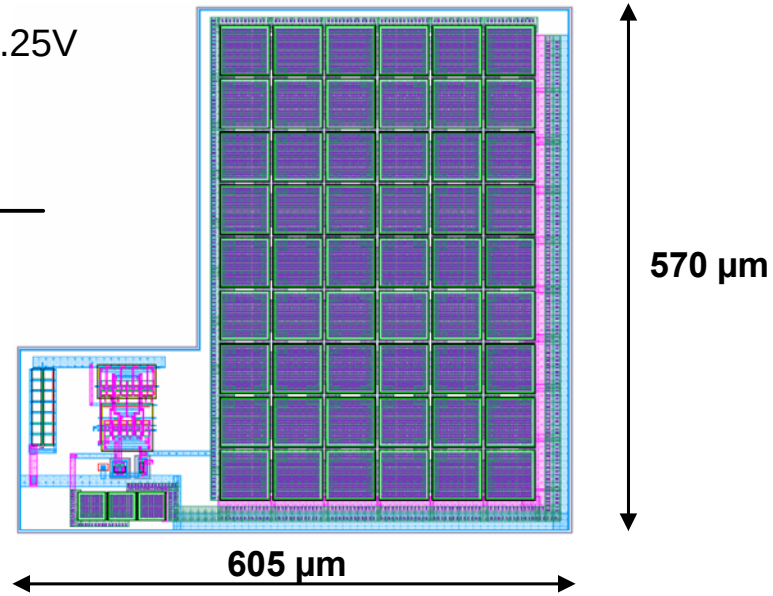
- Sample-and-hold function achieved by the auto-zeroed comparator.
- Switches Sz1, Sz2, Sz3 are used for auto-zeroing. Sz0 samples the input.
- Switch Sr closed during conversion phase.
- Debounce circuit at the output of the comparator improves noise rejection

	Achieved Specs. (–180ºC to 120ºC)
Error voltage over input range	< 150 µV
Average power	≈ 95 µW

Ramp Generator

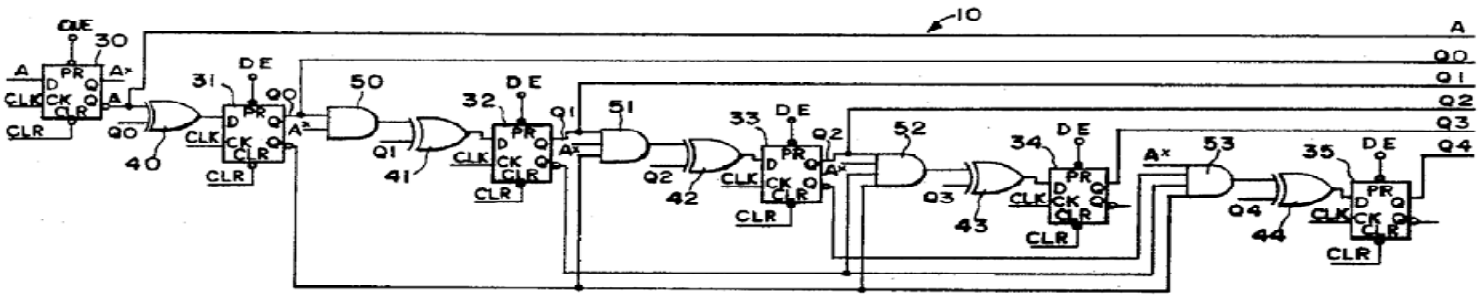






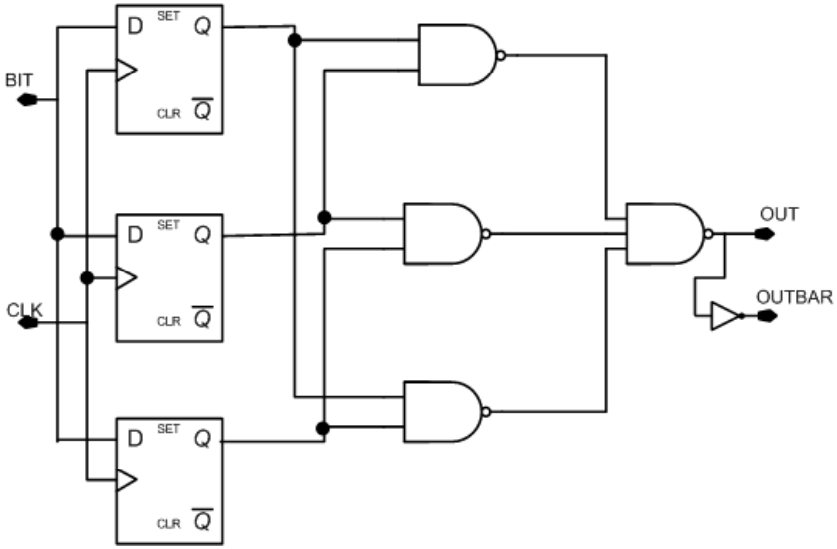
- I_{tune} can adjust the ramp slope, compensates slope change over temperature
- Extracted simulation results over temperature (–180°C to 125°C)
  - Average Power: 125 µW
  - Linearity: 12 bits, maximum error w.r.t. best fit line 75 µV

ADC Counter Voting Logic



A 5-bit Gray code counter[1]

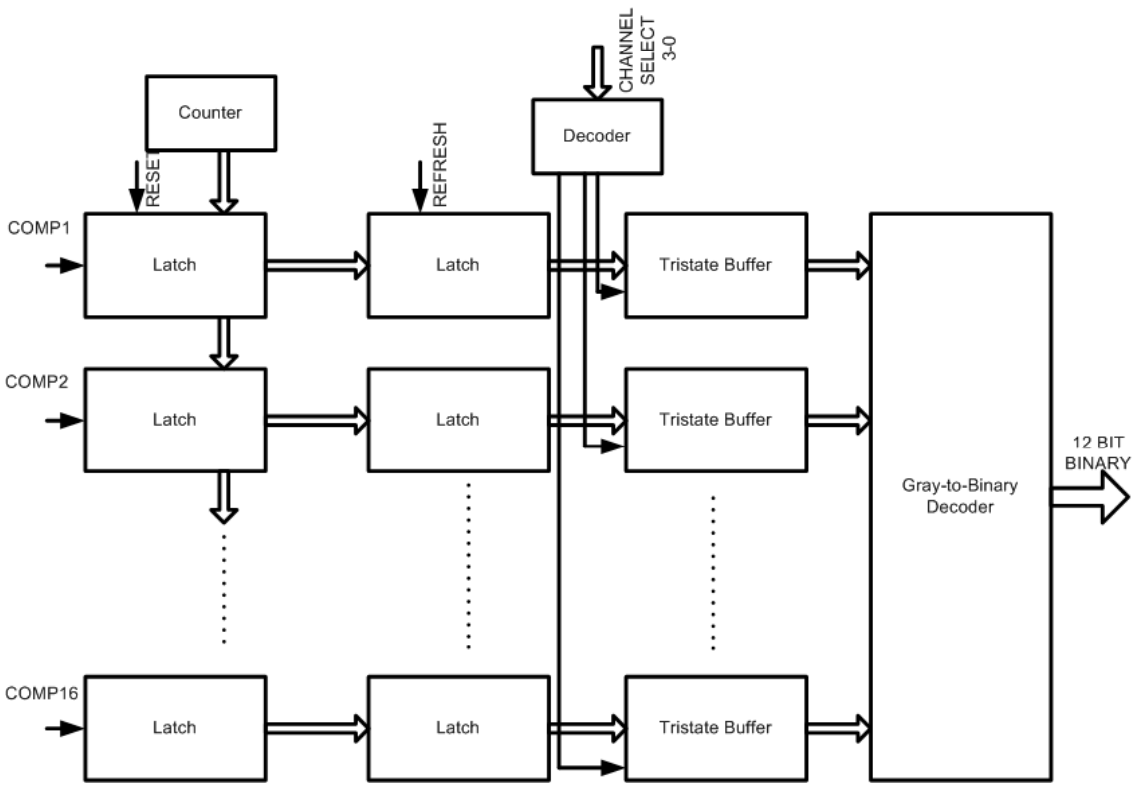
[1]K.J. Otto, "Nine Bit Gray Code Generator," US Patent 5,164,968, Nov 1992



Voting logic bit-slice for the ADC's Gray code counter

- **Counter required to operate at 85 MHz with low power consumption.**
- **Voting Logic implemented to mitigate potential SEU.**
- **Majority vote is taken of 3 FFs for each output bit of Gray code counter**
- **This logic is implemented at output of each counter bit.**

Digital Section

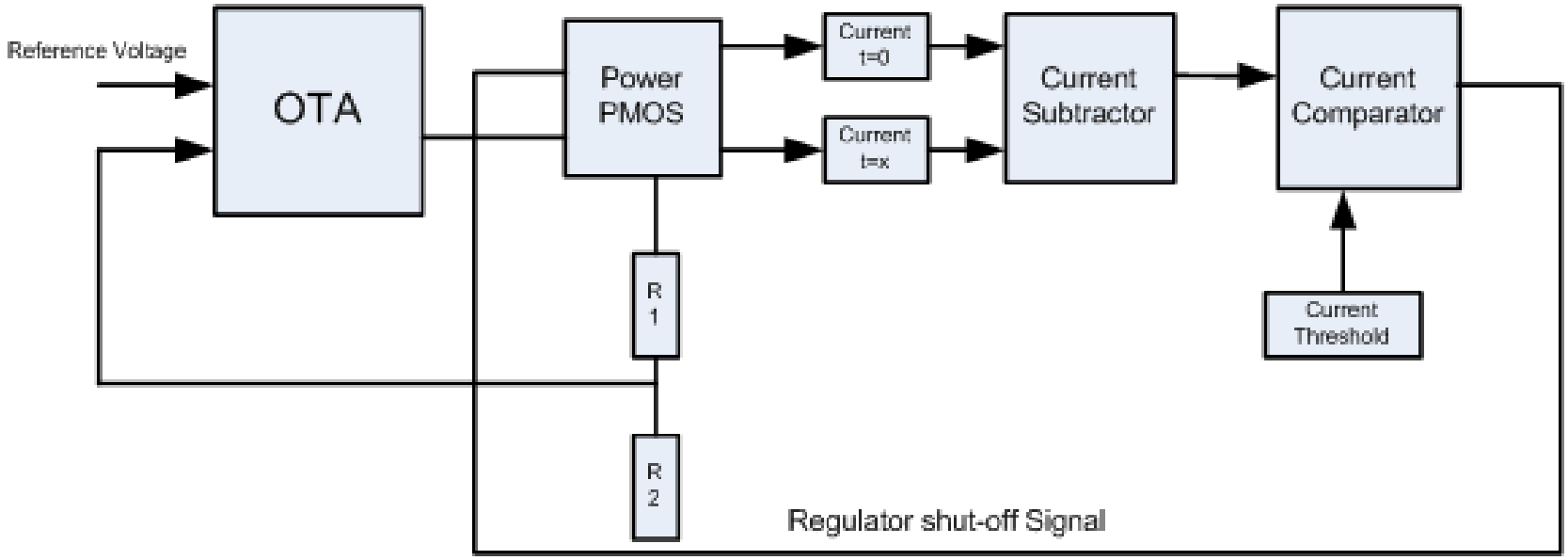


- **Digital Section**
  - Counter
  - 2-sets of latches
  - Tristate buffers
  - Decoder
  - Gray-to-binary decoder
- **Comparator latches counter data into latches.**
- **REFRESH signal transfers data from latch-1 to latch-2.**
- **Channel Select signals decide which channel data is read out.**
- **Gray-to-binary converter converts data to binary**
- **Using minimum *L* transistors for compact layout.**

Radiation Aware Power Management System (RAPM)

- **Background and motivation:**
  - Short *L* design required in digital section of ADC for low-power/high-speed/compact area tradeoff optimization
  - 2.5-V supply selected for digital to maintain long-term reliability at cold temperature (lower voltage to mitigate hot carrier effects)
- **The RAPM system:**
  - Provides 2.5-V power needed for digital section of the ADC
  - In the event of radiation induced single-event latchup (SEL), this power management scheme will automatically collapse the supply rail voltage to the digital section of the ADC to mitigate SEL, and then restore digital power to 2.5 V.
- **Other RAPM features:**
  - Designed to withstand high frequency current transients associated with digital (e.g. the Gray code counter)
  - Multiphase clock generator designed to generate the required clock signals

RAPM Schematic

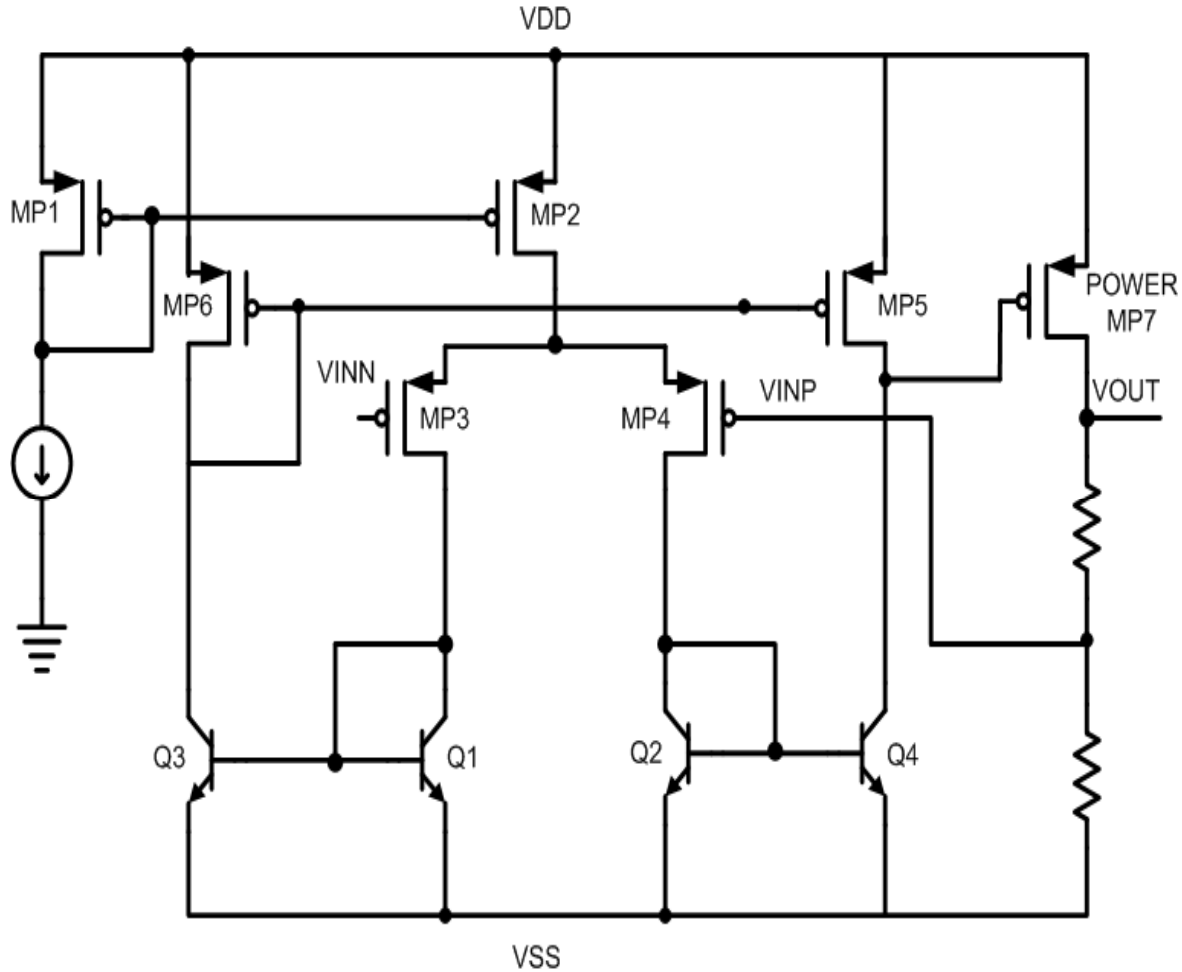


❑ Operation:

- Sample currents at time $t = 0$ and $t = x$. Sampled currents are scaled down from the actual currents.
- Subtract current $I_{t=x} - I_{t=0}$
- Compare the change in current with a constant current
- If change greater than constant current, comparator shuts down voltage regulator output to 0 V, then system brings it back to 2.5 V on the next sampling cycle.

RAPM Voltage Regulator Amplifier

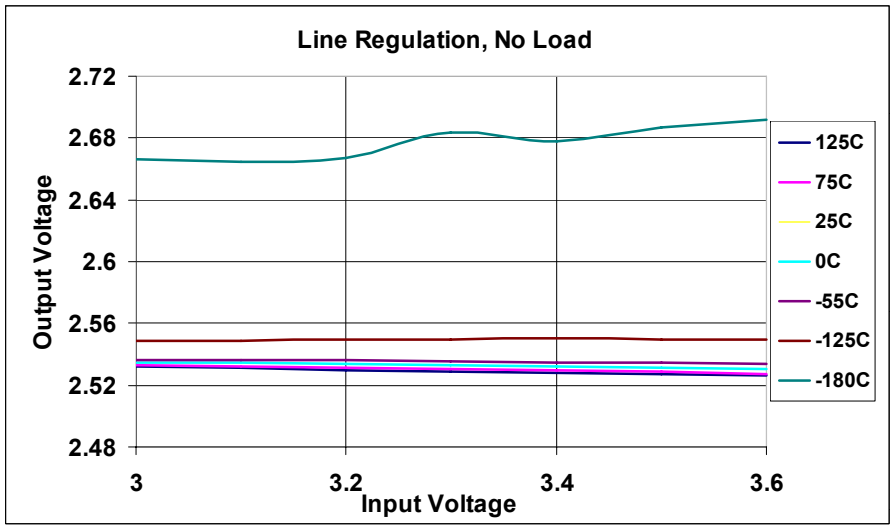
- RAPM voltage regulator uses a BiCMOS operational transconductance amplifier (OTA)
- BiCMOS OTA circuit topology

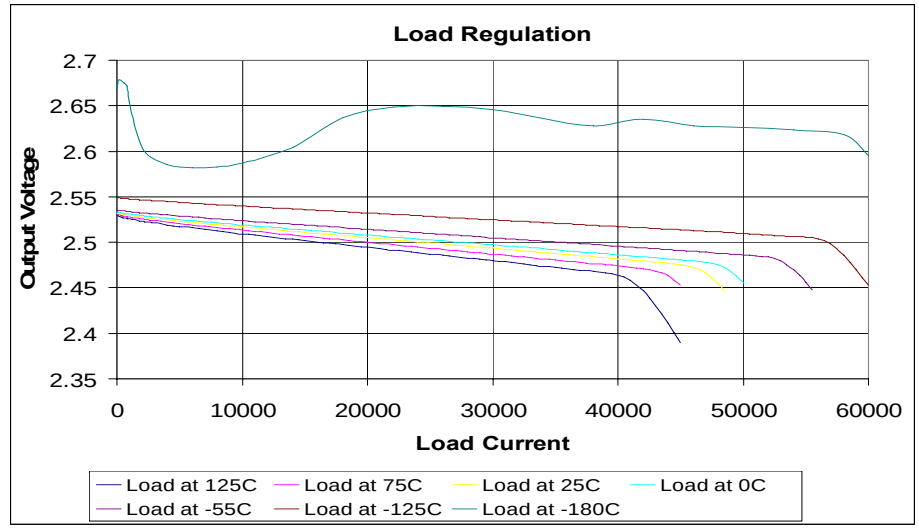


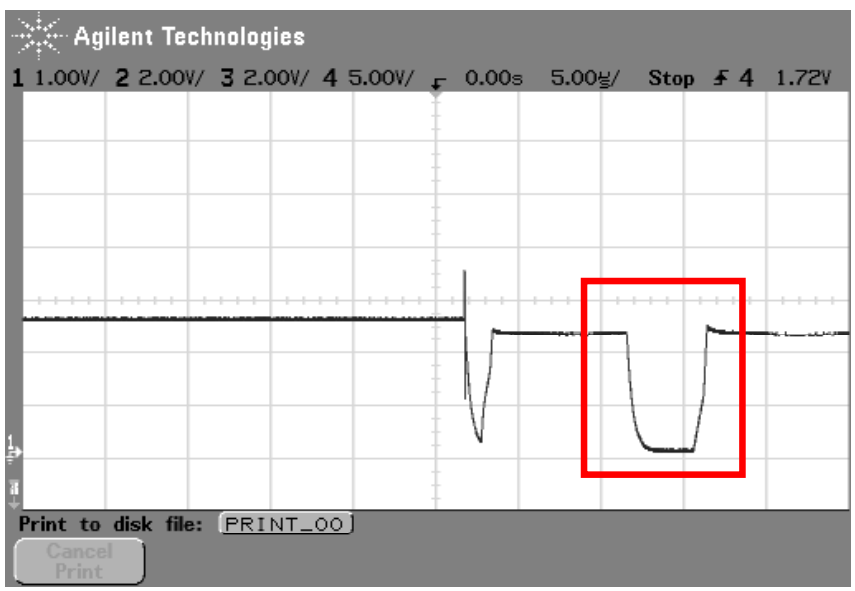
Amplifier topology reference: R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full On Chip CMOS Low Dropout Voltage Regulator," *IEEE Transactions on Circuits and Systems-I*, vol. 54, no. 9, Sept. 2007.

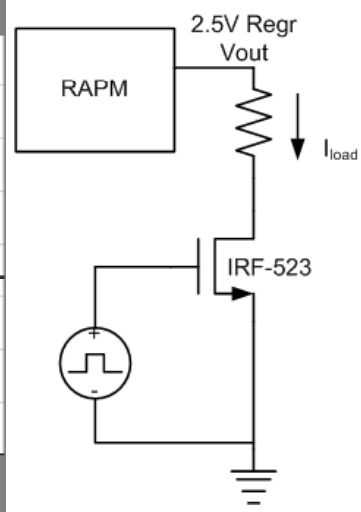
RAPM Test Results

❑ Line and Load Regulation characteristics:





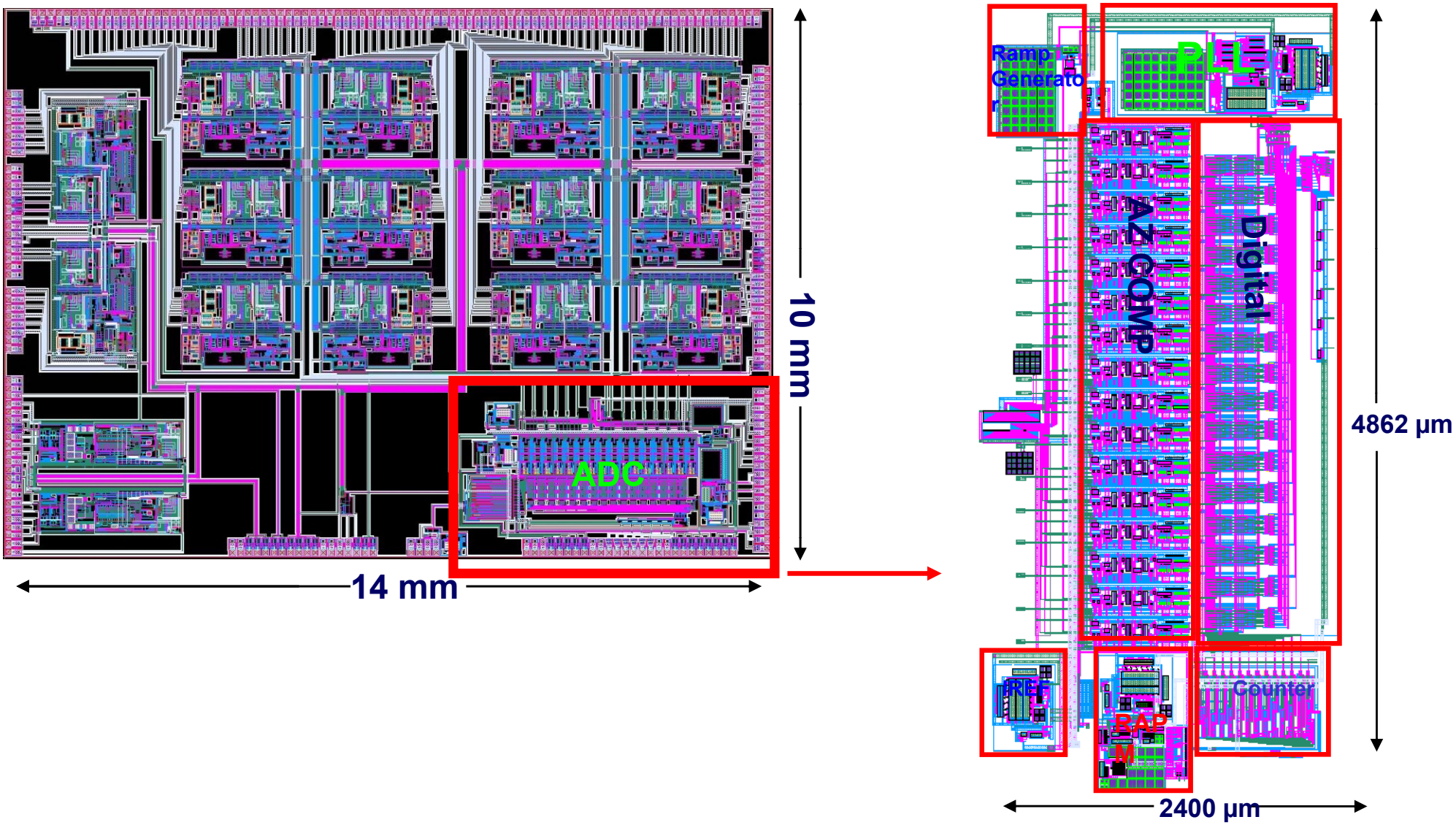




❑ Bench-level simulation of single-event latchup (SEL):

- Current pulses are simulated as a load to the 2.5-V regulator.
- Implemented using a discrete power NMOS switch with pulsed gate
- Output of the regulator shuts down and is pulled back up, automatically based on temporal comparison of current drawn from the RAPM regulator's output

Final Chip Layout

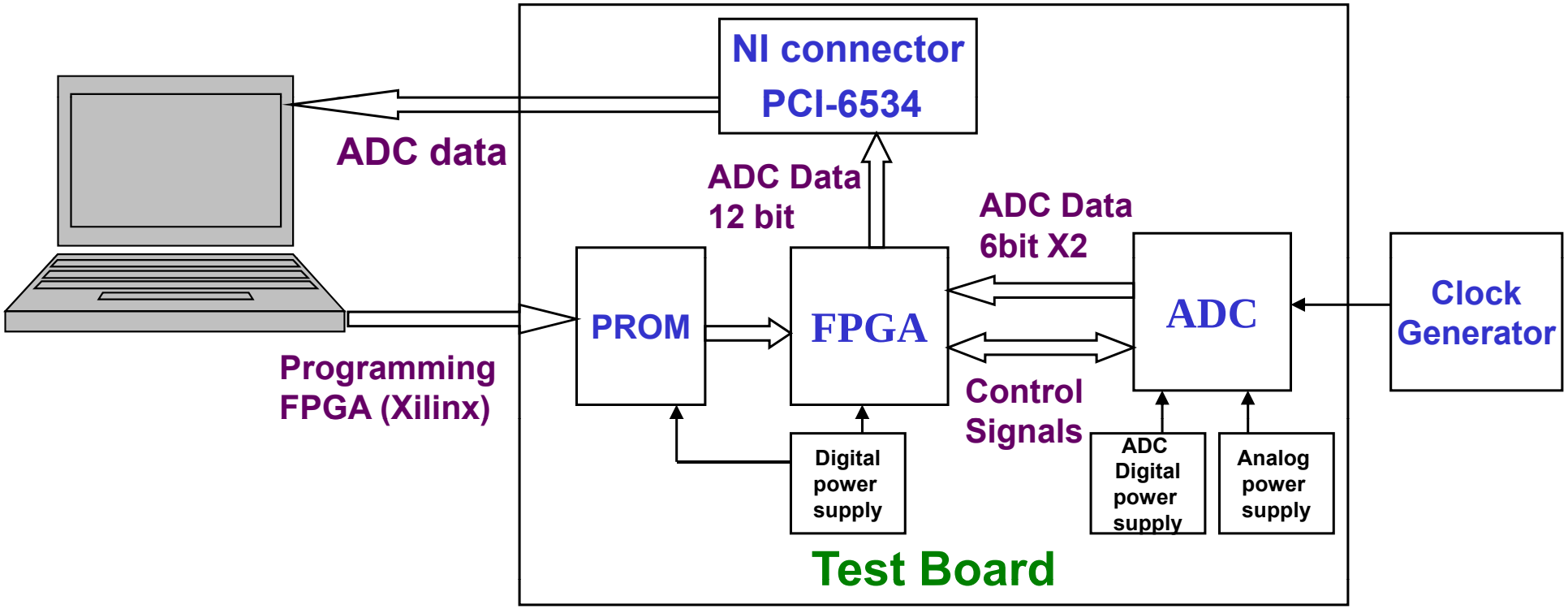


Power Consumption

Circuit Block	Power Consumption
Auto-zeroed Comparators	16 x 100 μW = 1.6 mW
Ramp Generator	130 μW
Counter	1.5 mW
RAPM	900 μW
Miscellaneous	≈ 3.6 mW
Simulated Average Power	**7.73 mW**

- Simulation of the complete ADC to measure power accurately requires a large amount of memory and CPU time, hence individual blocks were simulated separately to estimate the power consumption.

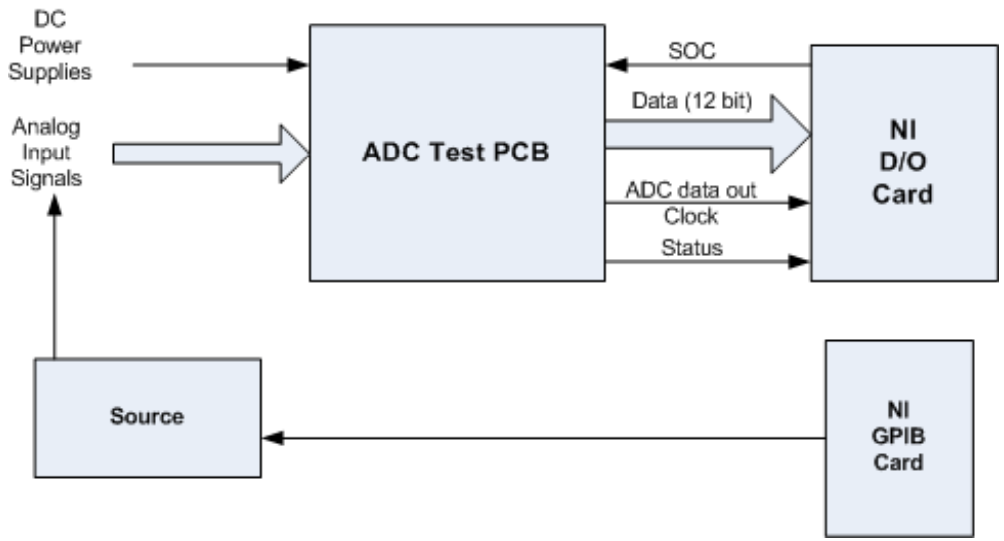
Test setup for the Wilkinson ADC



Testing Objectives:

- Perform Detailed ADC Characterization Over Temperature
- Enable Rapid Data Collection and Signal Processing
- Direct ADC Design Improvements for Future Integrated Systems

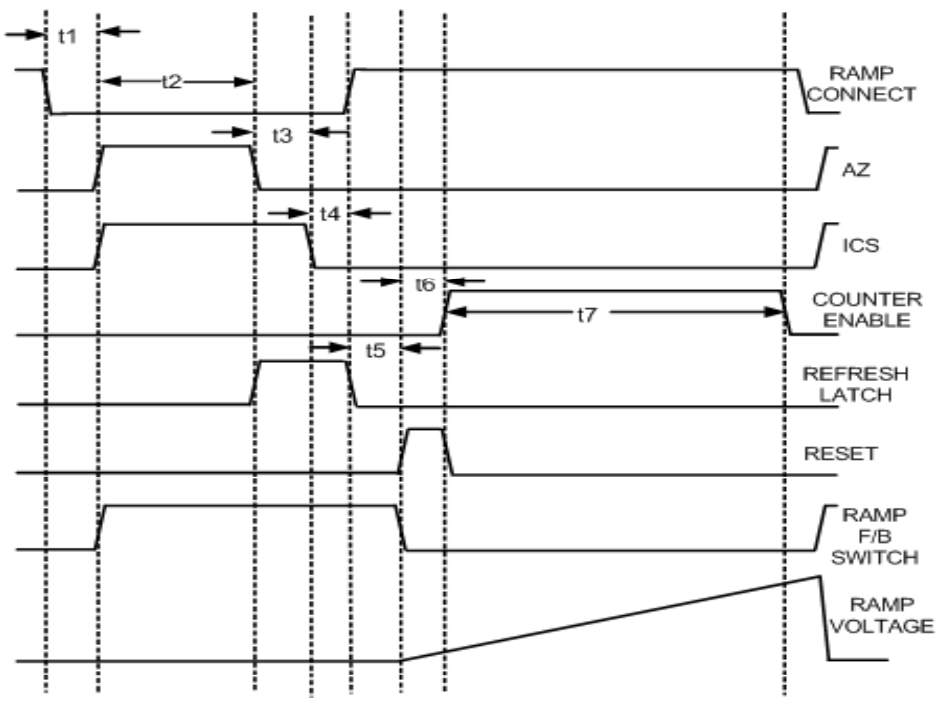
System Level Test Setup



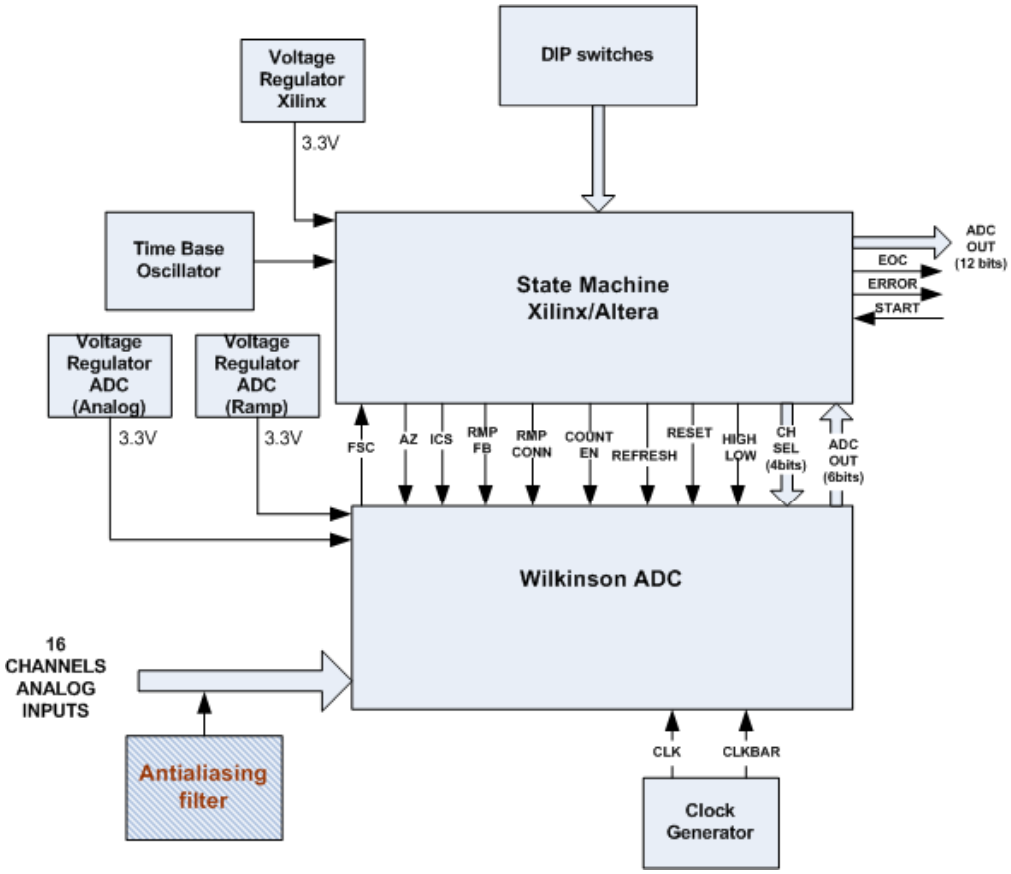
- LabView utilized
  - Programming the sources.
  - Analyzing data.
- Verilog
  - State machine to cycle through signals.
- Power proved through voltage regulators
- Analog input signals
- External clock going to FPGA and ADC counter.

Test Setup

- Digital signals required by the ADC
- Motherboard – 4 Layer
  - SPARTAN 3E FPGA
  - PROM Programmability
  - Voltage Regulators
  - Clock
  - Interface to NI card PCI 6534



- Daughter Card – 4 Layer
  - ADC chip
  - LVDS Transmitter

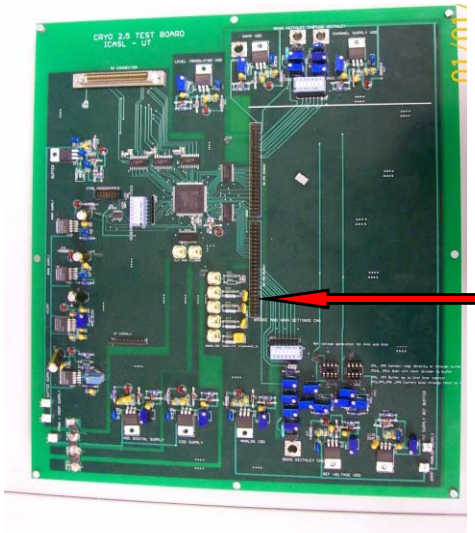


Test Boards

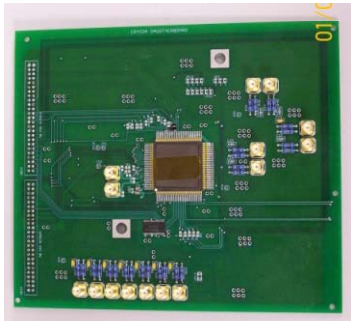
Digital Signal
Analog Digital Ground
Analog Digital Power
Analog Signals

- Mother board consists of programmable FPGA (PROM), regulators and voltage and current biases, NI connector.
- Daughter card for testing within the temperature chamber.
- Analog and digital grounds partitioned for reducing noise.

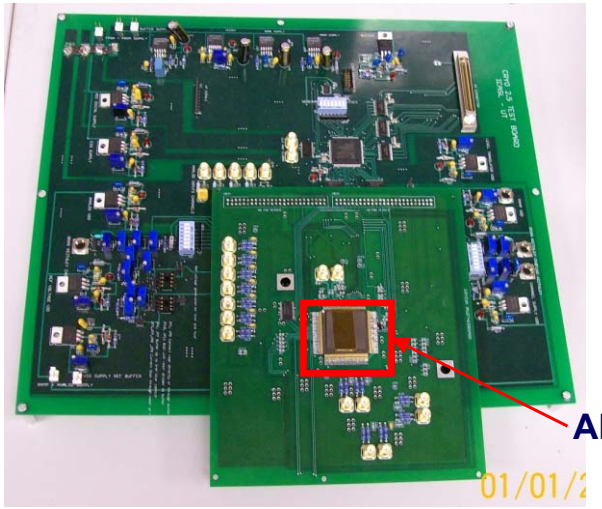
Mother Board



Daughter Card



Test Setup



DNL, INL and SNR Measurement

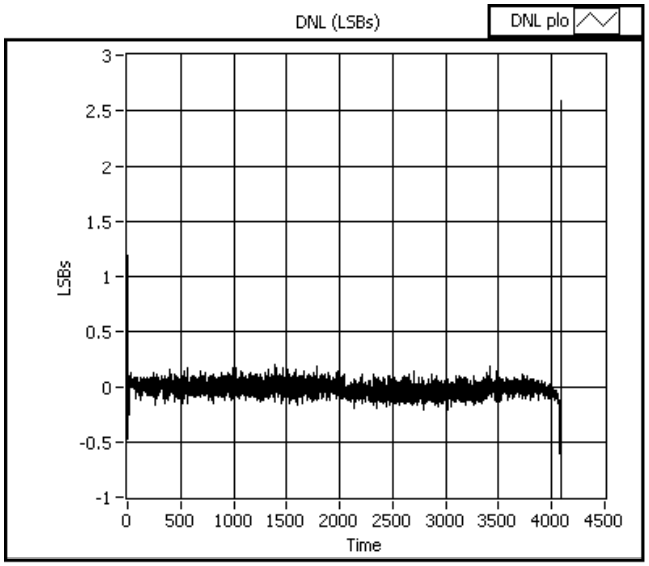
- Sine wave generated using a low distortion sine wave generator in series with a resistor and the input.
- DNL (Differential Nonlinearity) measured by histogram technique. Four million samples to satisfy accuracy requirement.
- Frequency is prime to the sampling frequency, to ensure random sampling.

$$DNL(i) = \frac{H(i)/Nt}{P(i)}$$

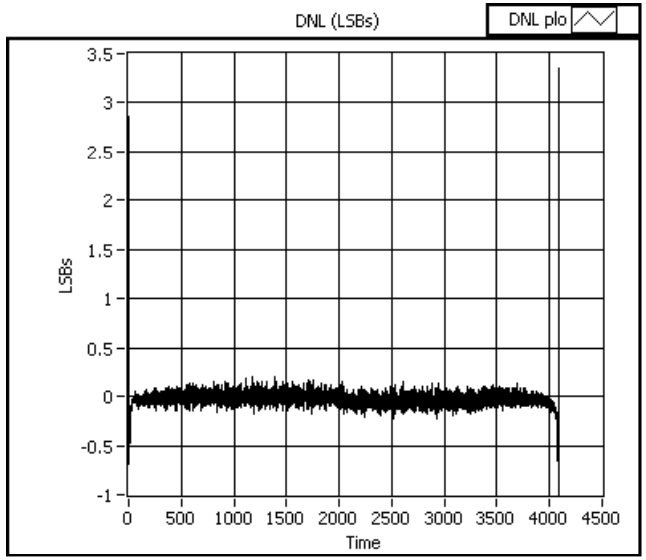
- INL (Integral Nonlinearity) measured by summation of DNL

$$INL(i) = \sum_{k=1}^{i-1} DNL(k)$$

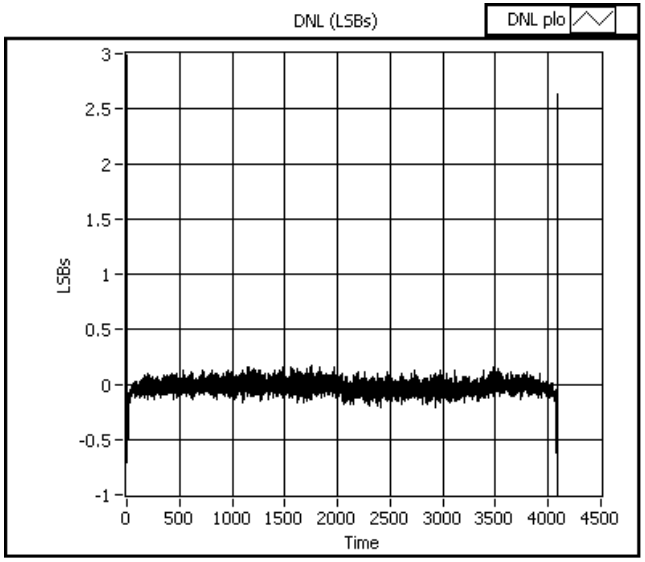
Differential Nonlinearity Over Temperature



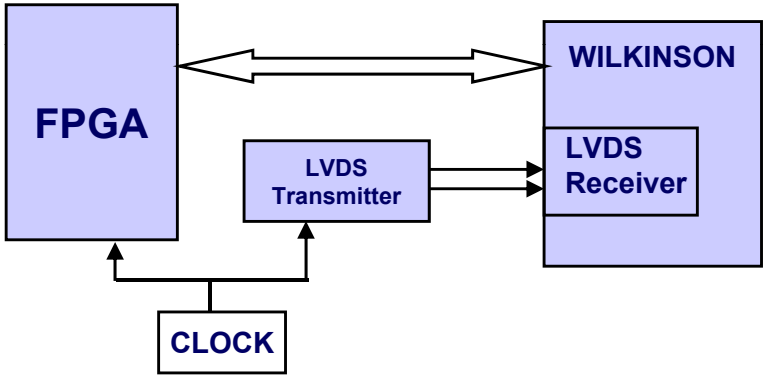
ADC DNL at Room Temperature



ADC DNL at 125ºC



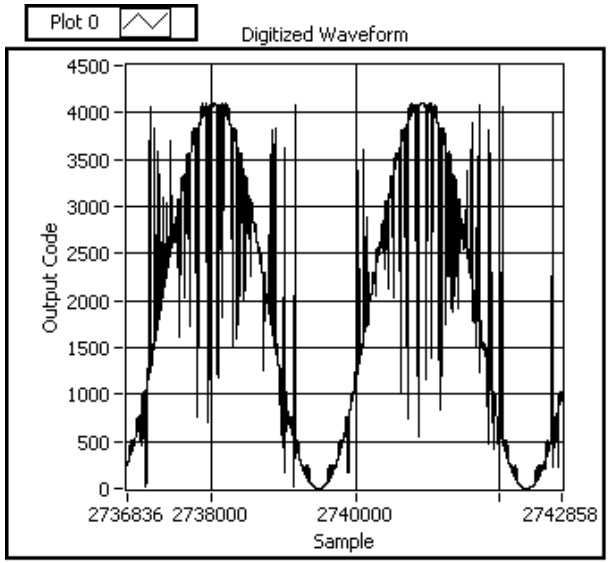
ADC DNL at 0ºC



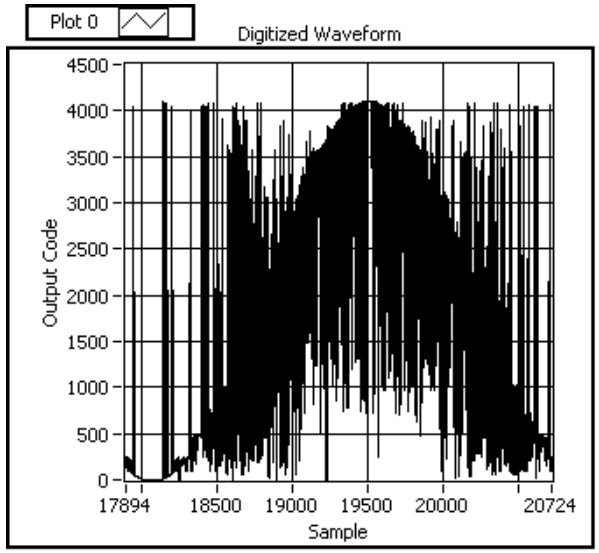
Test Setup

- Clean sine wave conversion obtained at room temperature with a clock frequency of 71 MHz.
  - Clock frequency lowered during test to reduce cabling EMI issues.
- A 12-bit differential nonlinearity was obtained.

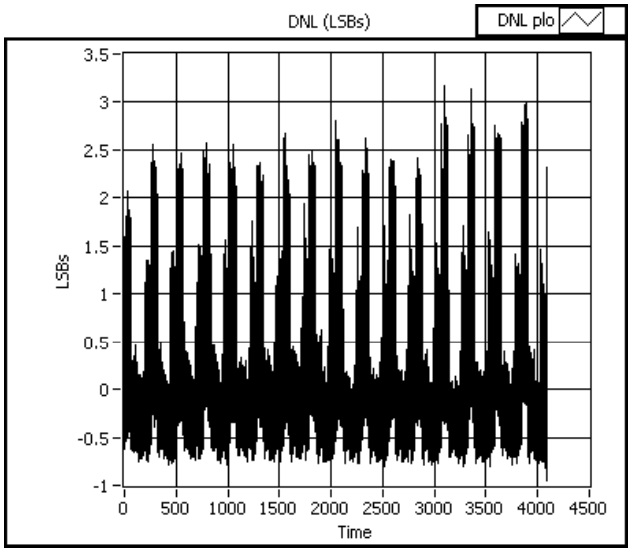
Results



Sine at -55ºC



Sine at -120ºC

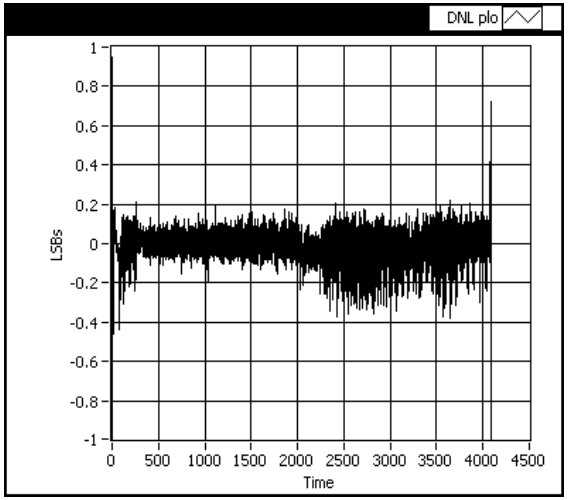


DNL at -120ºC

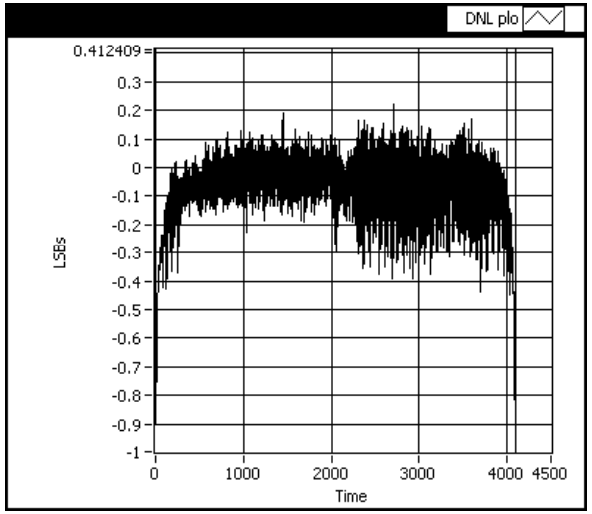
- At lower temperature, clock frequency needed to be further reduced to obtain clean sine wave conversion.
- Digital buffer IC on test board rated only to −40ºC.
- Shielded ribbon cable should help with the clock frequency issue.

Radiation Test Results

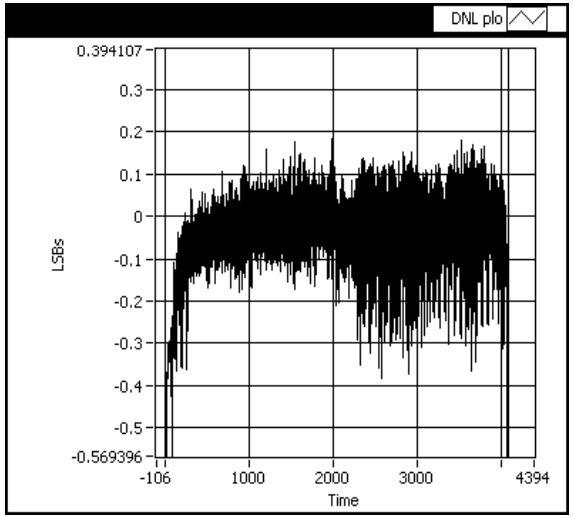
❑ ADC post-rad characterization:



DNL Proton: 100 Krad



DNL Proton: 300 Krad



DNL X-Ray: 300 Krad

Parameter	Pre-rad	100K Proton	300K Proton	300K X-ray
DNL	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB
SNR (dB)	60.8877	61.3268	61.8915	60.7922

⇒ **DNL and SNR show negligible change following TID irradiation.**

Conclusion

- Wilkinson ADC architecture described
- Design Blocks described
  - Auto-zero Comparator
  - Ramp Generator
  - Gray code counter
  - Radiation Aware Power Management System (RAPM)
- Test Setup described
  - Mother Board
  - Daughter Card
  - System Level
- Measurement results presented
  - Differential Nonlinearity (DNL)
  - Passive radiation results

Acknowledgements

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Thank You

Questions?