Multichannel Energy and Timing Measurements with the Peak Detector/Derandomizer ASIC

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Instrumentation Division Seminar

May18, 2005

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Instrumentation Division

*eV Products, Inc.

Instrumentation Seminars Presented Nov. 2001 -- Present

• O'Connor	4
• Rehak	3
• Yu	3
• Bolotnikov	3
• Woody	2
• Smith	2
• Li	2

OUTLINE

- Architecture
- Test set
- Spectroscopy performance
- High rate performance
- Simultaneous event handling
- New PDD version IC87
- New data acquisition MIOS
- Future applications

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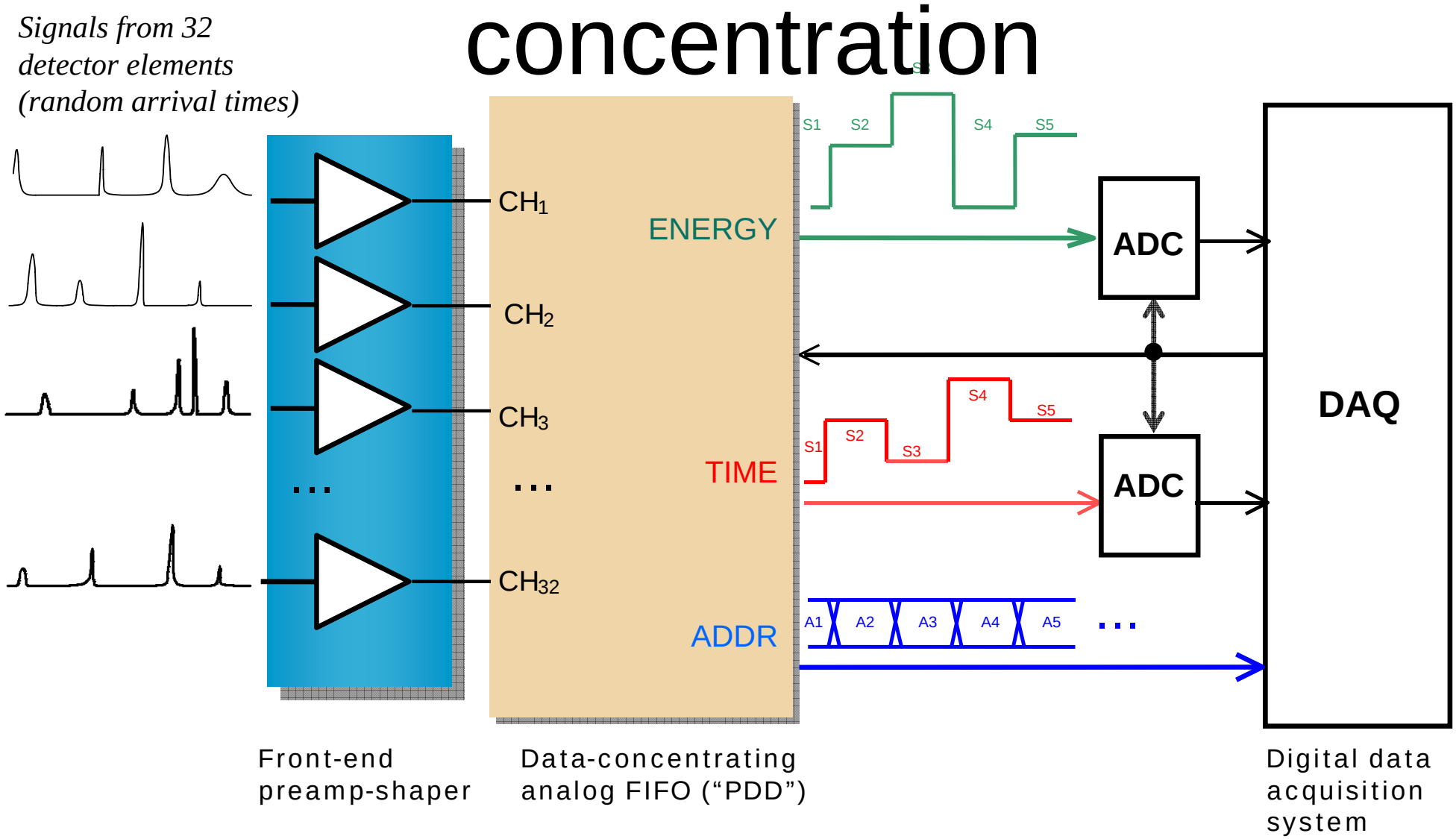
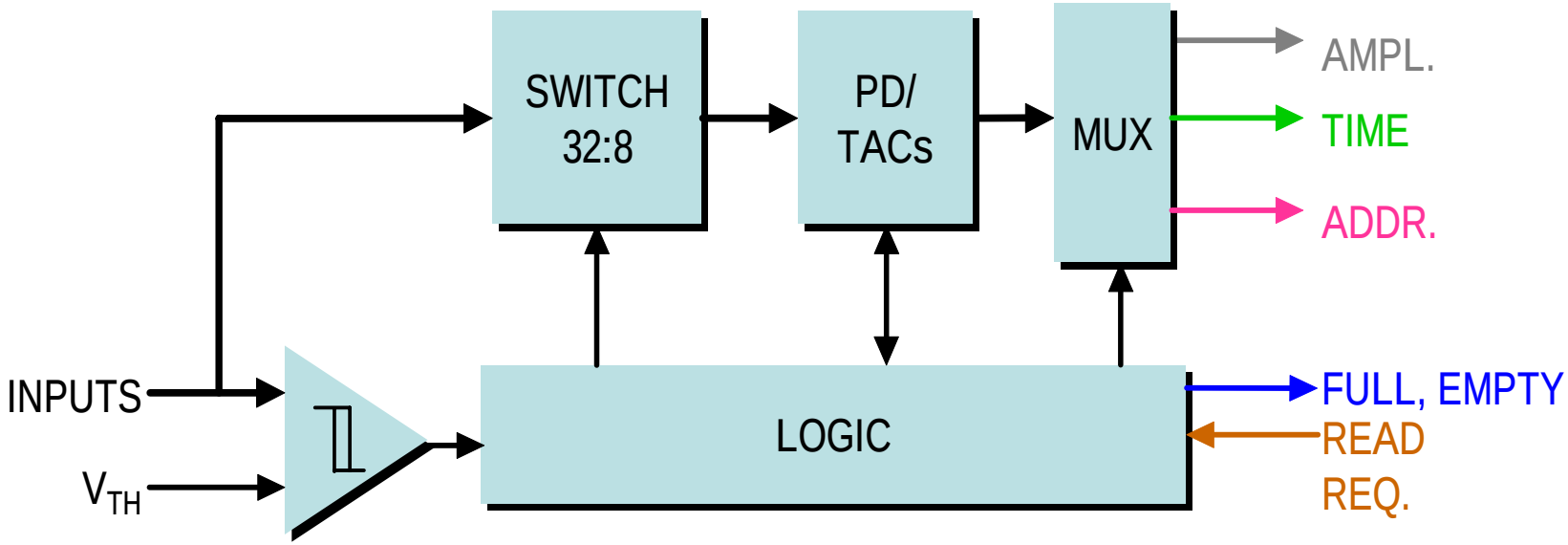
Multichannel pulse measurement with analog data concentration



PDD ASIC Block Diagram



- New architecture for efficient readout of multichannel detectors
  - *Self-triggered and self-sparsifying*
  - *Simultaneous amplitude, time, and address measurement for 32 input channels*
  - *Set of 8 peak detectors act as derandomizing analog memory*
  - *Rate capability improvement over present architectures*
- Based on new 2-phase peak detector combined with dual-mode TAC
  - *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
  - *Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel*
  - *Low power (3 mW per channel)*

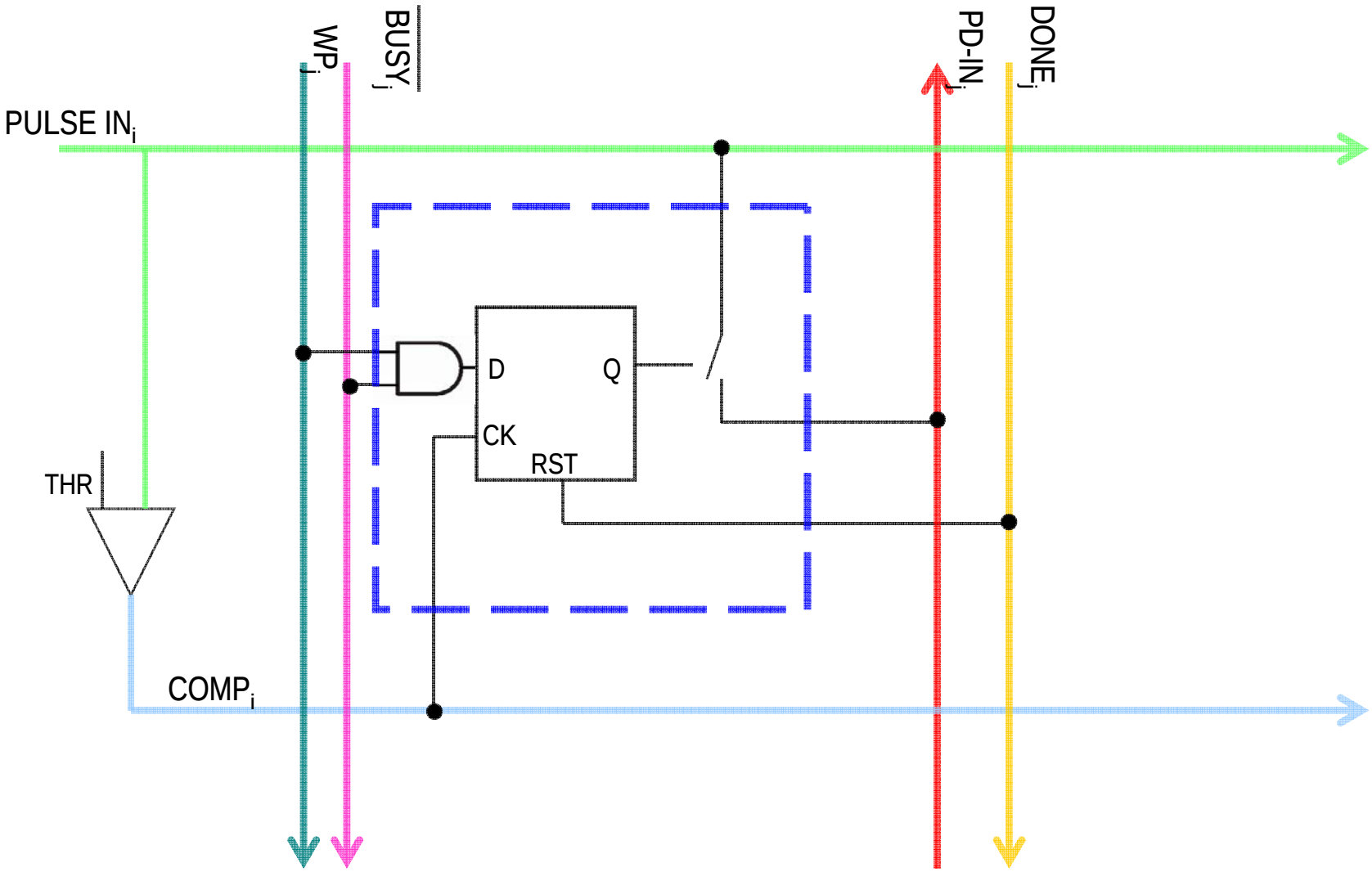
P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASIC with analog derandomization: first results*, IEEE Trans. Nucl. Sci. 50(4), pp. 892-897 (Aug. 2003).

Switch matrix

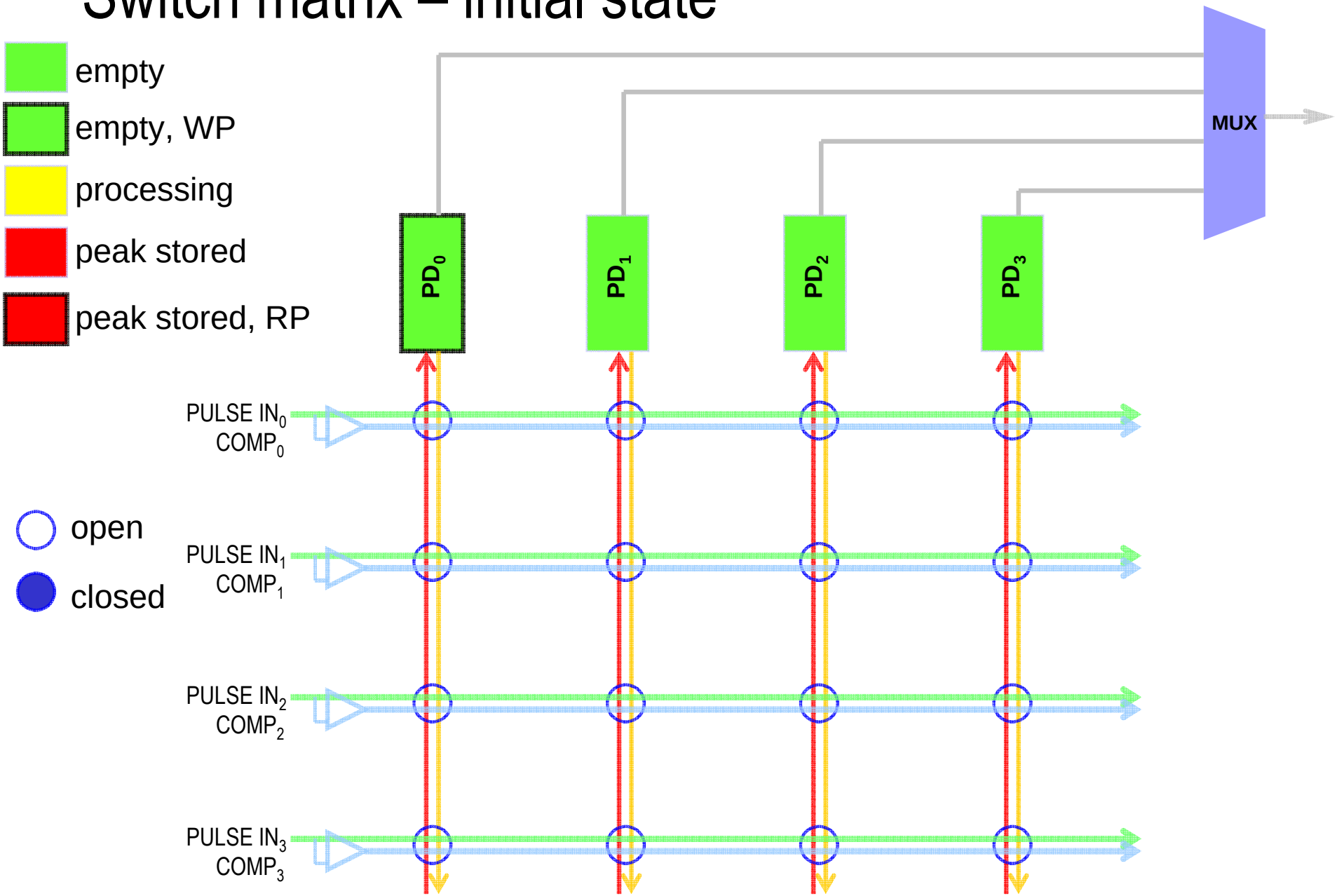
8 Simple Rules:

1. Only one switch in any row or column may be closed at a time.
2. Switch (i,j) closes when incoming pulse on row i crosses threshold and WP points to column j.
3. Switch remains closed until done acquiring peak and timing.
4. WP moves from left to right; when all PD are empty, WP reverts to column 0 and the EMPTY flag is raised.
5. RP is managed so that data is read out in the same order that events arrive (FIFO).
6. If two or more pulses arrive during close together so that the WP hasn't moved, the lower-numbered row generates an inhibit signal that blocks acquisition of all higher-numbered rows (dead time for simultaneous events).
7. If all PD are storing pulses, the FULL flag is raised and incoming pulses are blocked until the read request catches up.
8. The DATA VALID flag is asserted in response to a read request when there is data to be read out.

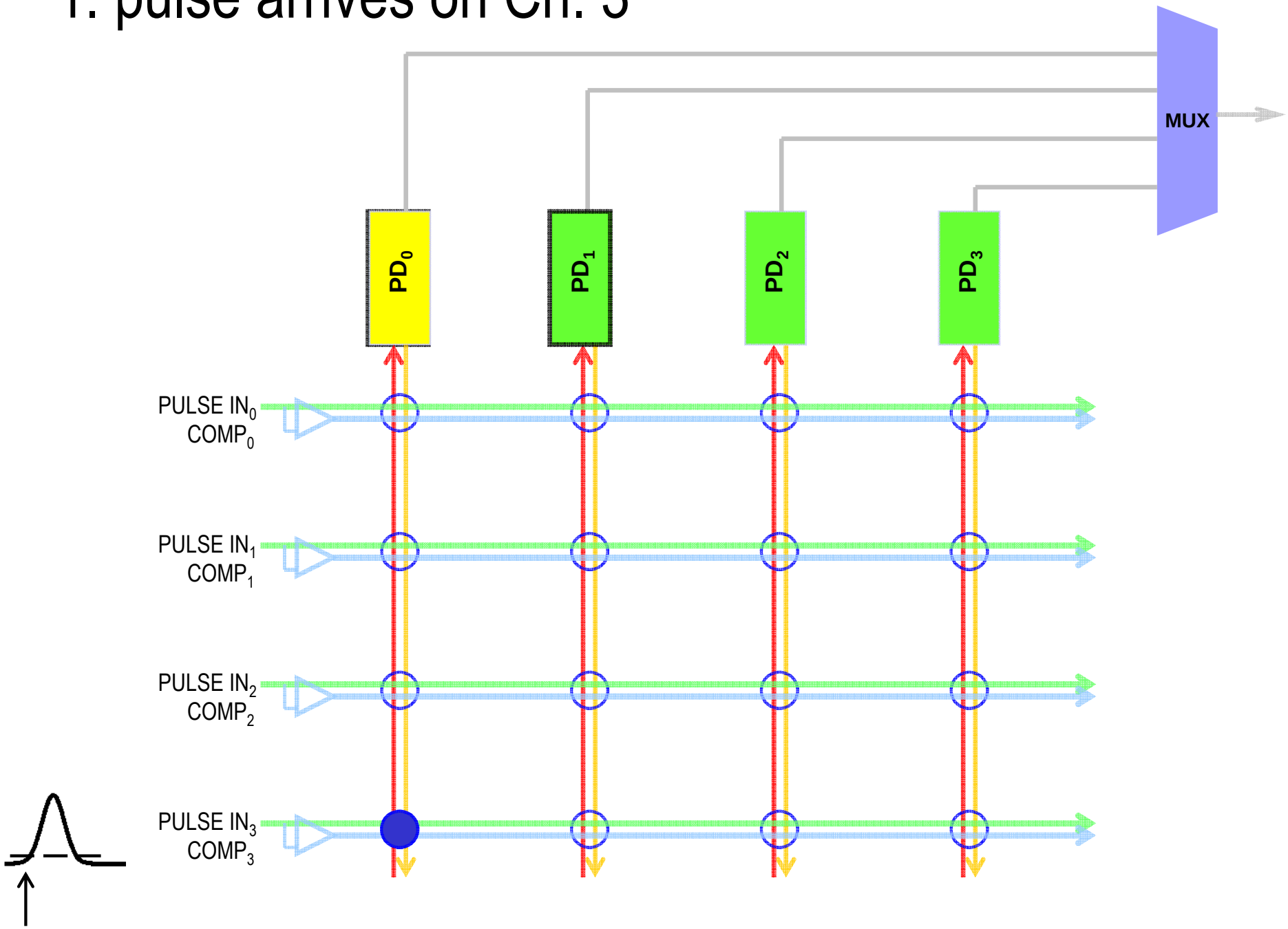
Matrix cell



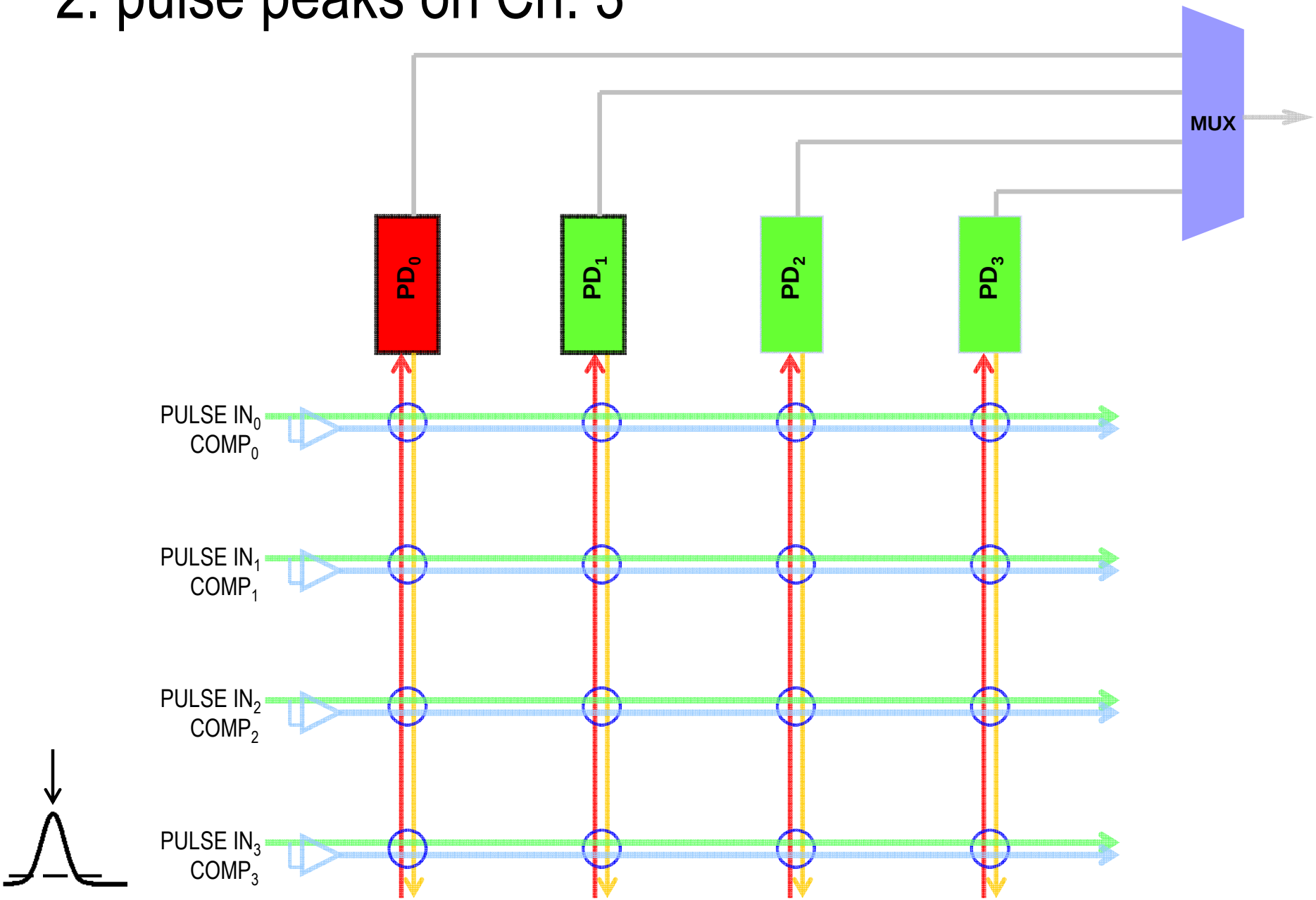
Switch matrix – initial state



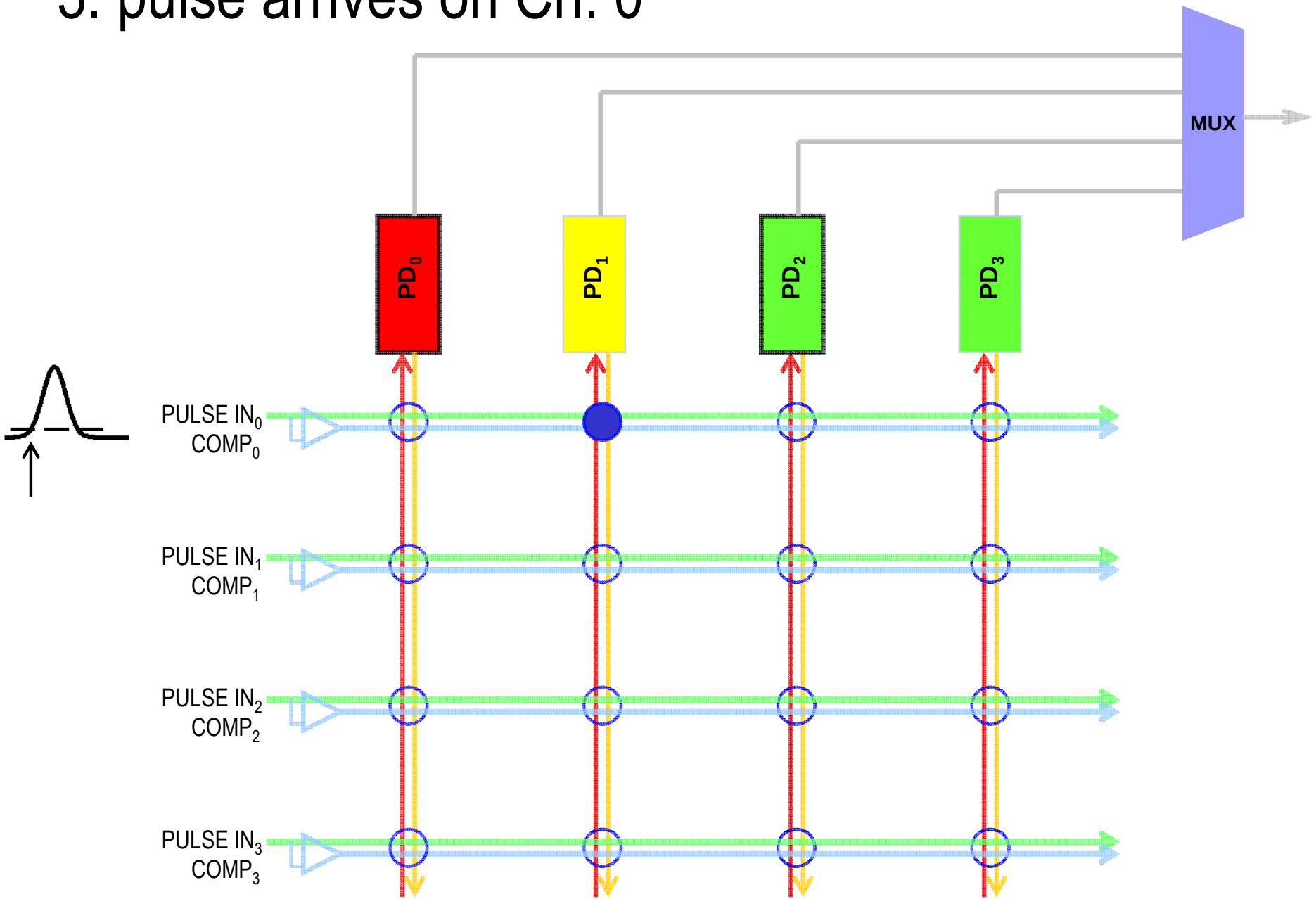
1. pulse arrives on Ch. 3



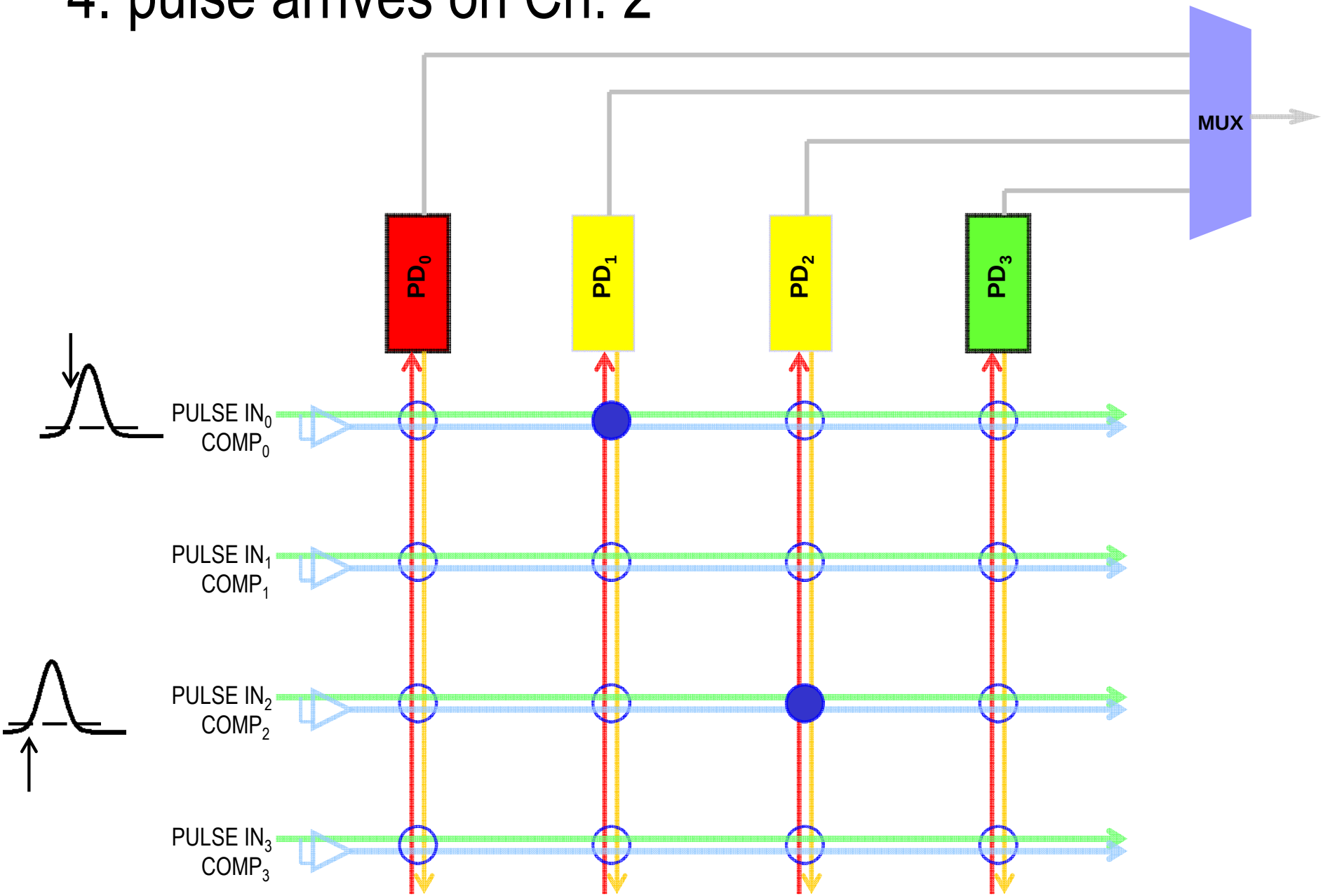
2. pulse peaks on Ch. 3



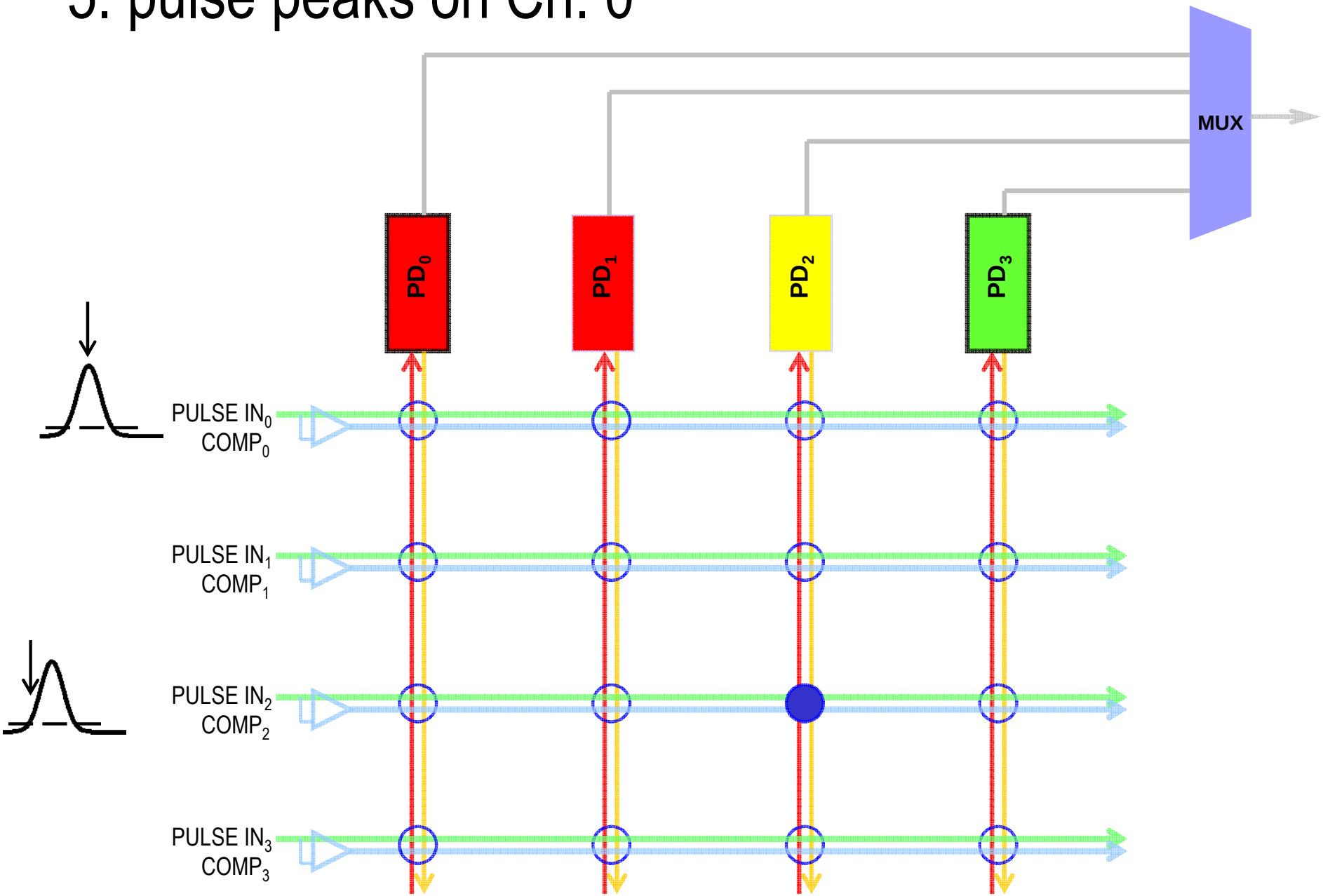
3. pulse arrives on Ch. 0



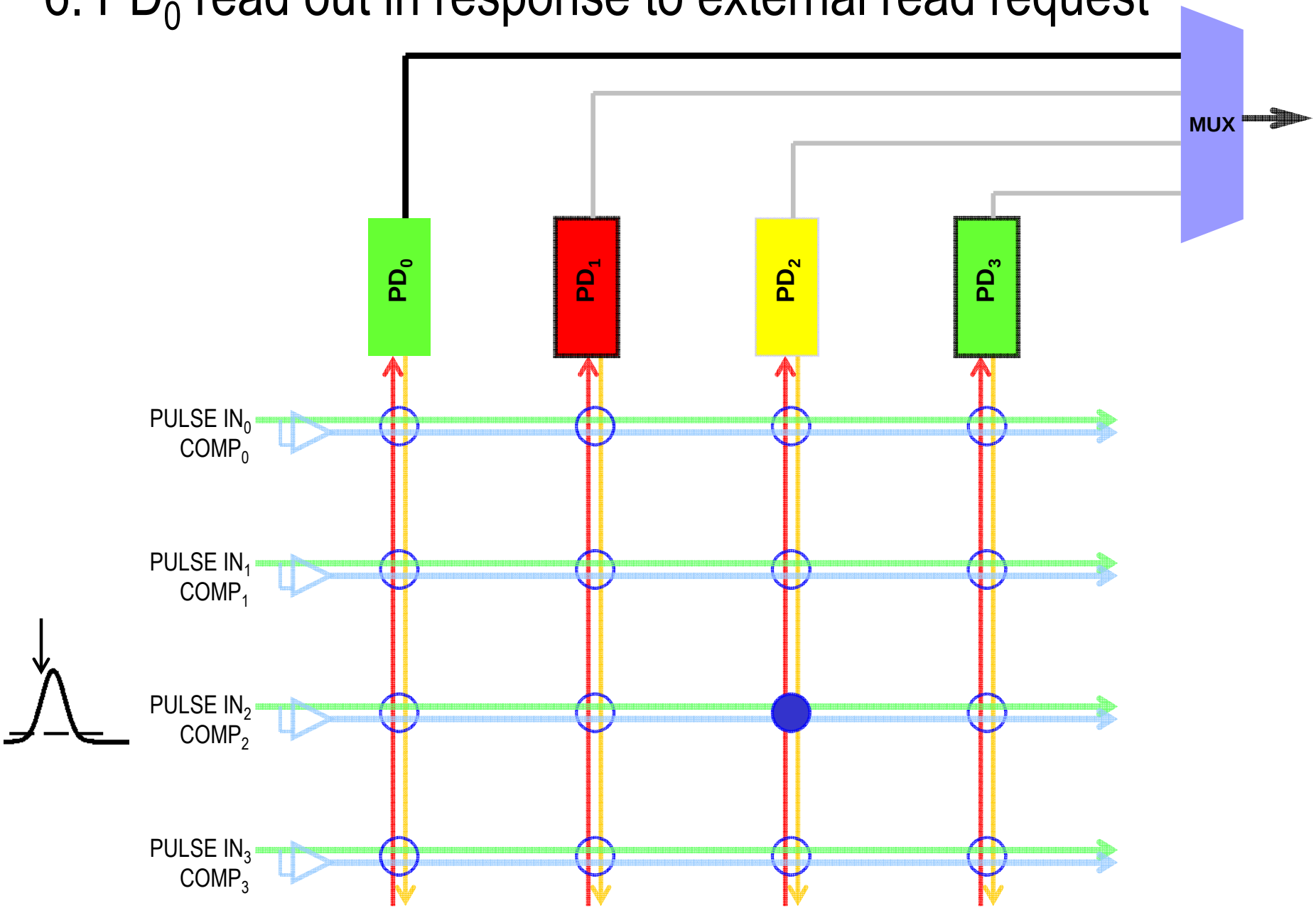
4. pulse arrives on Ch. 2



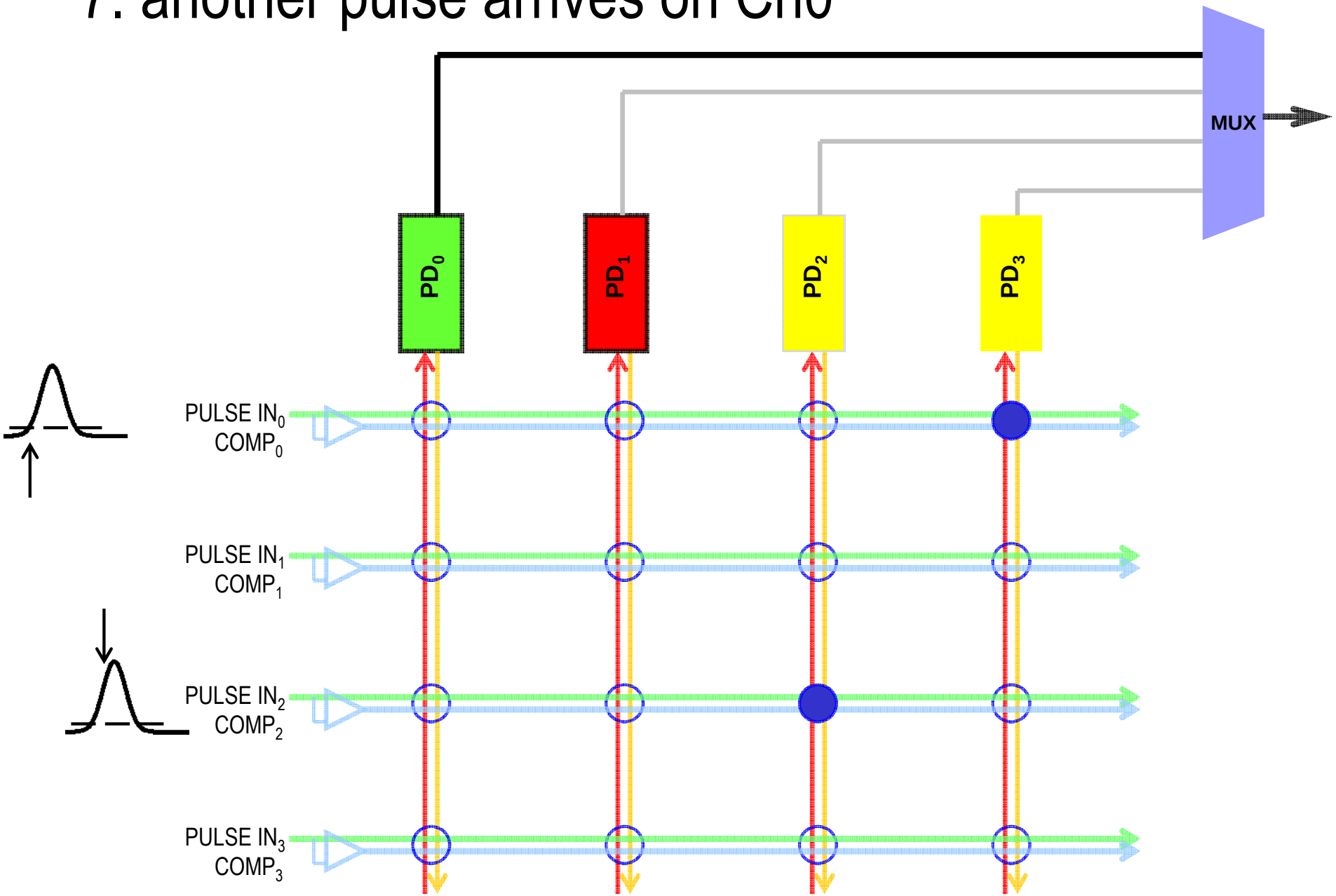
5. pulse peaks on Ch. 0



6. PD_0 read out in response to external read request



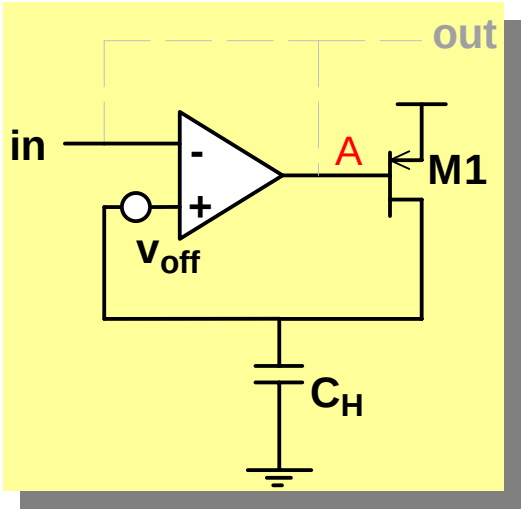
7. another pulse arrives on Ch0



Improved CMOS PD Using Two-Phase Configuration

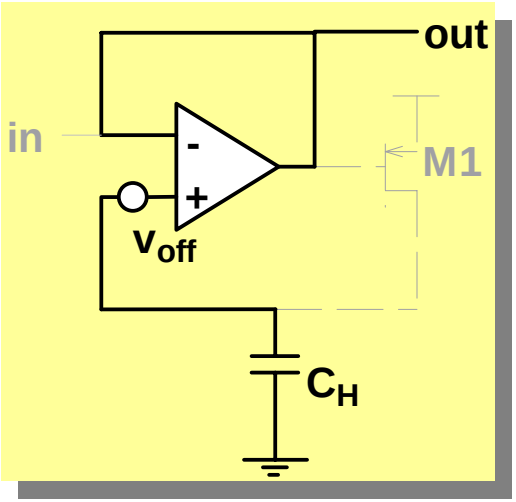
Write phase

- conventional peak detector
- M1: unidirectional current source
- voltage on C_H includes op-amp errors (offset, CMRR)



Read phase

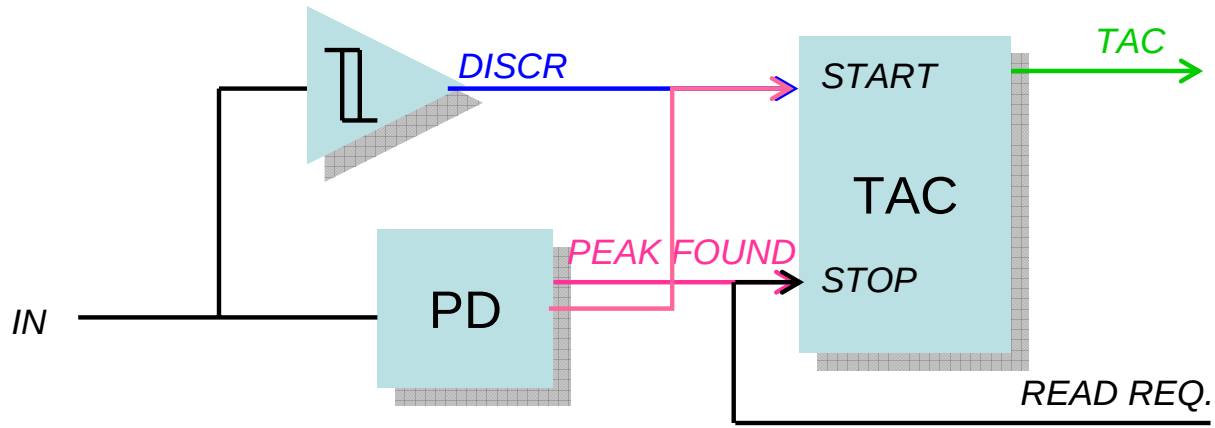
- same op-amp re-used as unity-gain buffer
- same CM voltage
- ***op-amp errors cancel***
- enables rail-to-rail sensing
- provides good drive capability

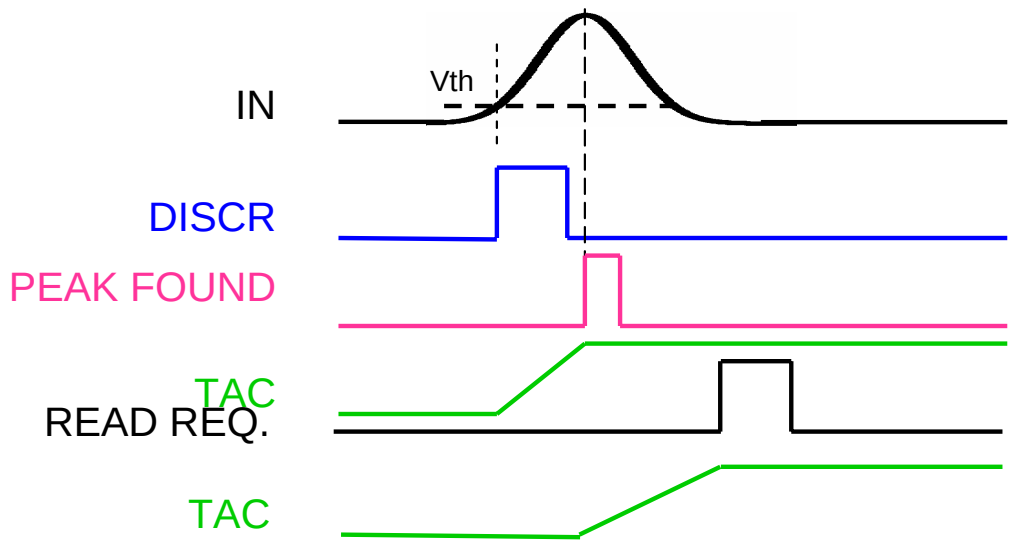


U.S. Pat. 6,512,399

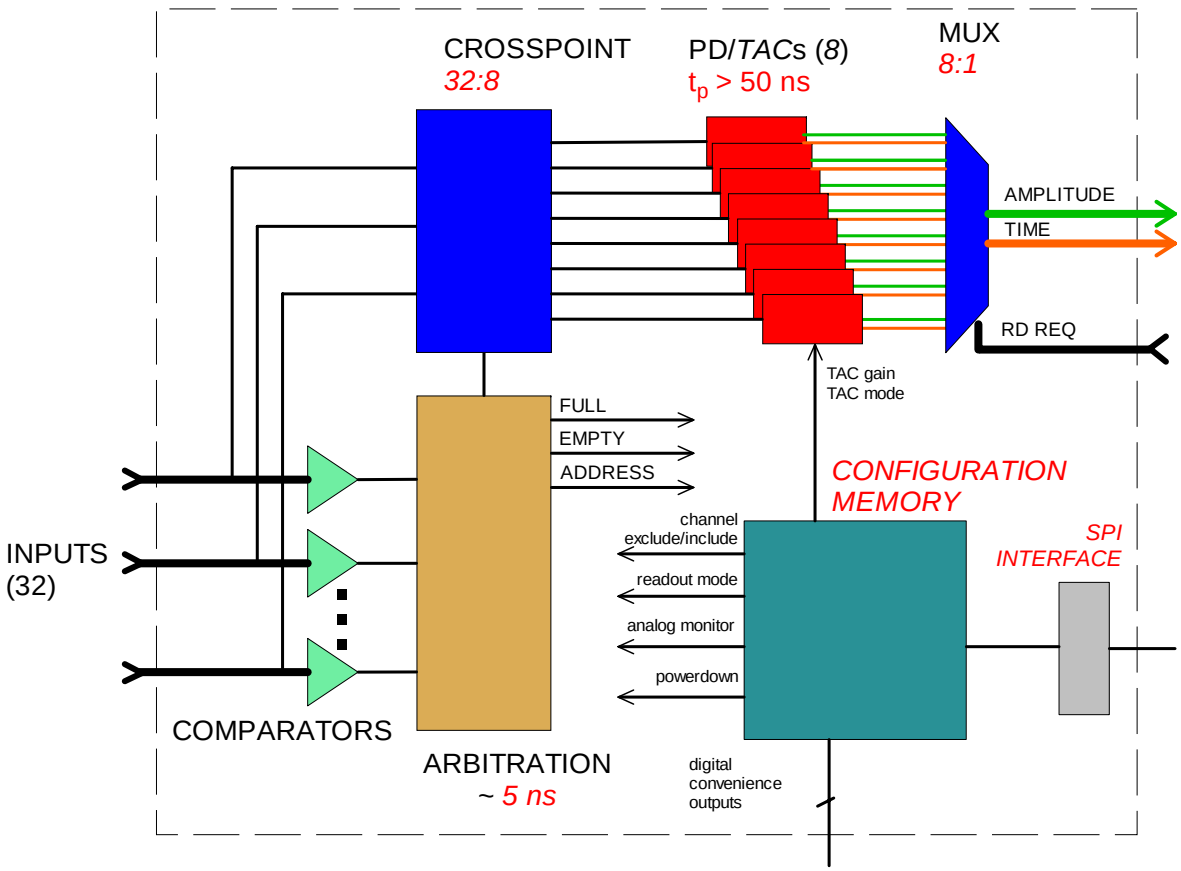
Dual-mode Time-to-Amplitude Converter

MODE 1
MODE 2



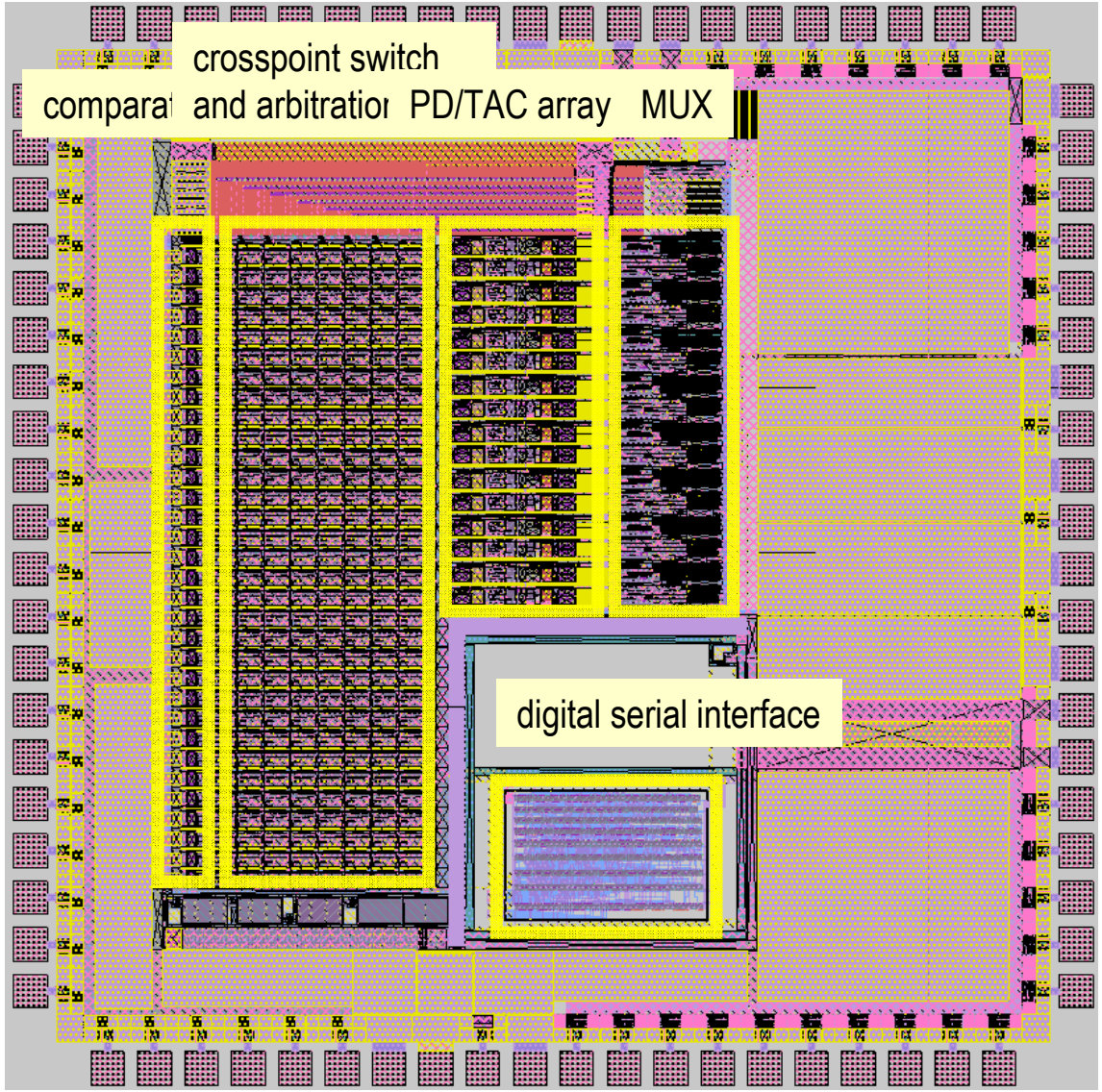


Block diagram



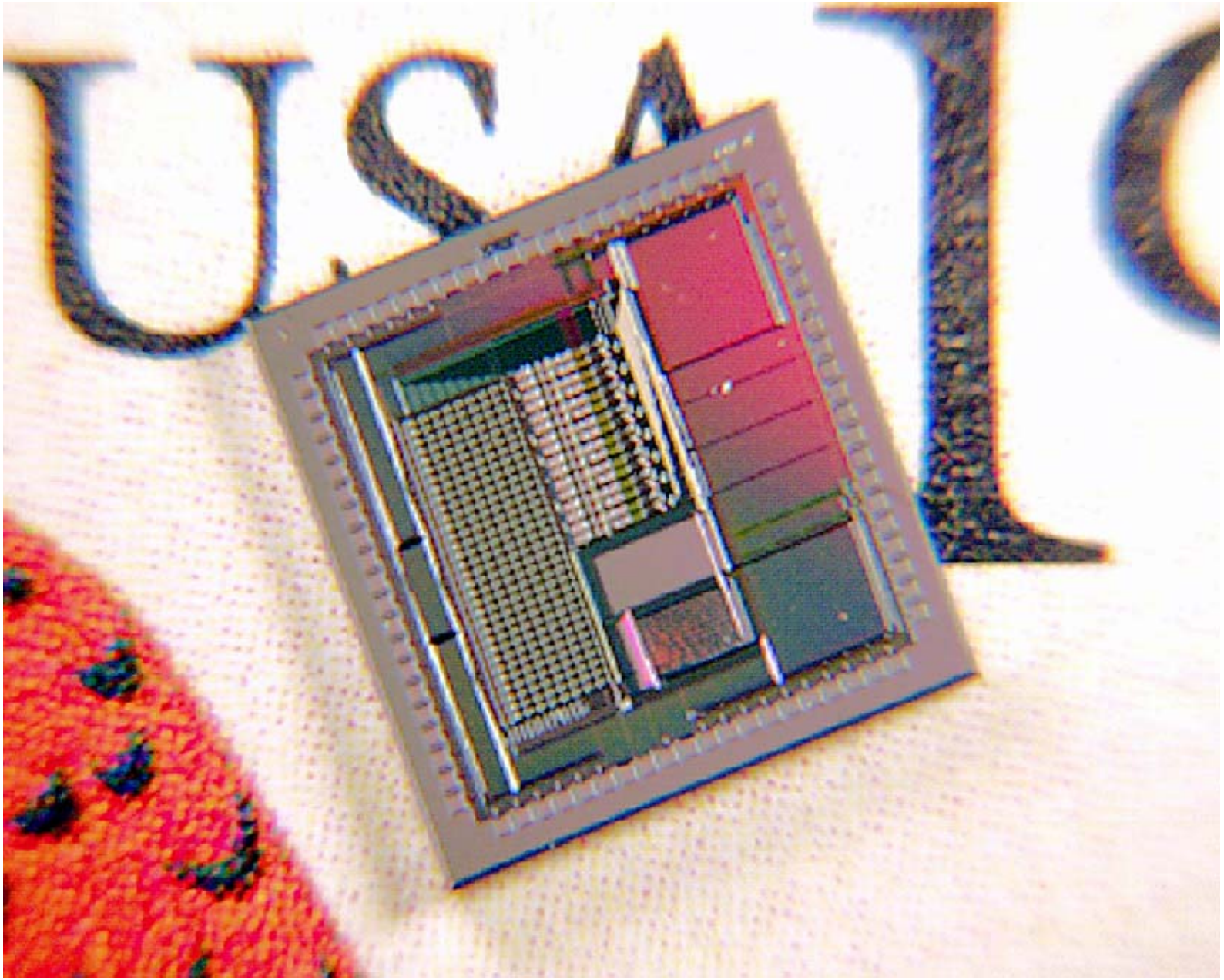
- One-chip solution
- N_{CHAN} = 32, N_{PD} = 8
- Dual-mode TAC
  - risetime
  - time of occurrence
- Amplitude, address, time outputs
- 50 ns minimum pulsewidth
- t_{ARB} ~ 5 ns
- Rate capability ~ 10 MHz
- SPI interface:
  - serial configuration of TAC gain and mode
  - arbitration locking
  - channel exclusion
  - powerdown
  - analog monitor
  - Digital convenience outputs (used for configuring companion amplifier chip)
- FIFO-like control and readout interface

Layout



size : 3.2 x 3.2 mm²
power : 2mW / channel
technology: 0.35µm CMOS DP4M

Die photo



OUTLINE

- Architecture
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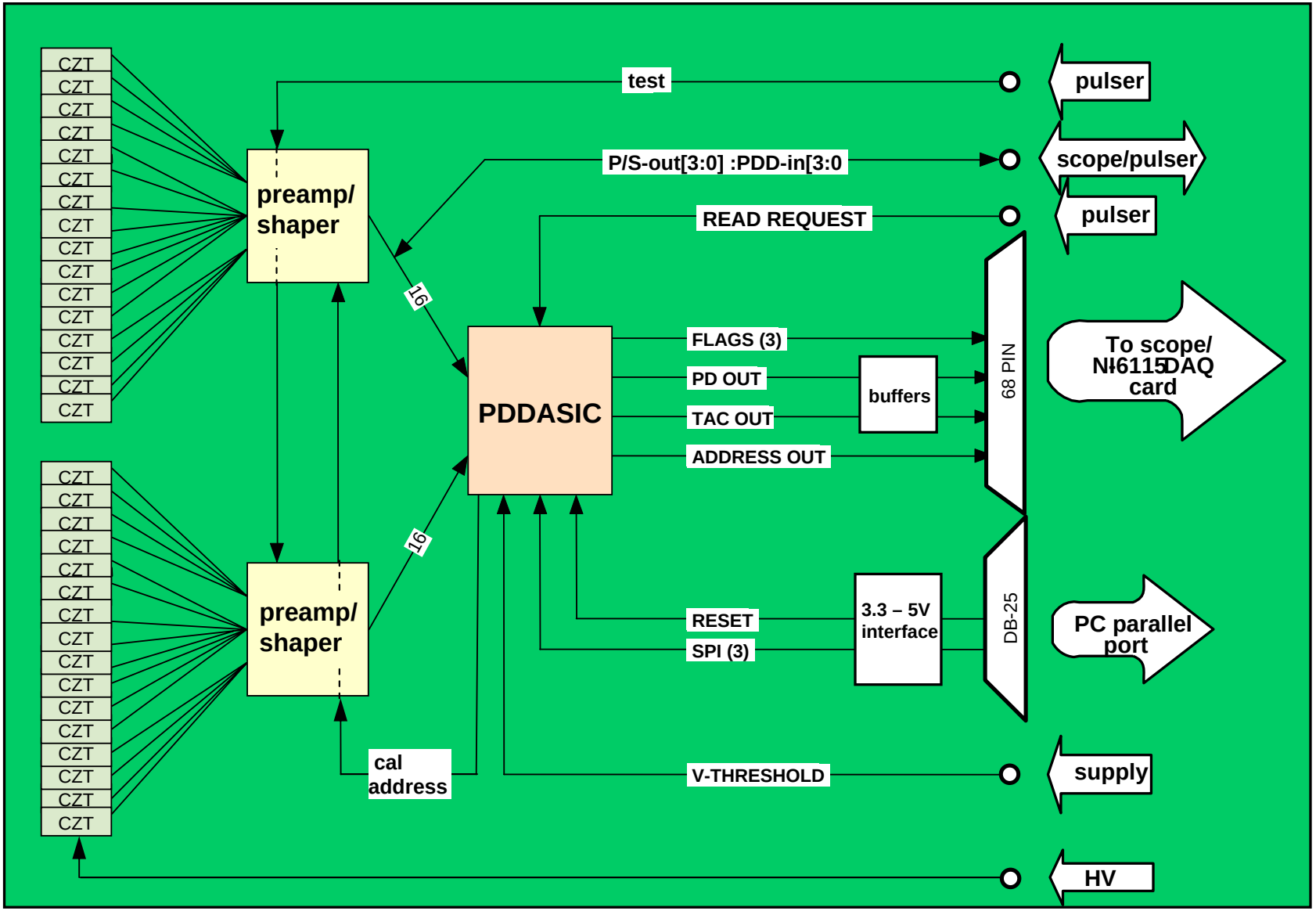
- Spectroscopy performance
- High rate performance
- Simultaneous event handling
- New PDD version IC87
- New data acquisition MIOS
- Future applications

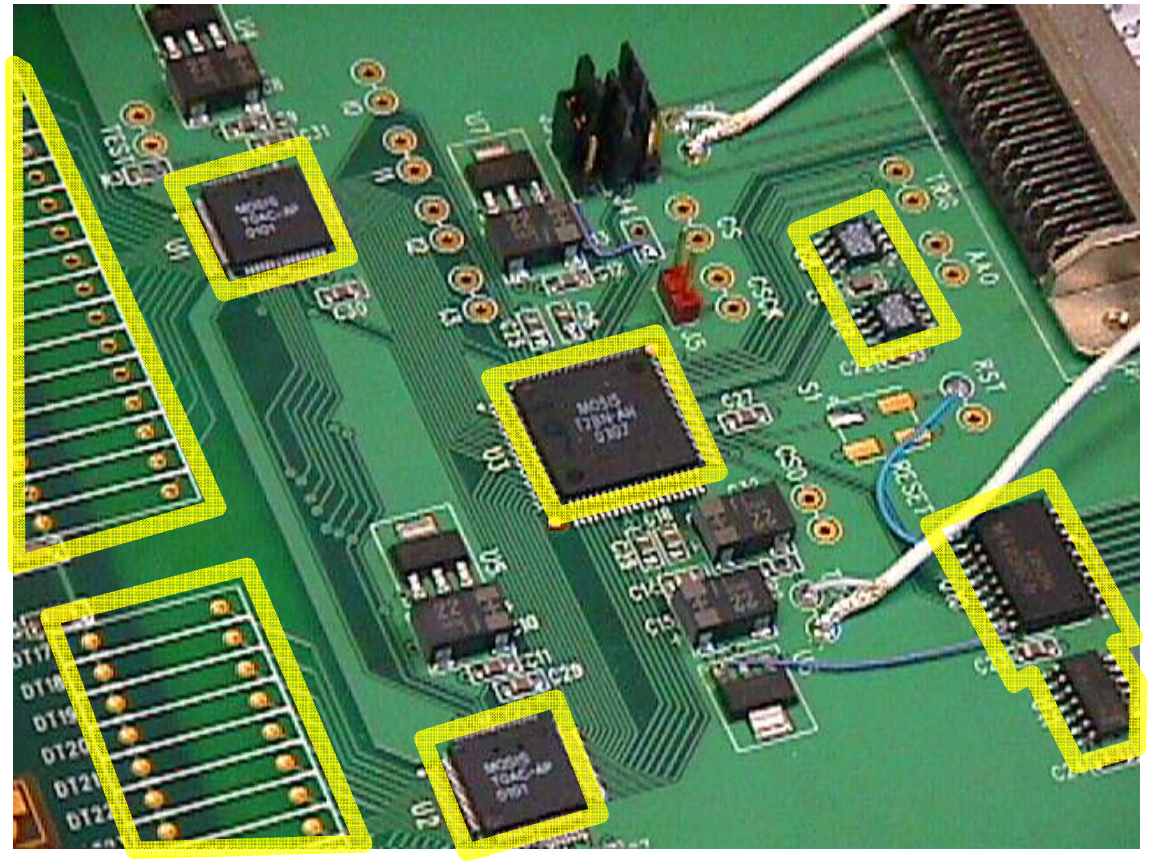
Test Board


CZT
preamp/ shaper
preamp/ shaper
16
16
PDDASIC
test
P/S-out[3:0] :PDD-in[3:0
READ REQUEST
FLAGS (3)
PD OUT
TAC OUT
ADDRESS OUT
buffers
68 PIN
DB-25
RESET
SPI (3)
3.3 – 5V interface
cal address
V-THRESHOLD
pulser
scope/pulser
pulser
To scope/ NI6115DAQ card
PC parallel port
supply
HV

Test Board – ASIC side

buffer amps

32-3x7x3mm^3
CZT

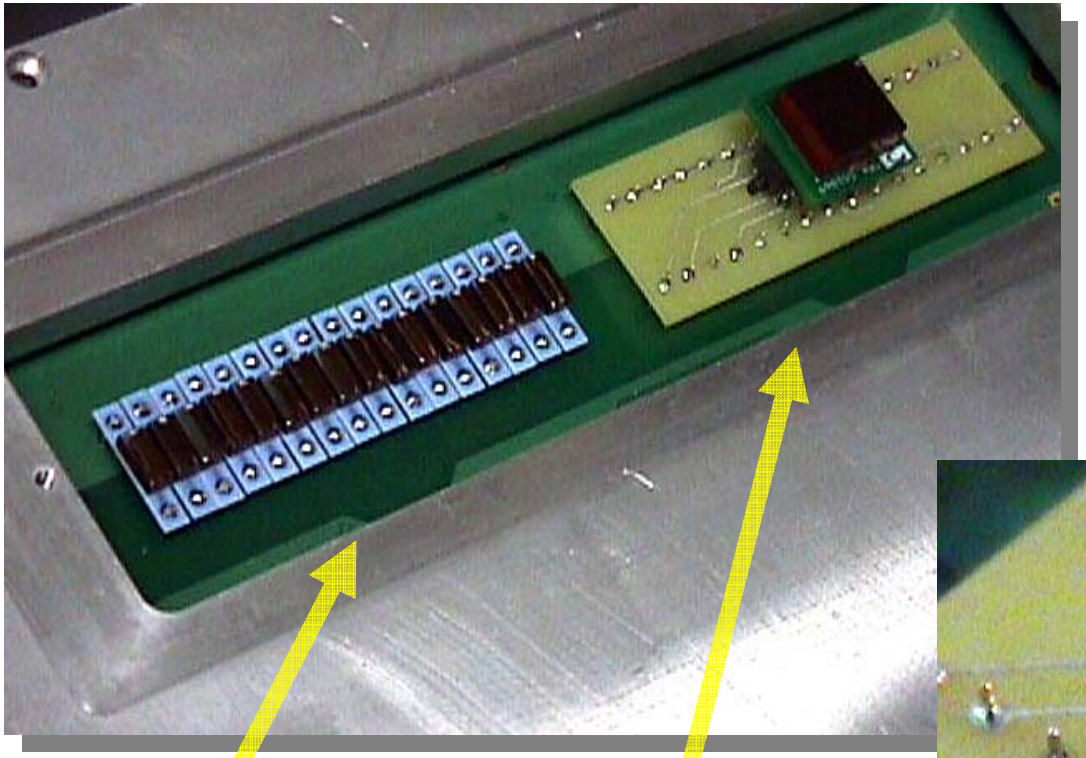


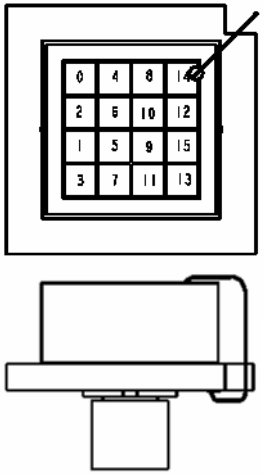
low-noise preamp/shapers

PDD ASIC

digital serial interface

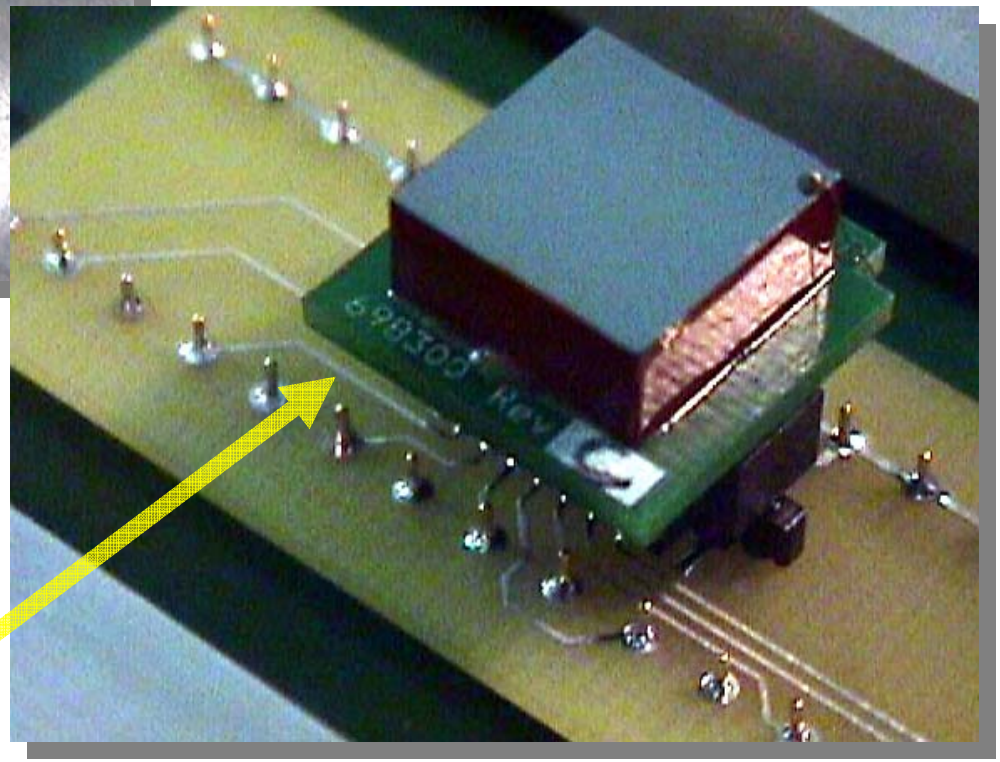
Test board – detector side



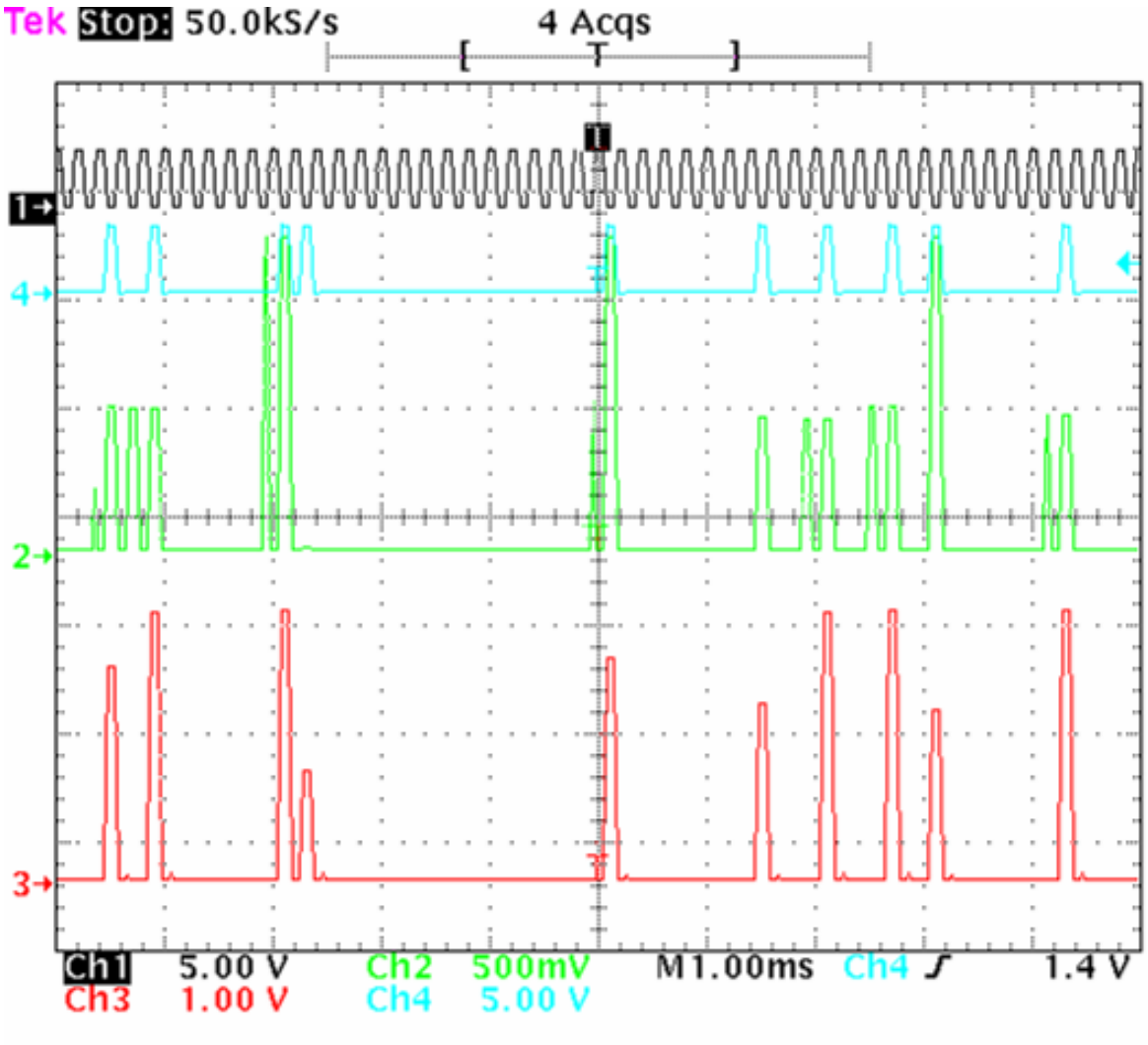


16 -- 3x7x3mm^3 planar CZT detectors

11x11x5 mm^3 pixilated CZT detector



PDD ASIC waveforms



READ REQ.

DATA VAL.

AMPLITUDE OUT

TIME OUT

Test Stand and Labview Software

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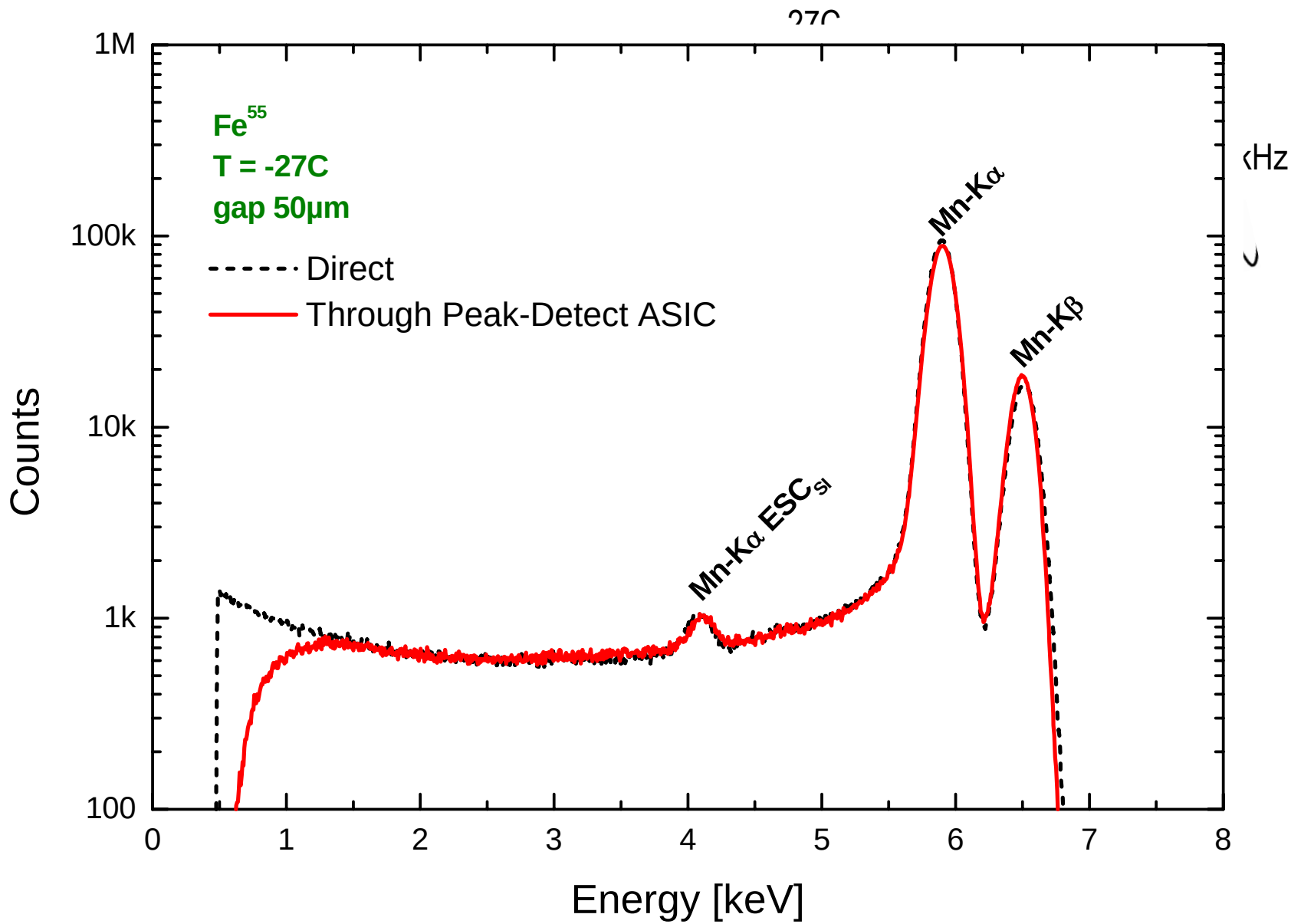
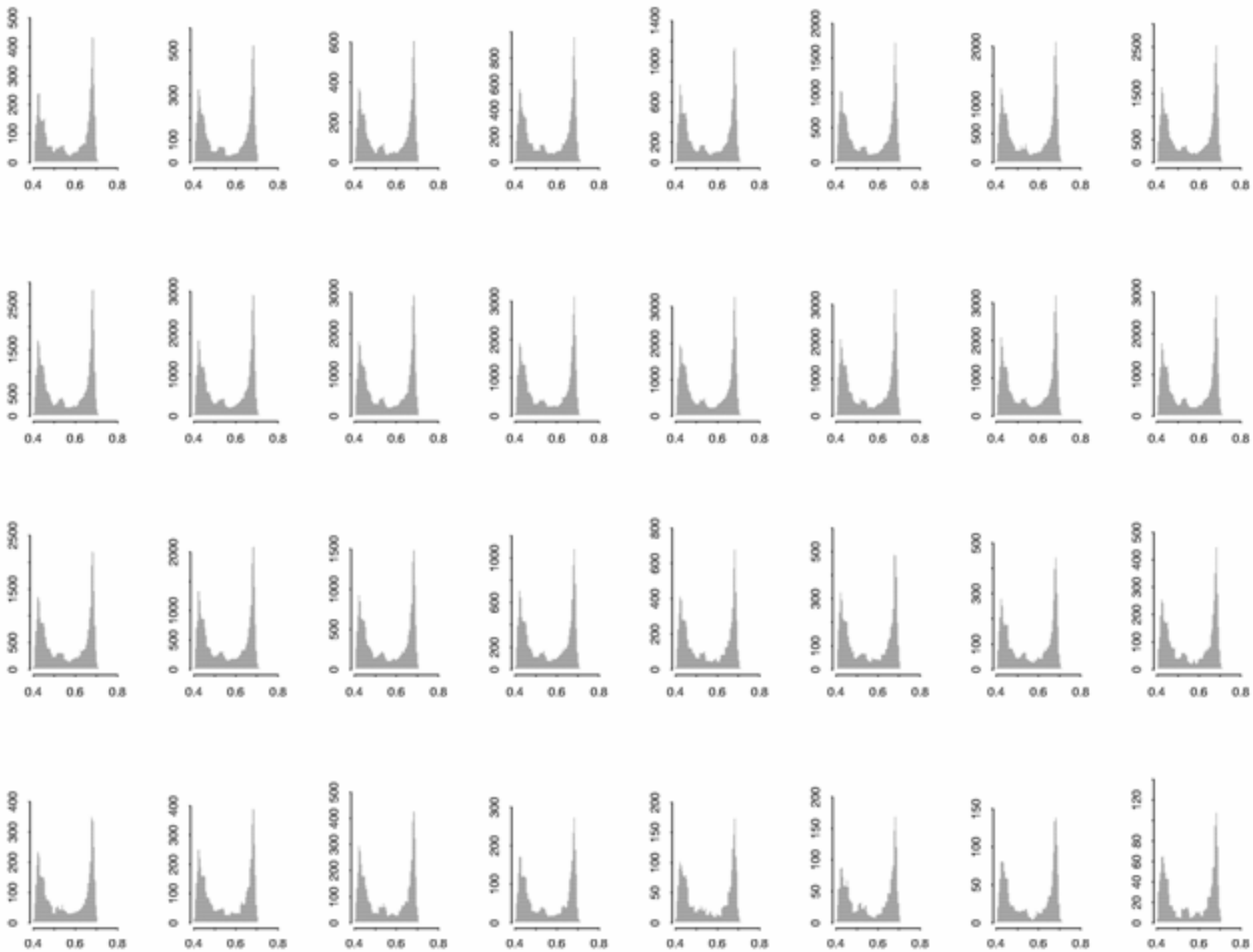
High resolution, single-channel spectroscopy

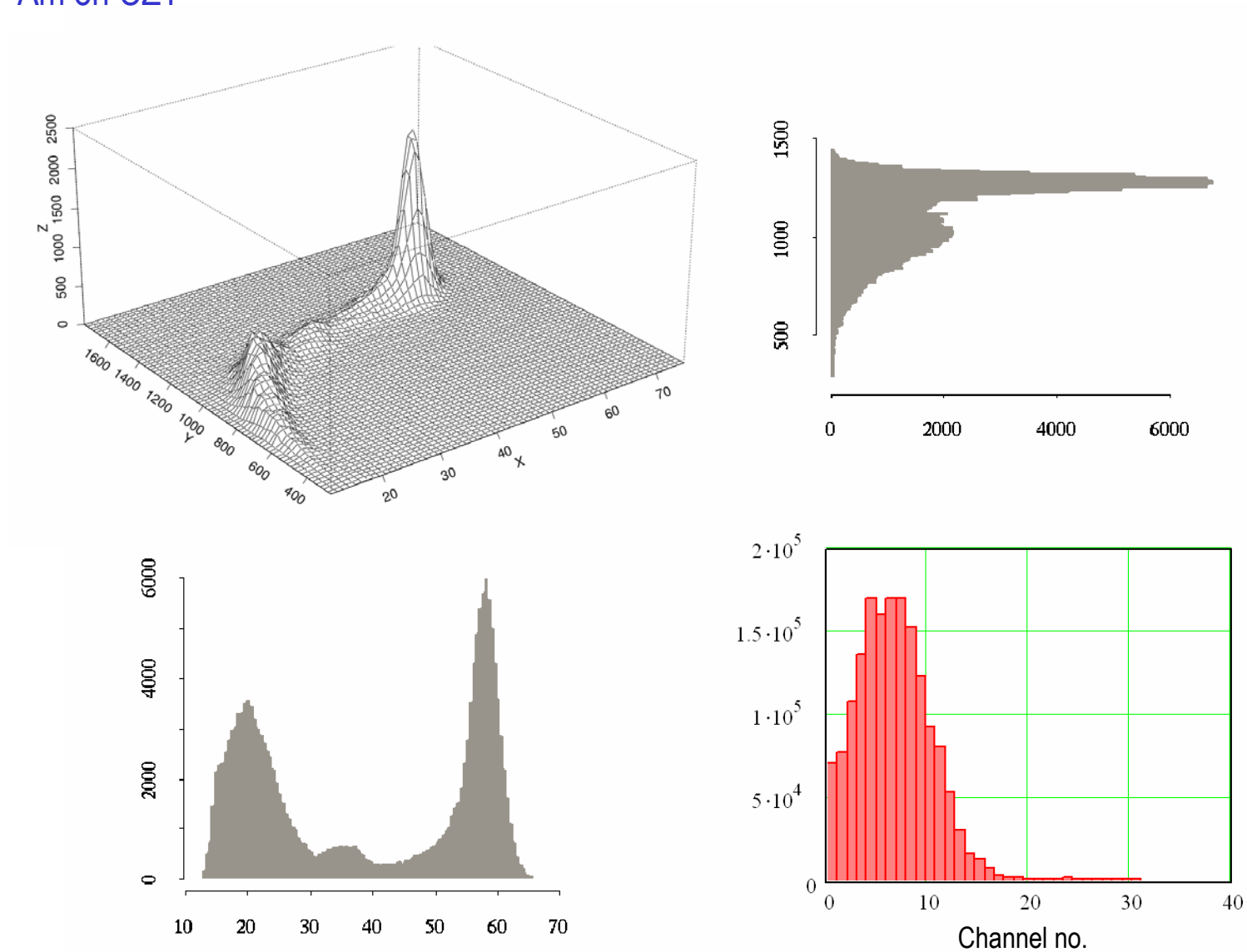


High rate, simultaneous multichannel spectrum collection

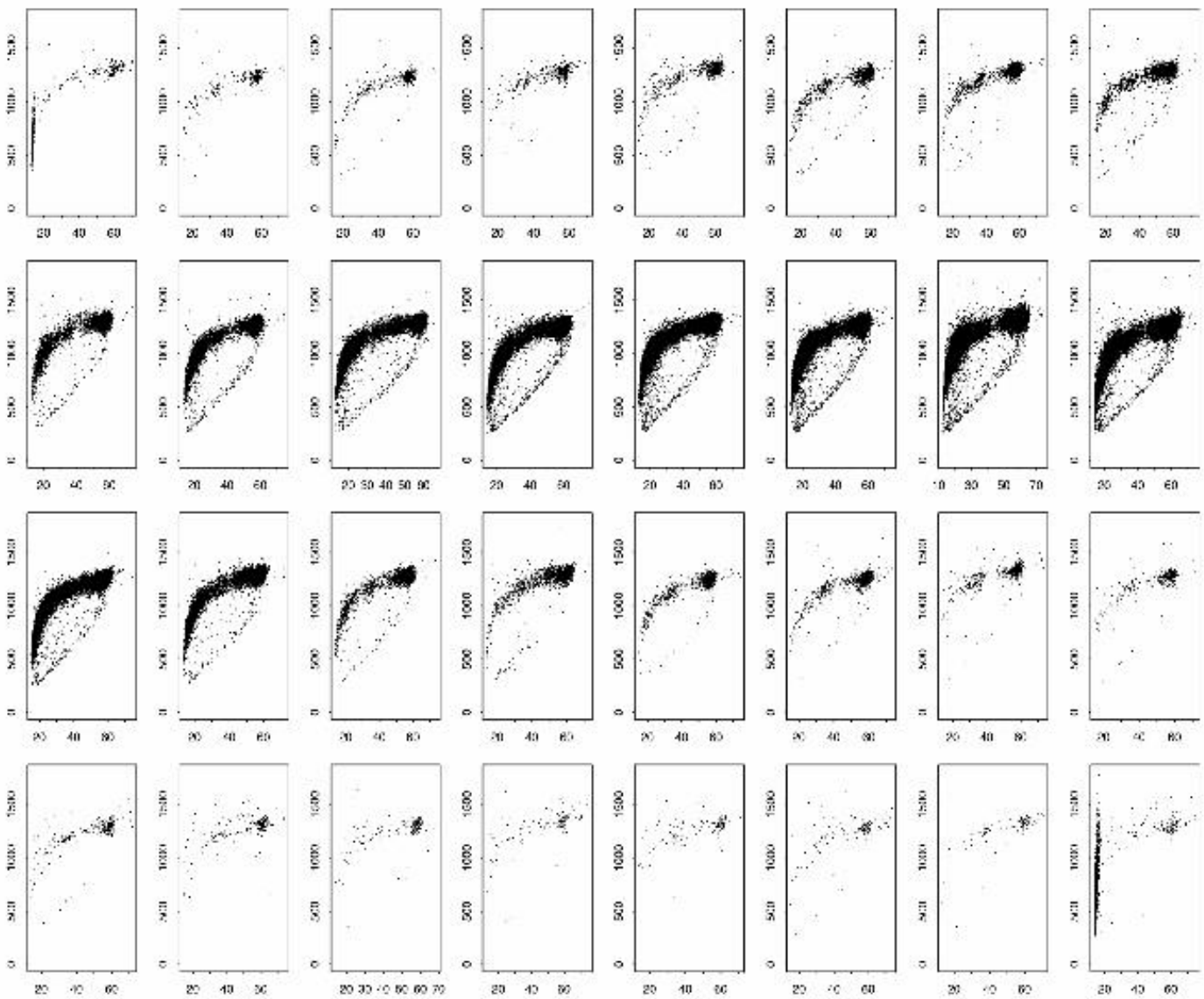


Biparametric spectrum

^{241}Am on CZT

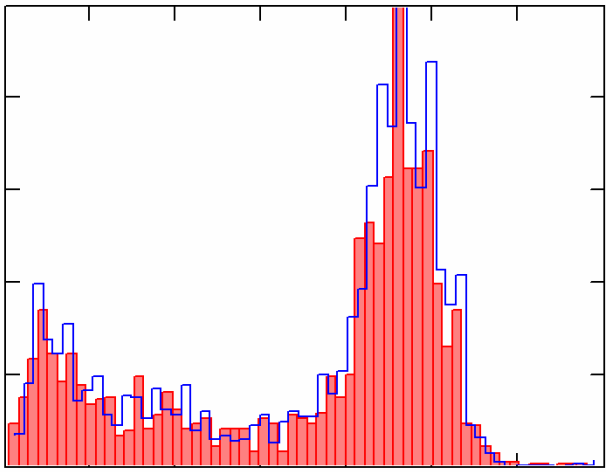


Multichannel biparametric spectra



CZT detectors – individual planar detectors vs. pixels

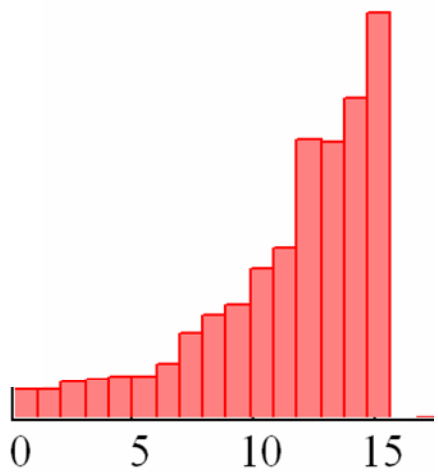
Energy



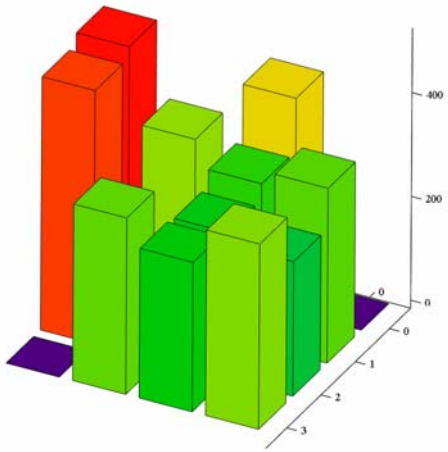
16 single planar det.

11 pixels

Counts vs. channel



16 single planar det.



11 pixels

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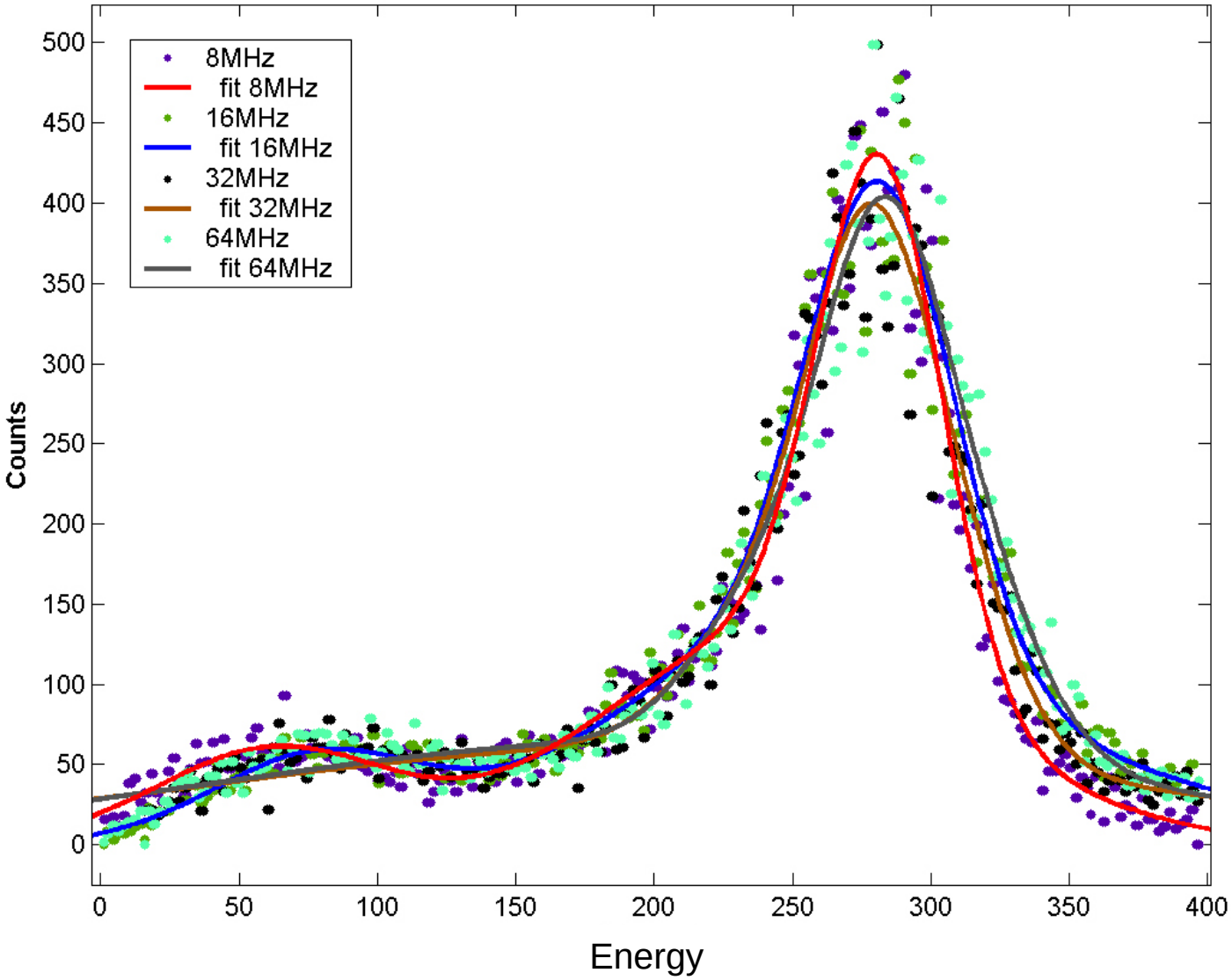
^{241}Am spectra for different RR rates



- 32 CZT sensors illuminated by ^{241}Am source
- Overall rate ~ 8MHz
- Shaper peaking time 600ns
- Rate of read request varied from 8 MHz to 64 MHz
- No peak shift or FWHM degradation seen
- Settling time of output mux ~ 10ns

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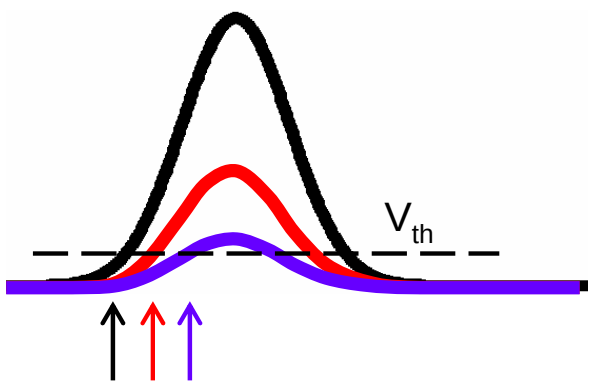
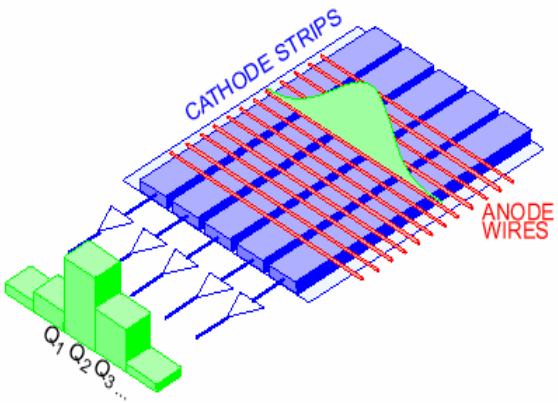
Simultaneous Events

Charge-shared events (e.g. pad and strip MWPCs)

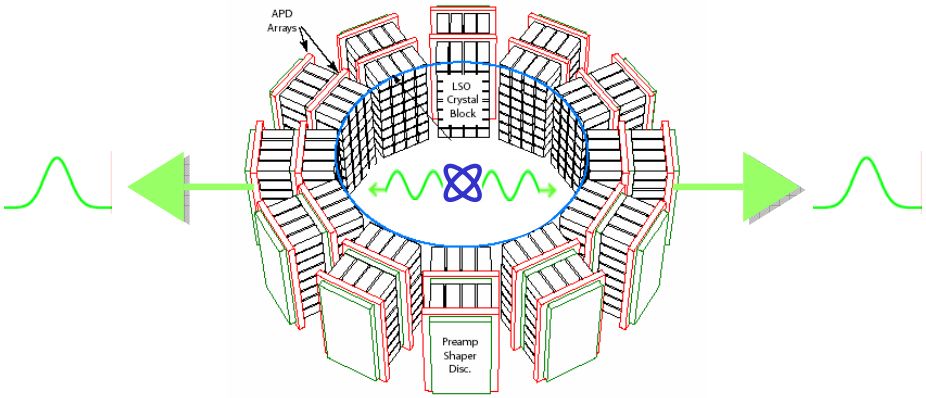
- occur in neighboring channels
- different amplitude (typically)
- more than 2 channels (often)



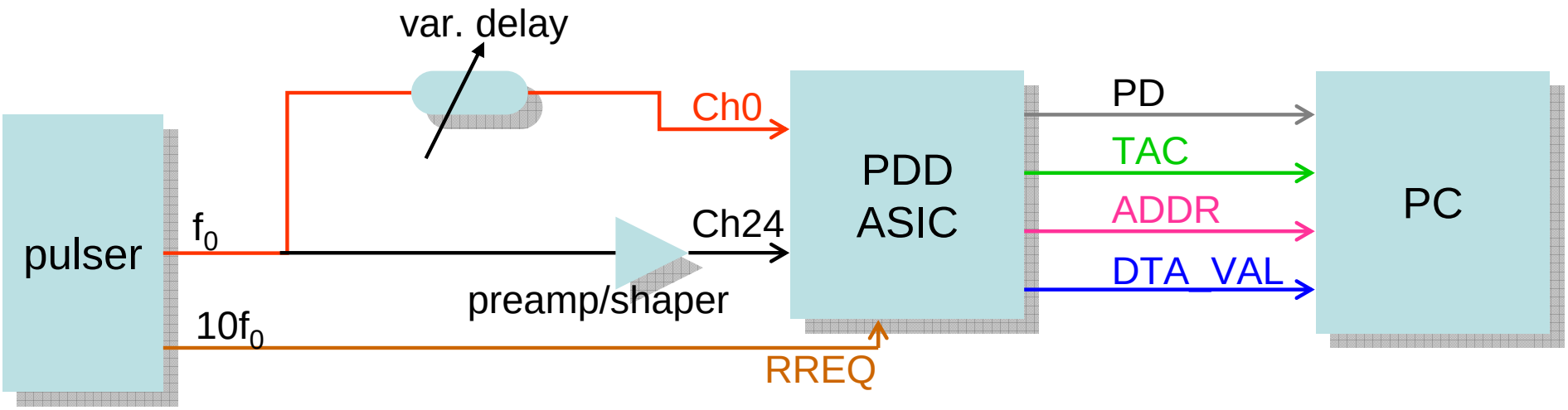


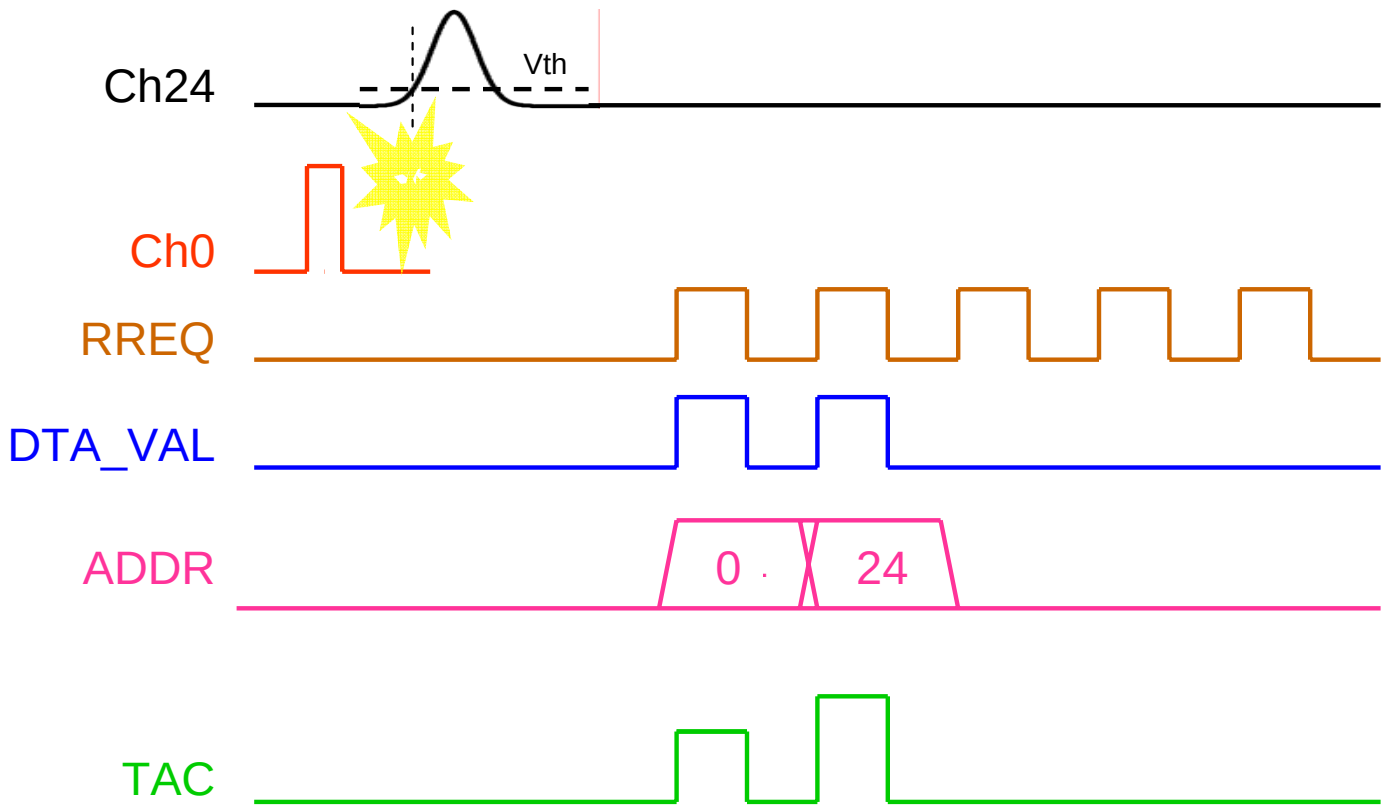
Coincident detection (e.g. PET)

- similar amplitudes
- typically only two channels
- usually non-neighboring



Measuring arbitration speed and efficiency





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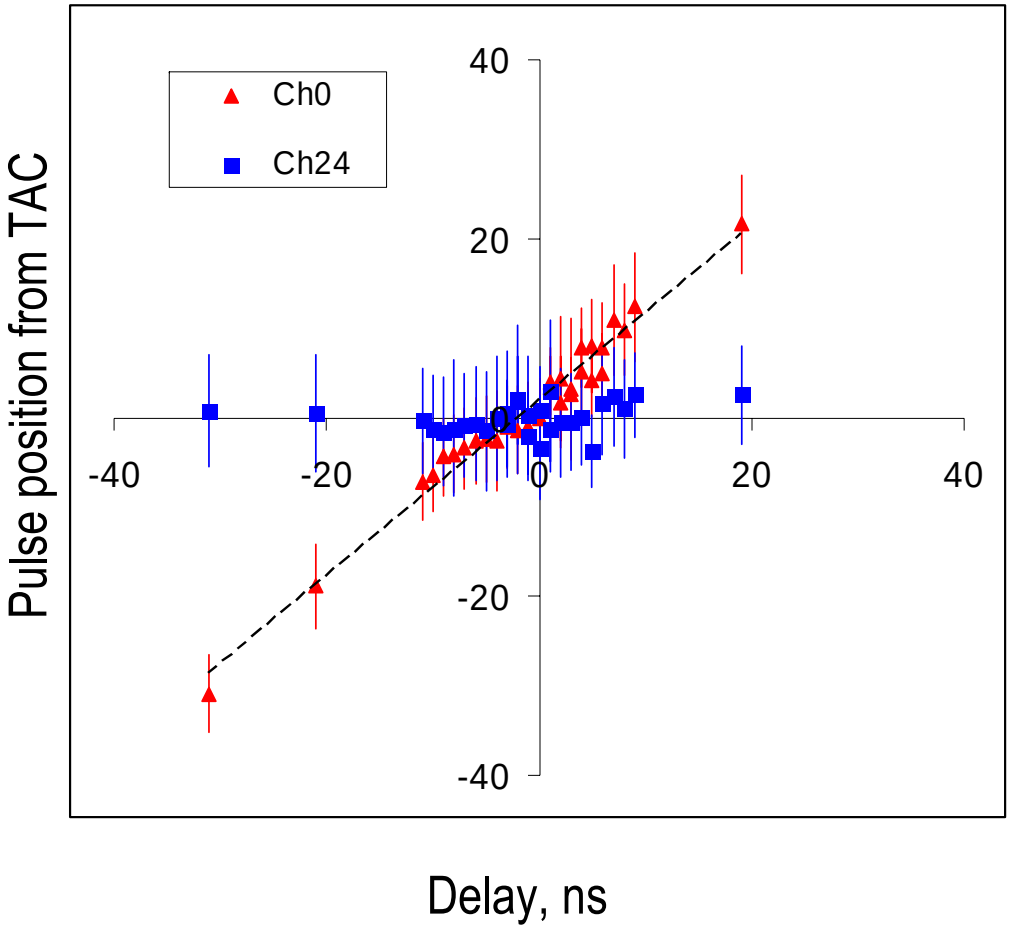

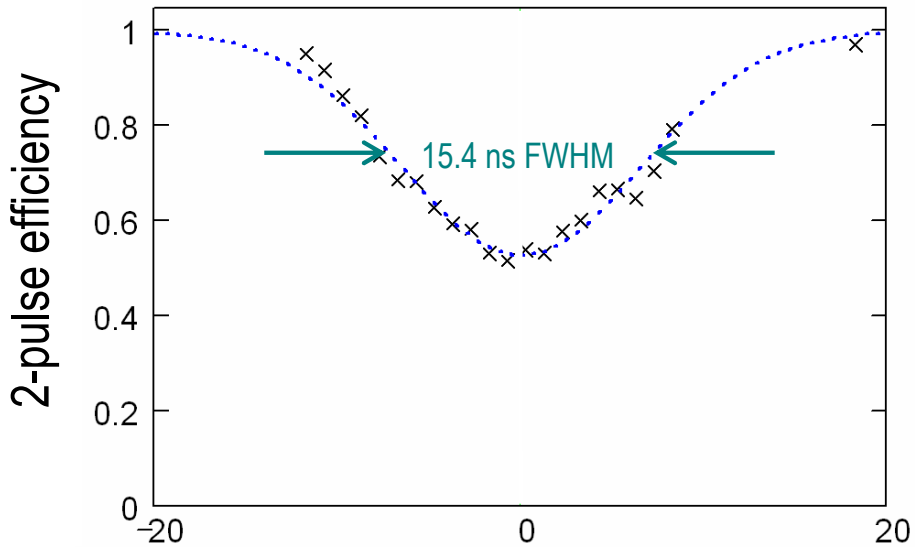

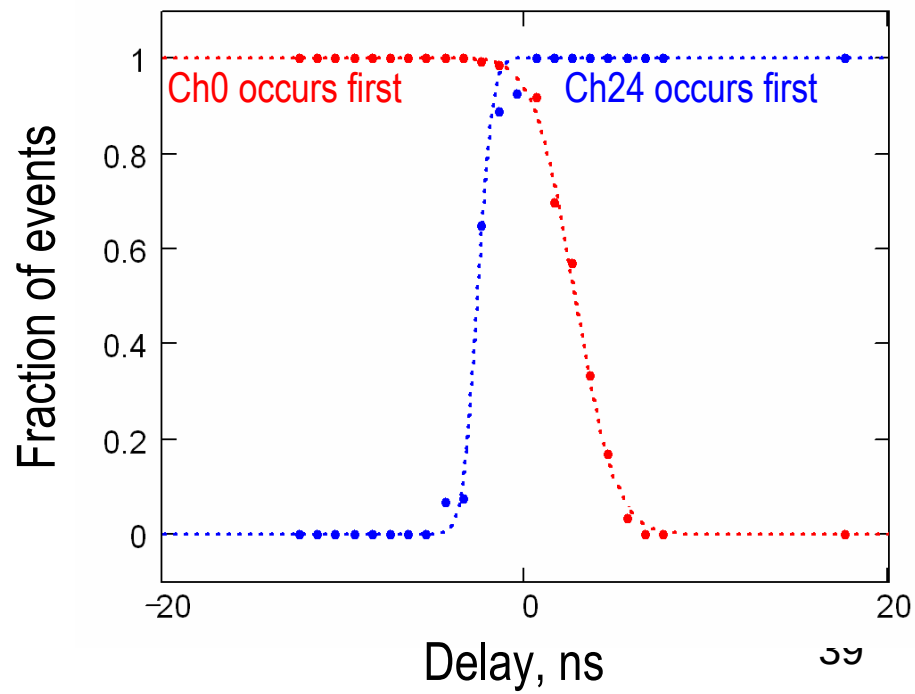

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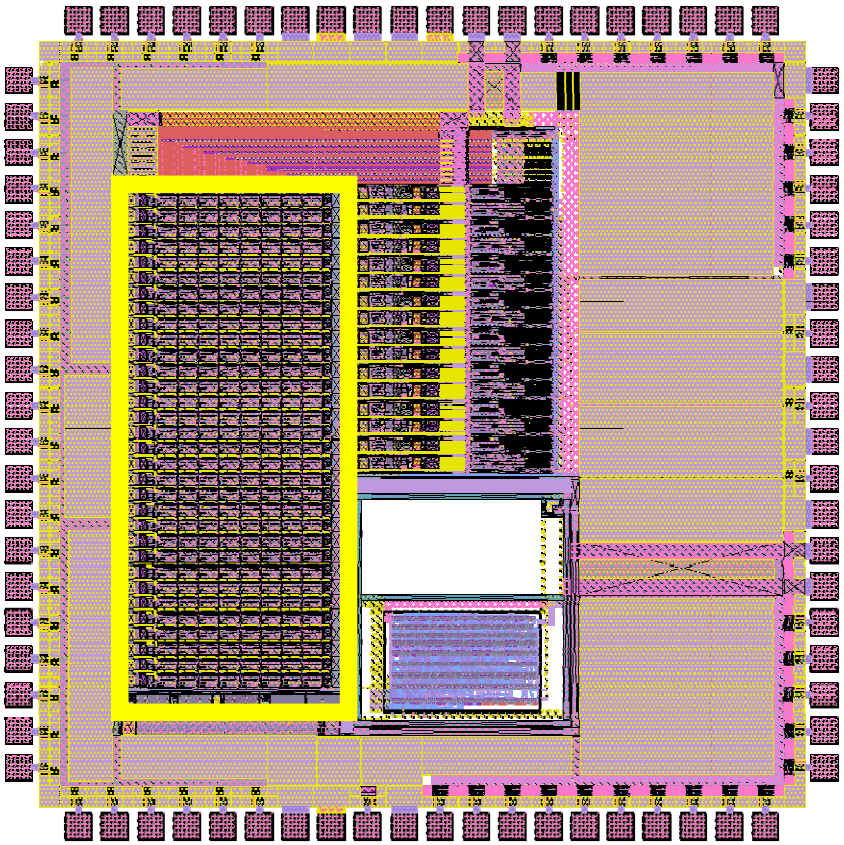
New version of chip to be fabricated summer 2005

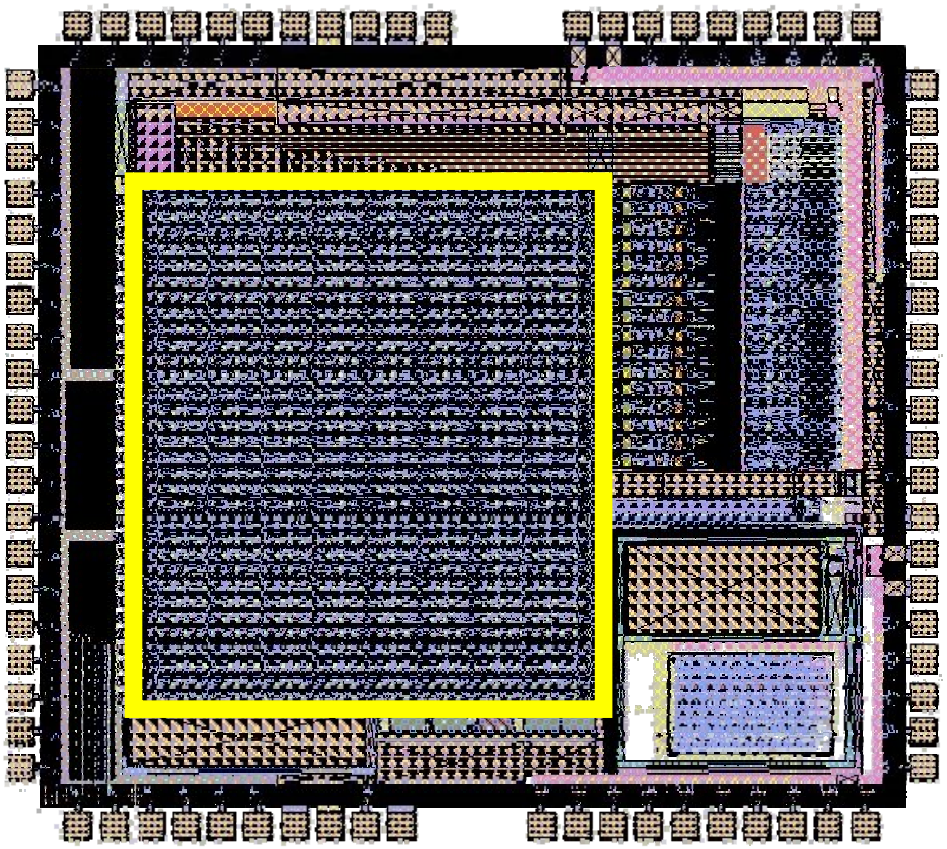
- Two new timing modes:
  - Time-over-threshold
    - *Pileup rejection for spectroscopy*
  - Peak-to-threshold (fall time)
- Simultaneous capture capability
  - Matrix cell logic replaces “row inhibit” with local re-trigger of next available column switch
    - *ambiguity window reduced to 50 ps (simulated)*
    - *Split event capture*
    - *Coincidence detection*
- Reduced dispersion of time detector slopes
  - Improved matching of ramp generators layout
  - Current averaging technique

Old and new die layouts

old matrix



new matrix



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Existing system based on National Instruments PCI-6115

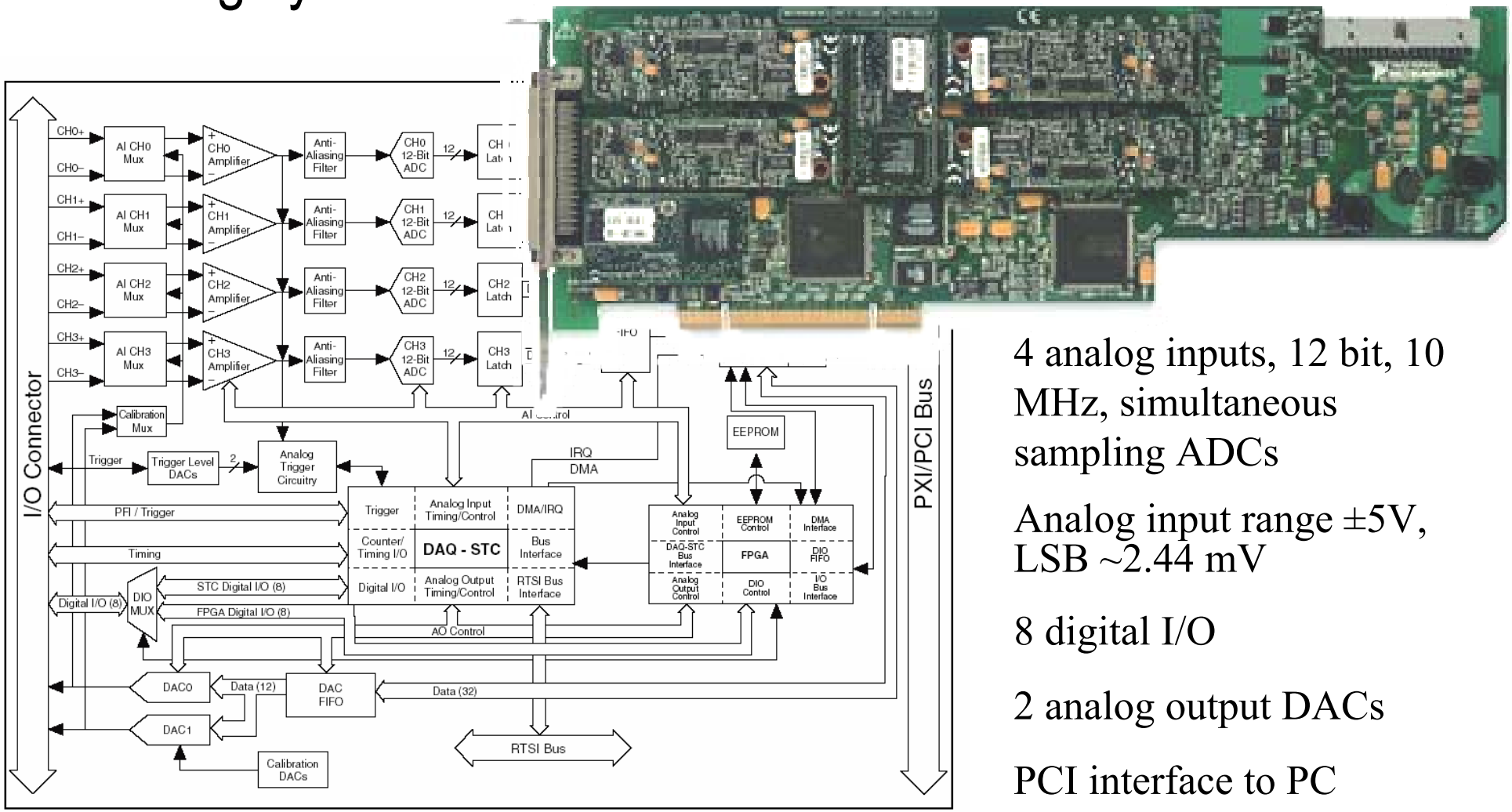


Figure 3-1. NI 6115 Block Diagram

4 analog inputs, 12 bit, 10 MHz, simultaneous sampling ADCs

Analog input range ±5V, LSB ~2.44 mV

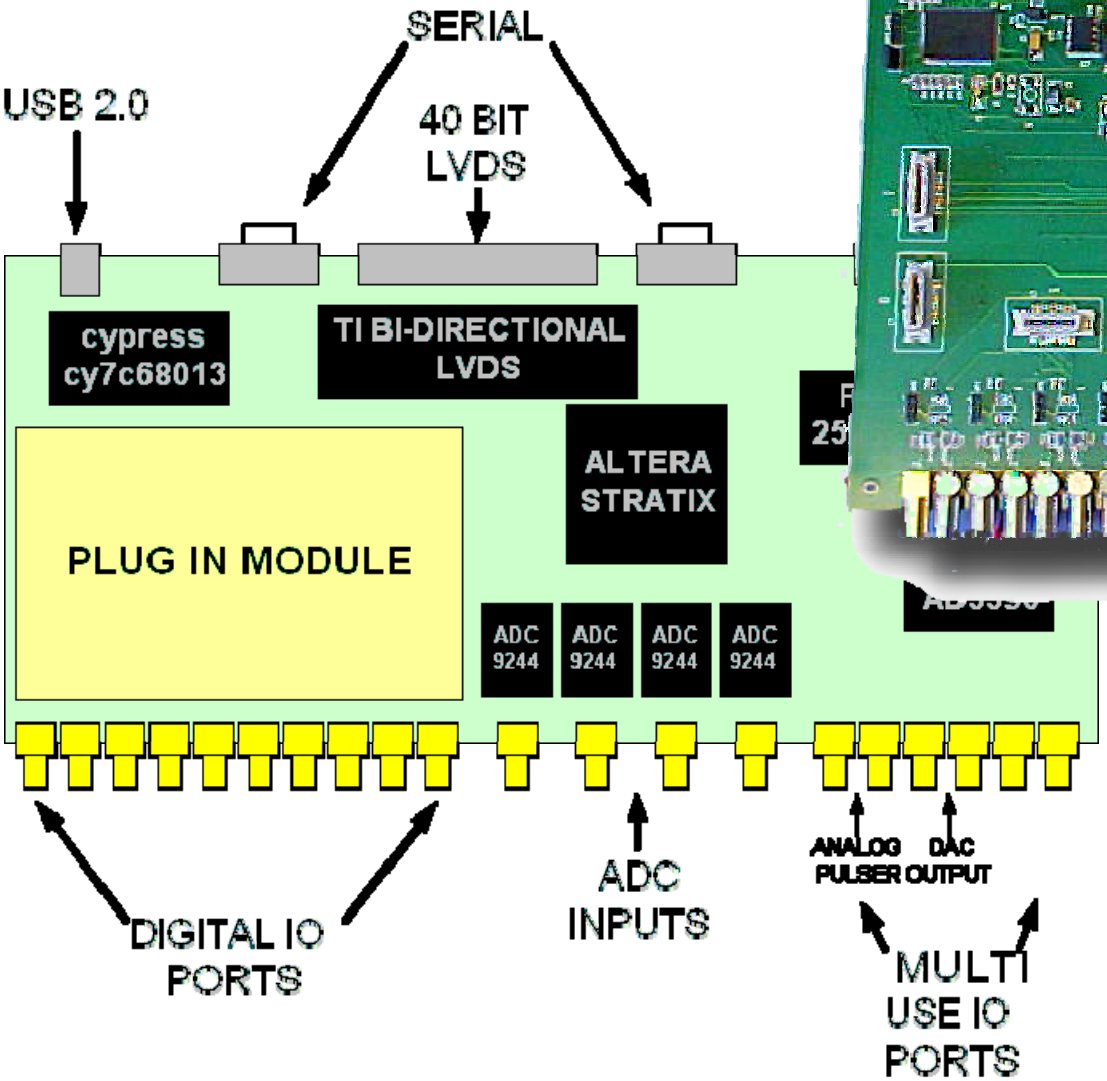
8 digital I/O

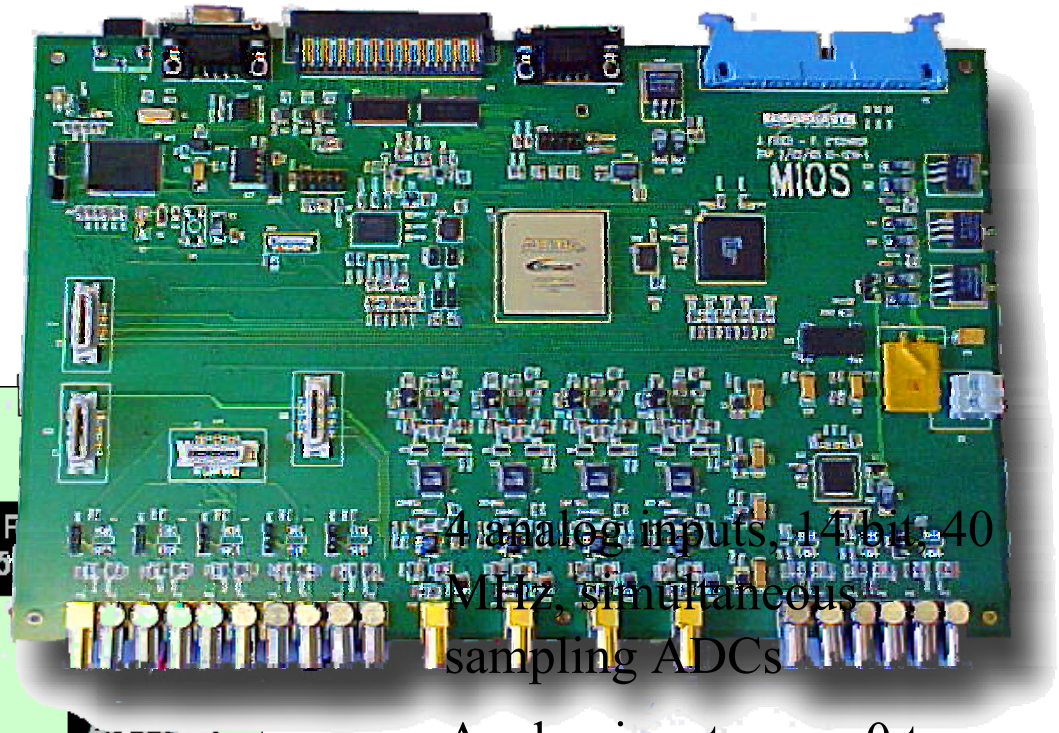
2 analog output DACs

PCI interface to PC

Effective data transfer rate to PC ~ 15Hz

MIOS board





4 analog inputs, 14 bit, 40 MHz, simultaneous sampling ADCs

Analog input range 0 to 3.3V, LSB ~200 µV

20 digital I/O

8 analog output DACs

USB + LVDS interface to PC

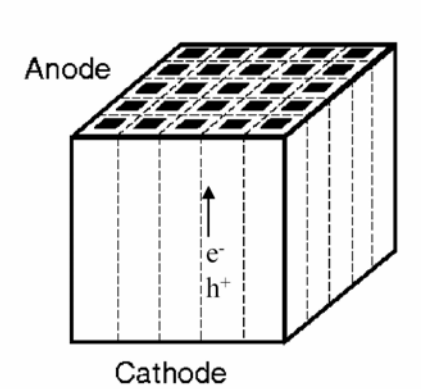
Projected data transfer rate to PC ≥ 10MHz

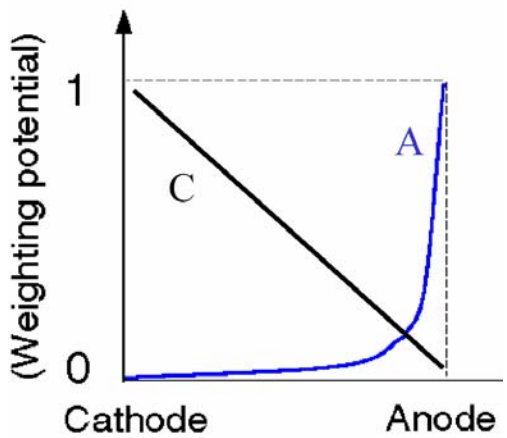
OUTLINE

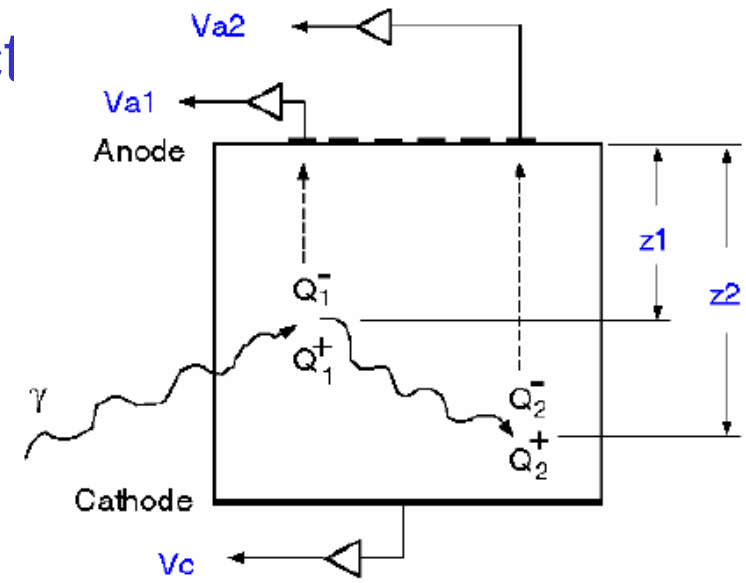
- **Architecture**
- Test set
- Spectroscopy performance
- High rate performance
- Simultaneous event handling
- New PDD version IC87
- New data acquisition MIOS
- **Future applications**

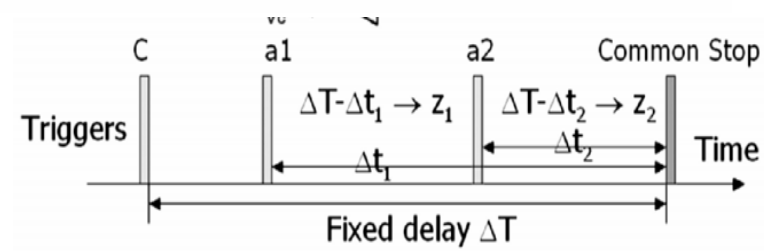
Planned future applications

- X-ray fluorescence with pileup rejection using silicon pad detectors
- Interpolating pad and strip detectors
- Split event reconstruction in pad/pixel detectors
- Coincidence timing for compact
- "3D" CZT pixel detectors

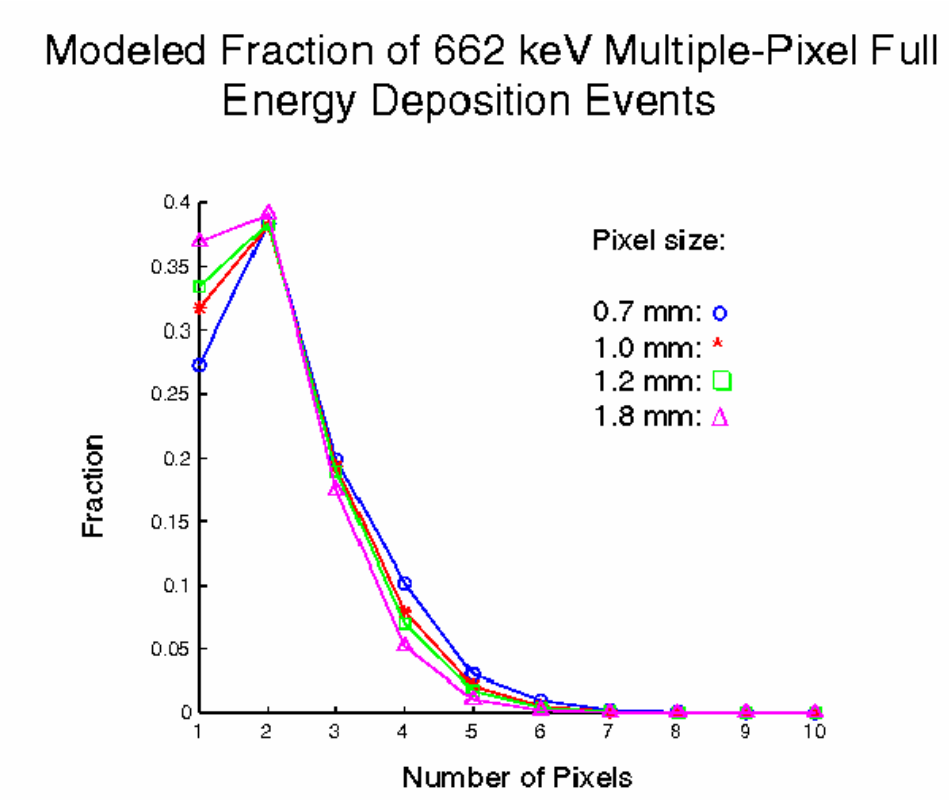


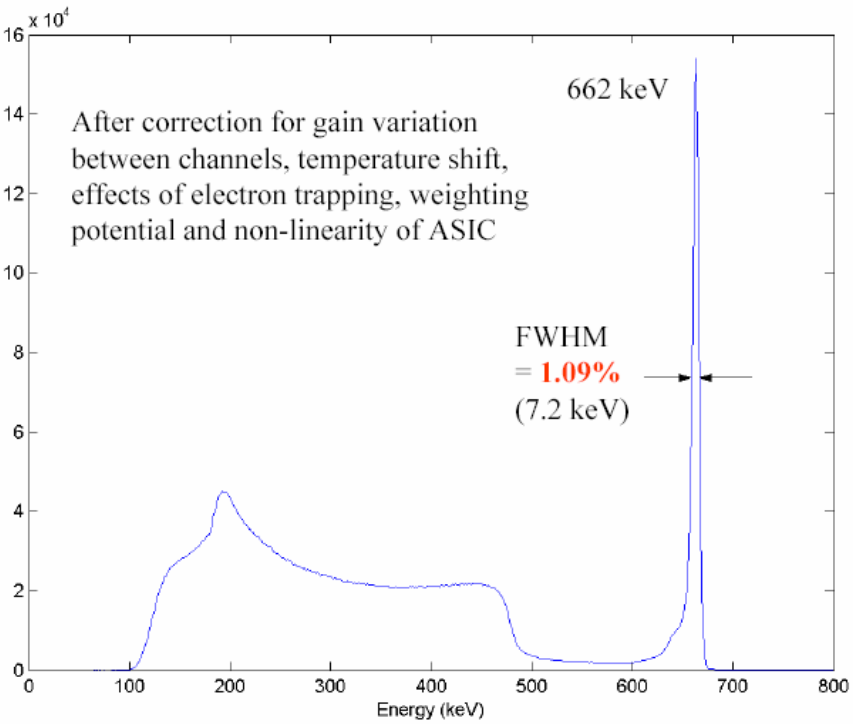


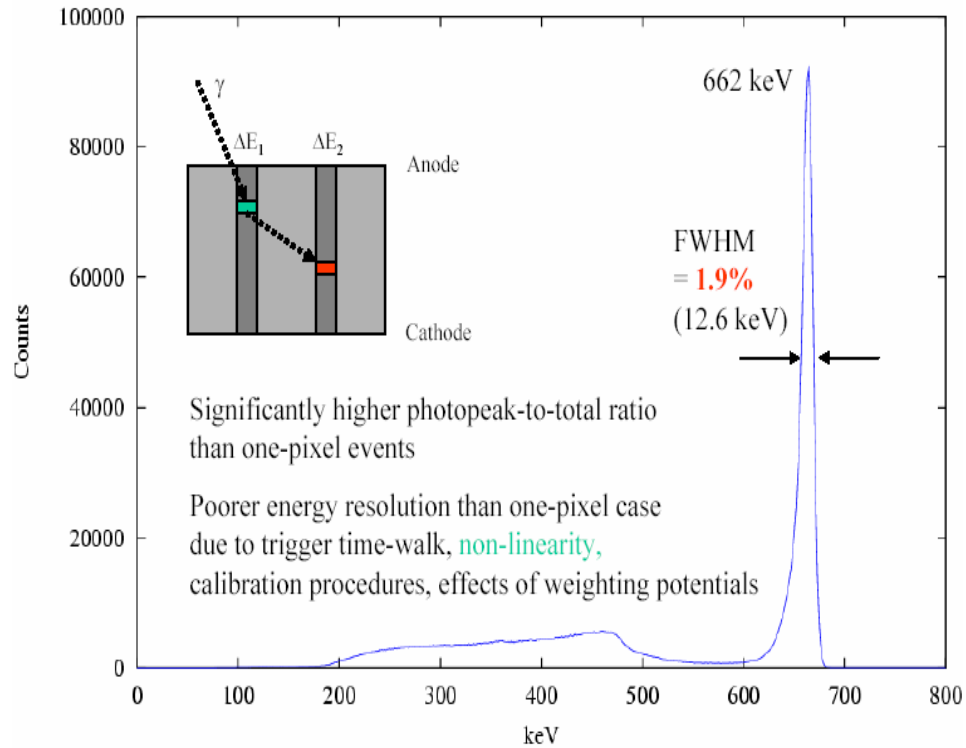


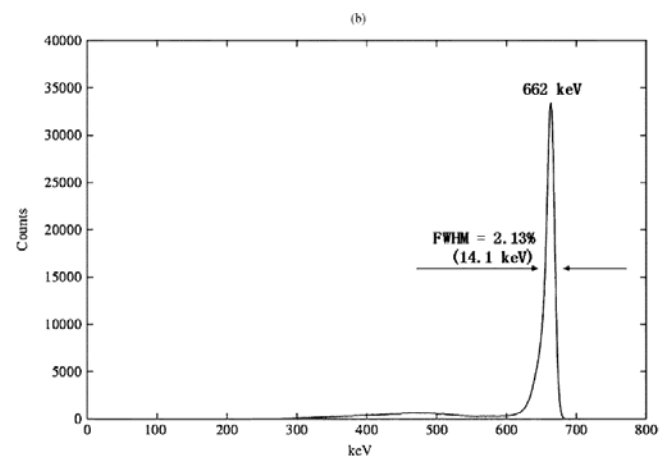


- anode pixels give single-carrier response
- pixel-by-pixel calibration maps electron trapping vs. depth of interaction to derive correction
- reconstruct multiple-interaction events


Modeled Fraction of 662 keV Multiple-Pixel Full Energy Deposition Events
Pixel size:
0.7 mm:
1.0 mm:
1.2 mm:
1.8 mm:
Fraction
Number of Pixels
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
1
2
3
4
5
6
7
8
9
10







Zhong He, FengZhang, Carolyn Lehner, Dan Xu,Glenn F. Knoll, David K. Wehe
3-DPosition-Sensitive CdZnTe γ-Ray Spectrometers