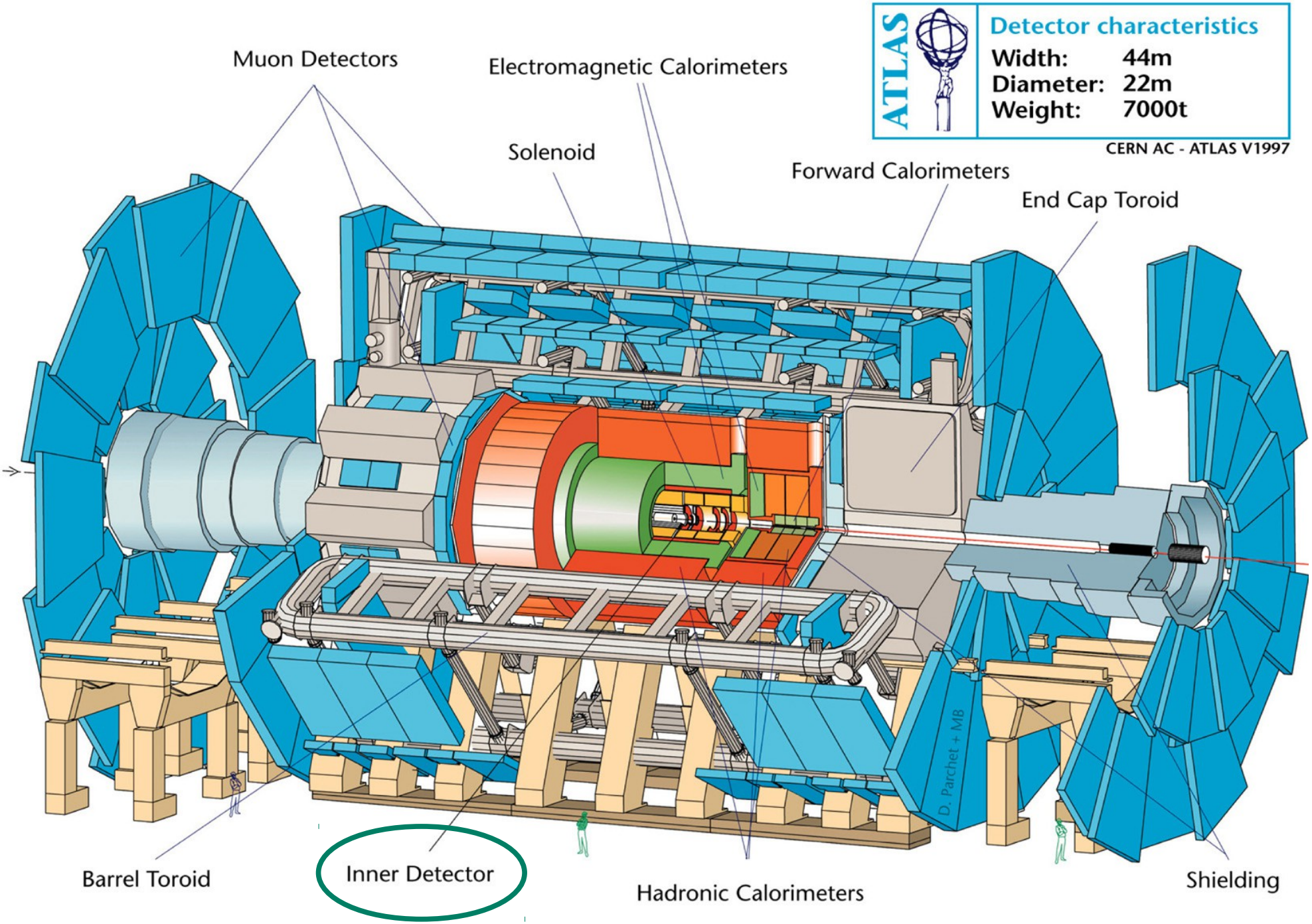
Novel CMOS-based sensors for the ATLAS Inner Tracker upgrade

Daniel Muenstermann

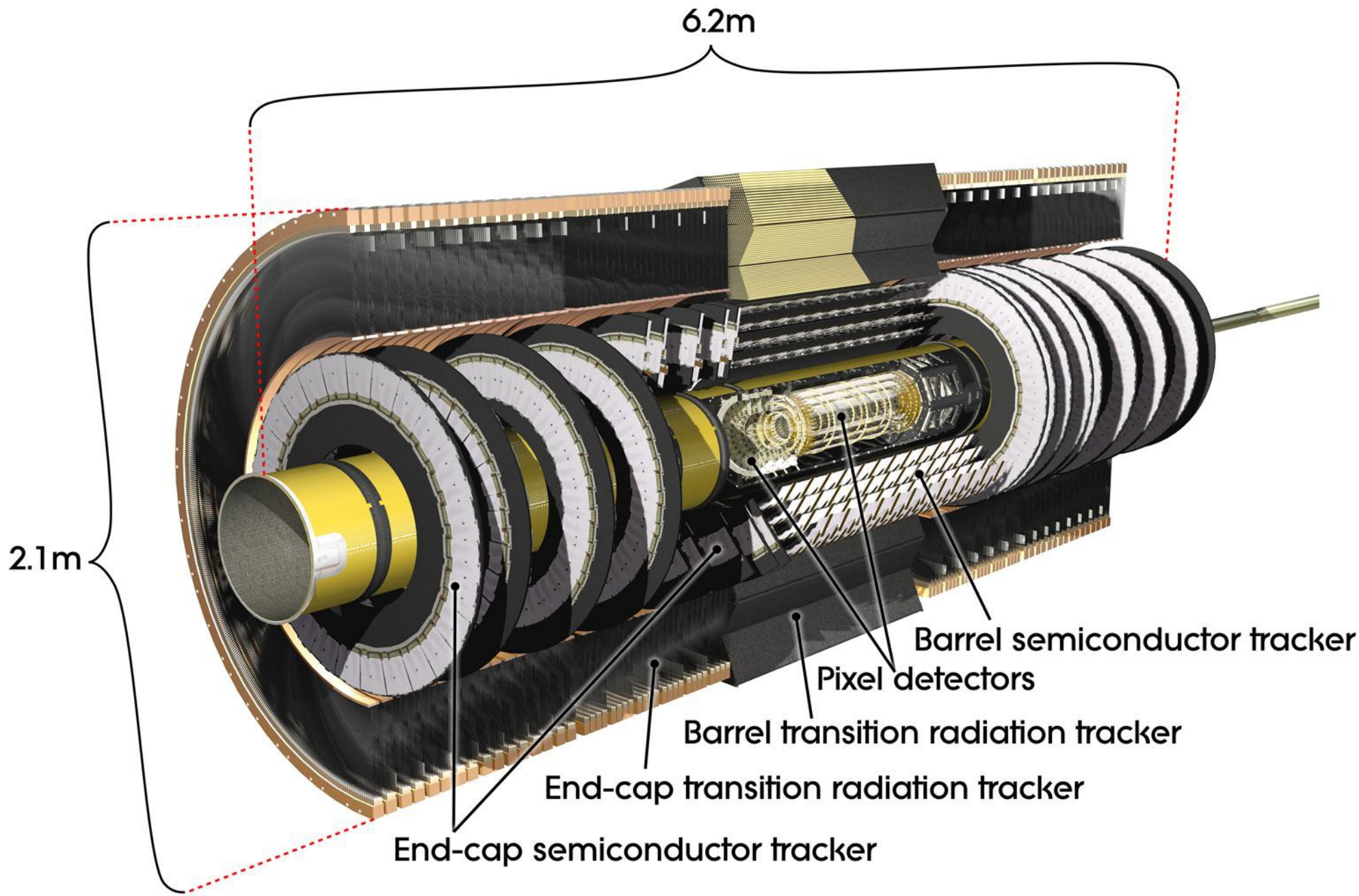
with many plots and drawings from ATLAS collaborators

ATLAS Inner Tracker ?

ATLAS: A multi-purpose particle detector at LHC

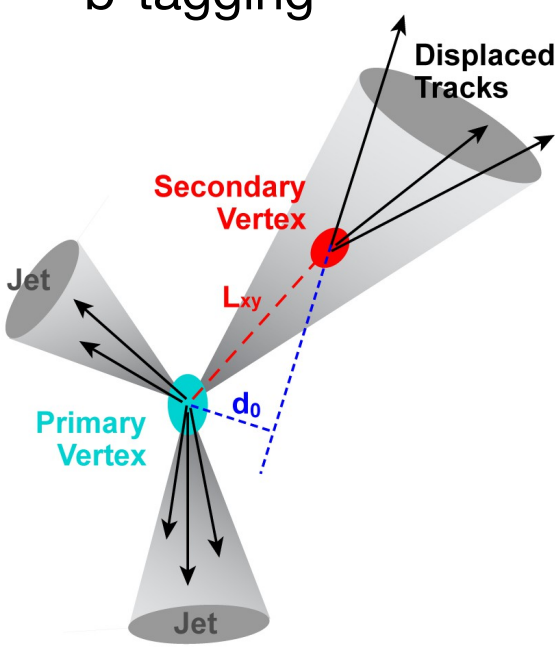


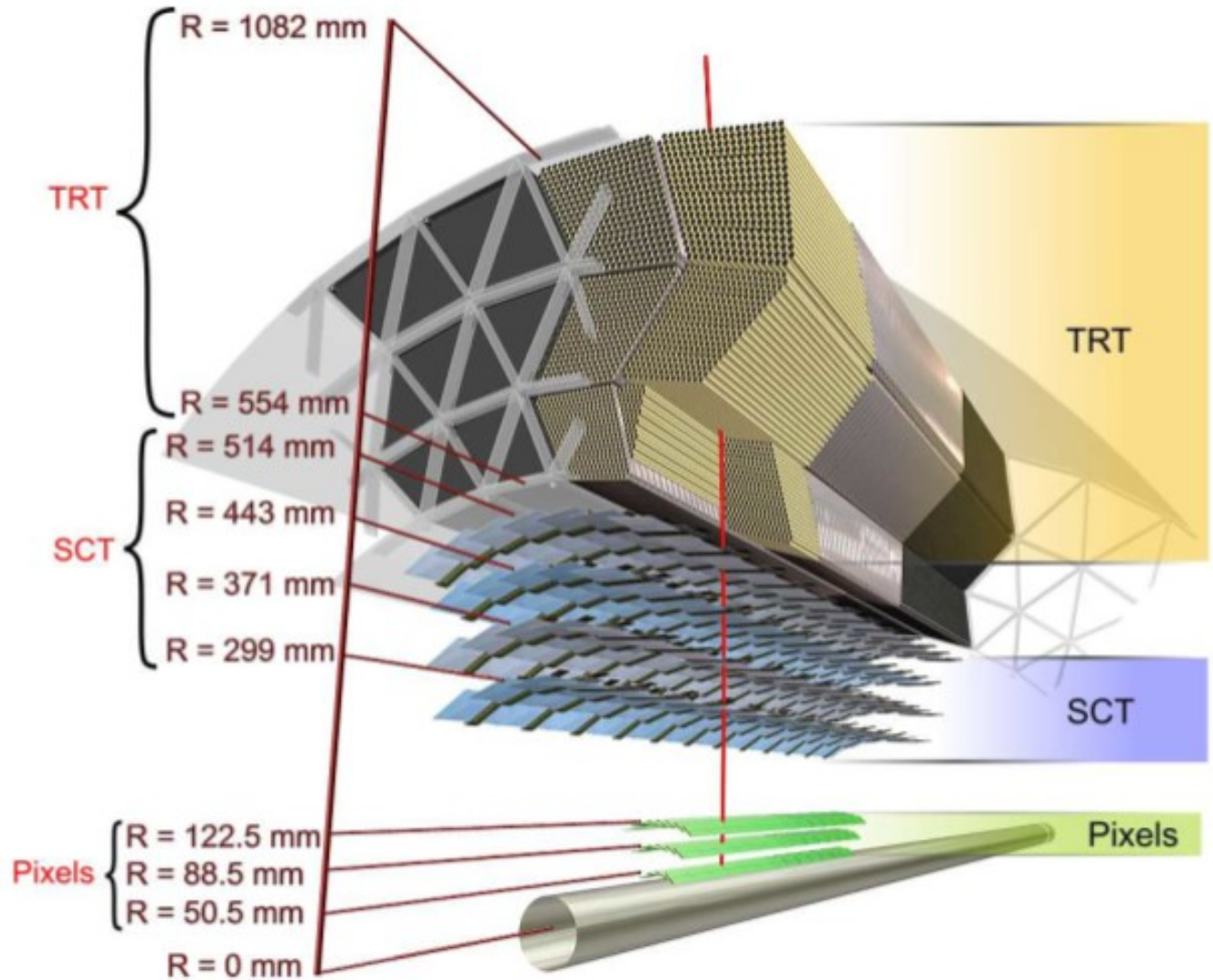
The current ATLAS Inner Tracker...



The current ATLAS Inner Tracker...

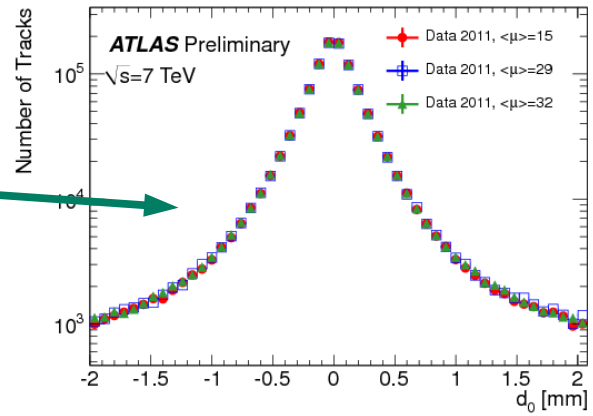
- The ATLAS inner tracker consists of TRT, SCT and Pixel
  - TRT: straw tube (gas) detector
  - SCT: silicon strips
    - 80 μm pitch
  - Pixel: silicon pixels
    - 50 μm pitch
- Tasks
  - pT-measurement
  - pile-up disentangling
  - b-tagging

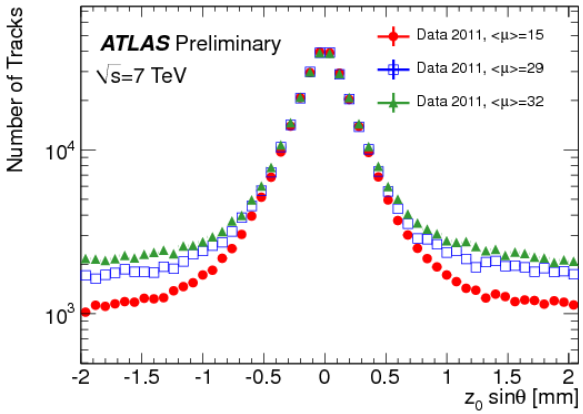


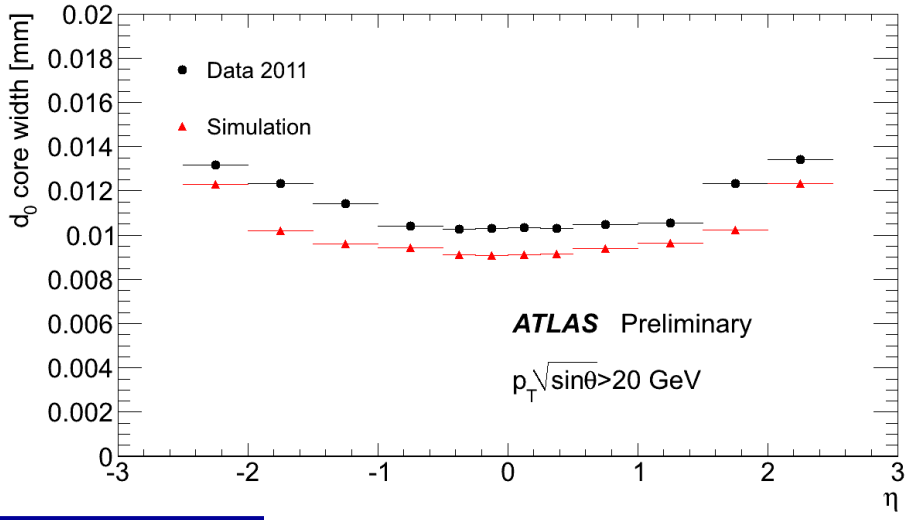


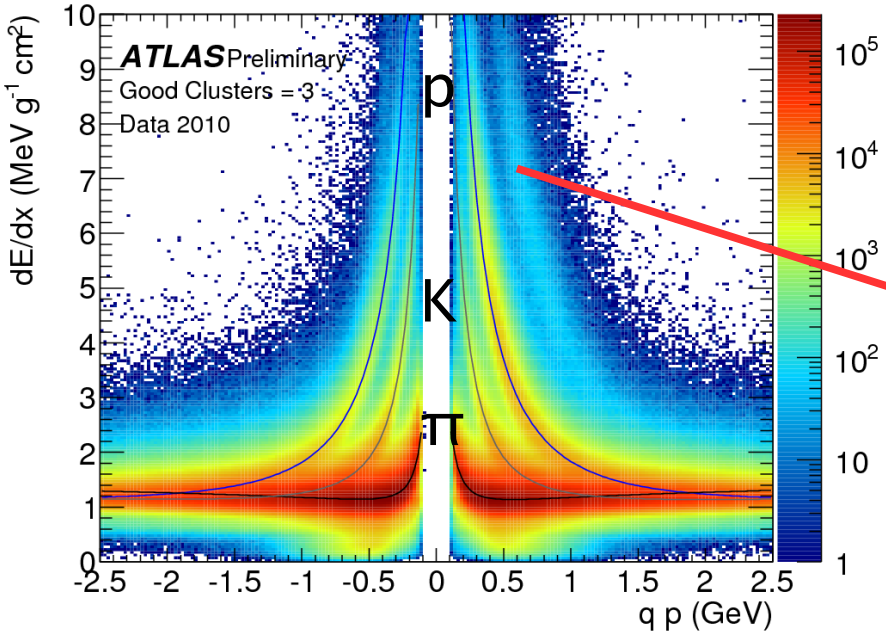
And how does it perform?

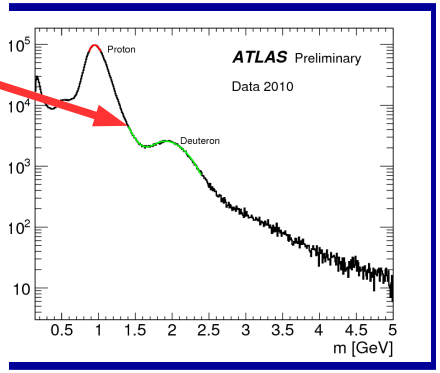
- Working smoothly, even at pile-ups not anticipated (50ns BC scheme)
- Impact parameter resolution down to ~10 μm for high-pT tracks!
- Nice: dE/dx shows several particle flavours → particle ID/discrimination

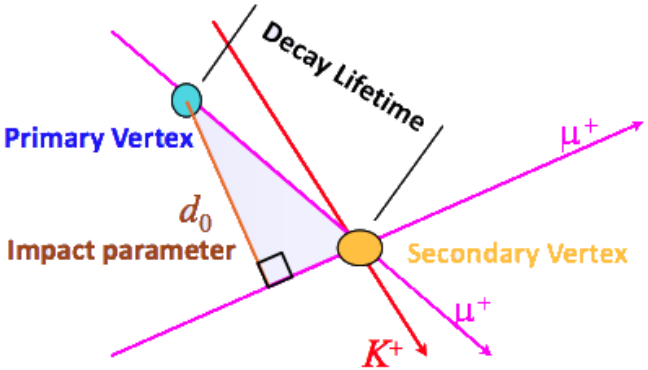










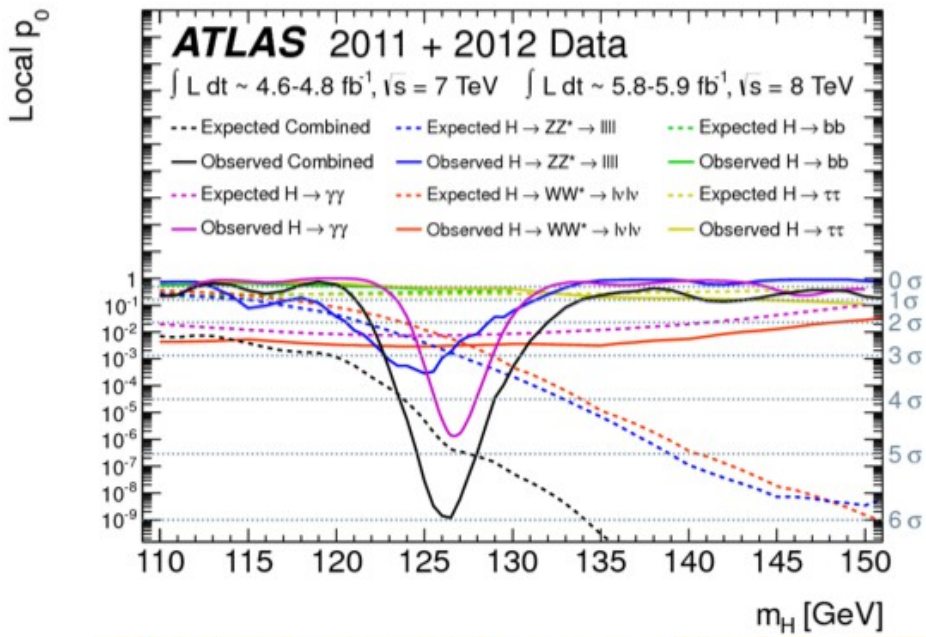


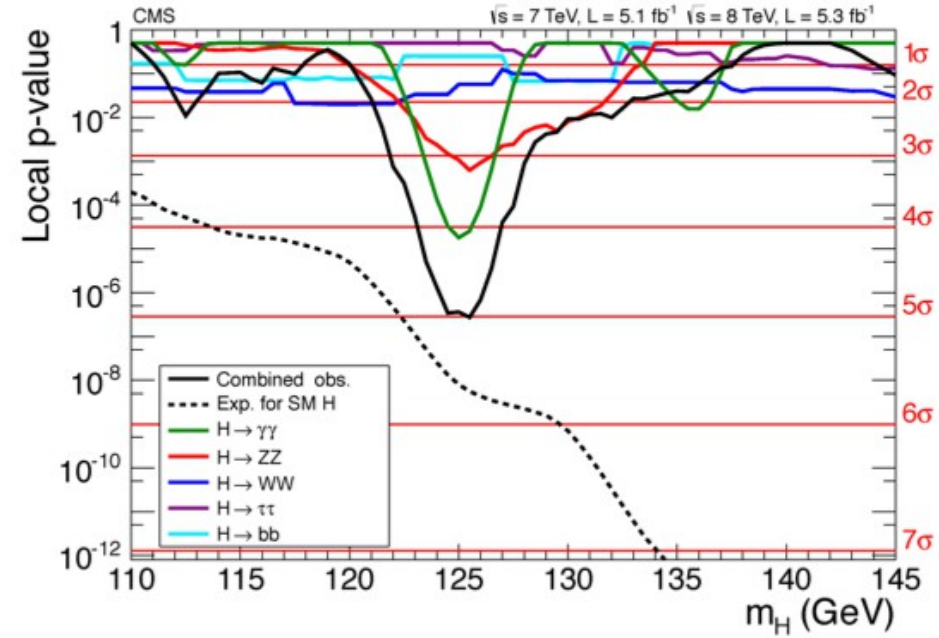
CMOS-based sensors

Works great, ok – and now? New physics?

Works great, ok – and now? New physics?

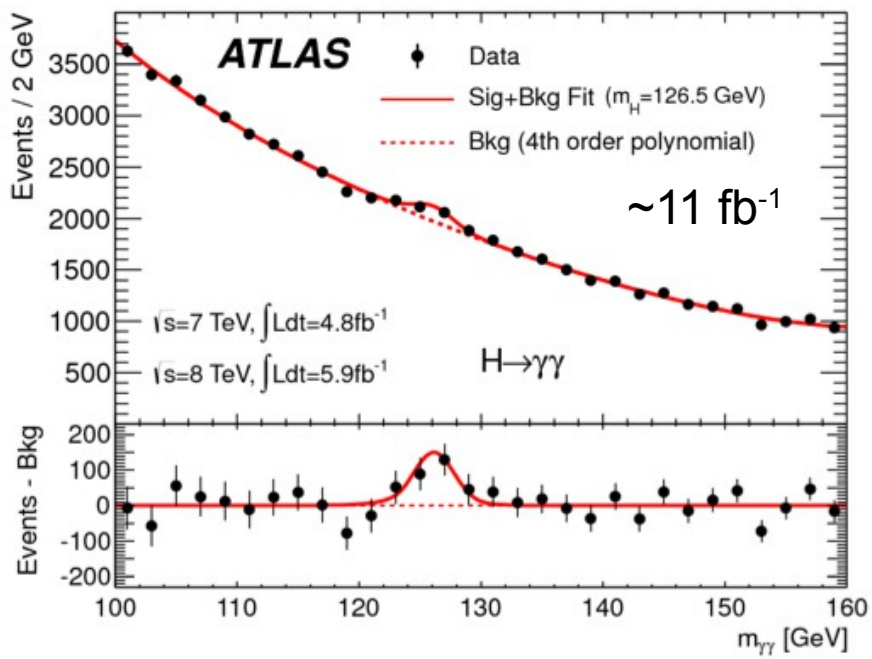
- July 4th, 2012, saw the most eagerly awaited particle discovery of all times – a new boson compatible with the standard model Higgs

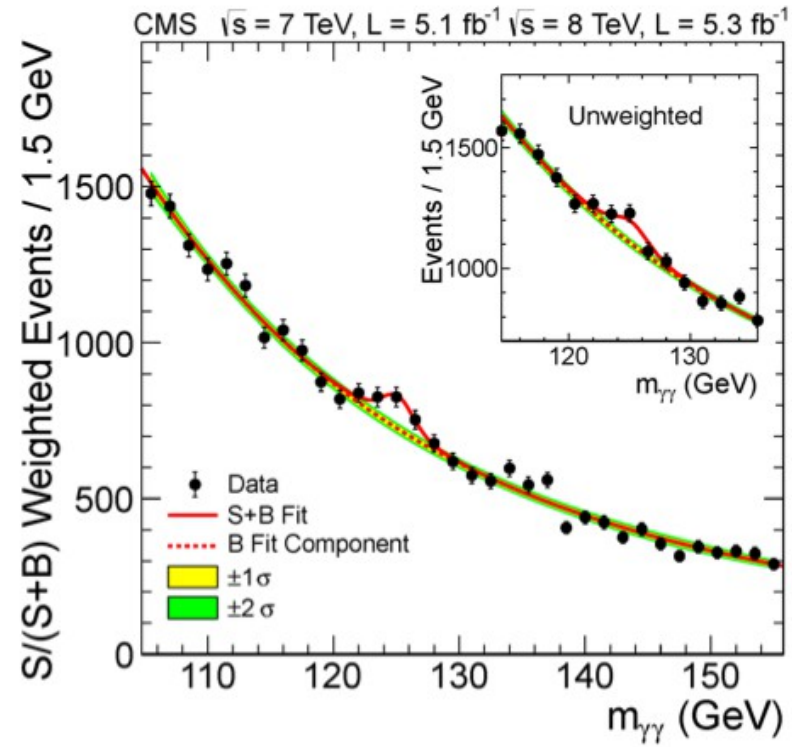




Stop now? Or continue? How?

- So all is good. Is it? What did we see? What do we know? Let's have a look at the data:
  - γγ:

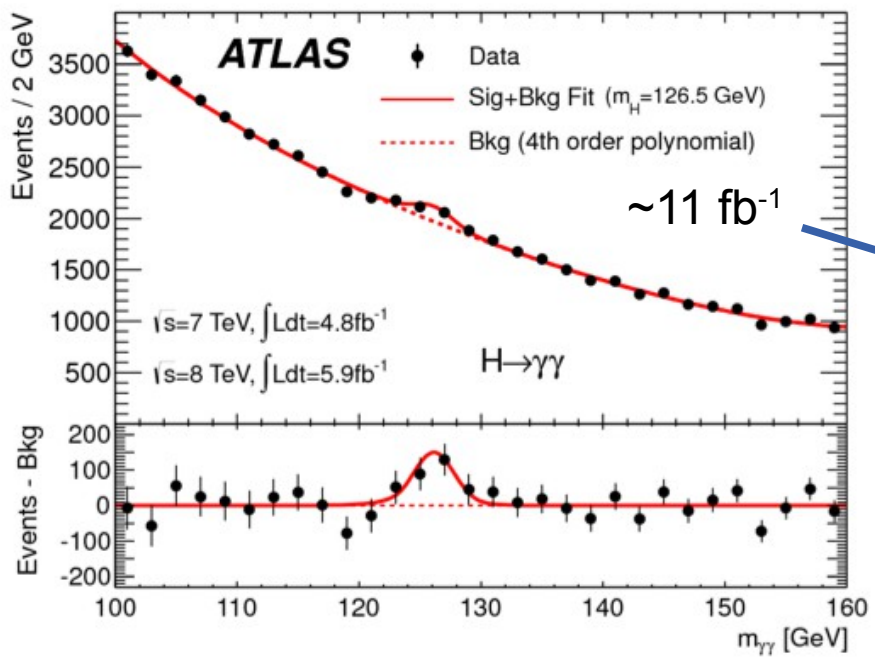


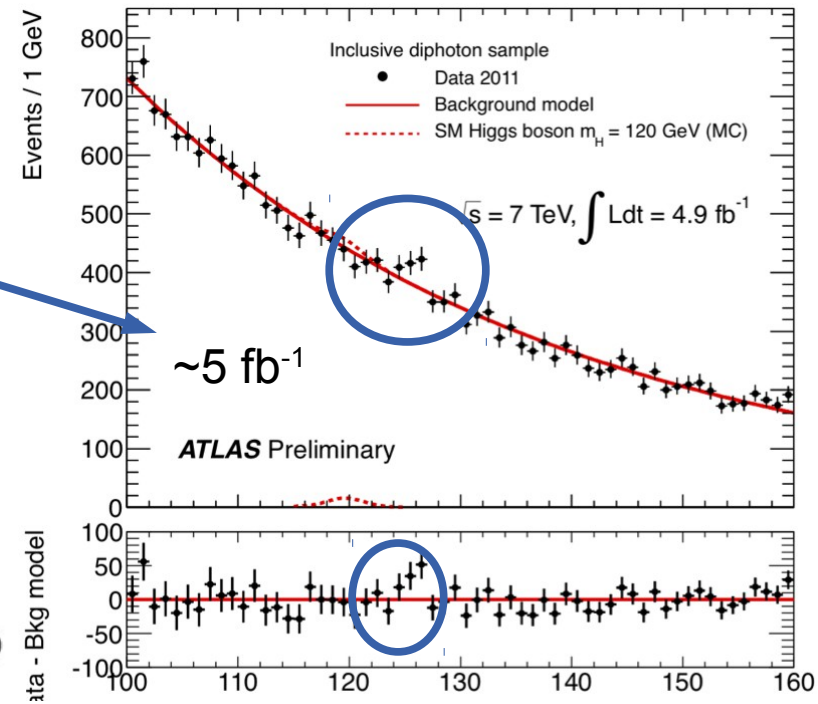


  - not too bad, signal clearly visible on background
    - but how did it look with less statistics?

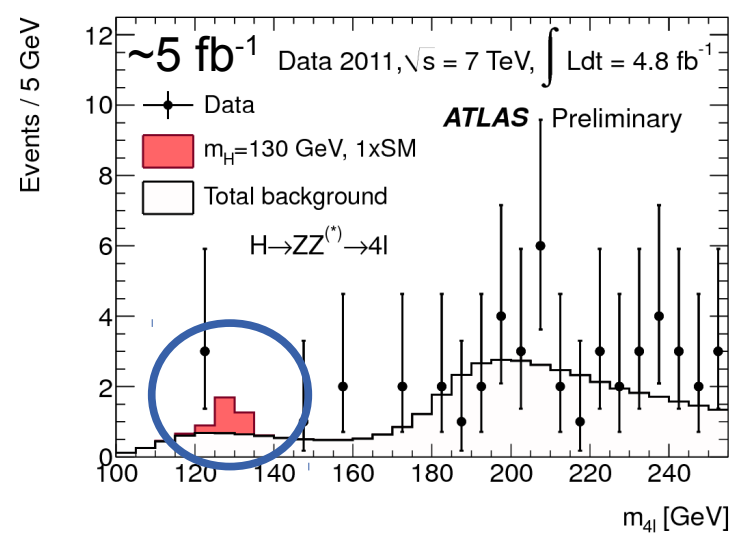
Stop now? Or continue? How?

- So all is good. Is it? What did we see? What do we know? Let's have a look at the data:
  - γγ:

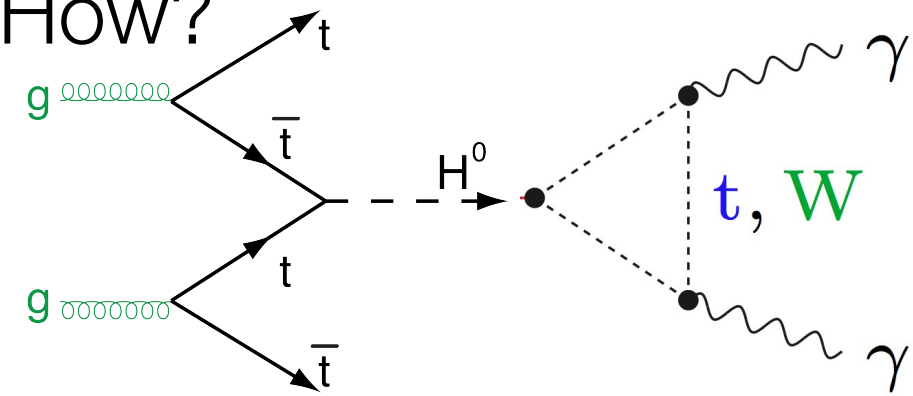




- lesson to learn: statistics helps
  - how much is necessary?
- What high-statistics channels and why?
  - Vector Boson Scattering
    - really a SM Higgs? Resonances?
  - Higgs self-coupling
    - unique measurement, hard and rare

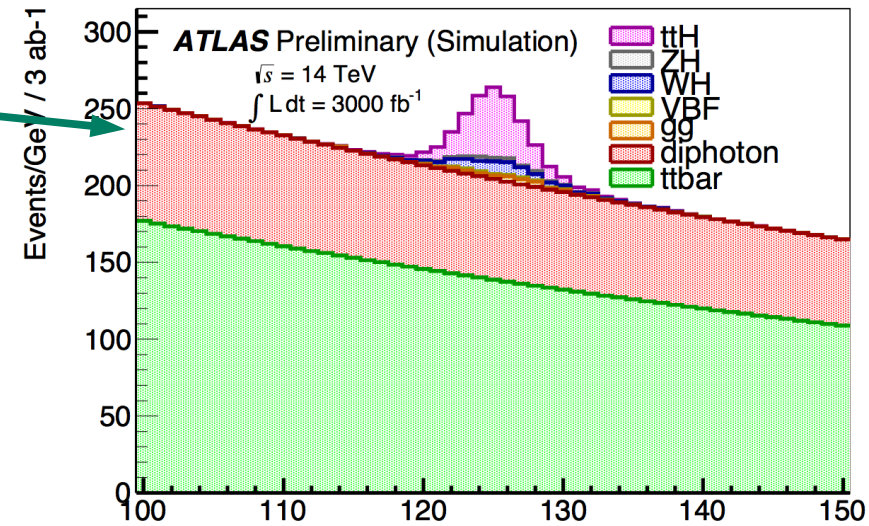


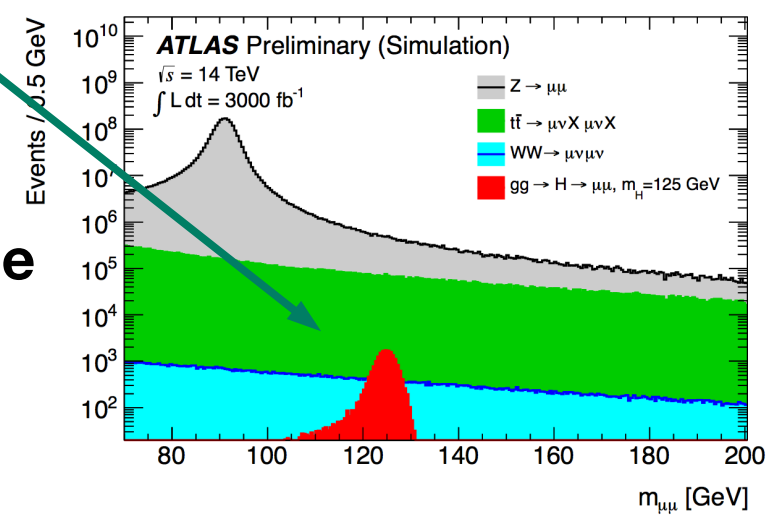
Stop now? Or continue? How?



More demanding Higgs channels:

- ttH → γγ
  - really difficult
  - enables to directly measure the top's Yukawa coupling
  - possible with 3000fb^{-1}
- (inclusive) H → μμ
  - very rare, large background
  - "immune" to high pile-up
- ttH → μμ
  - extremely rare
  - better S/N
  - ~30 events after 3000fb^{-1} (!)

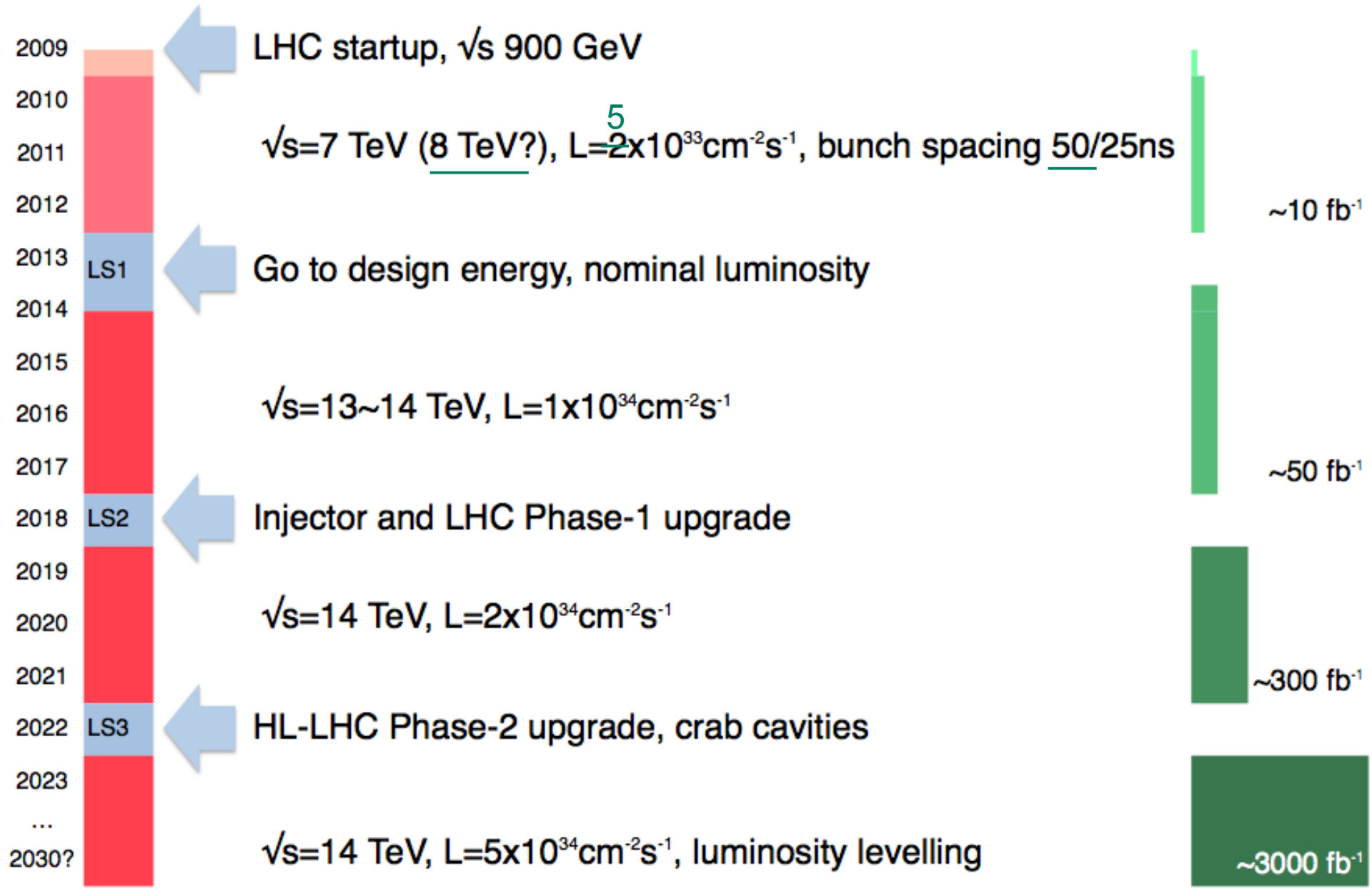




Many reasons to aim for a luminosity upgrade

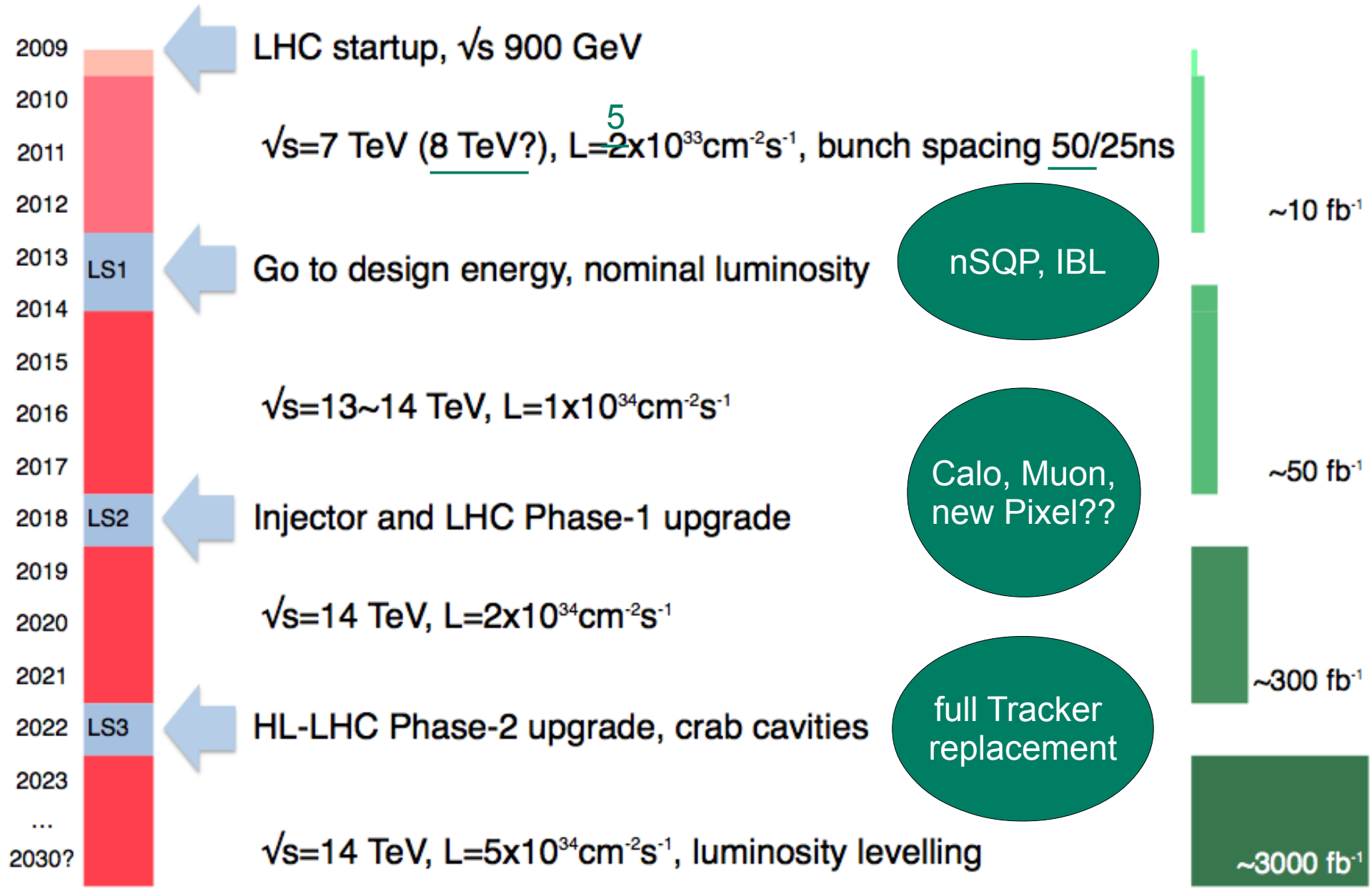
- LHC: some 100 fb^{-1}, HL-LHC: ~3000 fb^{-1}

Several upgrades: LHC draft plan



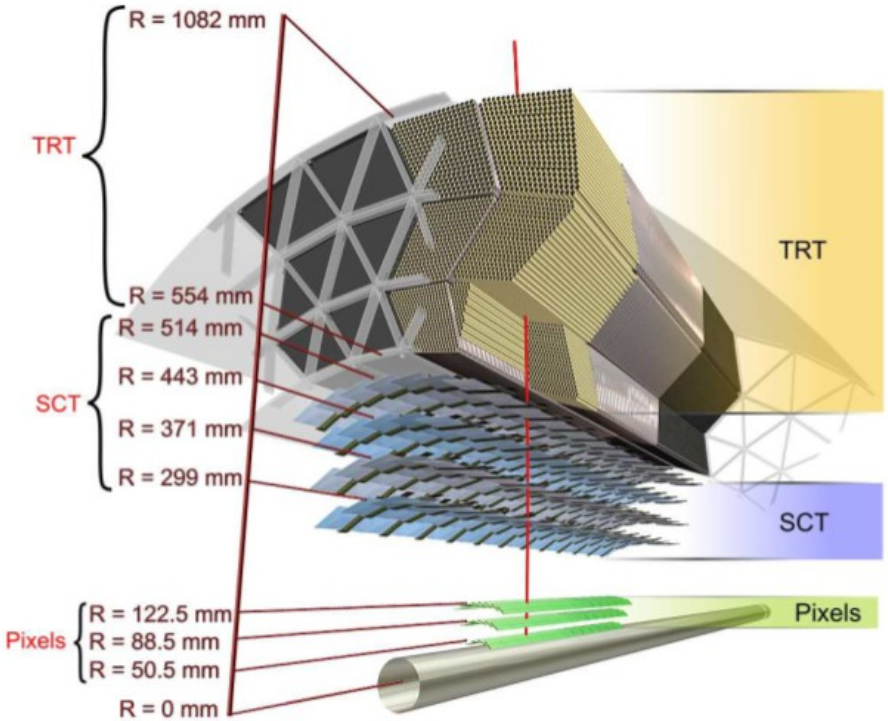
ATLAS Inner Tracker upgrade ?

Several upgrades: ATLAS draft plan



Phase 2: What to upgrade? How to upgrade?

- Main challenges:
  - occupancy
  - radiation damage
  - data rate/trigger rate
- Components needing upgrades:
  - TRT
    - occupancy-limited beyond about $2 \cdot 10^{34}$ cm^{-2} s^{-1} (40% occ.@ inner radii)
      → replace by all-silicon inner tracker

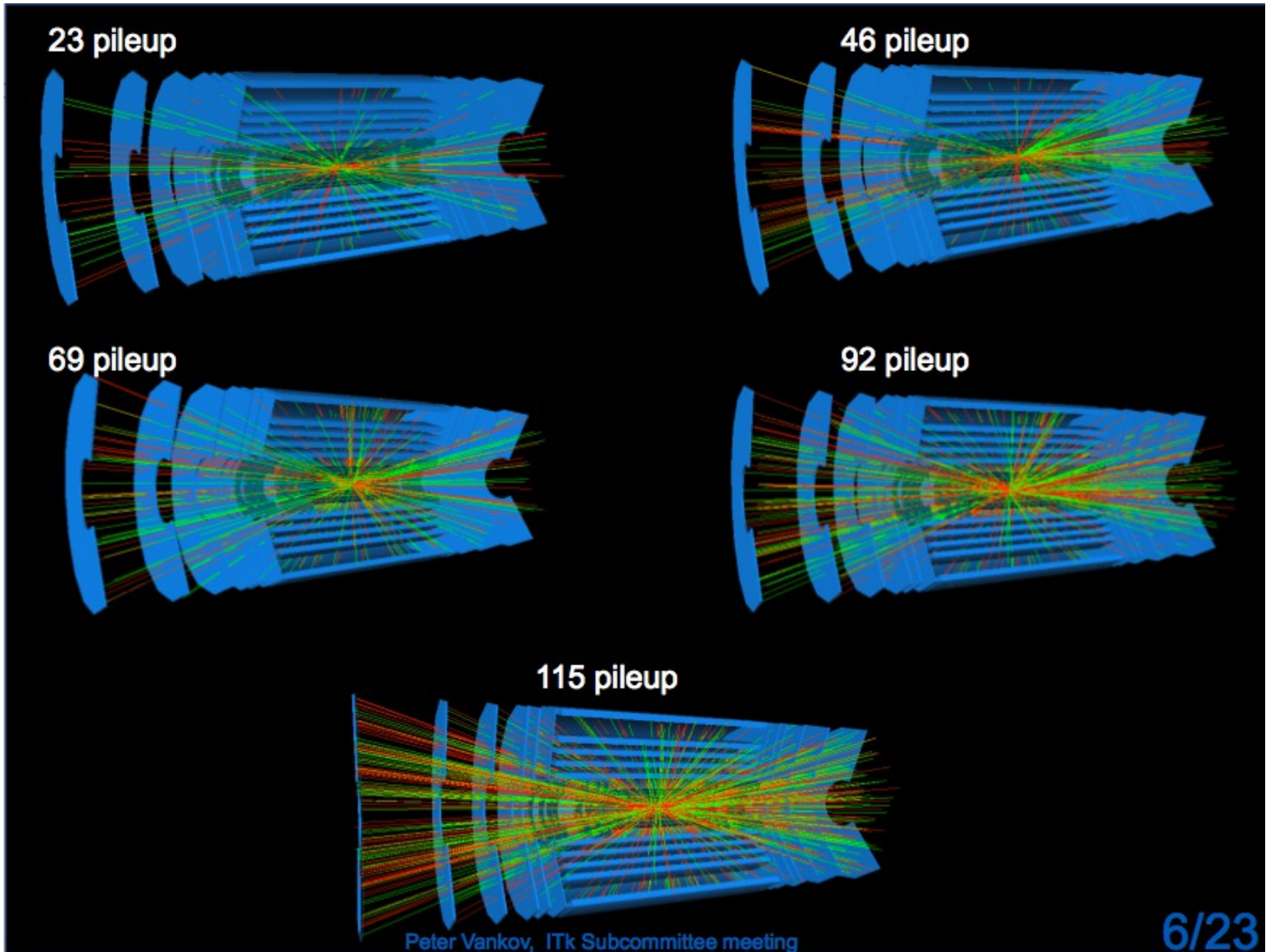


  - SCT
    - radiation damage limited (p-in-n sensors collect holes → n-in-p to collect e^-)
    - occupancy limited (long strips → replace inner layers by short strips)
    - self-seeded track trigger?
  - Pixel
    - radiation damage limited (?) for innermost layers → sensor R&D
    - data rate limited (inefficiency expected in b-layer above $3 \cdot 10^{34}$ cm^{-2} s^{-1})
      → replace with new readout chip
    - better resolution for pile-up rejection
    - very forward tracking to recover FCAL performance?

Occupancy

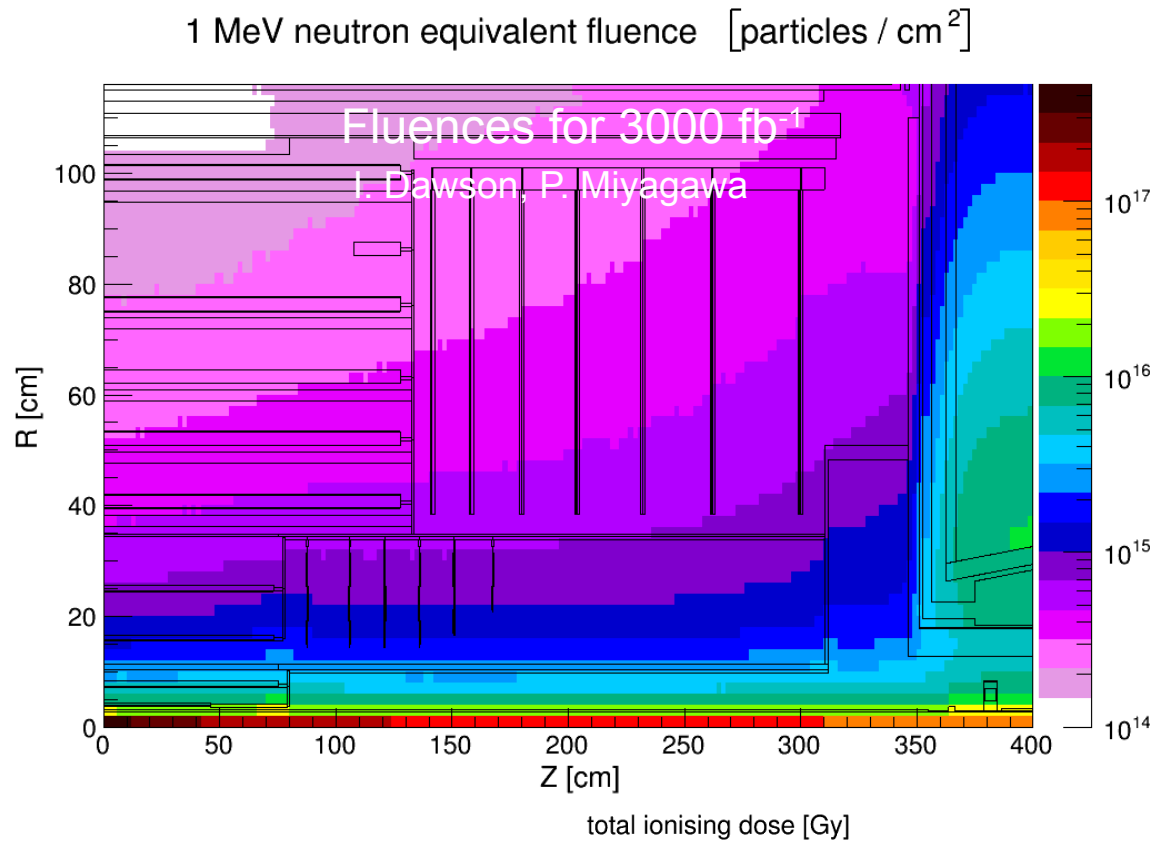
Occupancy will rise: depending on scenario and luminosity levelling

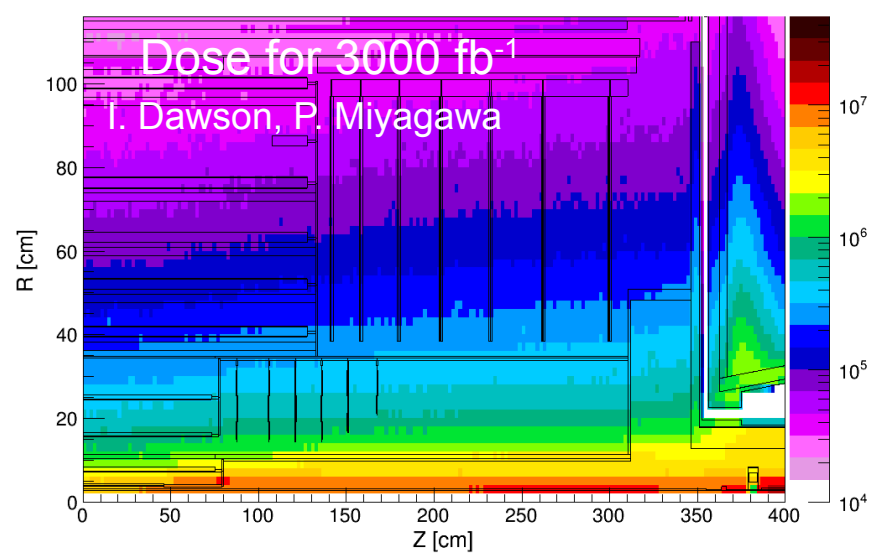
- 100 – 200 (– 400 for 50 ns scenarios) pile-up events
- up to 14000 tracks per BC (!)



Radiation Damage: Fluences at HL-LHC

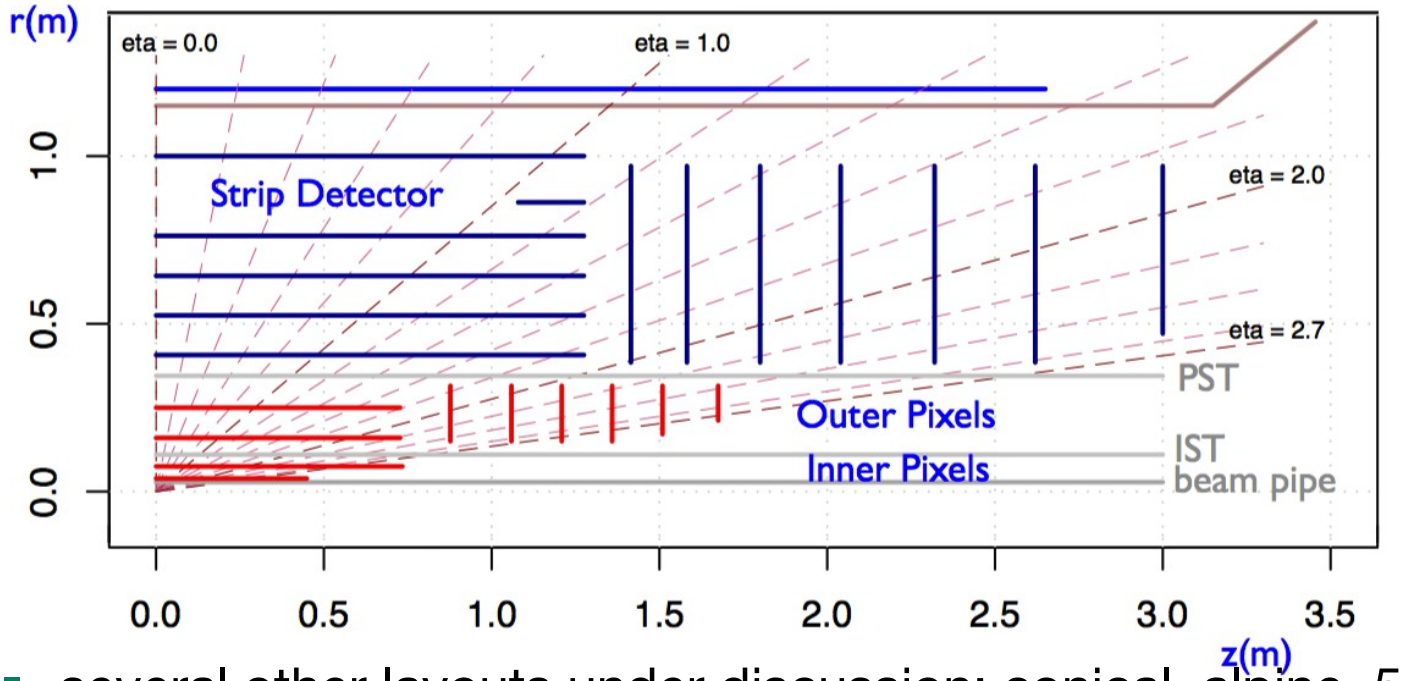
- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
    - ~1500 MRad
  - at 25 cm radius
    - up to 10^{15} n_{eq} cm^{-2}
    - ~100 MRad
    - several m^2 of silicon
  - strip region
    - many 10^{14} n_{eq} cm^{-2}
    - up to 60 MRad
    - up to ~200 m^2 of silicon
- new ID sensors need to be more rad-hard and cheaper at the same time (more area to cover)



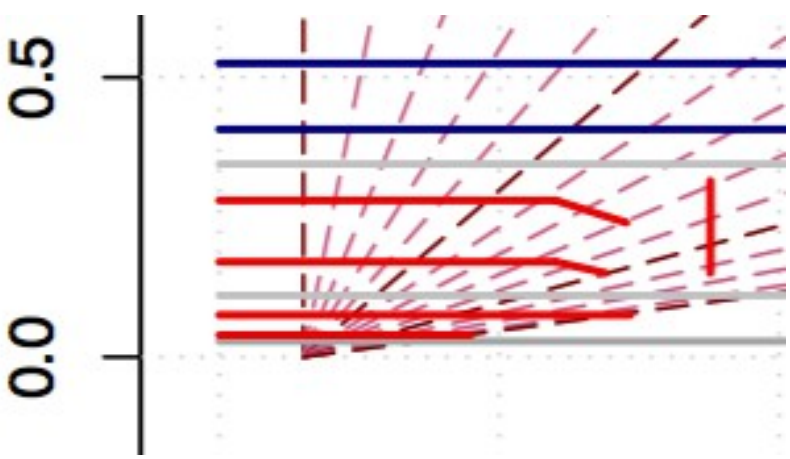


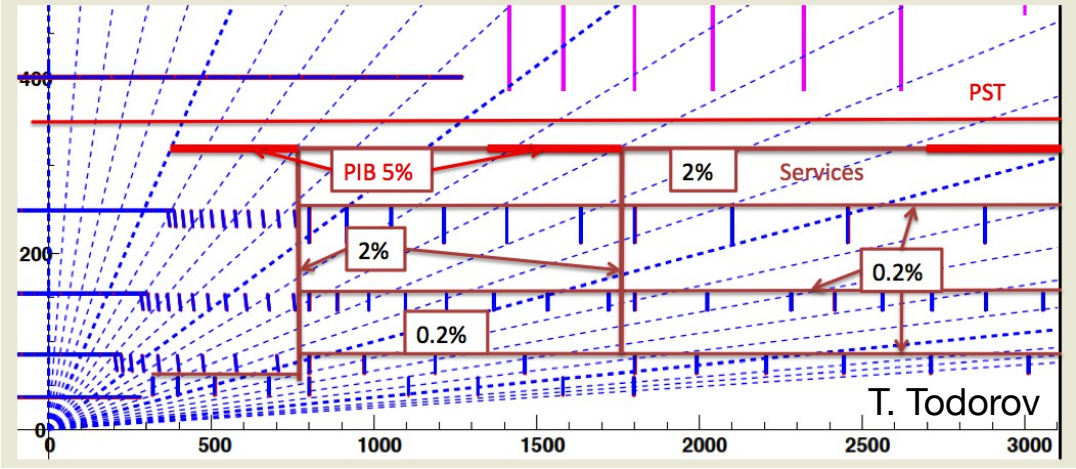
How to build? Layouts...

- Existing layout: Letter of Intent
  - ~200 m² of silicon strips (short and long), ~10 m² of pixels



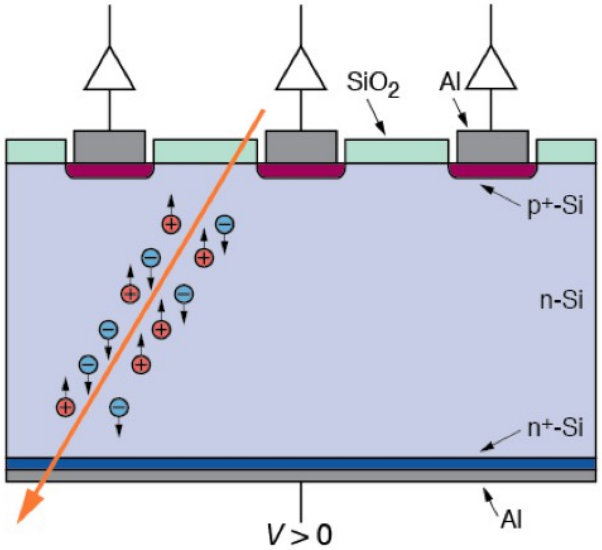
  - several other layouts under discussion: conical, alpine, 5th pixel layer...

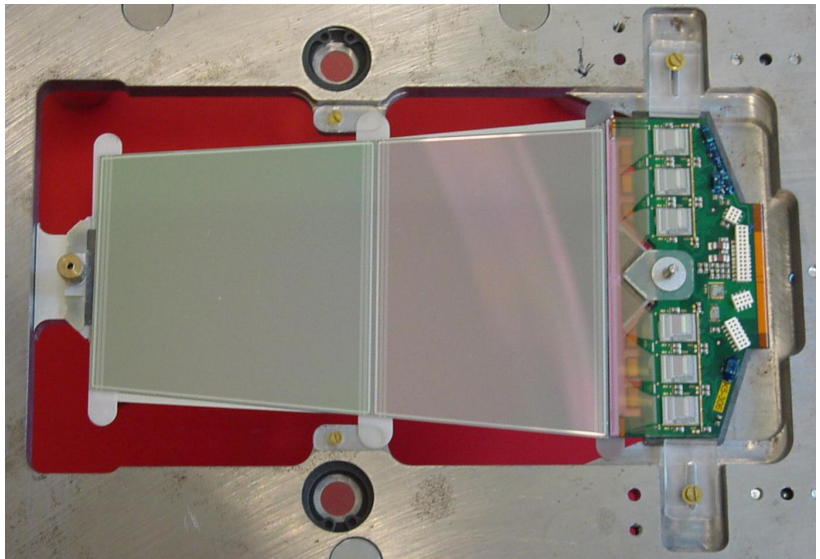


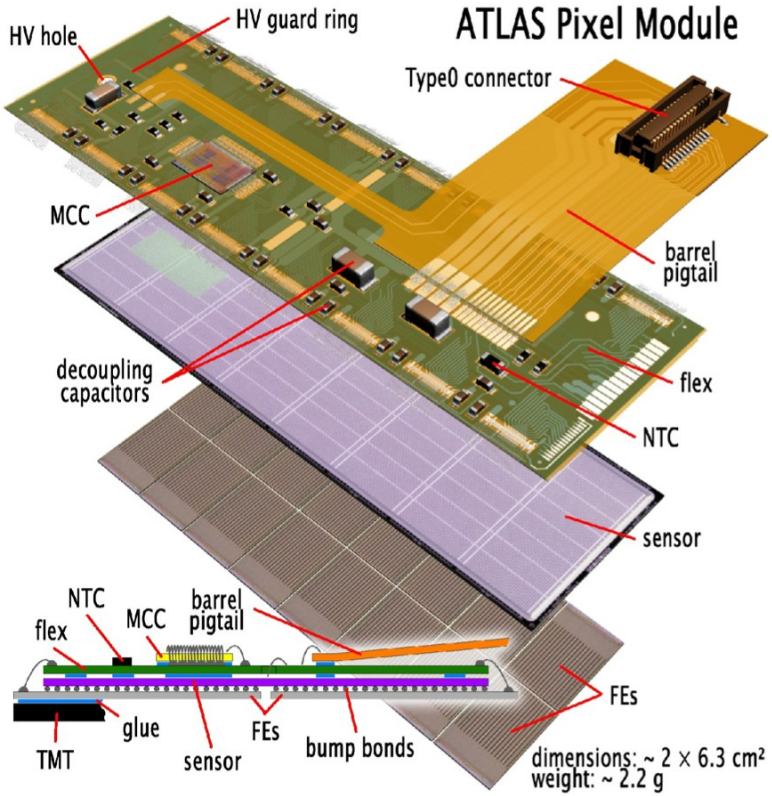


One step back: How do silicon detectors work?

- Interaction of charged particles with matter
  - main effect used in trackers: ionisation, generation of electron-hole-pairs in silicon bulk
- one side is patterned, many strip/pixel electrodes
- apply electric field across bulk, limit I_{leak}
- charges drift and induce signal on electrodes
- small signal, needs amplification
  - dedicated readout ASICs
  - connection with sensors via wirebonds (strips) or bump-bonding (pixels) → modules

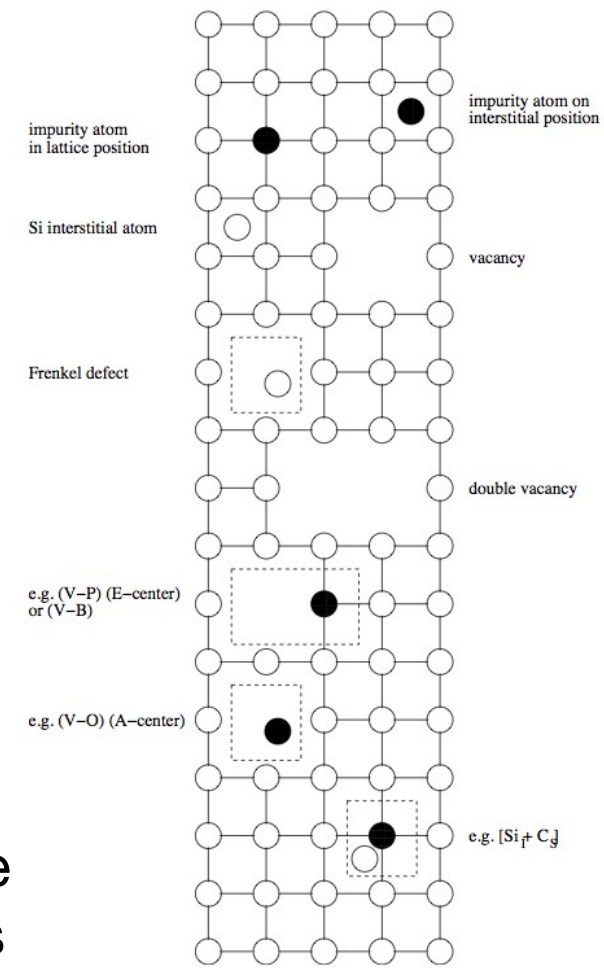






Silicon sensors and radiation damage

- Very brief introduction: The silicon crystal gets damaged by radiation – lattice atoms get moved around...
- There are 3 different effects all caused by radiation-induced damage to the crystal lattice:
  - charge-carrier trapping
    - localised trapping centers
    - thermal de-trapping timescale much longer than charge collection time
    - loss of induced charge → reduction of signal
  - leakage current
    - thermal generation of charge carriers → more noise → more cooling required
  - change of N_{eff}/V_{dep}
    - the material usually behaves effectively more "p-type" which leads to increasing full depletion voltages → higher bias voltages
- The usual unit for radiation damage is the particle fluence normalised to 1-MeV-equivalent neutrons
- Sometimes also dose is relevant (oxide charges, electronics)

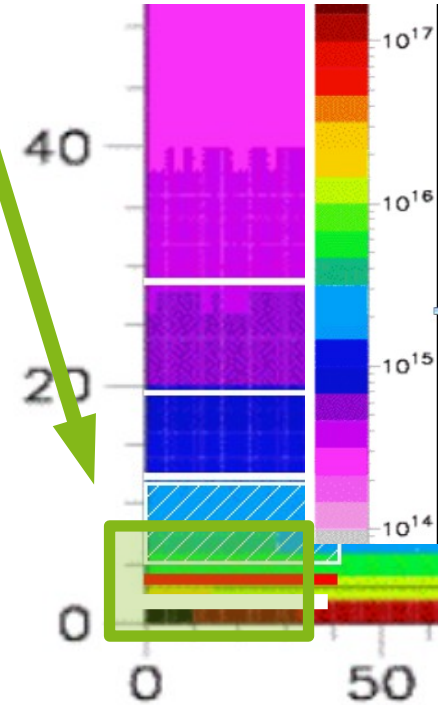


Pixel radii@HL-LHC: Different regimes

- Inner layers
  - Up to 2-3 · 10^{16} n_{eq}/cm^2
  - Trapping becoming the dominant effect
  - charge amplification?
  - data obtained with strip sensors indicate still significant collected charge after HL-LHC fluences

➔ valid also for planar pixel sensors?

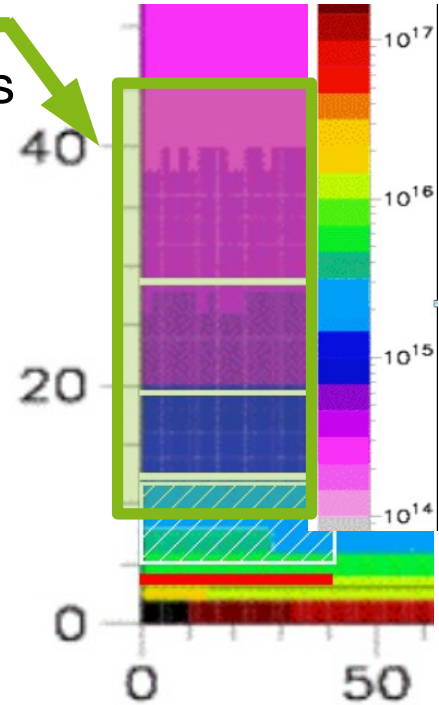
➔ different technologies better-suited?



- Outer layers
  - Rad-hardness up to 2 · 10^{15} n_{eq}/cm^2 at 600V bias voltage was already established for current ATLAS Pixel Detector

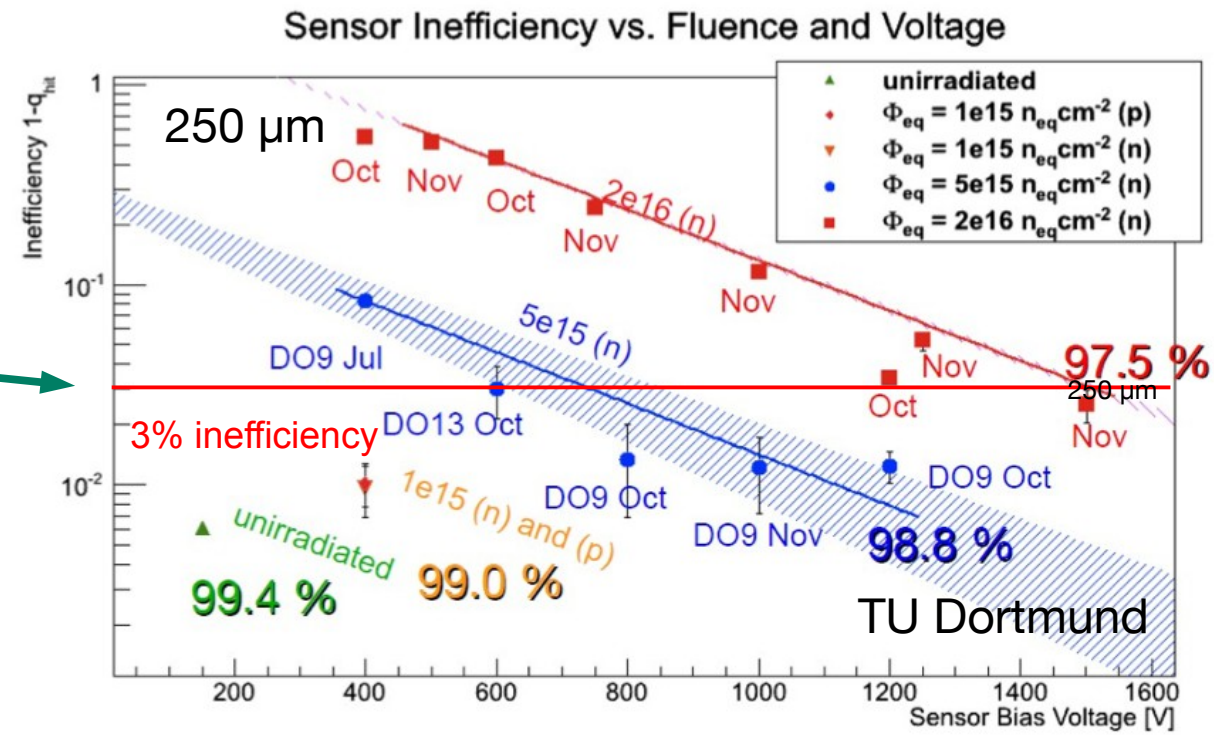
➔ sufficient rad-hardness likely

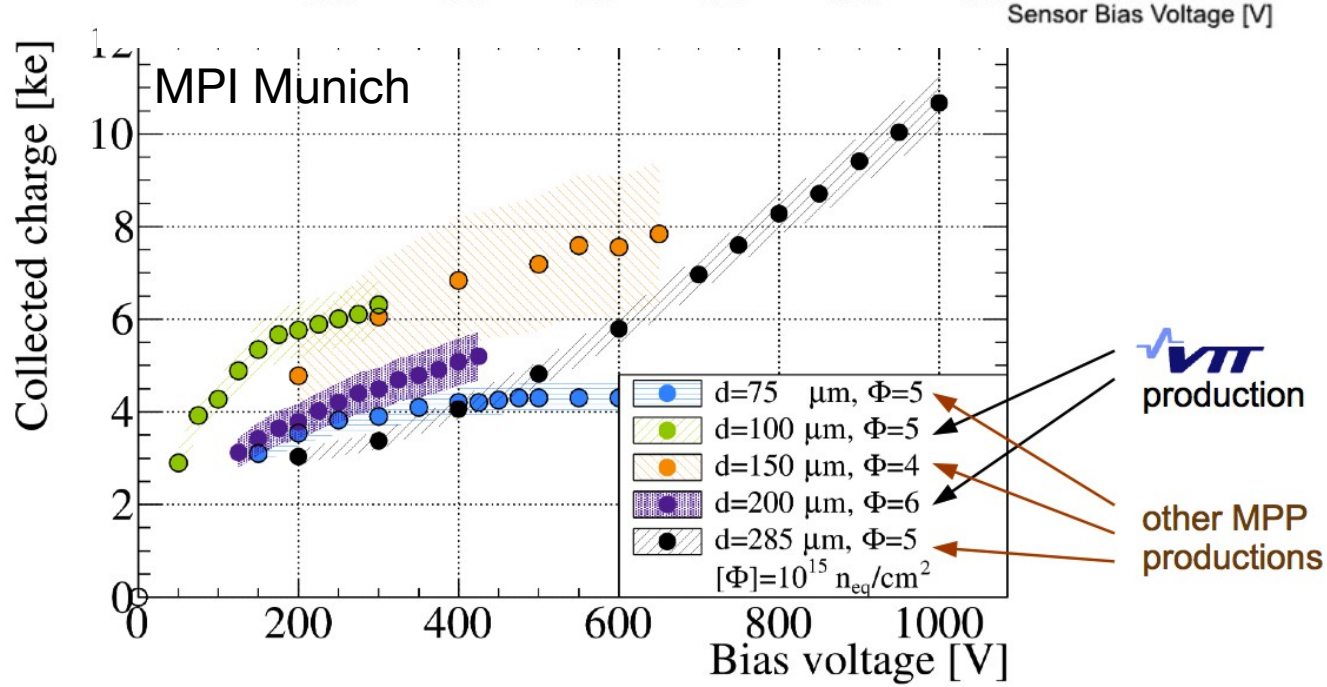
  - But: Costs? 1.8 m^2 → ~10+ m^2



Innermost layers: highest fluences

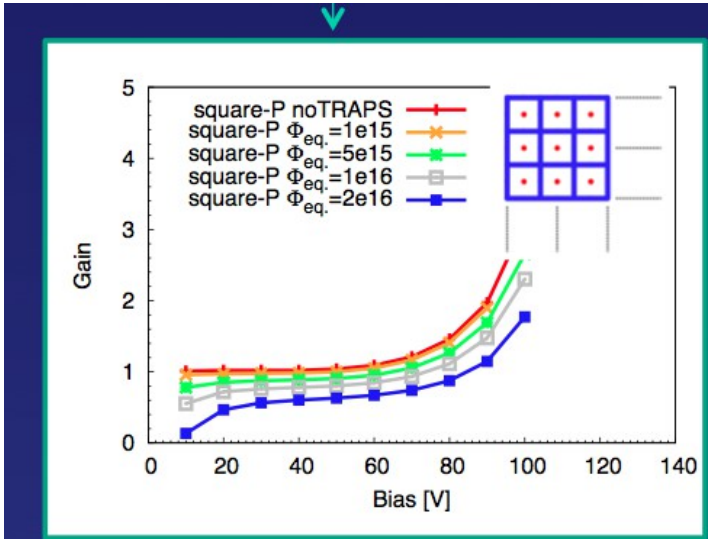
- Main issue: trapping → reduce drift time
  - Increase field: up to 2kV works stable!
    - less than 3% inefficiency achievable
  - Thin silicon demonstrated down to 50-75 µm
    - on handling wafers
    - 100-150 µm with standard production
  - Possible, but life is hard – better alternatives?

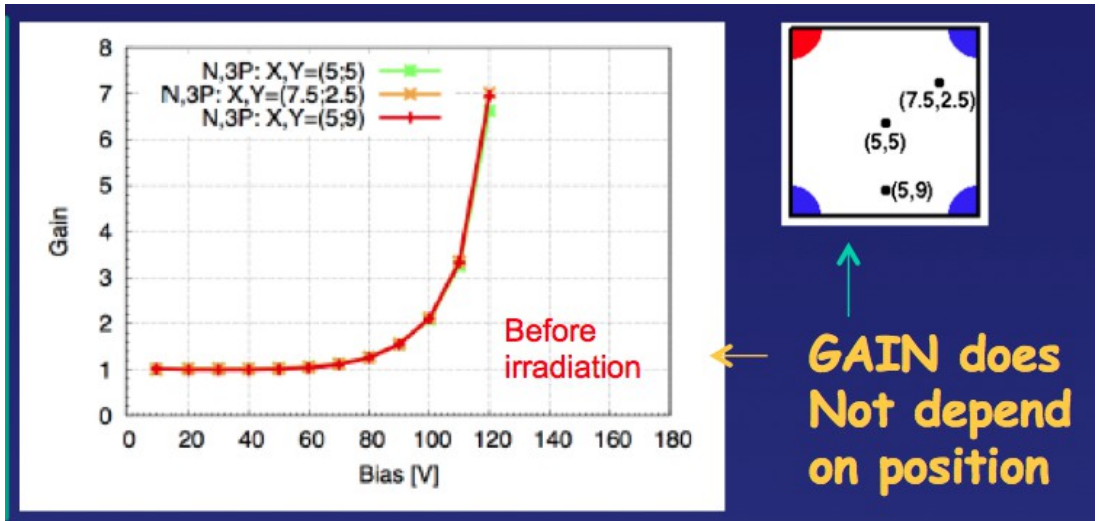


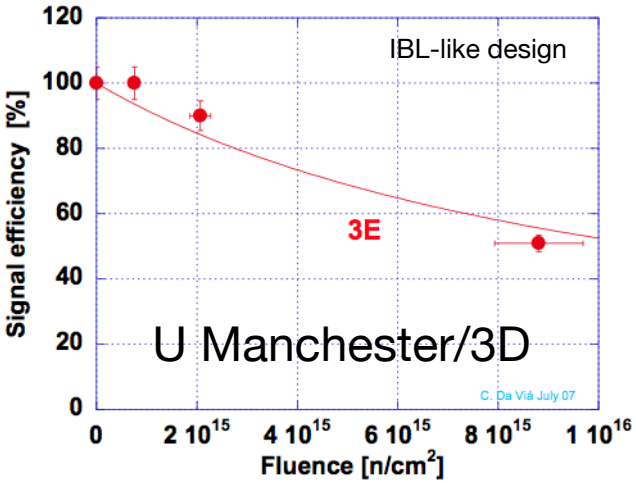


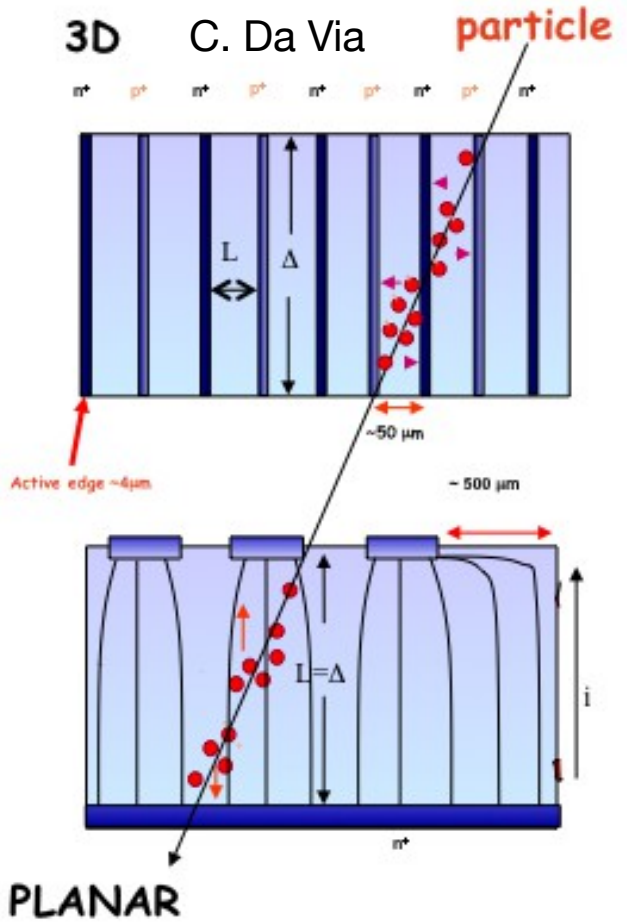
Innermost layers: highest fluences

- Main issue: trapping → reduce drift length
  - 3D silicon – IBL production successful
  - future: charge amplification on purpose?
  - but: non-standard process, low-volume, ...









CMOS-based sensors

Larger pixel radii: cost-efficiency

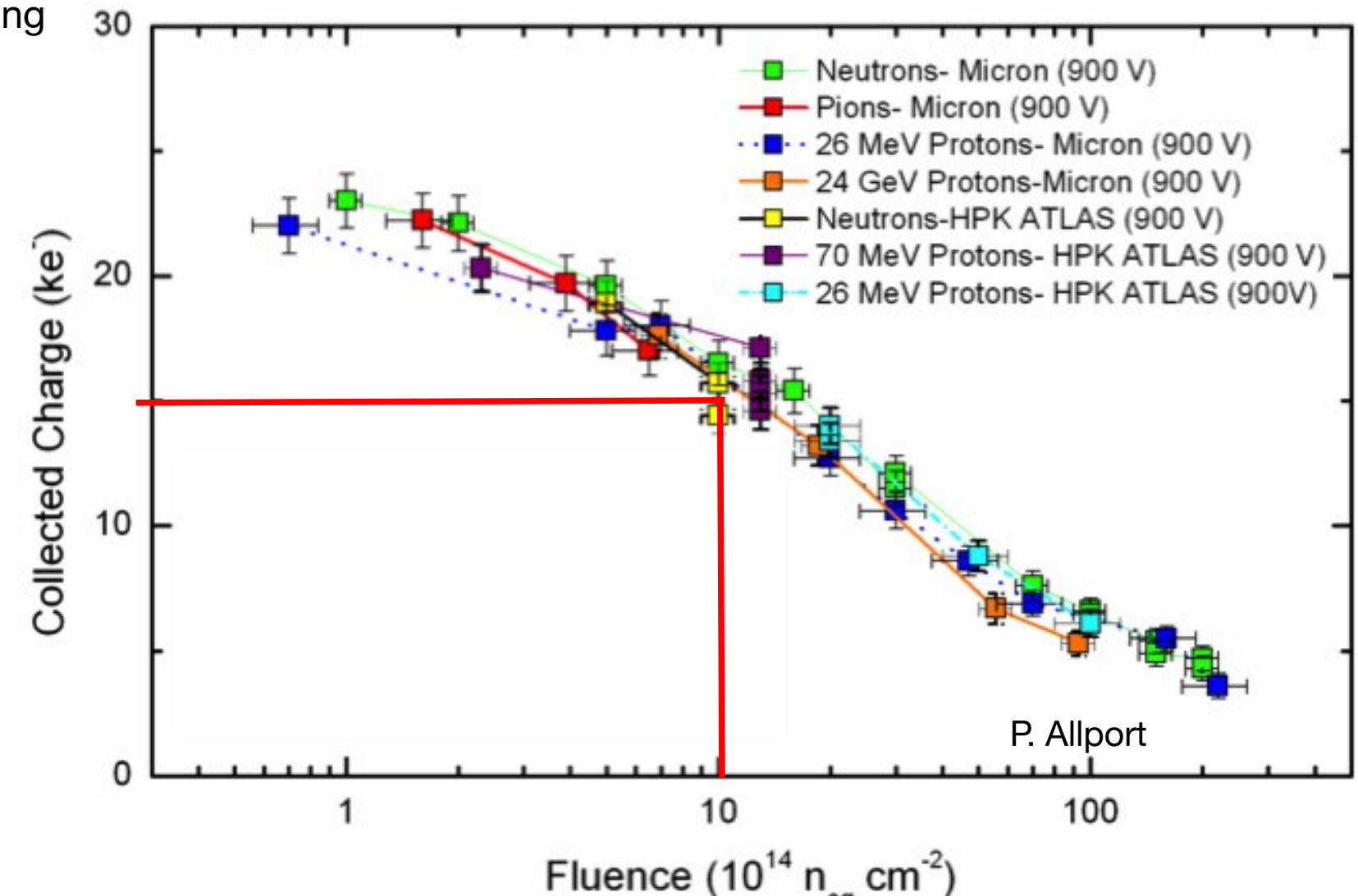
- pixel sensors offer improved spatial resolution and reduced occupancy
  - thus there are ideas to have 5 pixel layers and only 2 short strip layers
- since ATLAS production, large advances in cost efficiency:

Item	ATLAS Production	Costing goal 2008	Current best estimate for large volumes
Sensor	~ 55 CHF/cm^2	~ 50 CHF/cm^2	< 30 CHF/cm^2
Readout chip	~ 150 CHF/cm^2	< 50 CHF/cm^2	< 30 CHF/cm^2
Bump-bonding	~ 190 CHF/cm^2	< 50 CHF/cm^2	< 30 CHF/cm^2
Sum	~ 400 CHF/cm^2	< 150 CHF/cm^2	< 90 CHF/cm^2

- current cost estimate may still decrease significantly
  - possible sensor production on 8” wafers using CMOS foundry processes
  - readout chip production might be with cheaper vendor
  - industrial bump-bonding (C4NP) might become available for 50 μm pitch
- best option might be to get rid of bump-bonding anyway
  - glueing → capacitive coupling, no leakage current, but small signal
    - trials ongoing with planar sensors
    - valid option for HV-CMOS

Large strip radii: Collected charge with n-in-p strips

- collected charge > 14000 e^- at 10^{15} n_{eq} cm^{-2} and 900V bias voltage → perfect
- sensor self heating due to leakage current → sufficient operation temperature
- production on 6” wafers → less costly than before, but still (too?) expensive
  - trials with production on 8” wafers using modified CMOS foundry processes ongoing



Novel CMOS-based sensors
for the ATLAS Inner Tracker upgrade

Recap: rad-hard sensors

- Large efforts to assess and demonstrate rad-hardness using refined hybrid detectors
  - go to electron collection (n-in-n or n-in-p)
  - reduce drift distance (3D, thin silicon)
  - reduce/eliminate leakage current (CO2 cooling, diamond)
  - use deep-submicron rad-hard readout chips (130nm, 65nm)

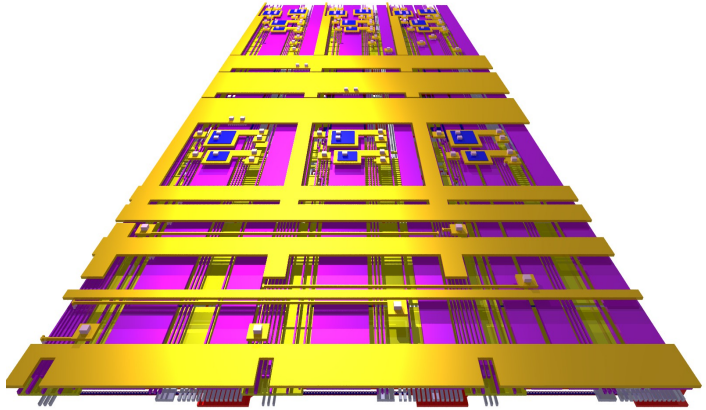
➔ in short: Hybrid detectors are rad-hard enough. Lots of experience with them. Could be used. The end?

- Main drawback: Price
  - hybridisation expensive, small pitches require special processes
  - sensor processes non-standard and on small wafers, hence more costly
  - new trackers require ~200m^2 of silicon, price is important for the financial feasibility of the upgrade

How to stay rad-hard, but get cheaper?

- Ways to reduce cost: use
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
    - but: application of **drift field** required for sufficient rad-hardness
      - ➔ requires careful choice of process and design
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips” for large volumes
    - wafer thinning quite standard
  - usually p-type Cz silicon
    - thin active layer, helpful to disentangle tracks in boosted jets and at high eta
      - requires low capacitance → small pixel
- Basic requirement: Deep n-well (→ allows high(er) substrate bias)
  - existing in many processes, e.g. even 65nm (!)
  - usually deepest in HV-CMOS → highest possible bias
  - also existing in specialised imaging processes → HR-CMOS

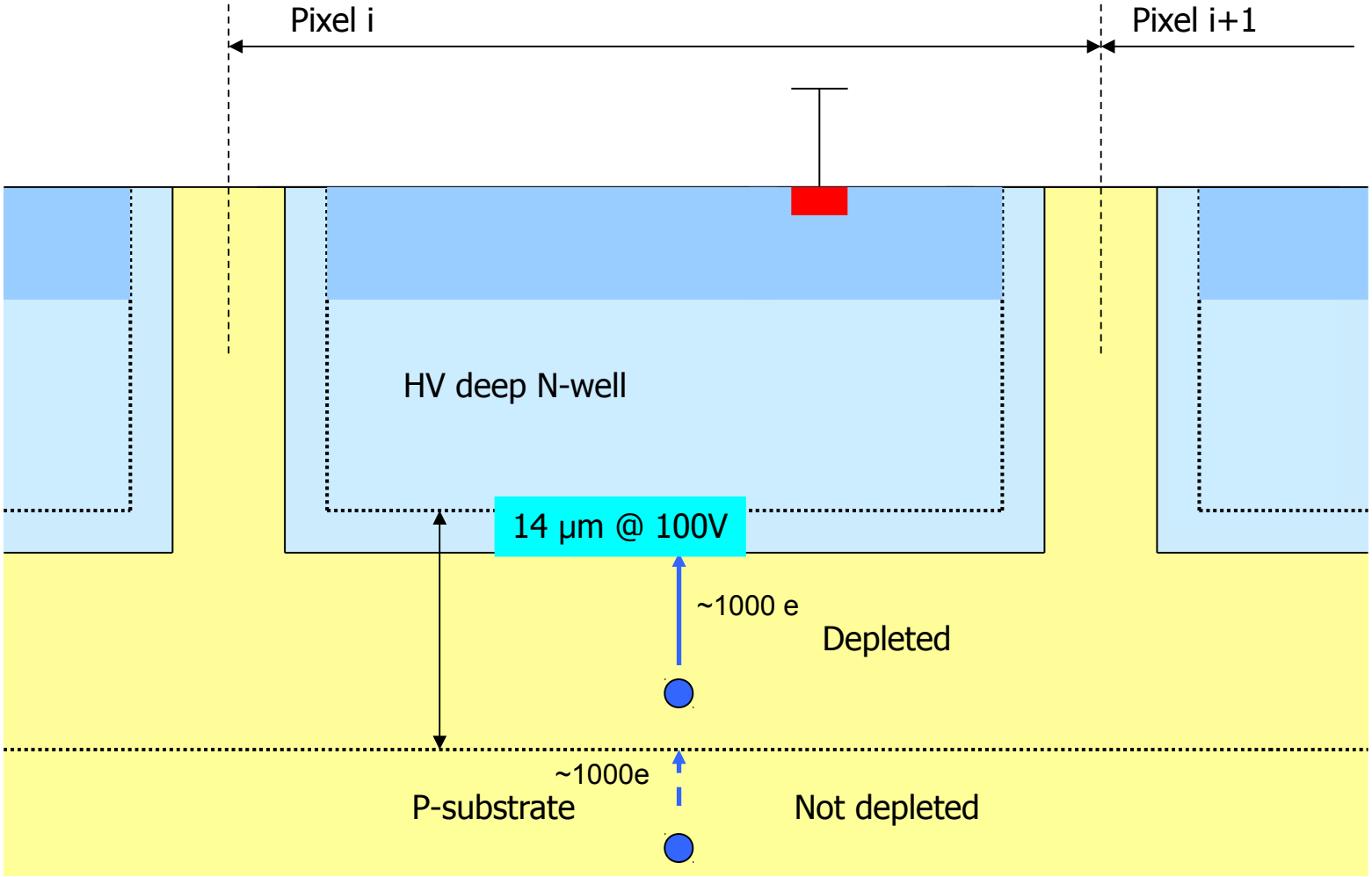
AMS H18 HV-CMOS



- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
  - biasing of substrate to ~60-100V possible
  - substrate resistivity ~10 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth theoretically in the order of 10 μm → drift signal ~1 ke^-
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk → avoid clocked circuits
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - “digital” area at the expense of significant inactive edge/balcony
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

A HV-CMOS sensor...

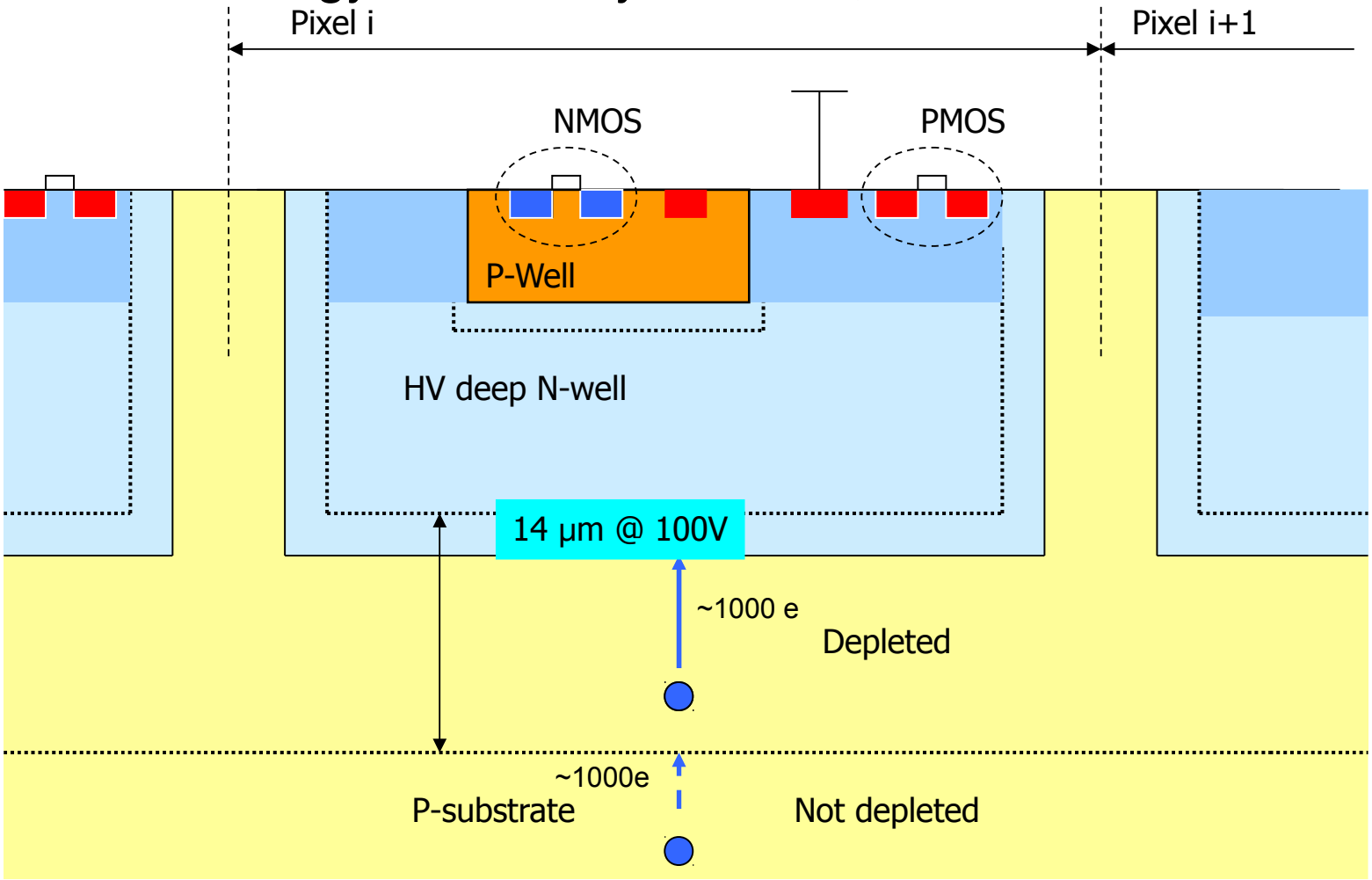
- essentially a standard n-in-p sensor
- depletion zone ~10 μm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard, but watch out...



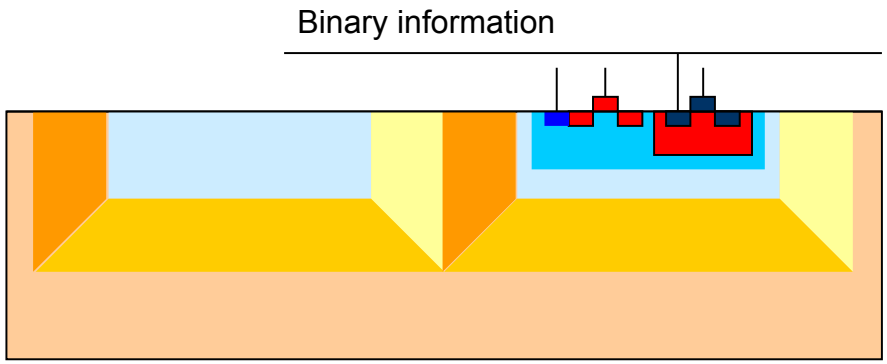
CMOS electronics placed inside the diode (inside the n-well)

Proof of concept prototypes

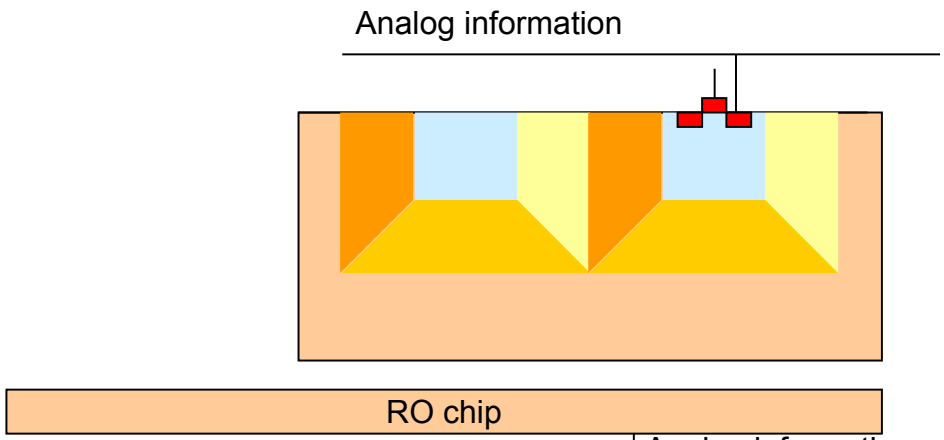
- Several test-chips already existing (many in AMS 350 nm HV-CMOS process), see backup slides for more detailed results

SDA with sparse readout
(“intelligent” CMOS pixels)
HV2/MuPixel chip

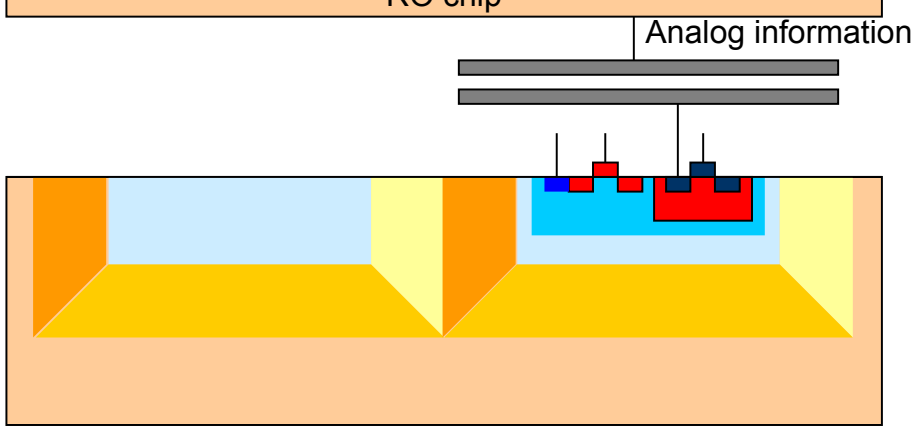
→ baseline for μ3e experiment at PSI



SDA with frame readout
(simple PMOS pixels)
HVM chip



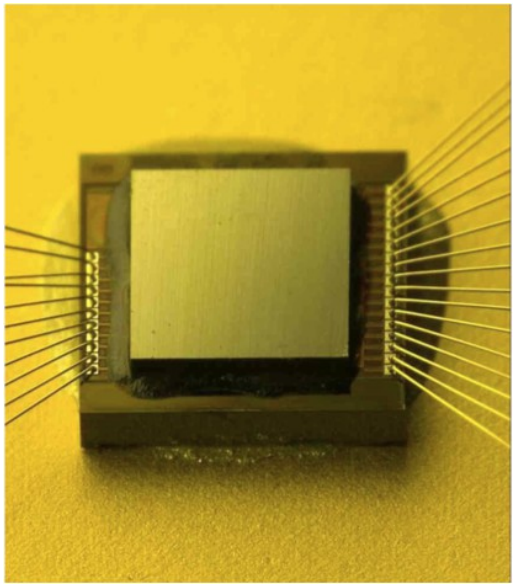
SDA with capacitive readout
(“intelligent” pixels)
Capacitive coupled pixel detectors
CCPD1 and CCPD2 detectors



Prototype summaries

CMOS-based sensors

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55μm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns



Bumpless hybrid detecto

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60μm
RO type: capacitive
Noise: 80e
MIP signal 1800e

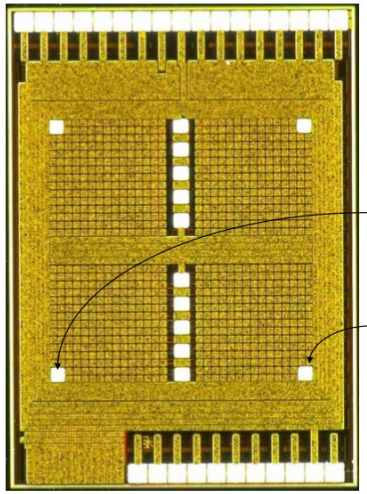
CCPD2 Chip
Edgeless CCPD
Pixel size 50x50μm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

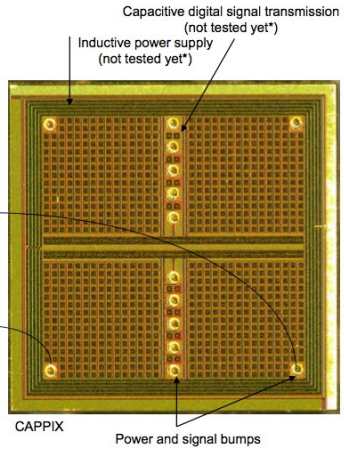
Frame readout - monolithic

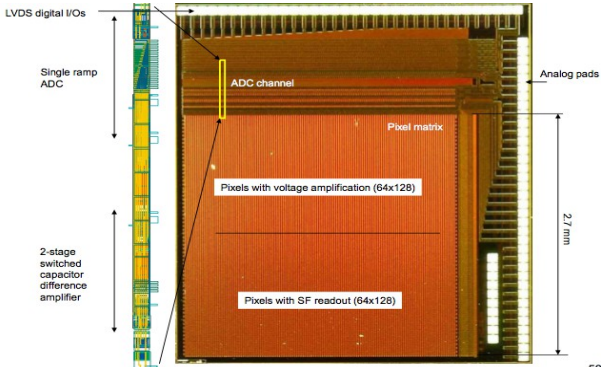
PM1 Chip
Pixel size 21x21μm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7μm
Uniform detection

PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 μm

Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15} n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)



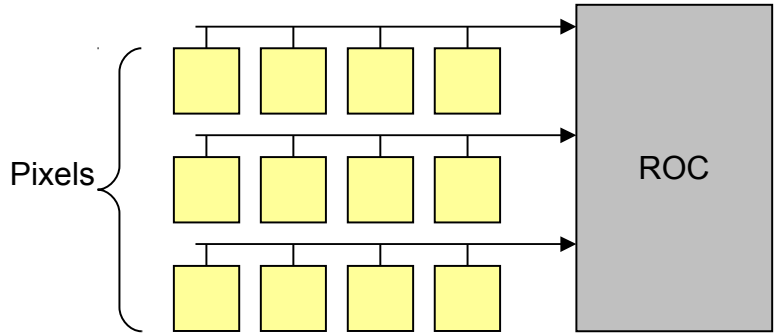




I. Peric

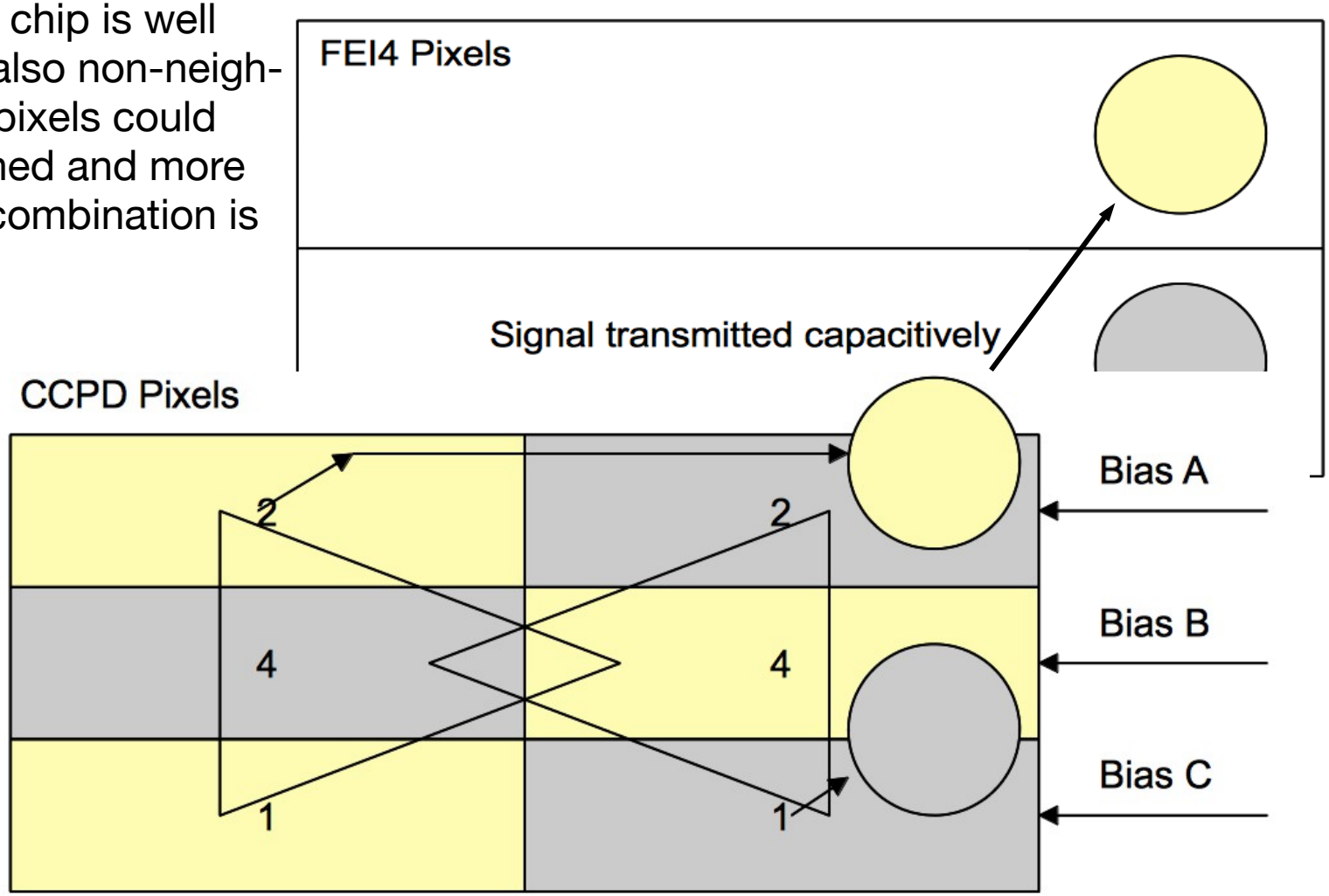
From MAPS to active sensors

- Existing prototypes were not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



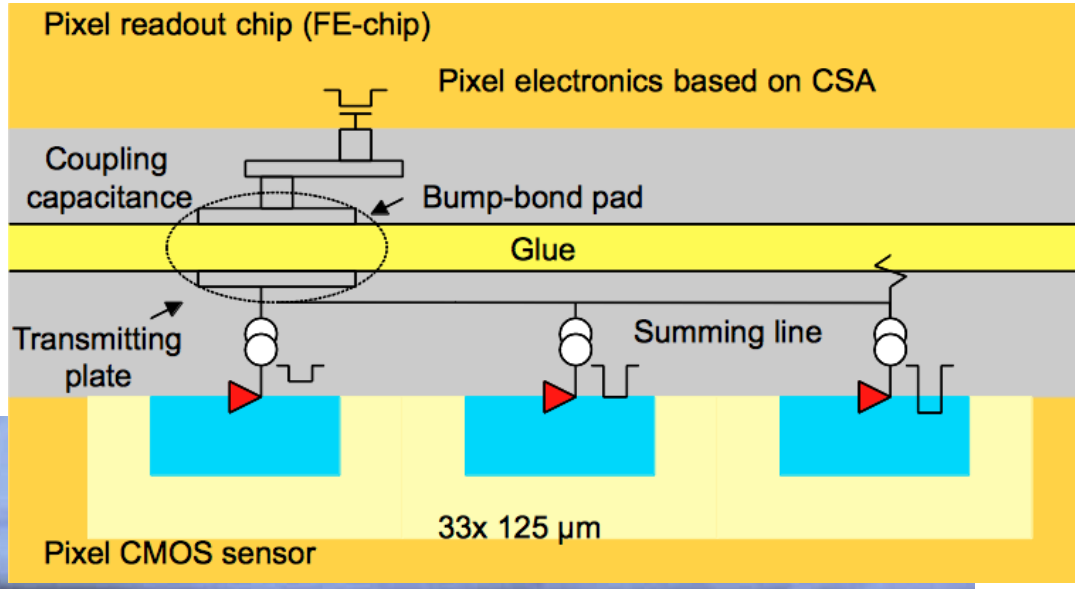
Pixels: sizes and combinations

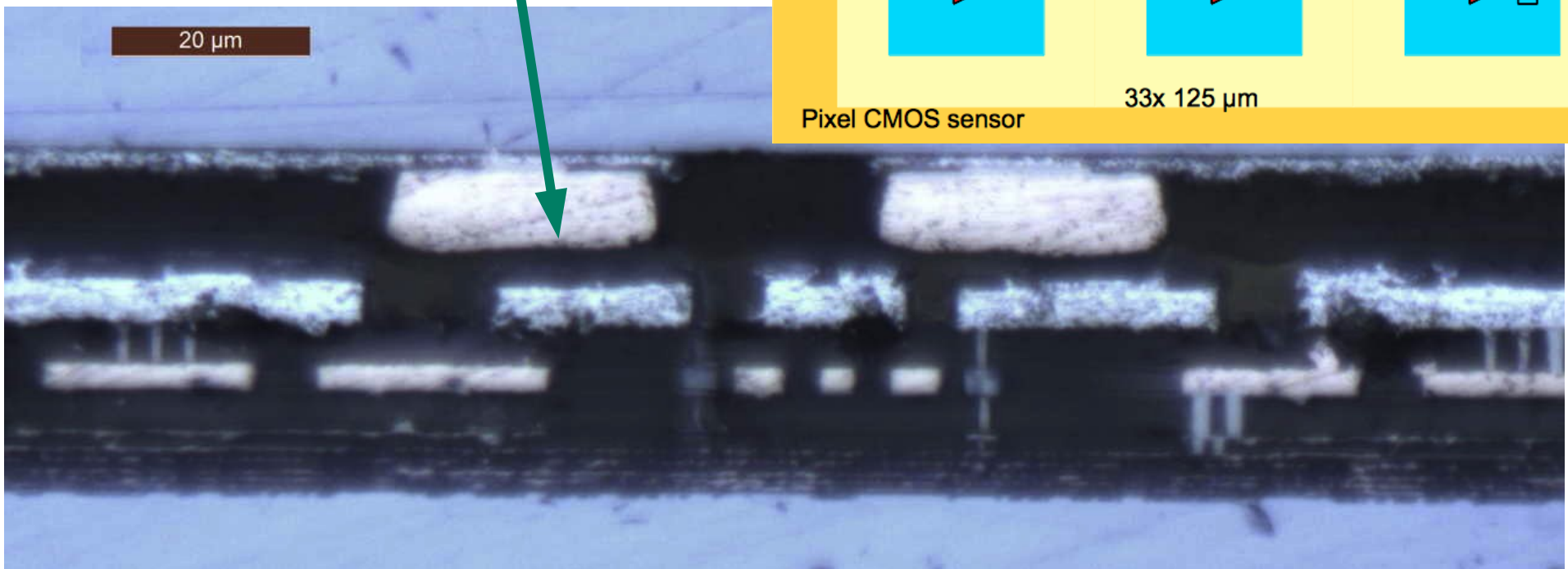
- Possible/sensible pixel sizes: 20x20 to 50x125 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



Pixels: bonding?

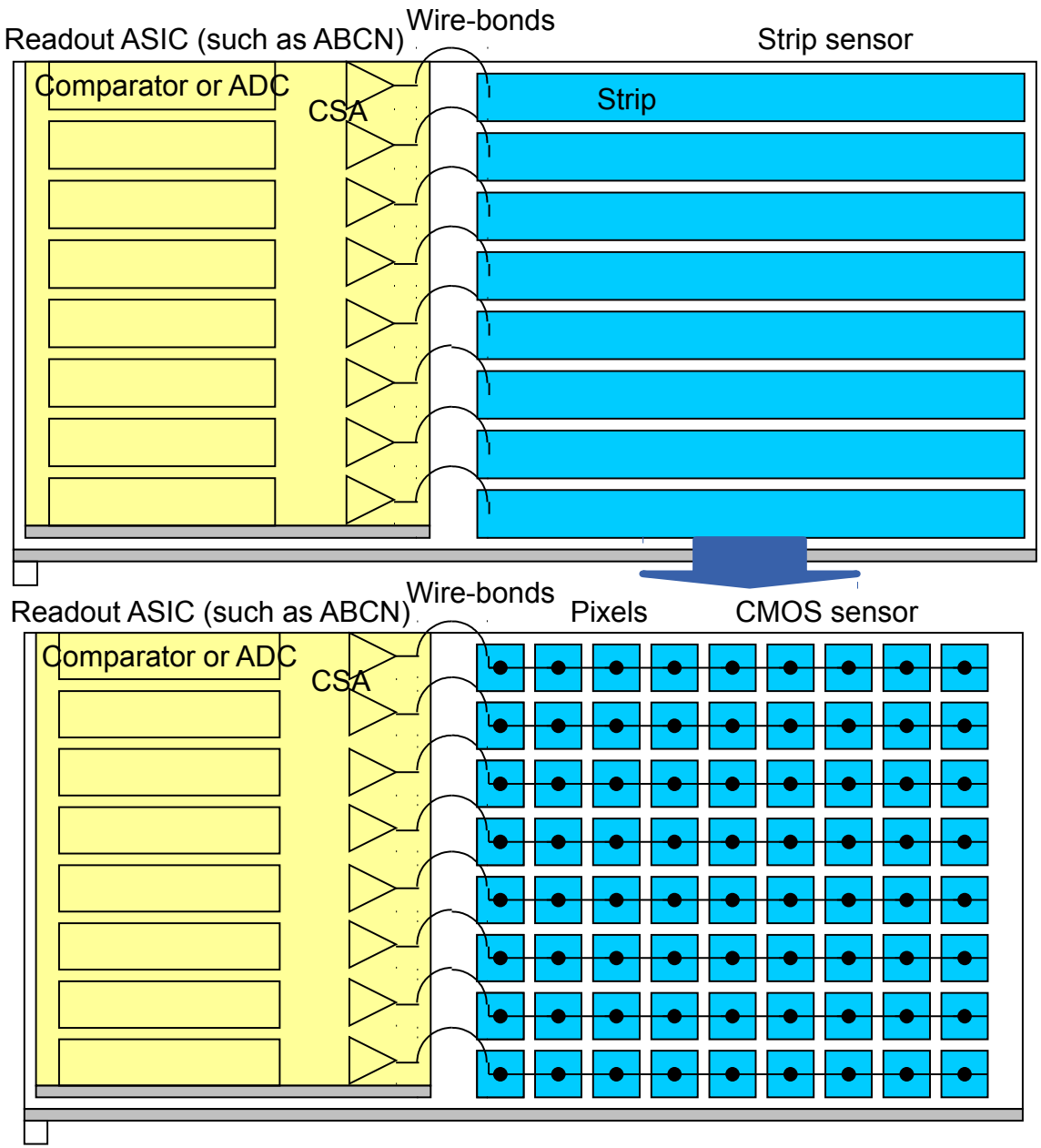
- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - variations in glue thickness can be handled by tuning procedures and offline corrections if necessary
  - avoids costly bump-bonding
  - no thermal bowing during reflow
  - glue layer thicknesses <10 μm were achieved across 2x2cm

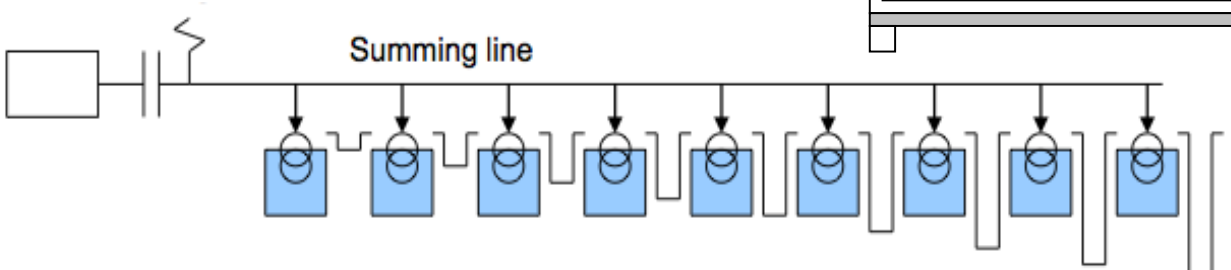




Strips

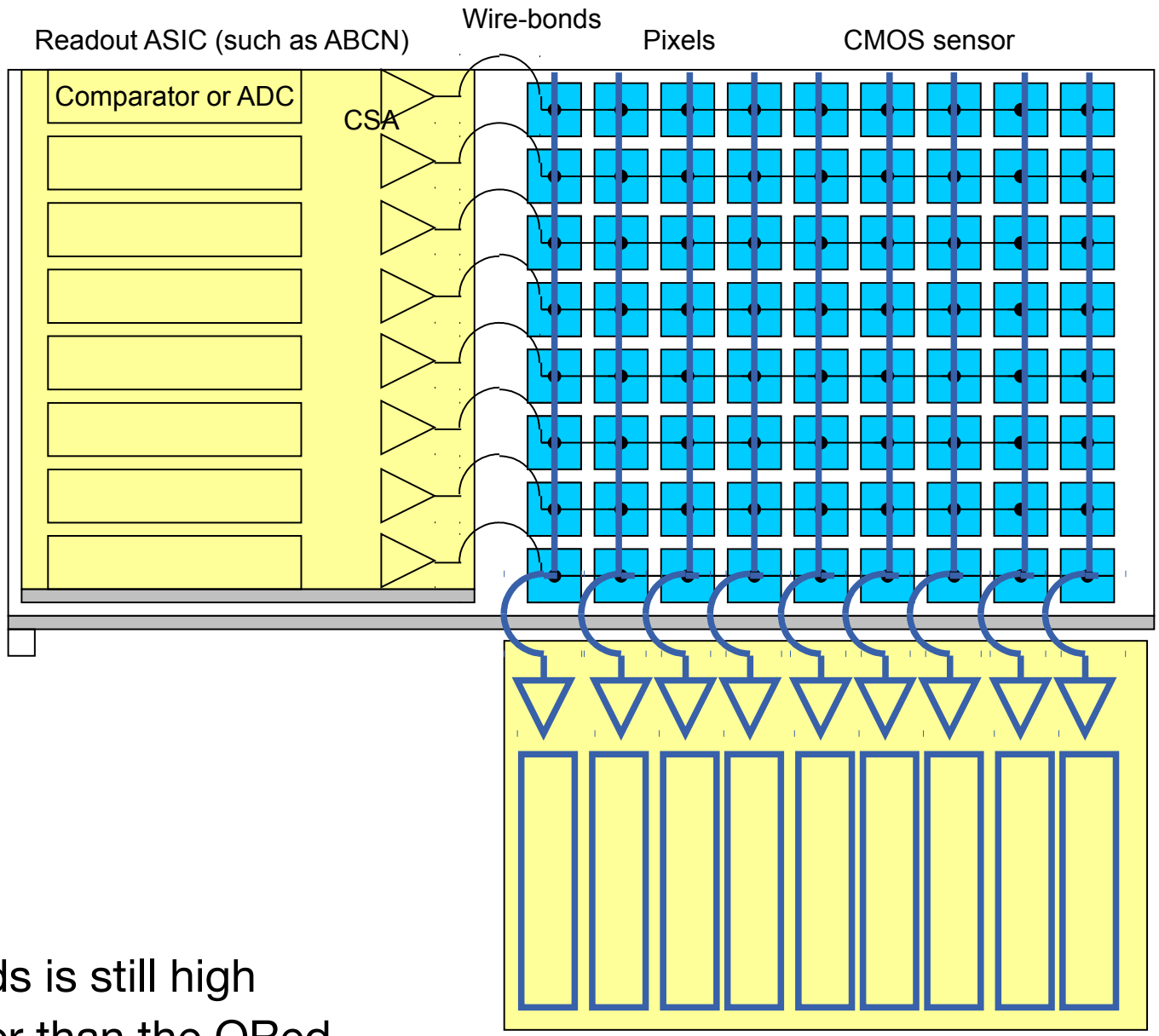
- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip can be again encoded by pulse height for analogue readout chips (e.g. Beetle)





Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double length but only half the pitch in r-phi
  - Multiple combinations to resolve ambiguities – pixel precision with only ~4N channels instead of N^2

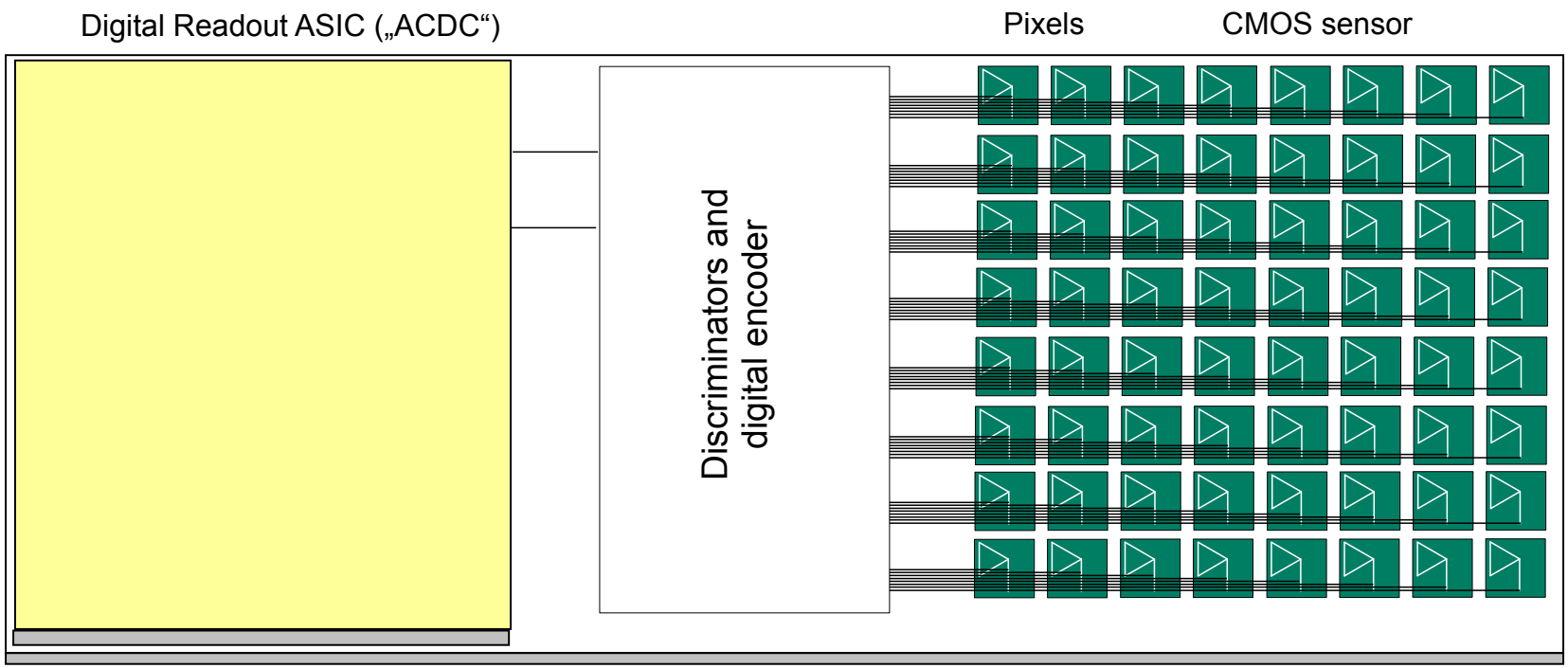


- Drawbacks:
  - number of wirebonds is still high
  - hit efficiency is lower than the ORed combination of two full sensor layers

Strips: Possible Improvements

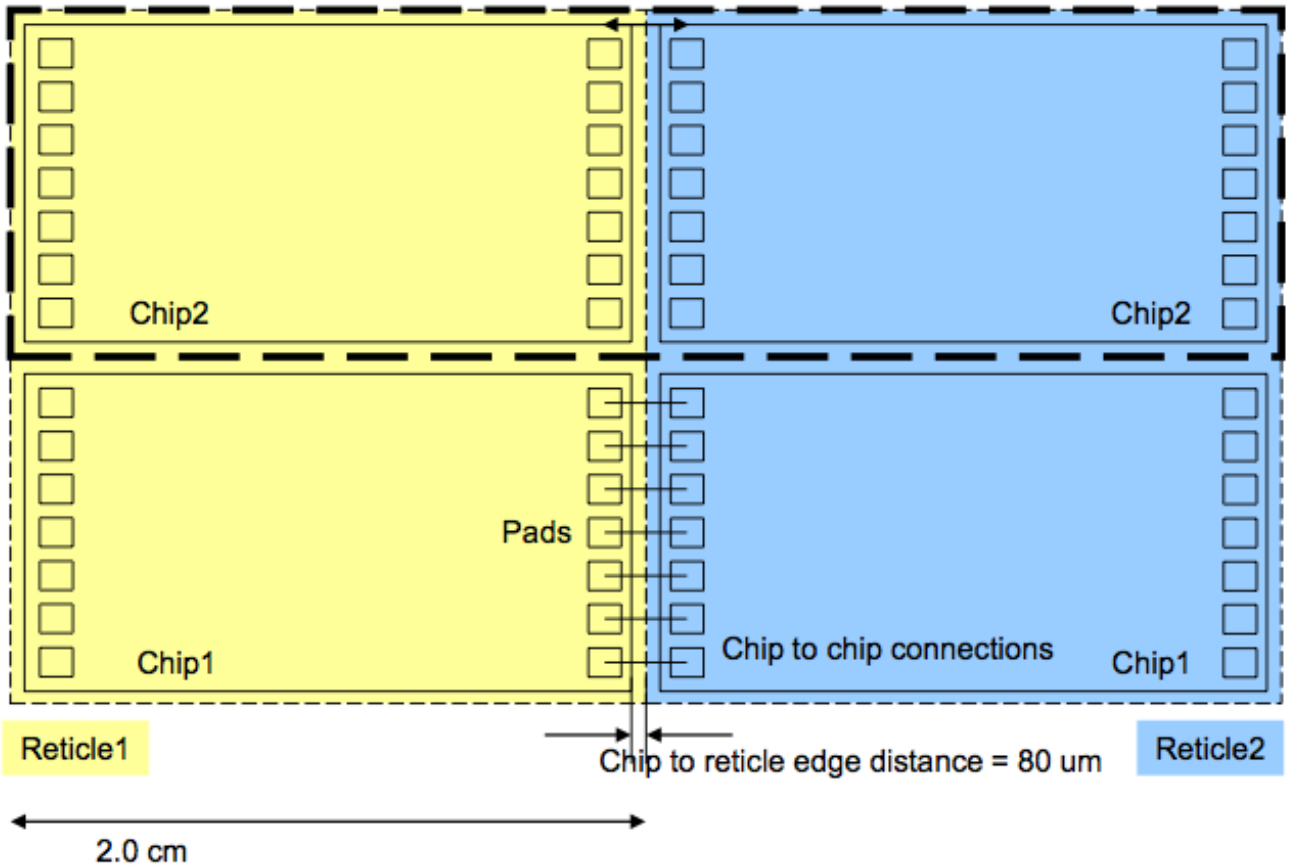
- increase signal-to-threshold, e.g. by going to high-resistive substrates
- use a digital encoding scheme to “concentrate”/zero-suppress data already on the “sensor”:
  - each pixels CSA has a dedicated line to the periphery
  - low-time-walk comparators implemented at periphery (less crosstalk)
  - digital encoder block reduces number of wirebonds by a large factor (LVDS communication with 160 to 320 MBit/s should be possible)
  - Digital readout ASIC mainly responsible for trigger handling and data storage

➔ less power, less material than “true” pixels, but with pixel-resolution



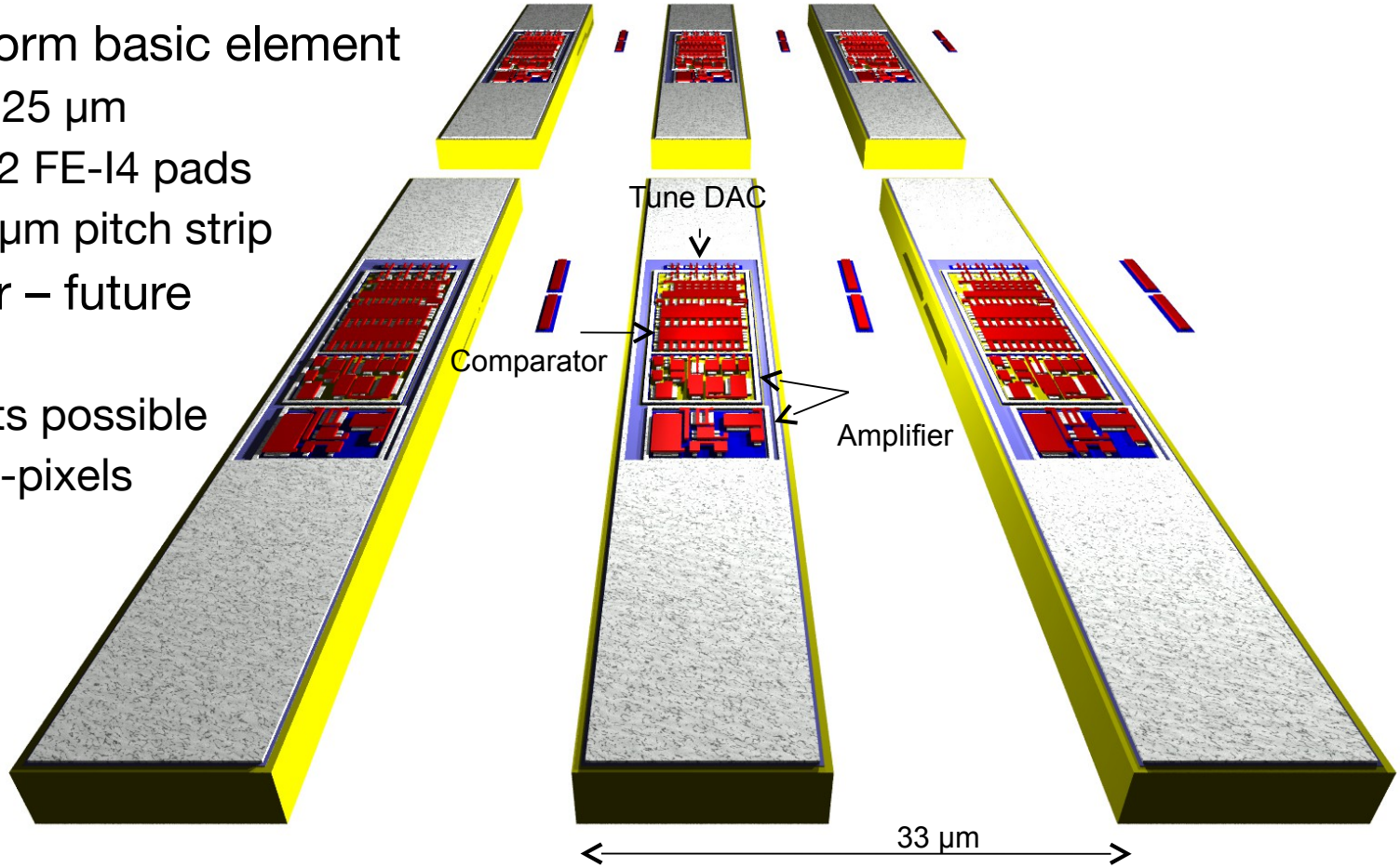
Reticule size/stitching

- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be good (very simple circuit, very few "central" parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



HV2FEI4

- A combined active strip/pixel sensor was designed and produced
  - strips compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
- Structure
  - 6 sub-pixels form basic element
    - each 33 x 125 μm
    - connect to 2 FE-I4 pads
    - form a 100 μm pitch strip
  - small fill factor – future options:
    - more circuits possible
    - smaller sub-pixels

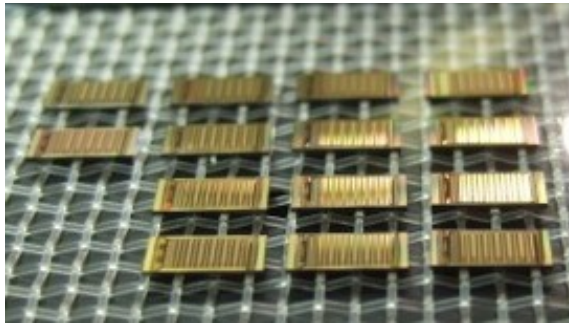


HV2FEI4

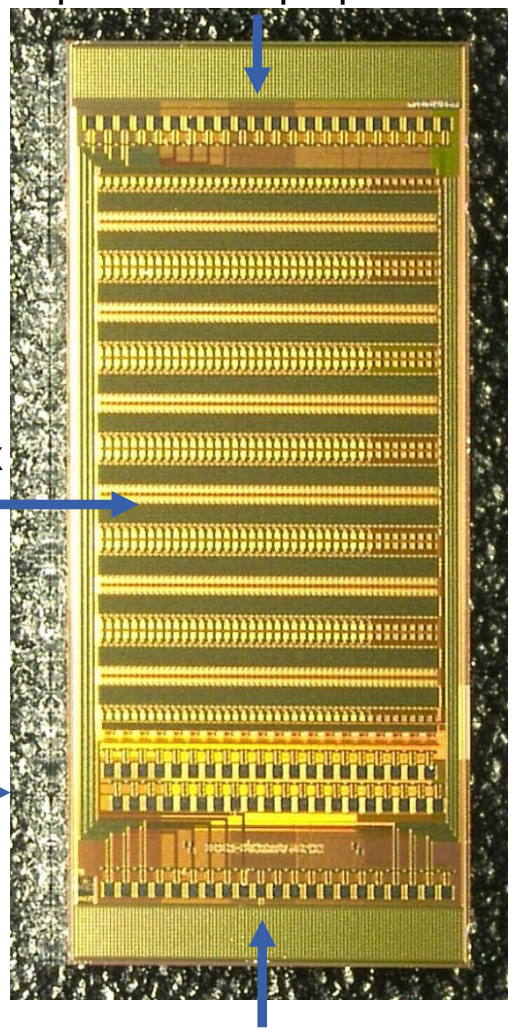
- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33 µm x 125 µm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 µm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or µC: 4 CMOS lines (1.8V)

3 possible operation modes

- standalone on test PCB
- strip-like operation
- pixel (FE-I4) readout



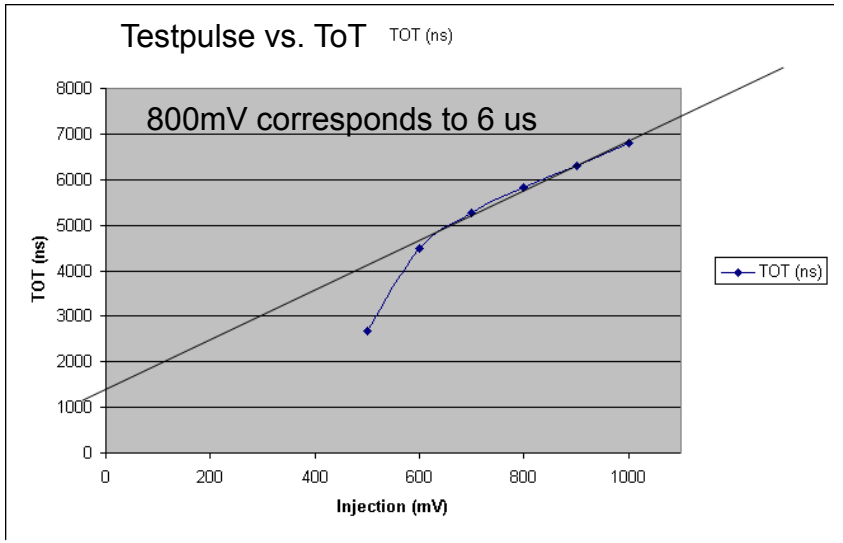
IO pads for strip operation

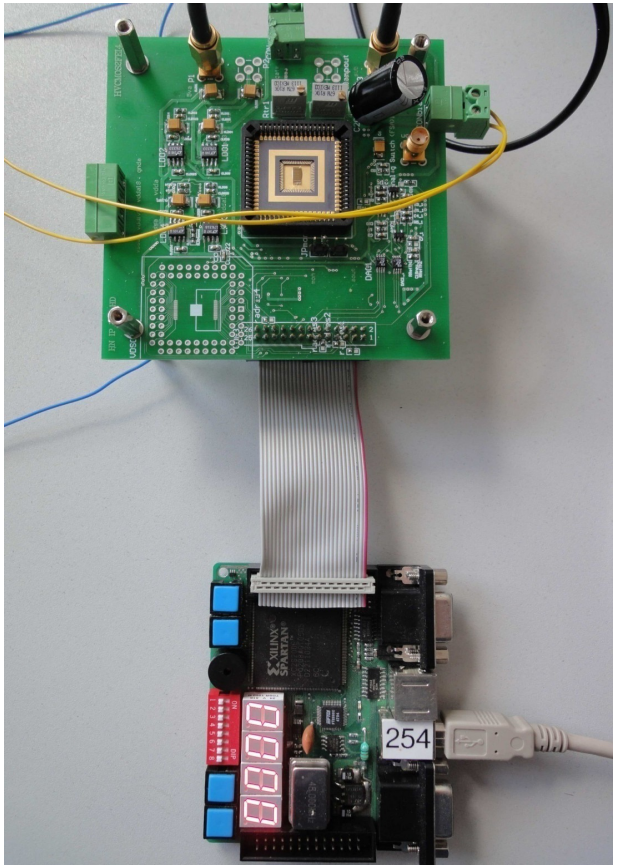


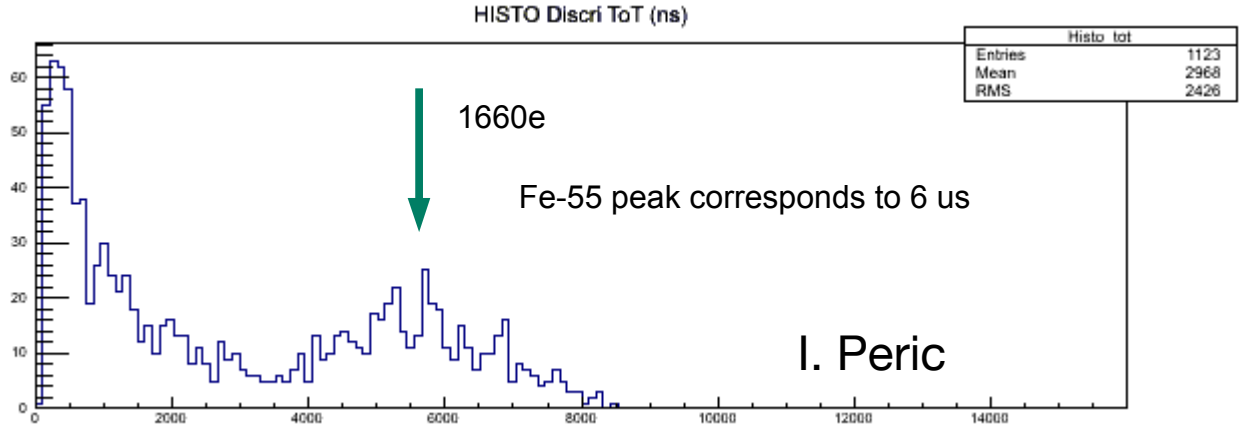
IO pads for CCPD operation

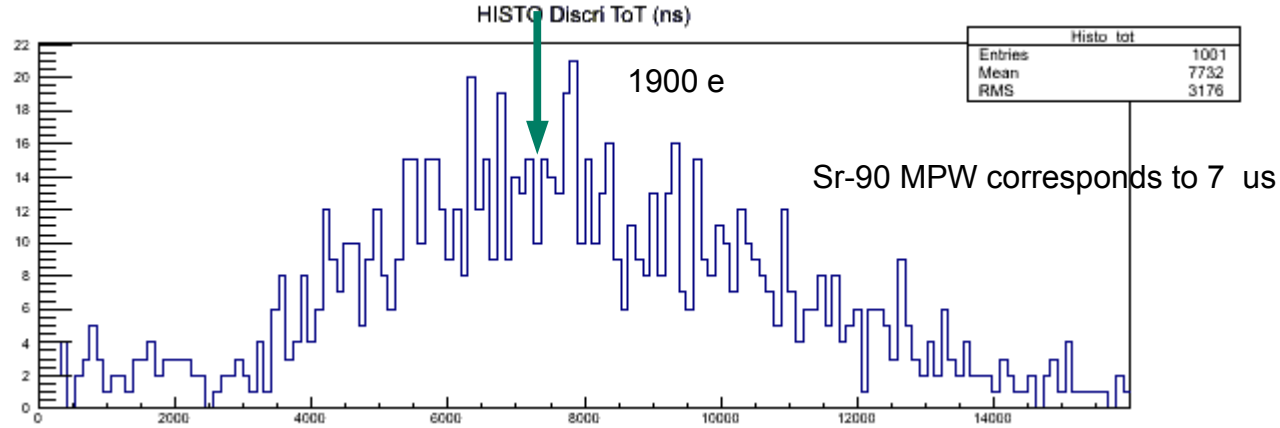
HV2FEI4: characterisation

- standalone, using monitor output
- MPW for ^{90}Sr at 60V: ~1900 e^-
  - would mean more than 20µm active depth? Diffusion? Unexpected field?
    → try eTCT
  - corresponds to 900mV injection







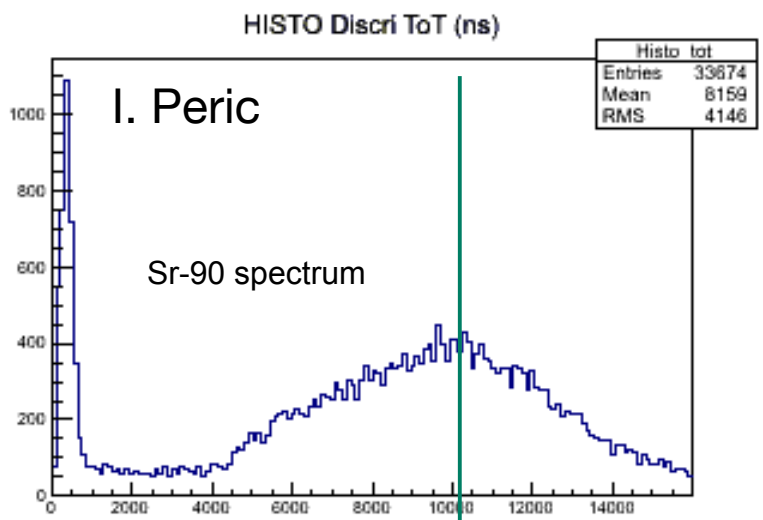


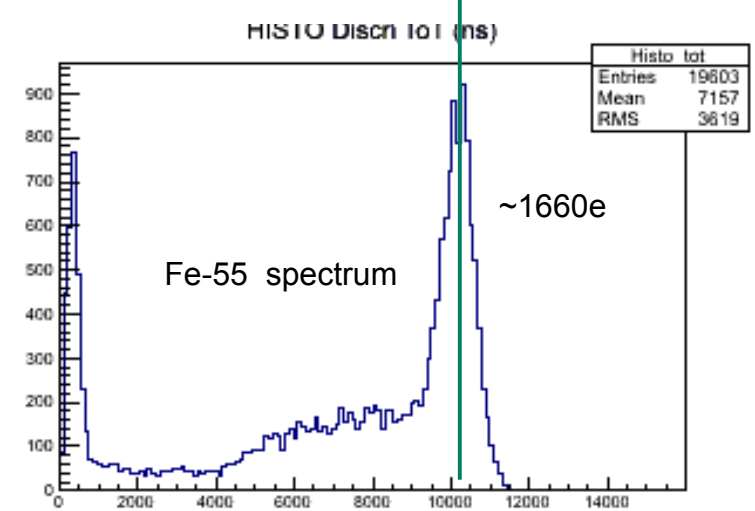
Sr-90 MPW corresponds to ~ 900mV injection amplitude

HV2FEI4: irradiation

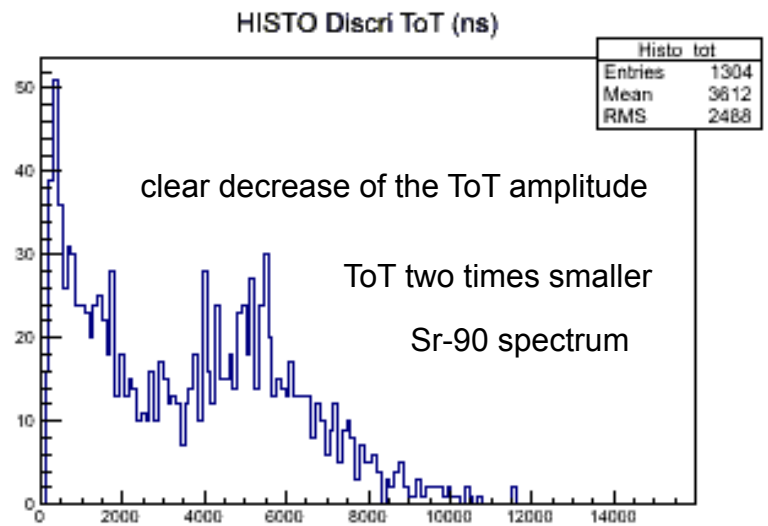
- Irradiations at CERN/PS, with reactor neutrons and with x-rays
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation

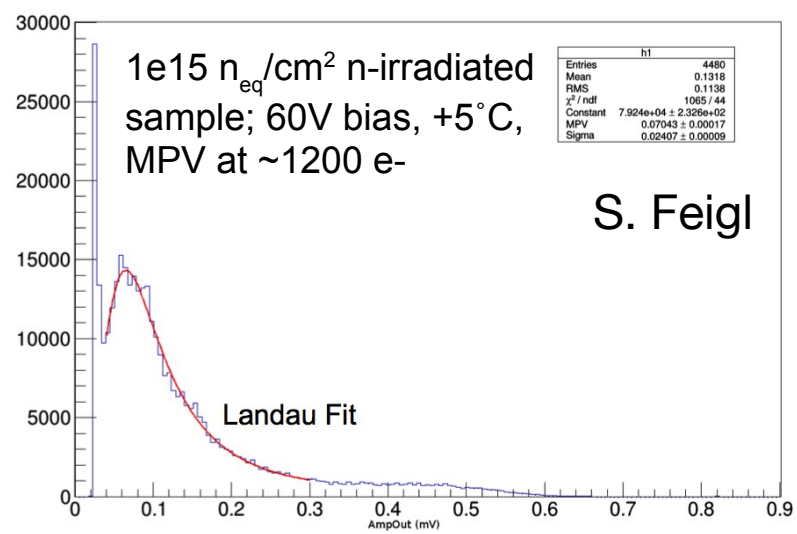
un-irradiated device





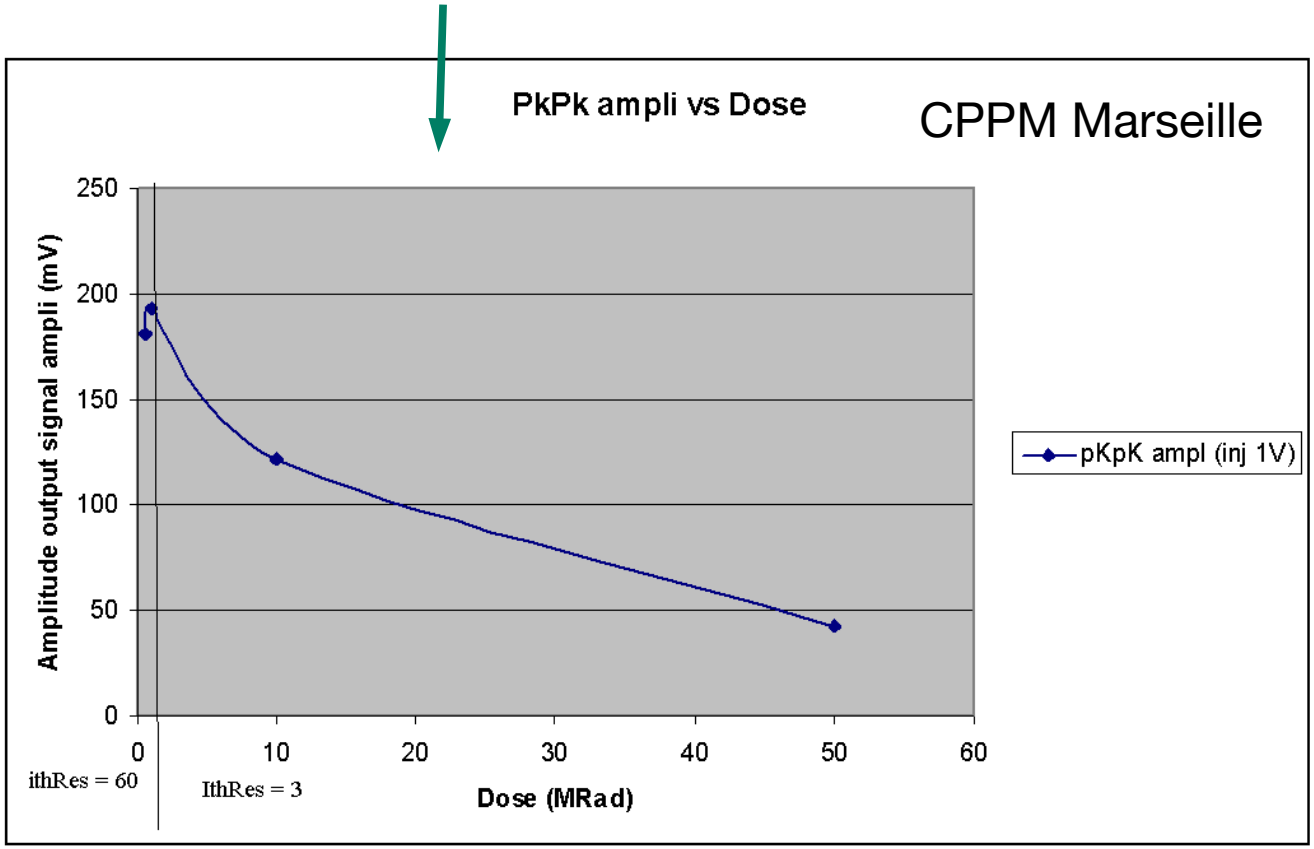
CCPD9 irradiated at 80 MRad





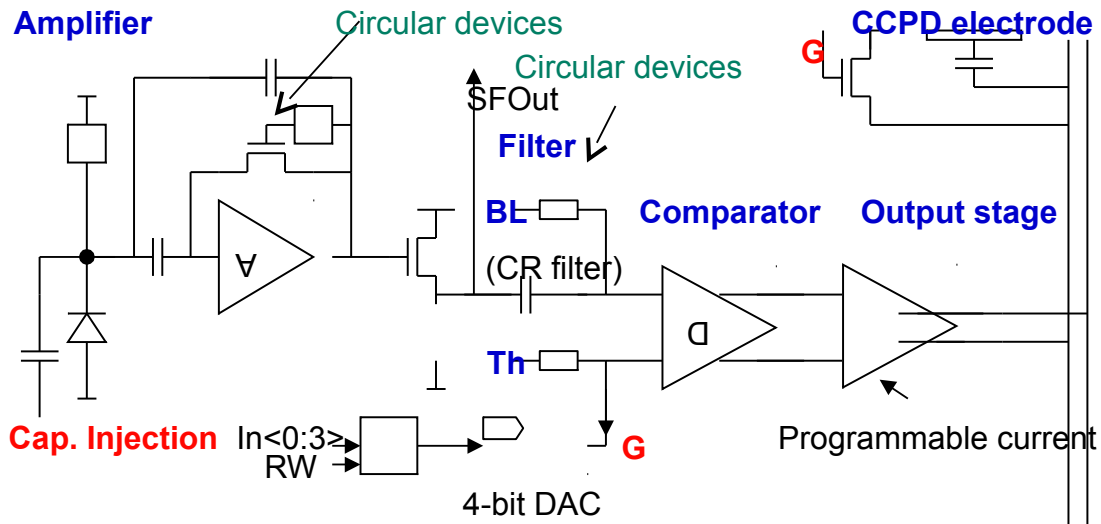
HV2FEI4: irradiation

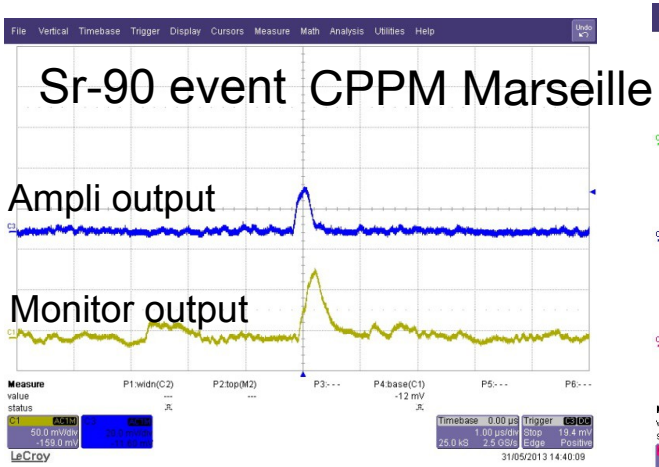
- First irradiations conducted at CERN/PS and with an x-ray tube
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation
- clear radiation effects seen after proton and x-ray irradiation
  - drop in amplitude/amplification
  - also seen with test pulser input → electronics effect, rad-soft design

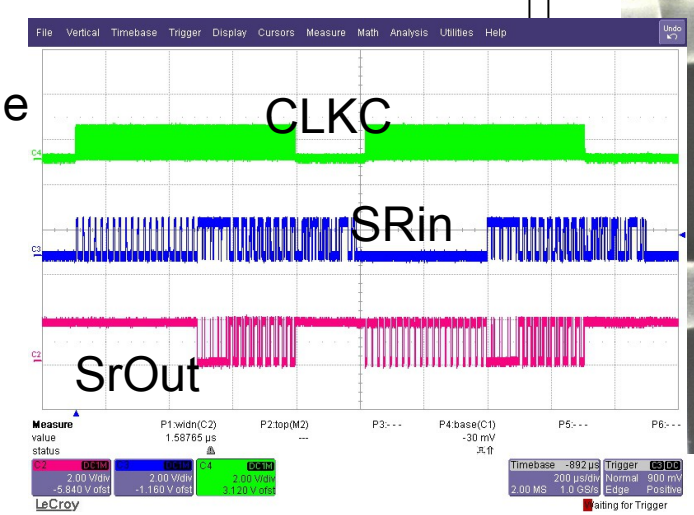


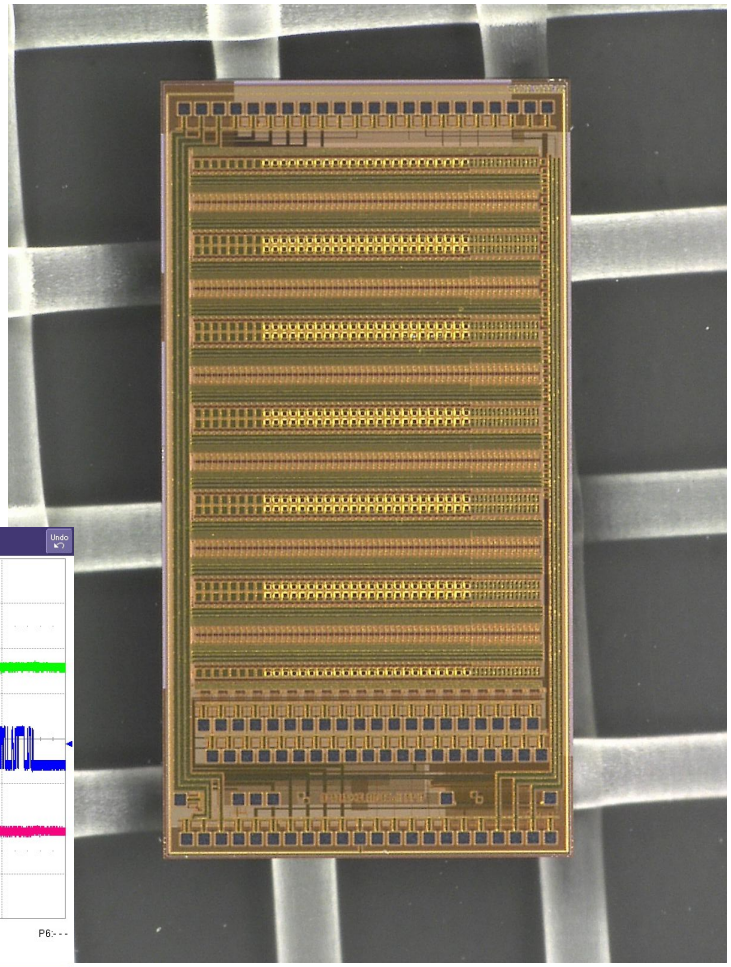
Rad-hardness: consequences

- deliberately chose “standard” design to see how far it would get
  - not far enough... → “harden” design by guard rings, circular transistors, …
- HV2FEI4_v2 contains “fully” rad-hard design at the cost of higher noise





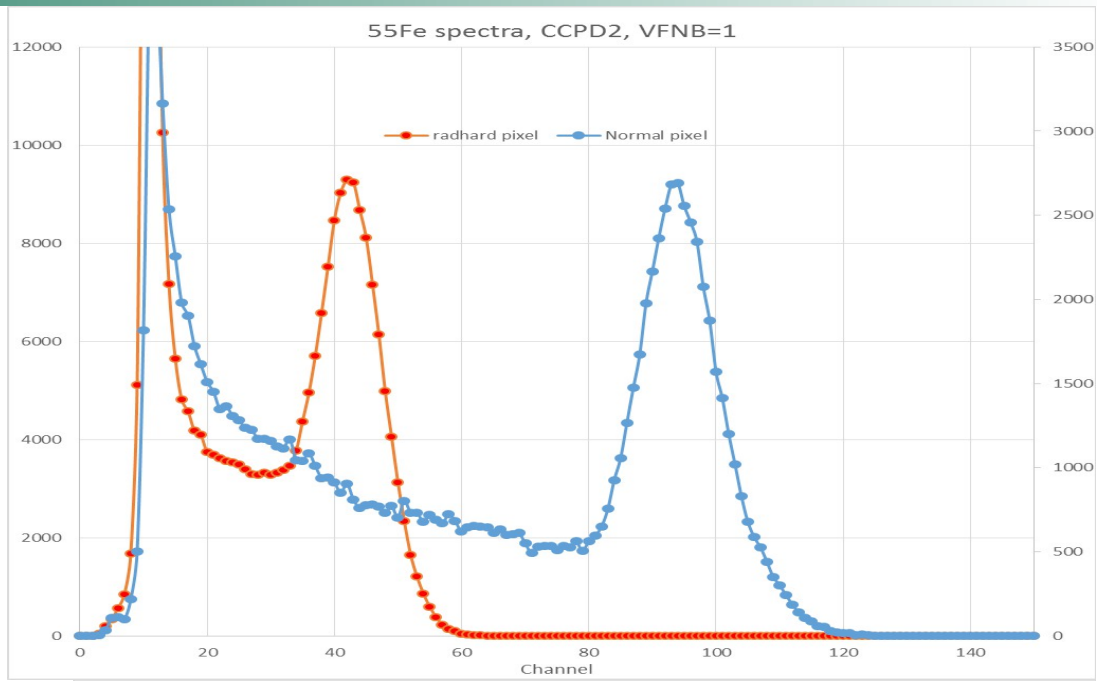


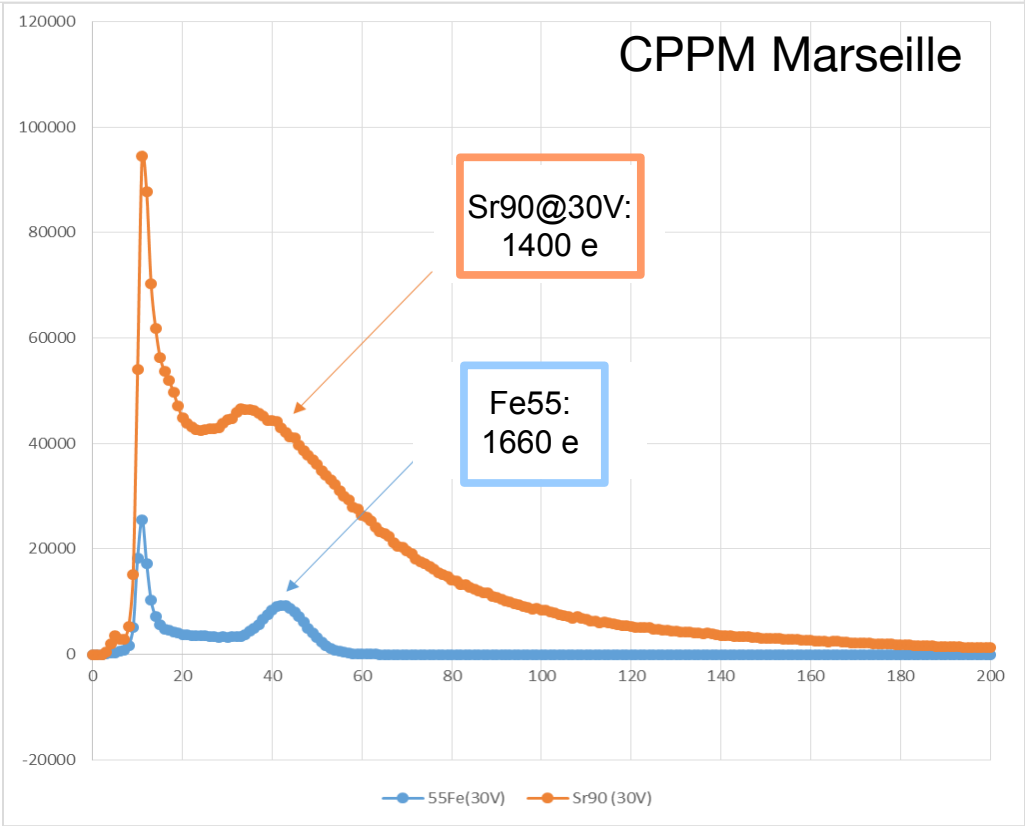


HV2FEI4_v2

- Circuits generally optimised for rad-hardness, but 2 different designs tested:
  - "normal pixels": mainly added guard rings around transistors
  - "rad-hard pixels": all relevant transistors circular

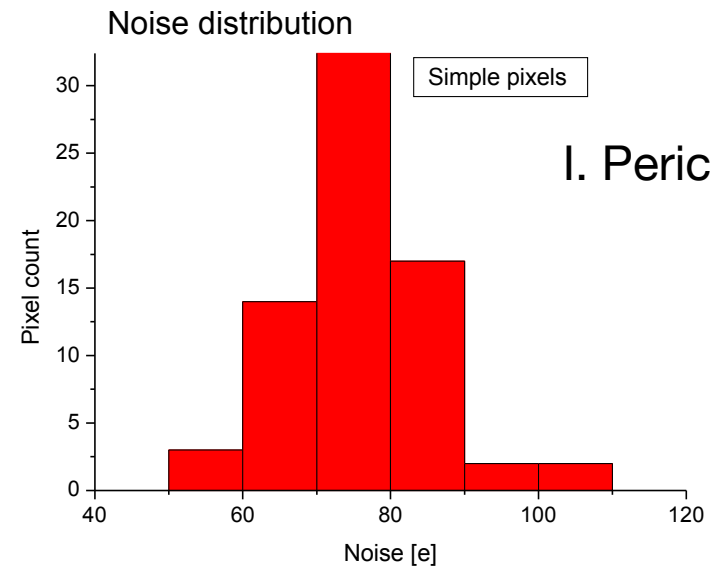
    → more capacitance, lower gain at identical settings
- More measurements:
  - Sr-90 at 30V now at ~1400e

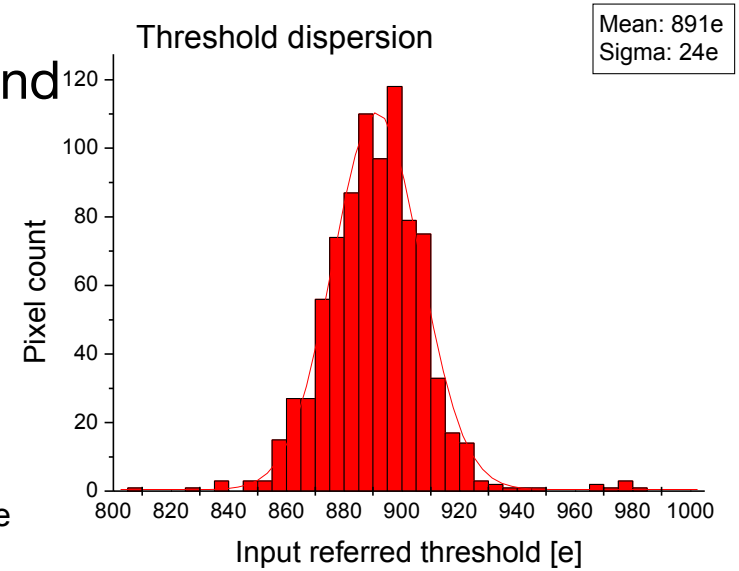


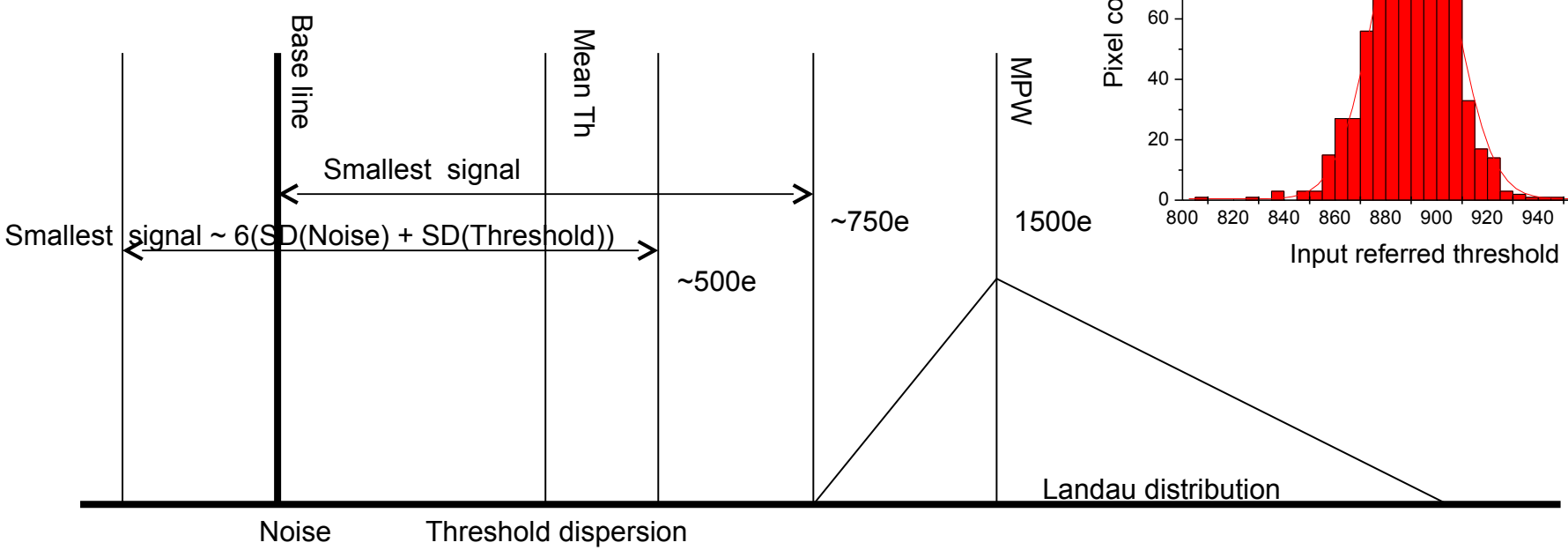


HV2FEI4_v2

- Noise inferred from threshold scan, now around 75e
- Threshold tuning implemented, threshold dispersion sigma ~25e
- Fundamentally, the treshold is required to be lower than low energy end of the MIP landau
  - usually MPW/2 is specified
  - looks promising (achieved thresholds of around 400-500 e^-), but still work to do



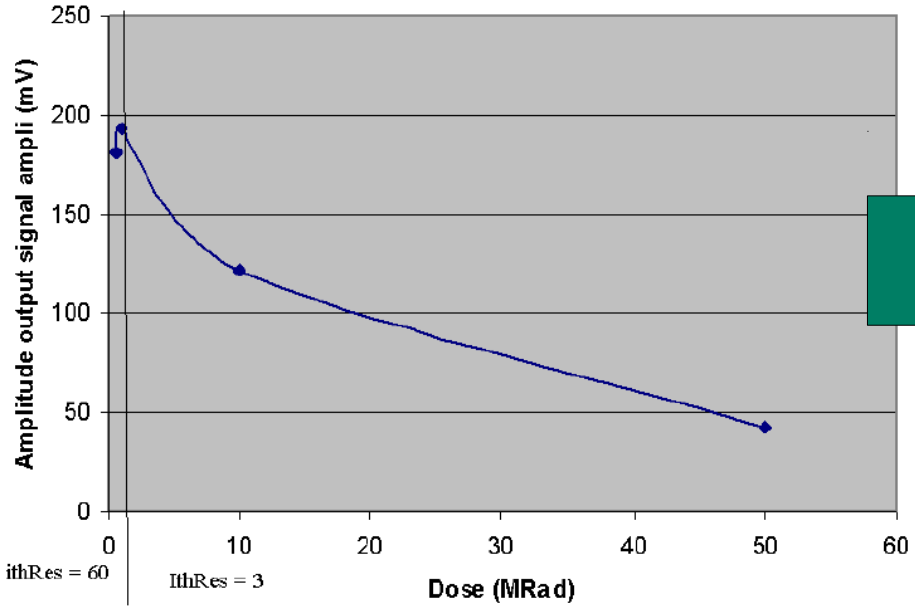


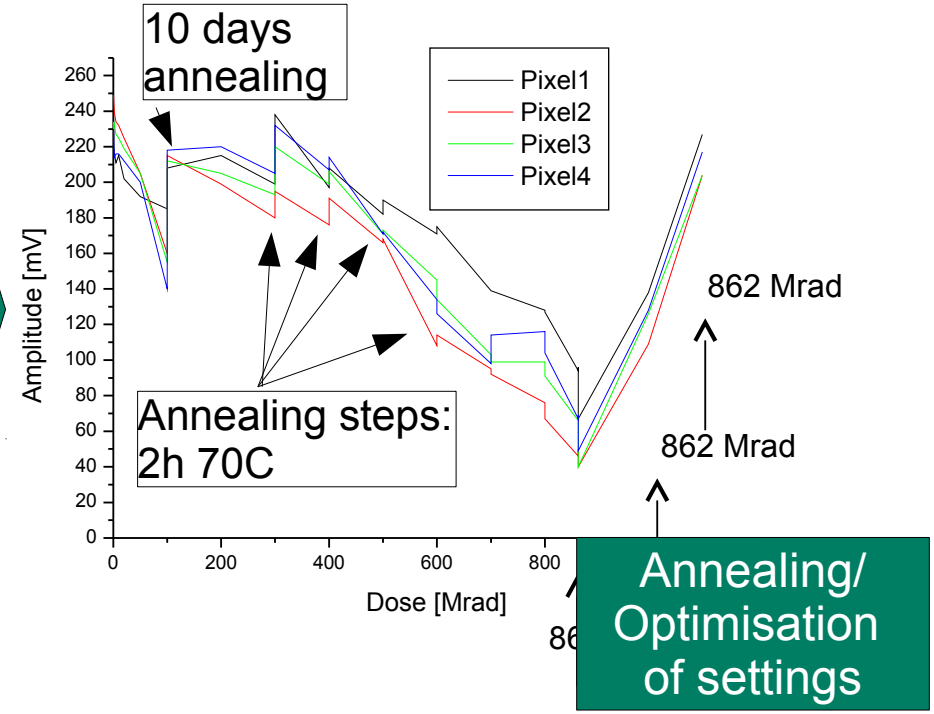


HV2FEI4_v2: rad-hardness

- Radiation effects due to dose, could be reproduced by x-ray irradiation
  - CERN PS currently down, but x-ray tube available
  - very fast irradiation, requires annealing to be mimic realistic dose rate
- Signal amplitude clearly much more stable
  - irradiated up to 862 Mrad (!), drop visible after ~500 MRad
    - dose rate effect, annealing brings signal back to ~100%

➔ rad-hardness significantly improved, hadron irradiations to follow





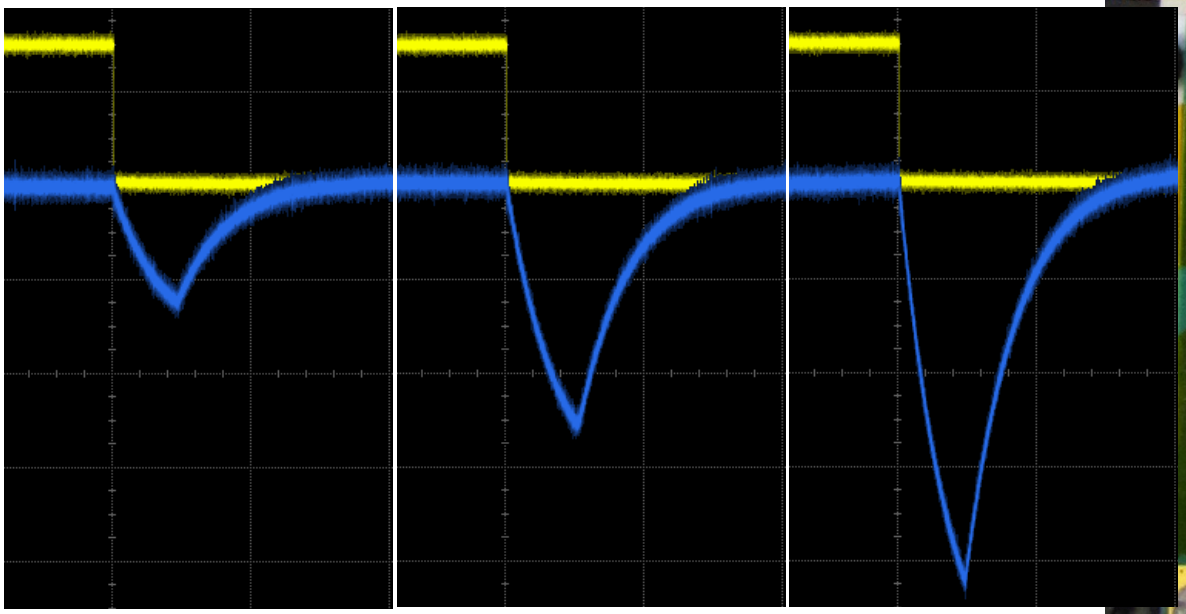
CCPD1 irradiated with x-rays
Amplifier gain loss

CPPM Marseille

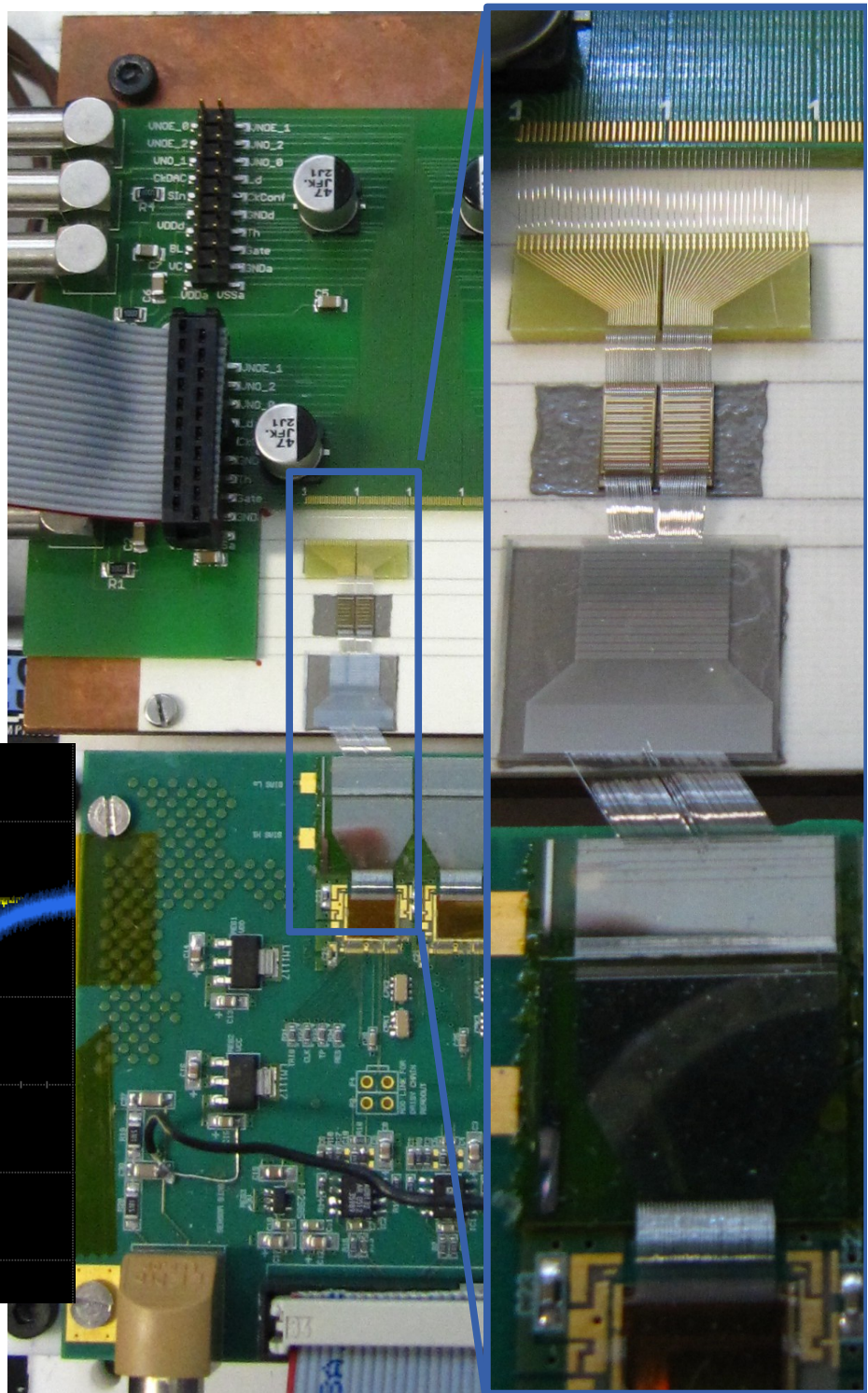
CCPD2 irradiated with x-rays
Amplifier gain loss
Rad hard pixels

HV2FEI4: strip readout

- Beetle/Alibava readout had issues with noise/common mode pickup
- configuration worked, “strips” could be switched on/off
- however, position-encoding works:
  - monitor output on scope
  - same principle on strip readout pads
- Supply PCB design changed
  - threshold now at reasonable values

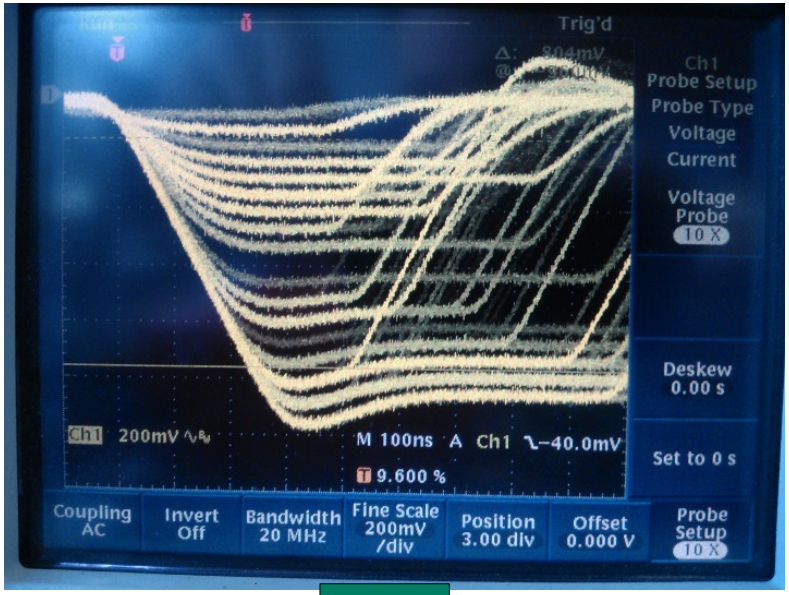


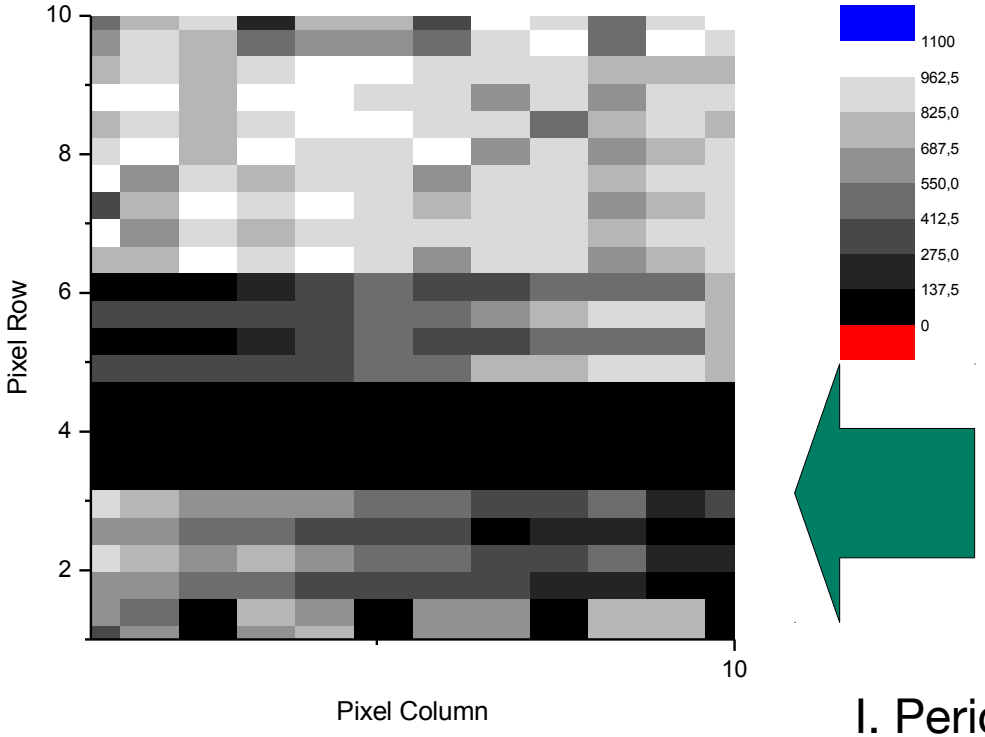
Row 0 Row 12 Row 23

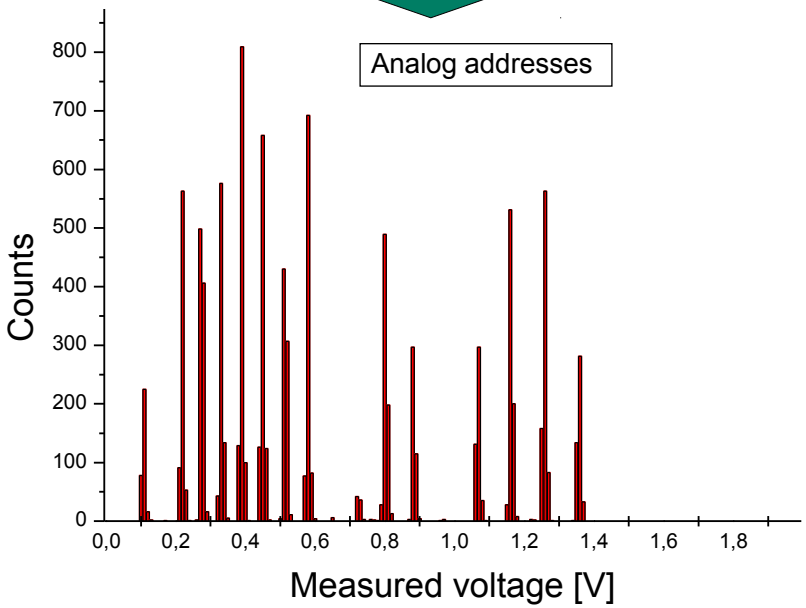


HV2FEI4_v2: strip performance

- First measurements again using an oscilloscope
- Fe-55 source illuminating a wire
  - shadow ~visible in pulse heights
  - can be decoded to give a pixel hitmap using only strip information



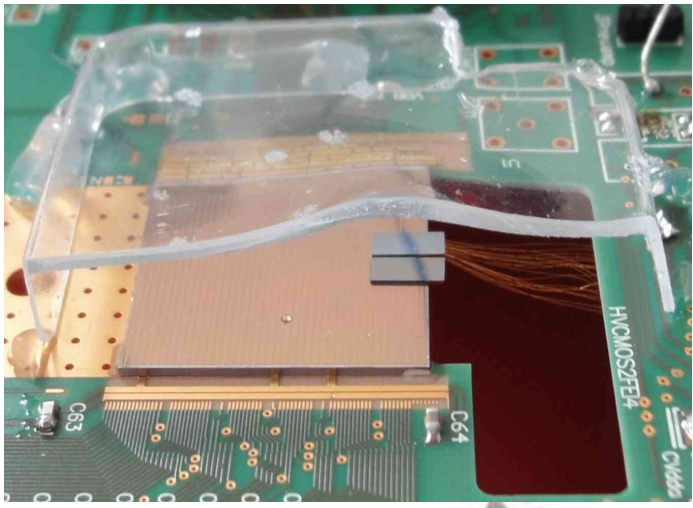


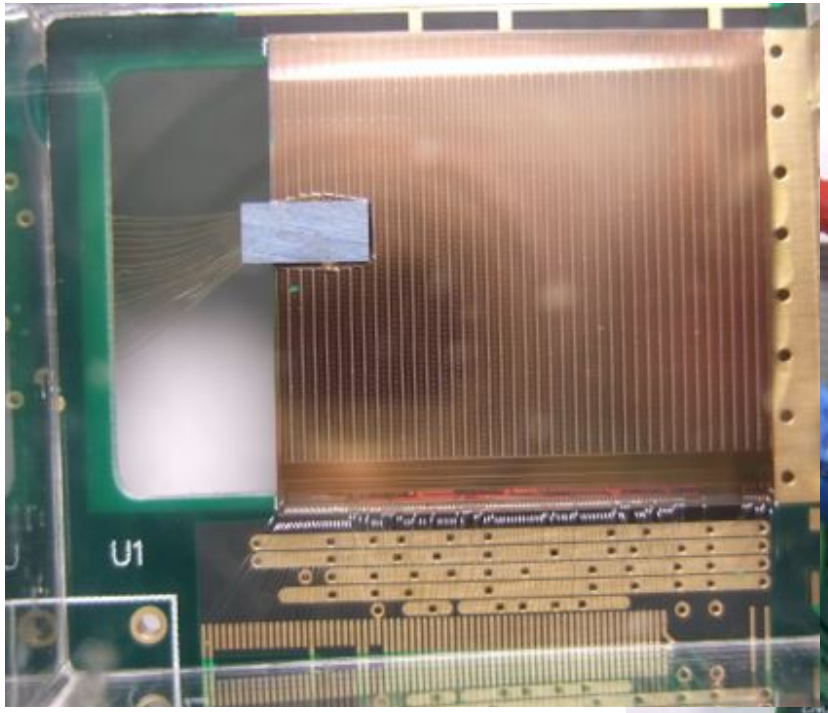


I. Peric

HV2FEI4: Pixel readout

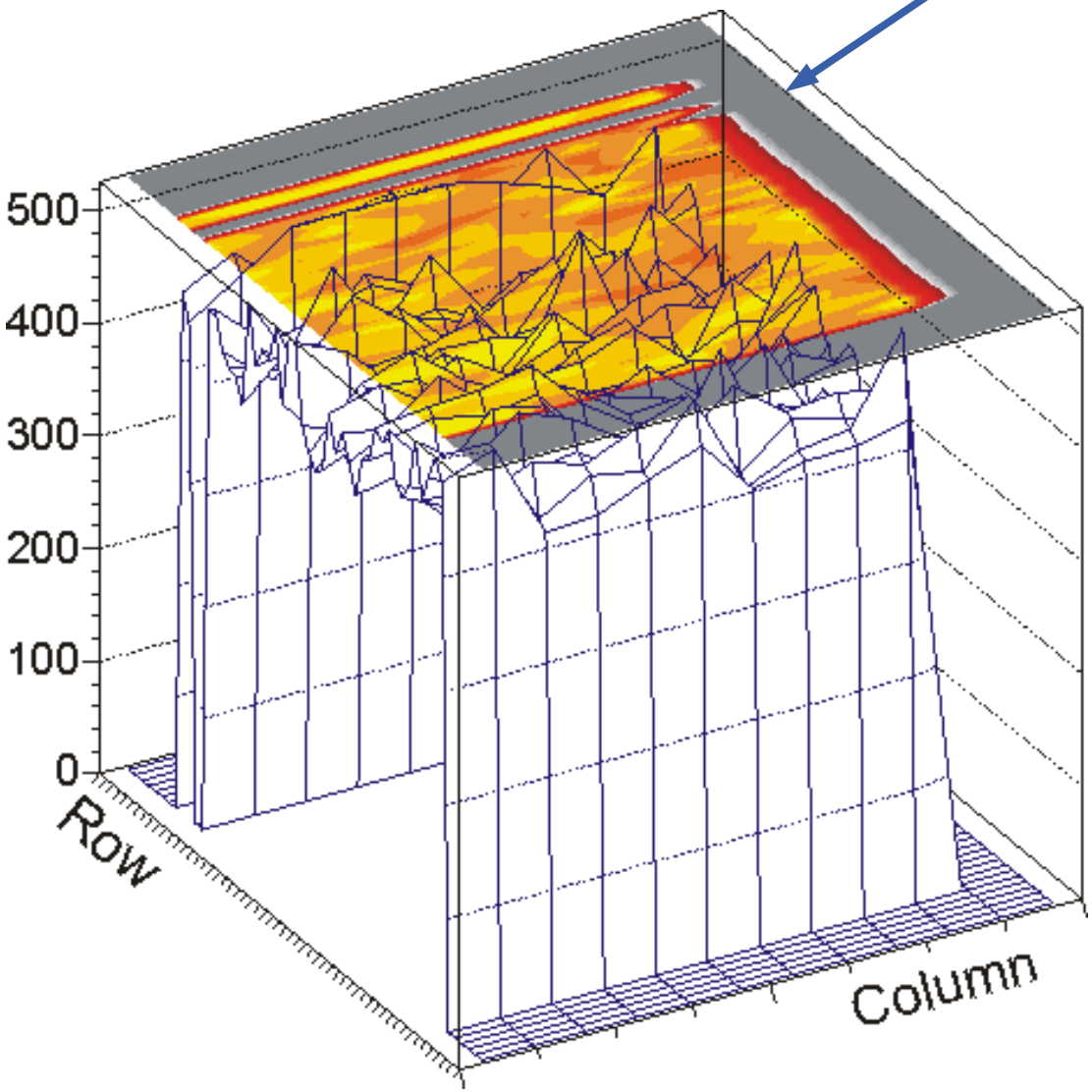
- Several HV2FEI4s glued to FE-I4A and FE-I4B
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps or TSVs later

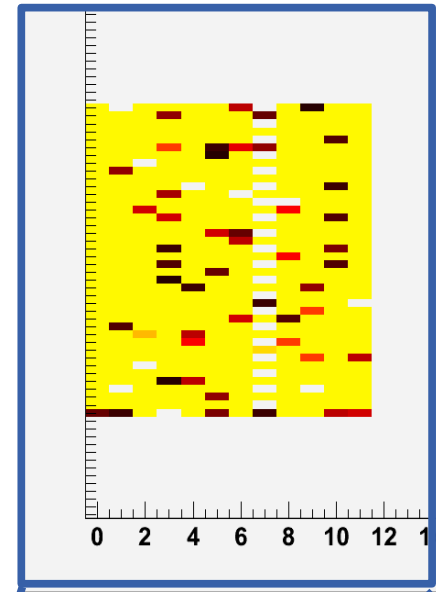


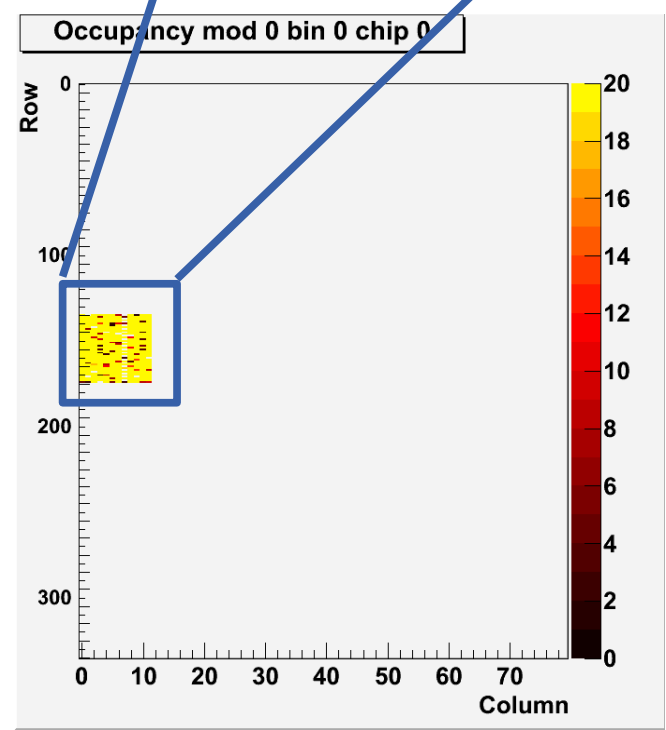


HV2FEI4: Pixel readout

- First measurements:
  - FE-I4A (w/ bumps) sees HV2FEI4 being glued to it
  - Physics (^{22}Na source) is seen by FE-I4B (w/o bumps)

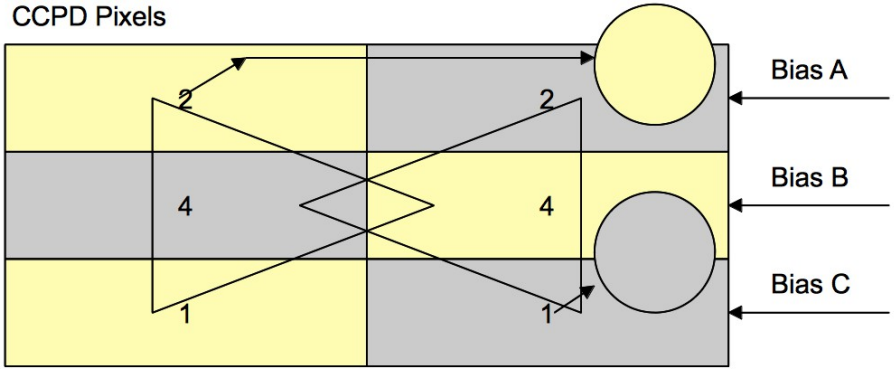


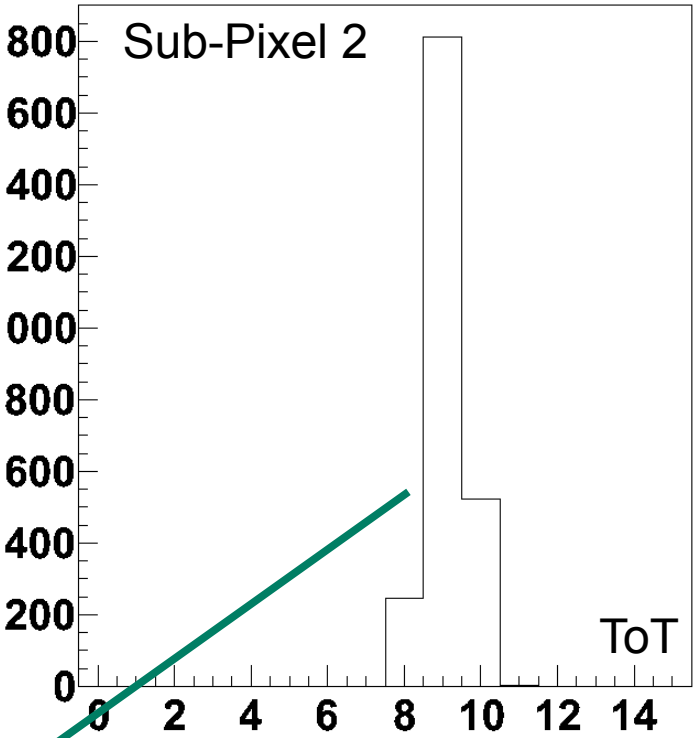




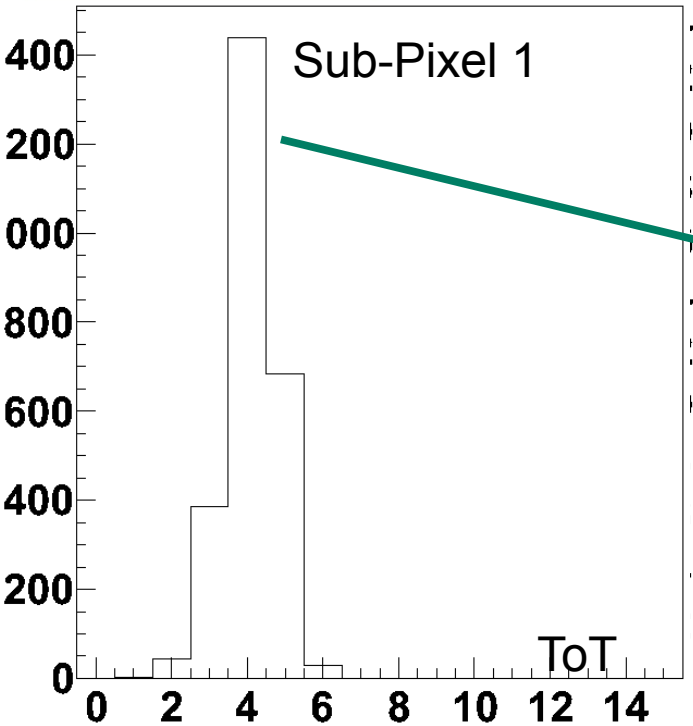
HV2FEI4: Pixel readout

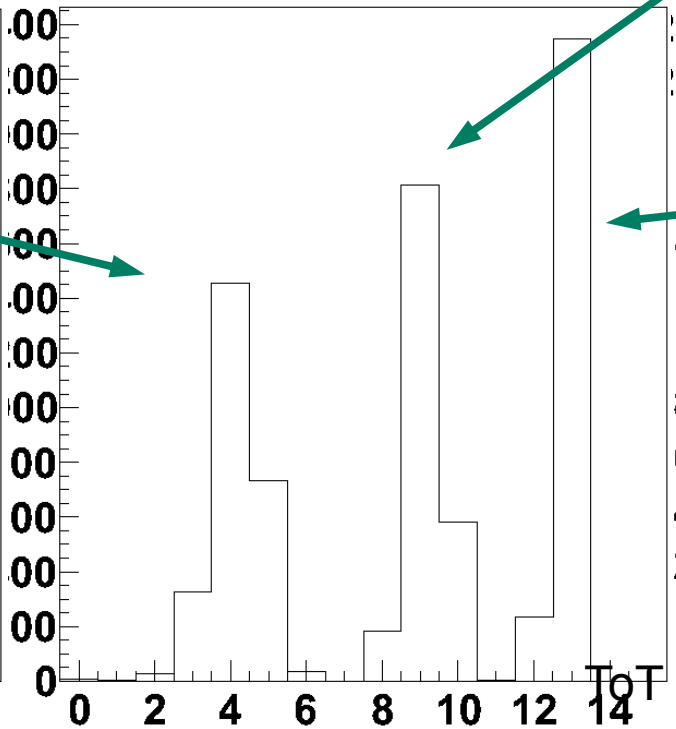
- ToT encoding:
  - 3 sub-pixels clearly distinguishable
    → sub-pixel encoding works!
  - to do: dynamic range matching, array tuning

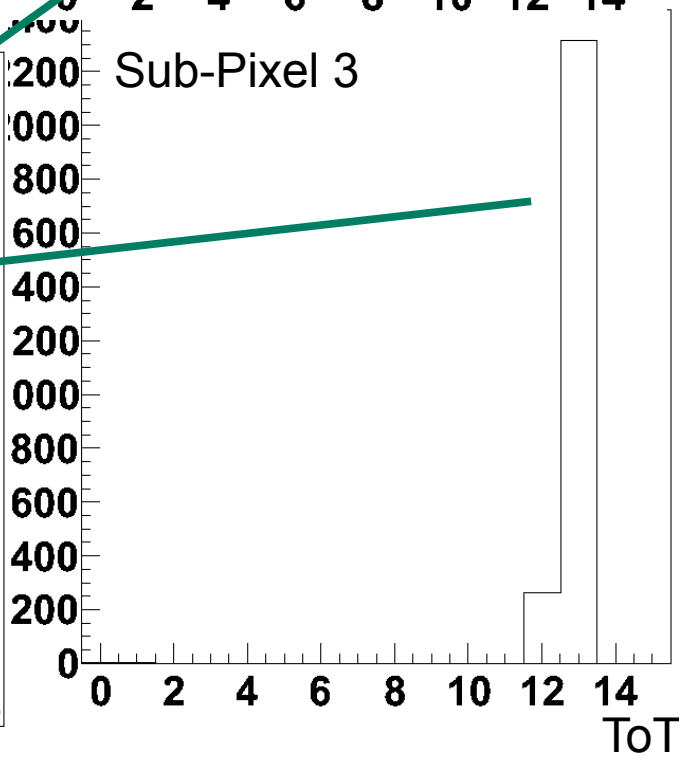




All on

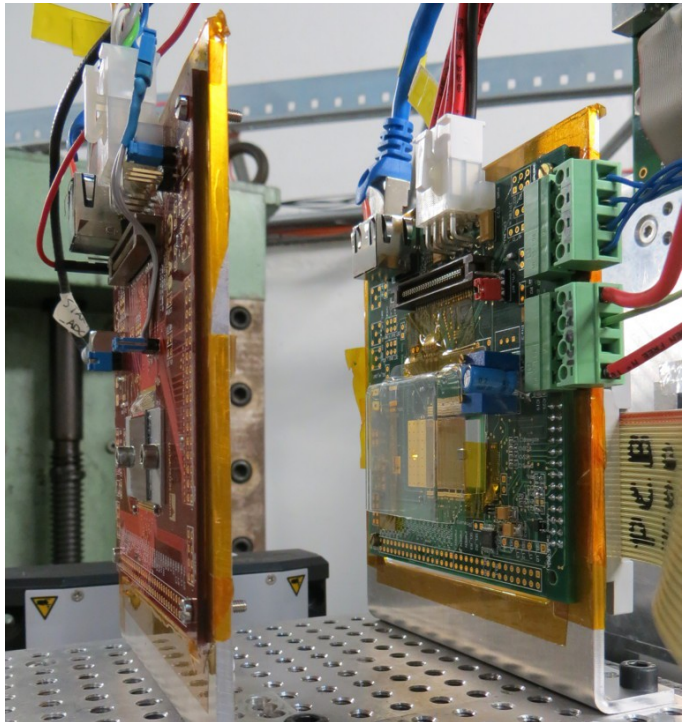


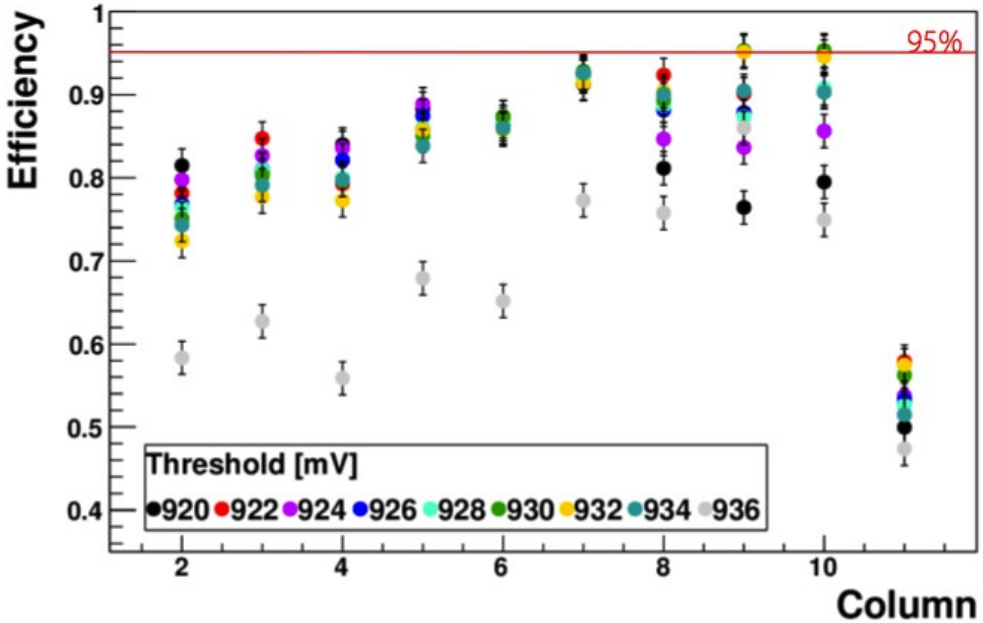


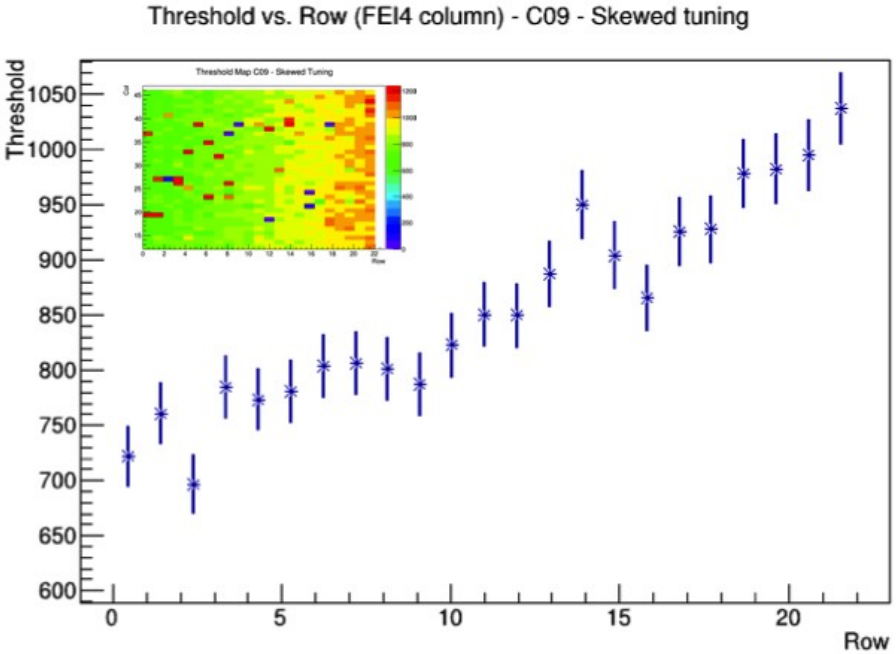


HV2FEI4: Pixel readout in testbeam

- First data taken at 2013 DESY testbeams
  - unirradiated and reactor neutron (JSI) irradiated devices: 1e15 neq/cm2
  - complex geometry complicates alignment
  - non-optimal tunings lead to less efficiency
    - tuning procedures quite fresh at time of testbeam
    - unintentional “skewed” tuning: ~700-1000 e-
    - resulting efficiency unirradiated: ~95-80%

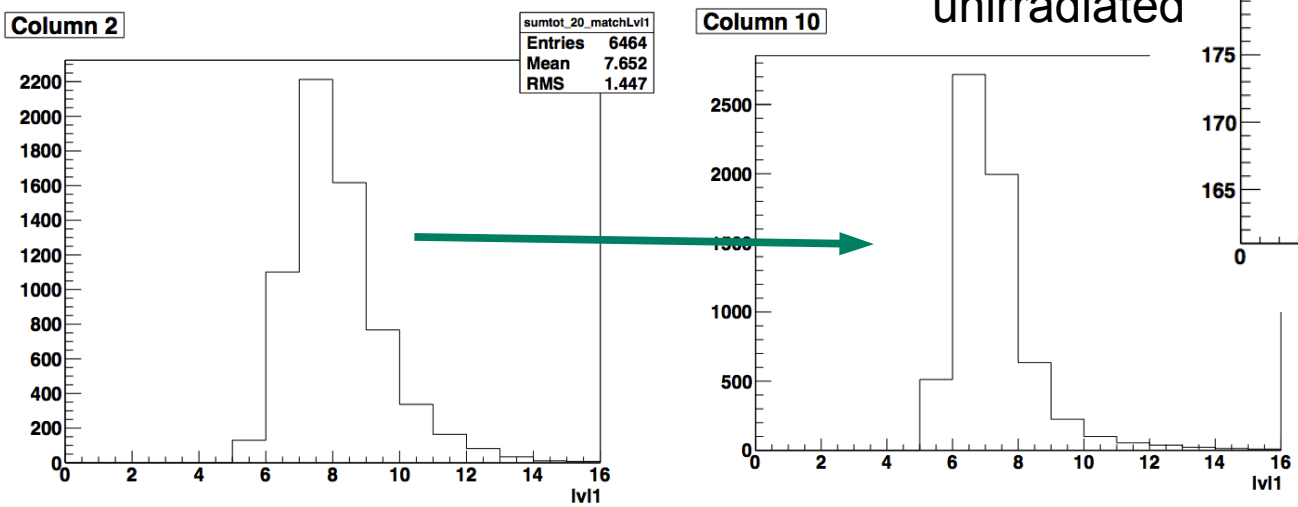




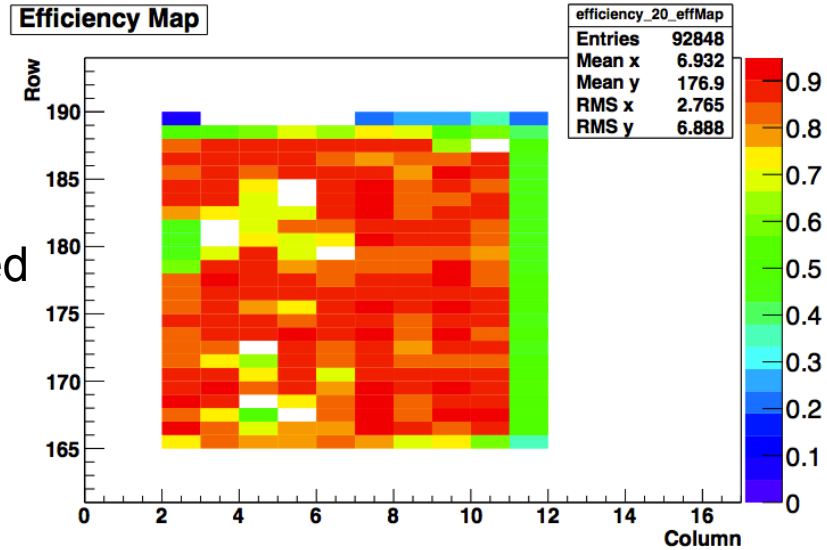


HV2FEI4: Pixel readout in testbeam

- First data taken at 2013 DESY testbeams
  - time-walk depending on threshold – low threshold → better timing

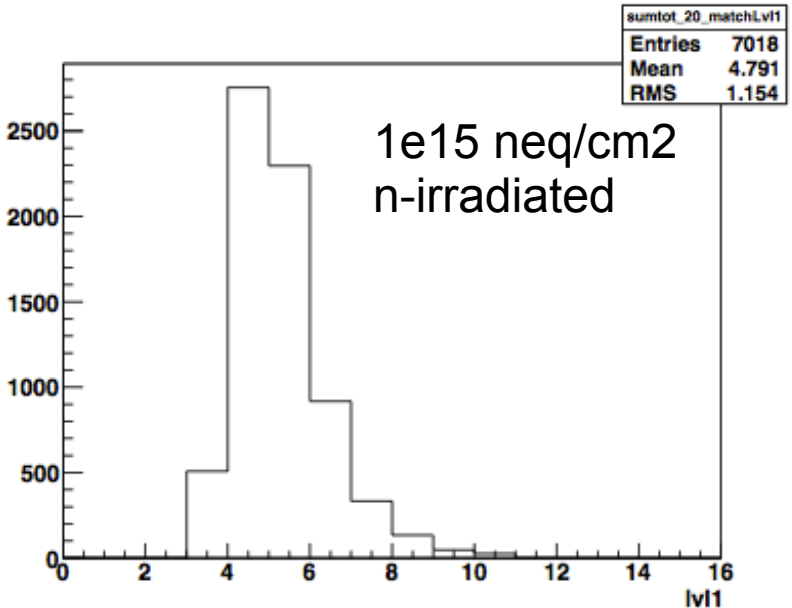


unirradiated



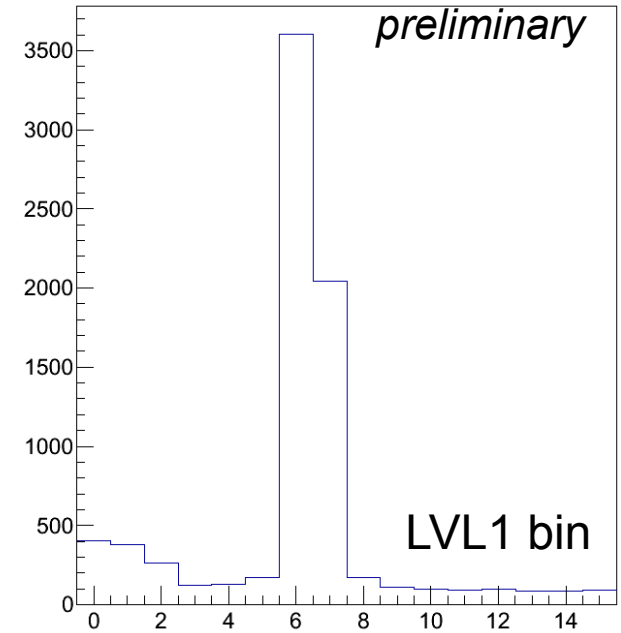
  - irradiated sample shows strong HV-dependence of efficiency, timing similar

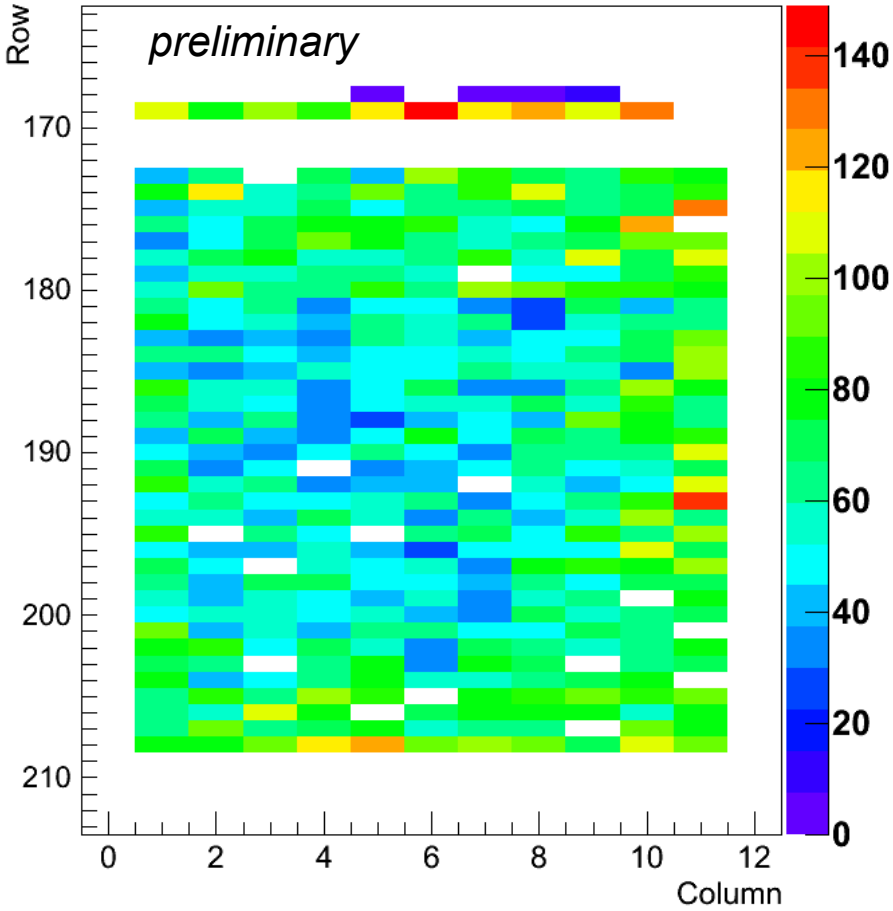
Runs	HV [V]	Trigger	Tracks	Eff
230-232	-57.6	566k	6011	62.9%
224-225	-48.0	517k	10993	54.8%
233-235	-38.4	551k	9783	64.0%
236-238	-28.8	543k	437	51.7%
239-241	-19.2	543k	2590	38.2%
242-244	-9.6	587k	6804	28.2%
245-247	0.0	553k	8969	12.5%

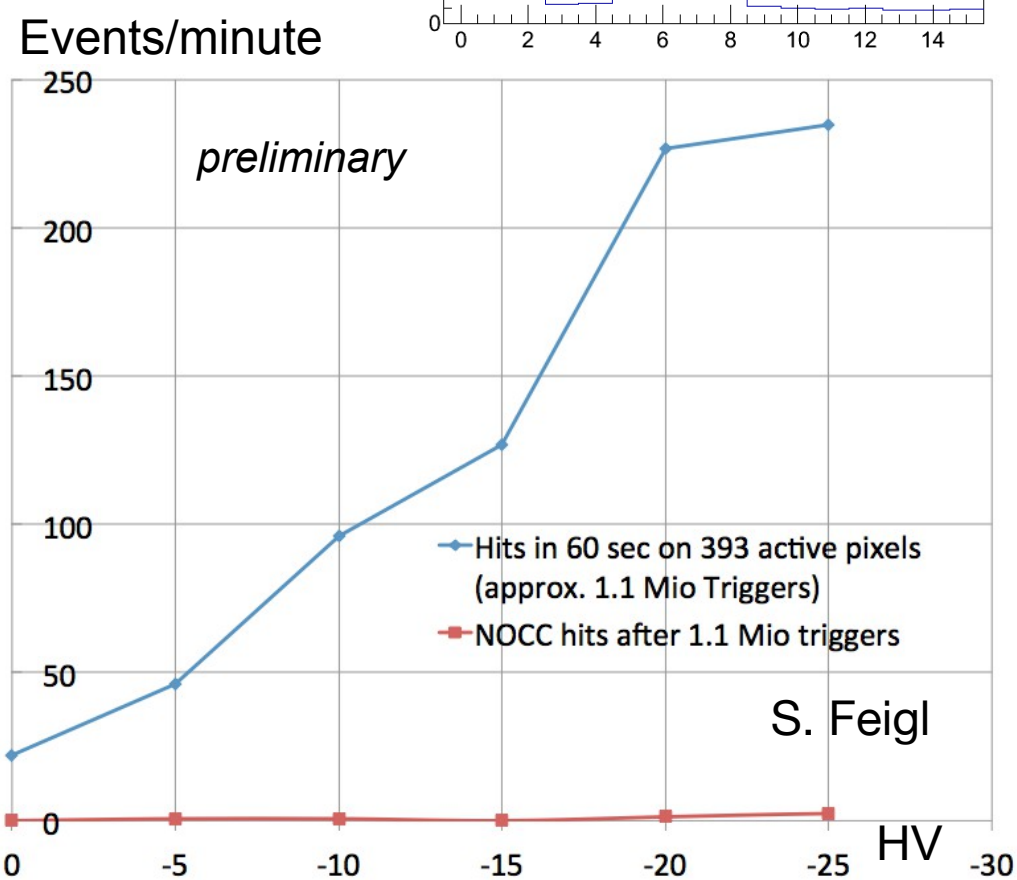


Irradiated behaviour: 1e16 n_{eq}/cm^2

- measurements with scintillator trigger
  - makes sure we select MIP-like electrons
  - avoids “noise” triggers
  - rate rises with HV as expected, but (rate) saturation not yet seen → go higher in HV, cool
- next steps: calibration, cooled operation

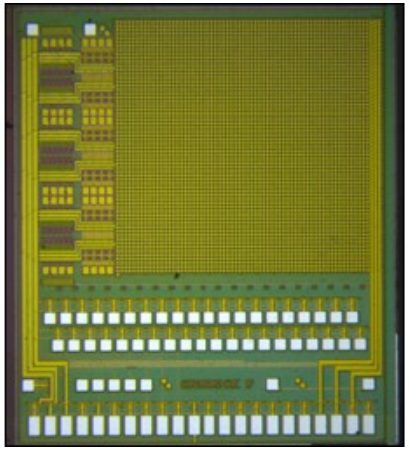


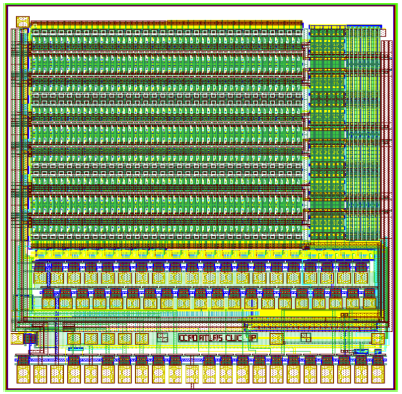


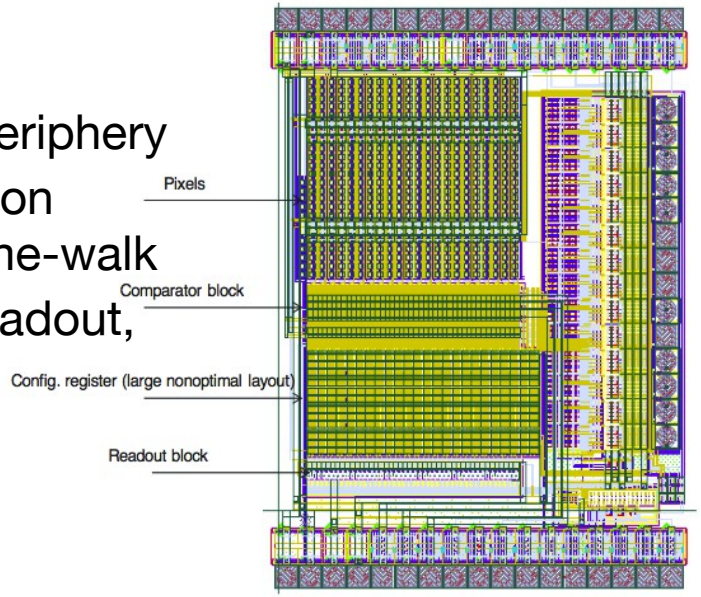


Future plans

- Submissions:
  - H18_v3
    - shared with CLIC, contains Amplifier-only 25x25µm pixels and some ATLAS test pixels
    - first measurements indicate good noise behaviour in particular of CLIC-pixels
    - dedicated passive eTCT-diode and test structures, measurements being prepared
  - H18_v4
    - focused on ATLAS-pixel readout, several noise improvements, segmented pixels, analogue pixels (25x250µm), pulse-width encoding of sub-pixel address promising better ToT encoding
  - H35_v1
    - analogue 40 x 400 µm pixels with traces to the periphery
    - discriminator block contains also “constant fraction disciminator”-like circuits aiming for improved time-walk
    - digital encoding, followed by 320 MBit/s LVDS readout, two concurrent hits can be read out
    - several test structures for rad-hardness testing





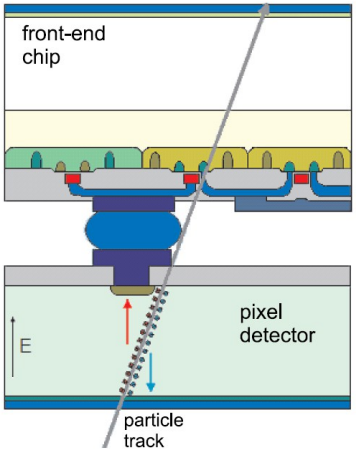


Future plans

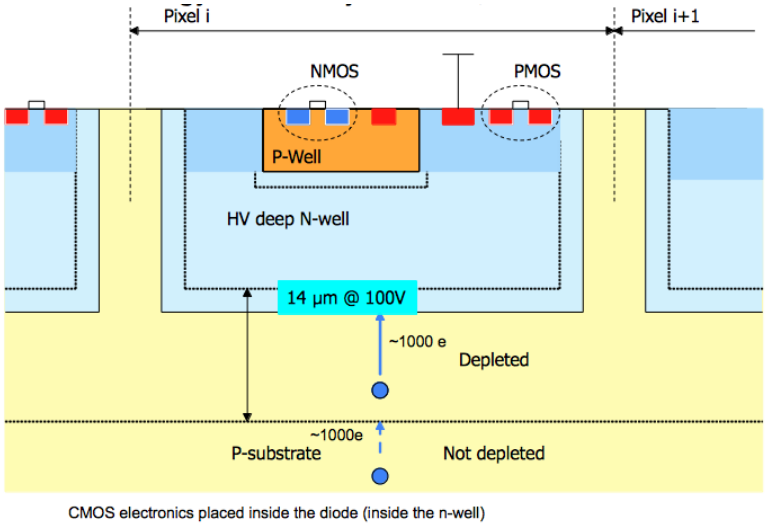
- More pixel assemblies being put together
  - some unirradiated for technology development
  - some n-irradiated HV2FEI4_v2 assemblies for testbeam study
  - some HV2FEI4_v3 to have a first look at analogue pixels with FE-I4
- USBPix is being modified to enable configuration only with USBPix/STControl
  - makes implementation of scans much easier
  - will probably enable sub-pixel disentanglement for the whole matrix without the need for pixel-by-pixel analysis
- further submissions are being discussed
  - higher resistivity wafers
  - full-size submissions for strips and pixels

HR-CMOS

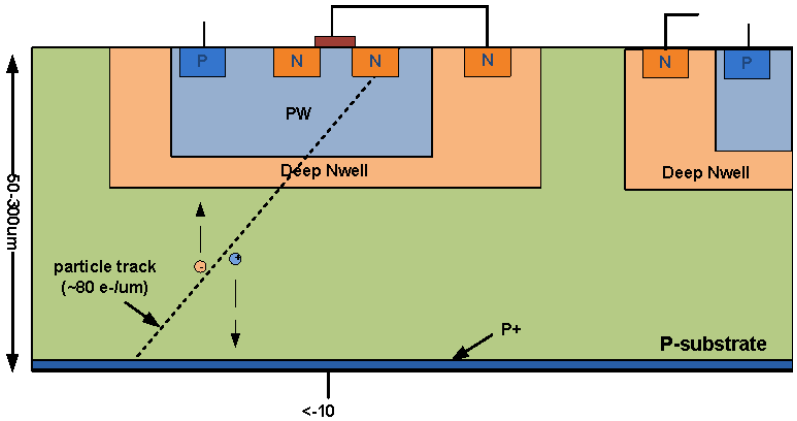
- As mentioned, main requirement for drift-based MAPS is a deep n-well
- Higher substrate resistivity would allow for full depletion
  - certainly larger initial signal, reduction of depletion depth to be studied
  - charge sharing possible again allowing for higher resolution at low fluences
- Several CMOS imager processes available from different foundries
  - back-side illumination requires full depletion and thin sensors
  - high-resistivity FZ base material available in an industrialised process
- HR-CMOS efforts started at University of Bonn
  - several foundries and processes
  - some first preliminary results available



Hybrid



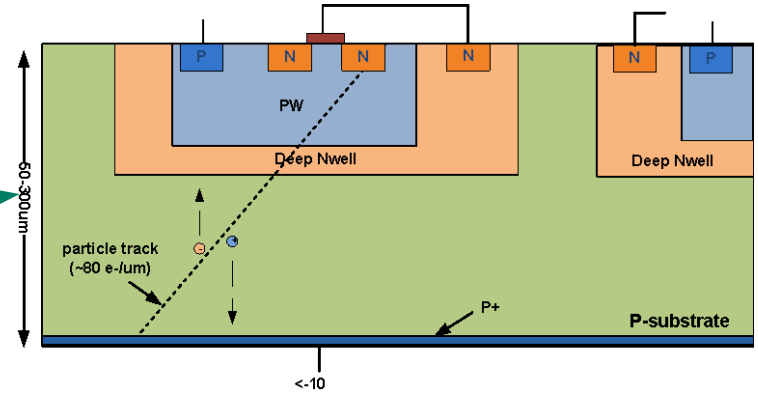
HV-CMOS

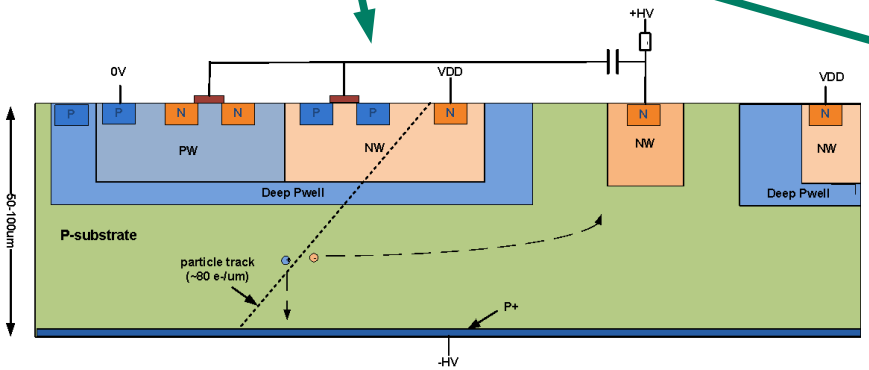


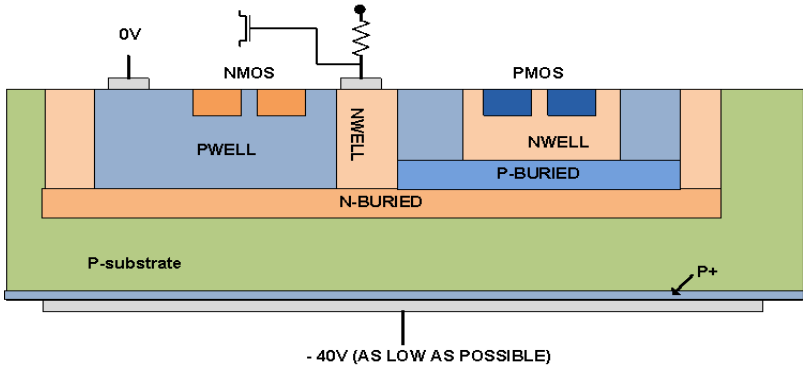
HR-CMOS

HR-CMOS

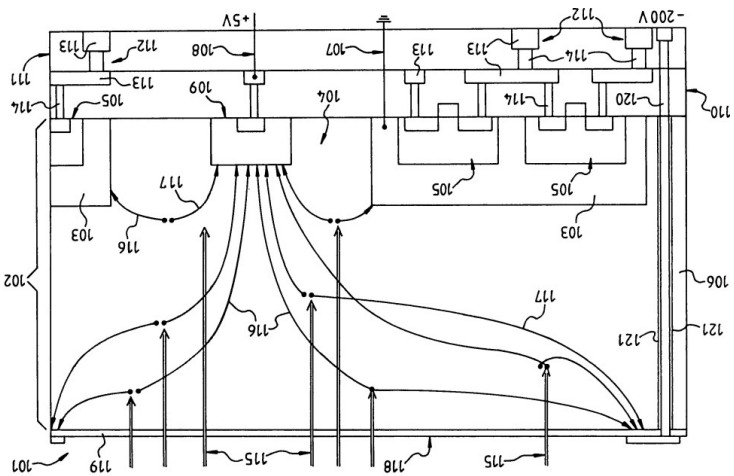
- Many different designs possible:
  - HV-CMOS like (deep n-well, no triple-well)
  - triple-well
  - Alice-like

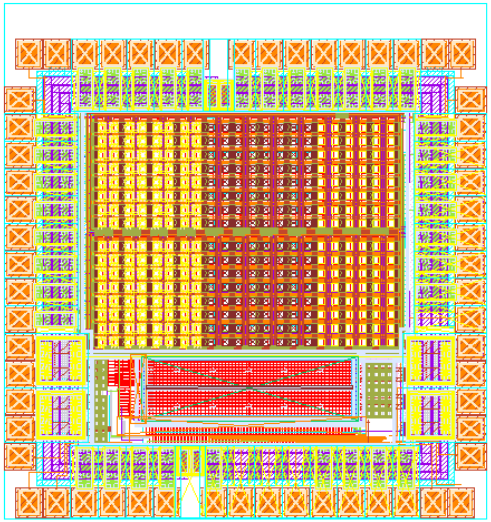


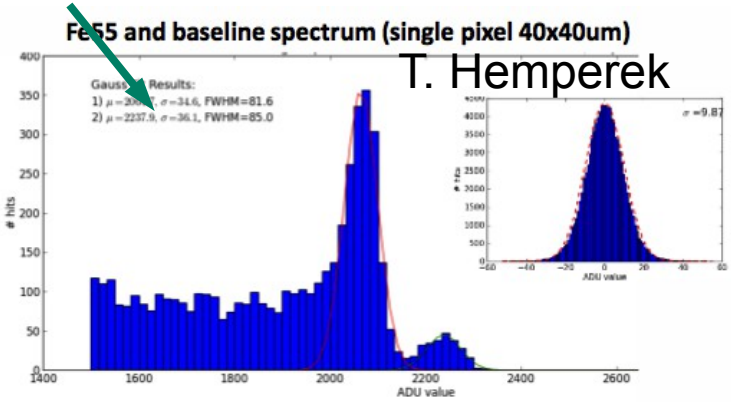




- First prototypes back from ESPROS, see physics
  - characterisation, irradiations to follow



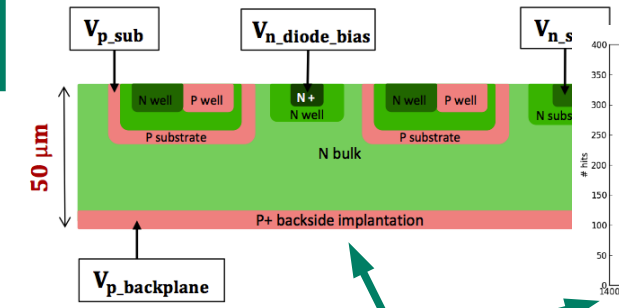


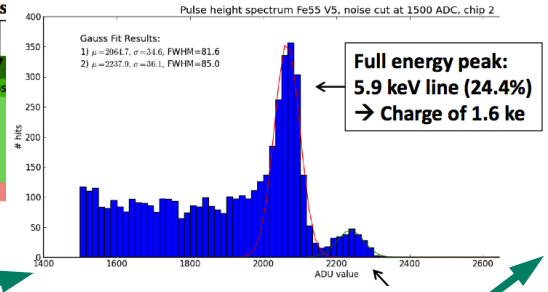


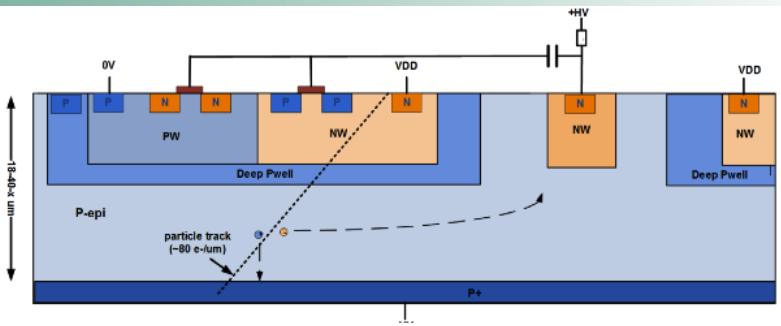
T. Hemperek

Gain: ~ 100 µV/e (200 mV ~ 2 ke)
Power: ~5uW
Peaking time: <25ns
Sahping time: ~200ns-2us (for continous reset)

CMOS-based sensors





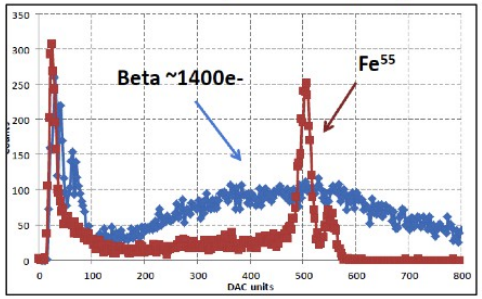


CMOS vendors considered (providing full depletion)

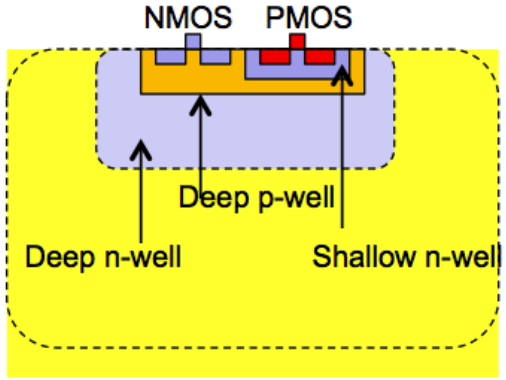
- Vendor A: 150nm, 2kΩ-cm n-bulk, 50µm thick
  → MPW submitted Q4 2012, testing ongoing; MPW submitted Q1 2014
- Vendor B: 180nm, 1kΩ-cm p-bulk + epi (various)
  → submitted Q1 2013, preliminary results
- Vendor C: 180nm, SOI HV process,100Ω-cm p-bulk
  → MPW submitted Q1 2013, preliminary results
- Vendor D: 130nm, 3kΩ-cm p-bulk
  → MLM (full wafers) submission in preparation
- Vendor E: 150nm, 2(4-5) kΩ-cm p-bulk, >50 µm possible
  → MLM submission in preparation

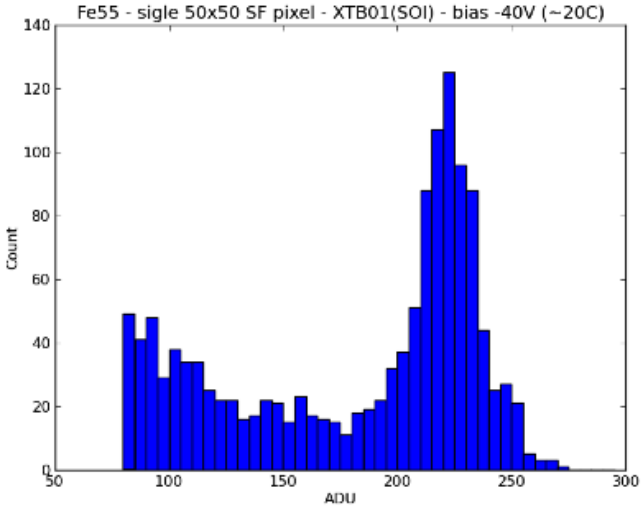
L. Gonella,
T. Obermann

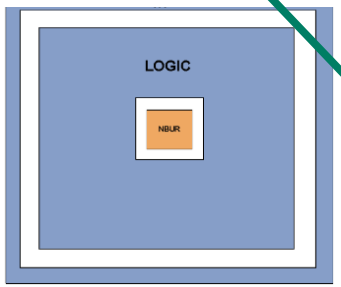
Sr^{90} and Fe^{55} Spectra for 18µm epi

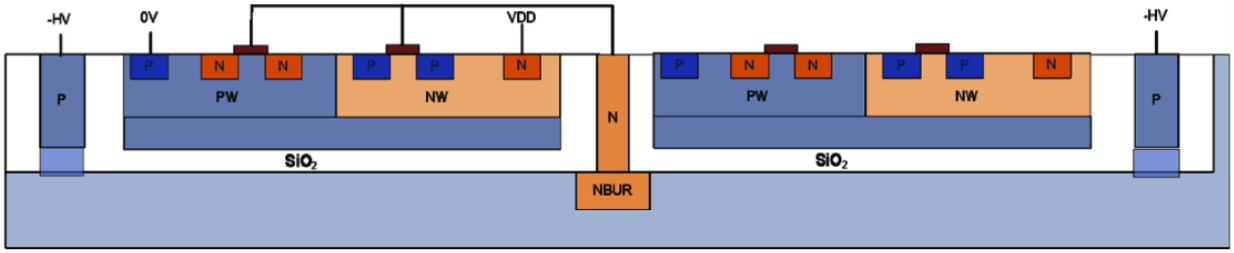


Testing:
M. Kachel (IPHC)



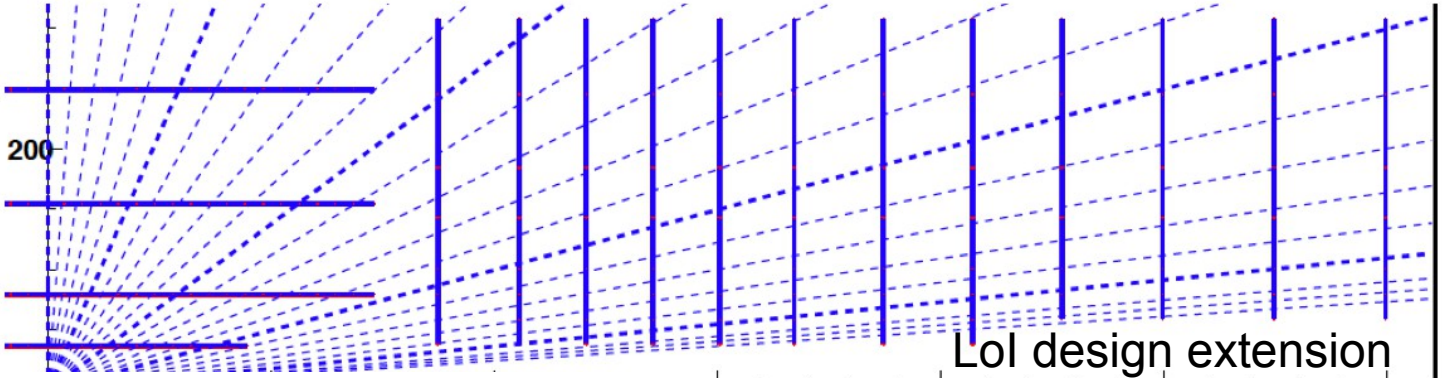






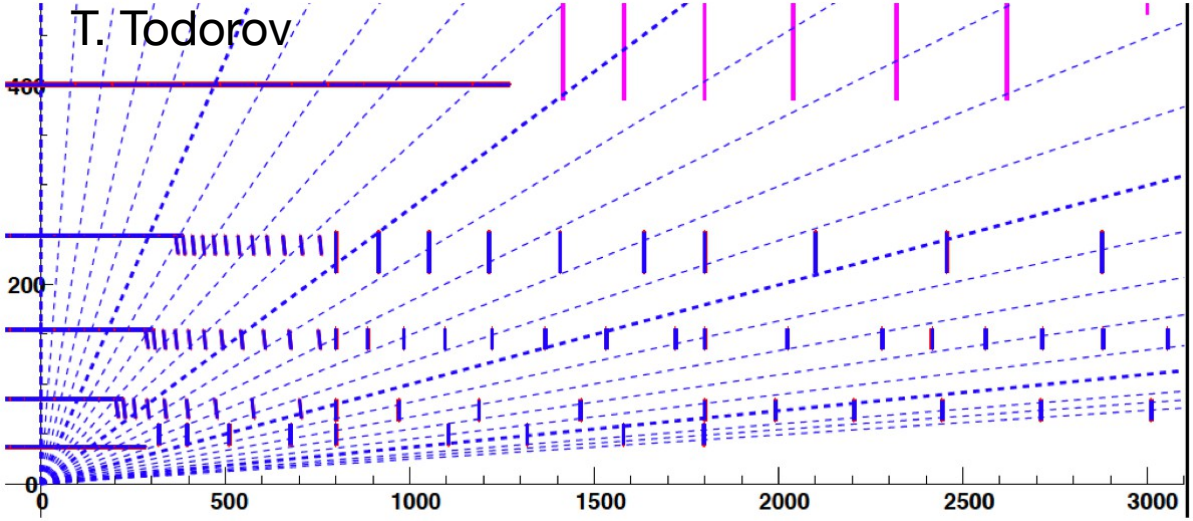
Case study: Very forward tracking

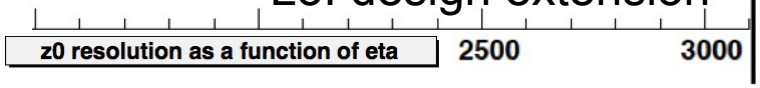
- Limitation to pseudorapidity of eta = 2.5 inappropriate wrt VBF/VBS
- Design studies ongoing for an extension to eta~4 (phase 2 upgrade)
  - physics: Higgs self-coupling, vector boson scattering
  - layout: acceptable area increase
  - sensor challenges: mass production, rad-hardness at small radii, square pixels/small eta pitch preferred → HV-CMOS?

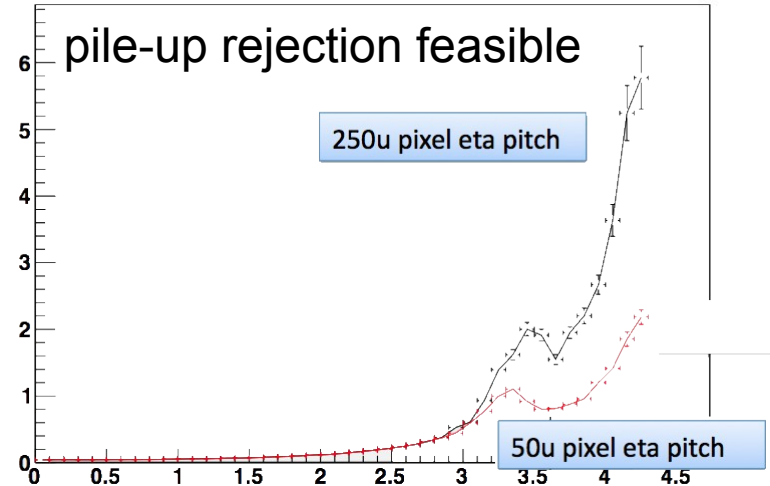


Alpine stave design extension

T. Todorov

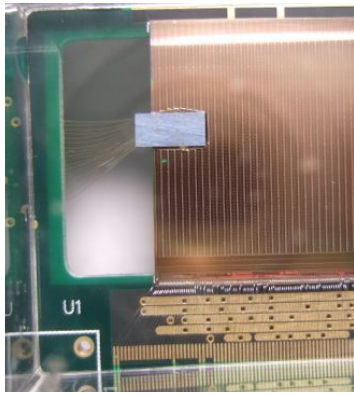


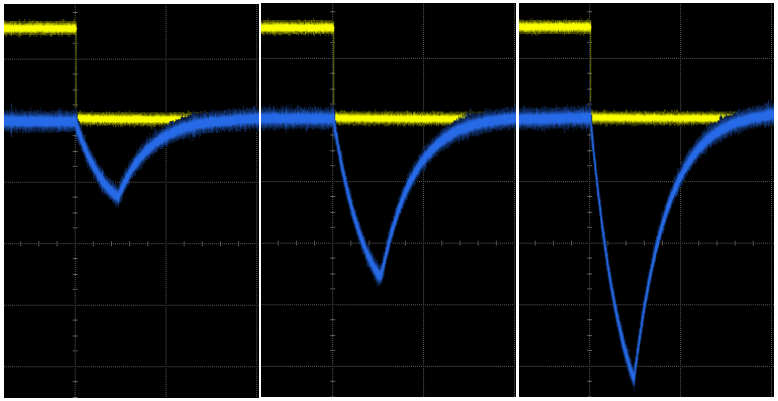




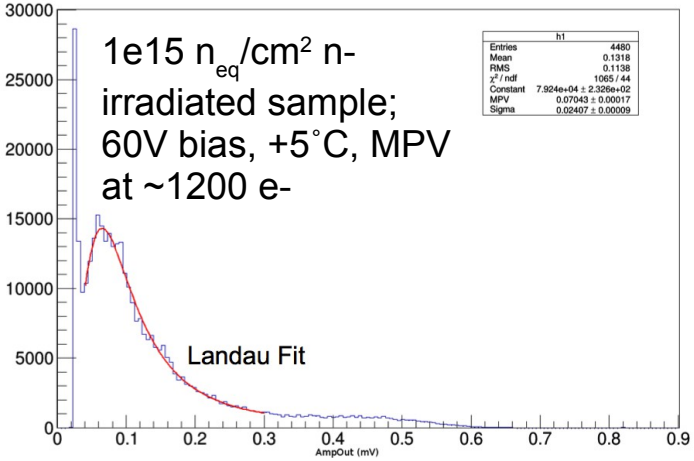
Conclusions

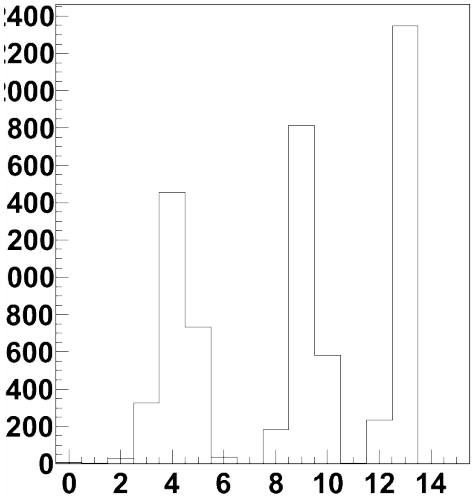
- HV/HR-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- Process can be used for
  - 'active' n-in-p sensors (with capacitive coupling)
  - drift-based close-to-MAPS chips (digitally encoded strips)
- First prototypes being explored within ATLAS
  - First HR-CMOS measurements encouraging
  - results with capacitively coupled HV-CMOS pixel sensors look promising
  - “virtual” strip sensors – z-position encoding works





Row 0 Row 12 Row 23



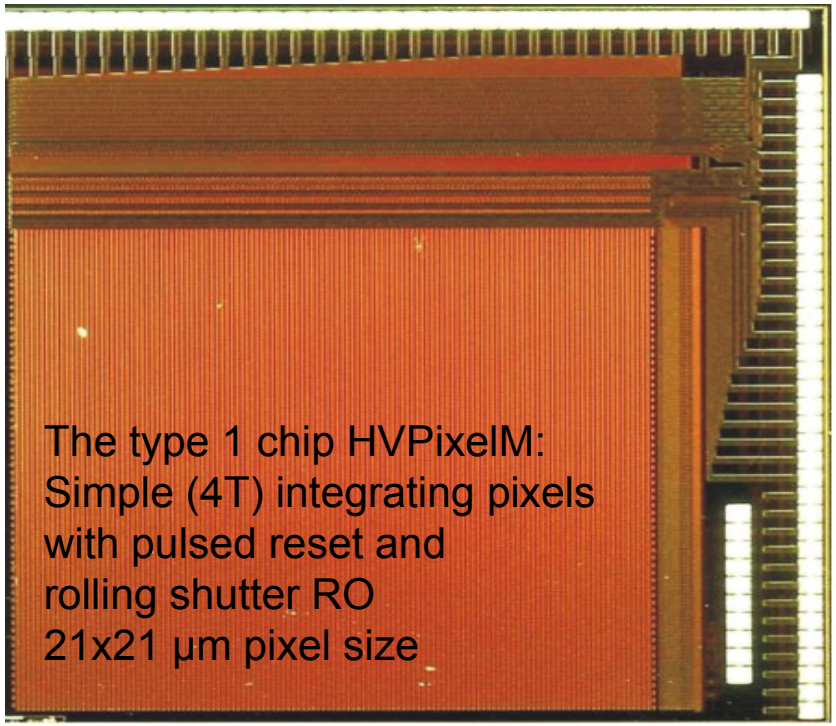


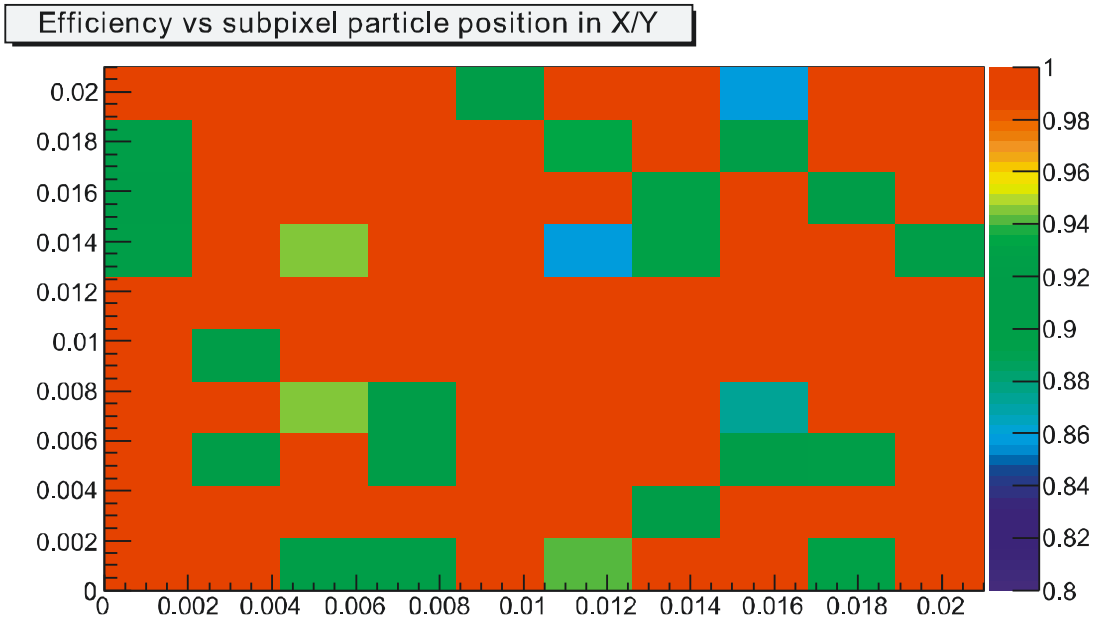
- Drift-based CMOS very promising candidate for rad-hard detectors

Backup slides

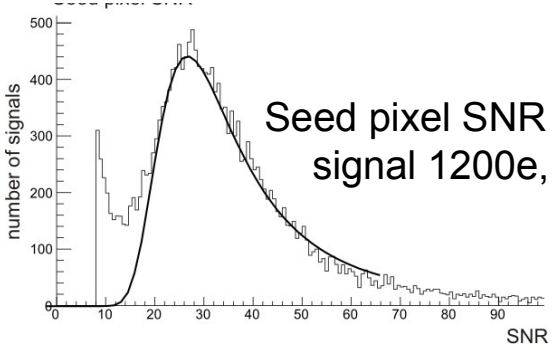
Test beam results: monolithic

- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics

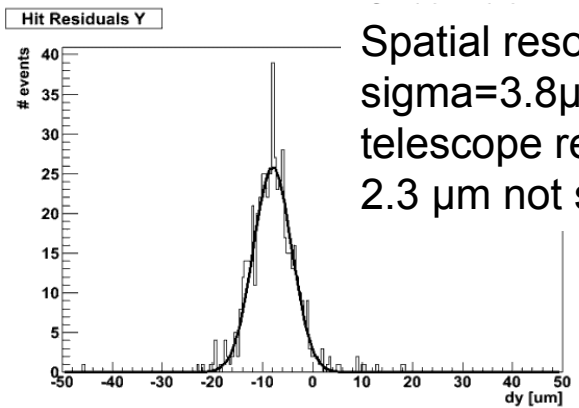




Efficiency vs. the in-pixel position of the fitted hit. Efficiency at TB: ~98% (probably due to a rolling shutter effect)



Seed pixel SNR 27, seed signal 1200e, cluster 2000e

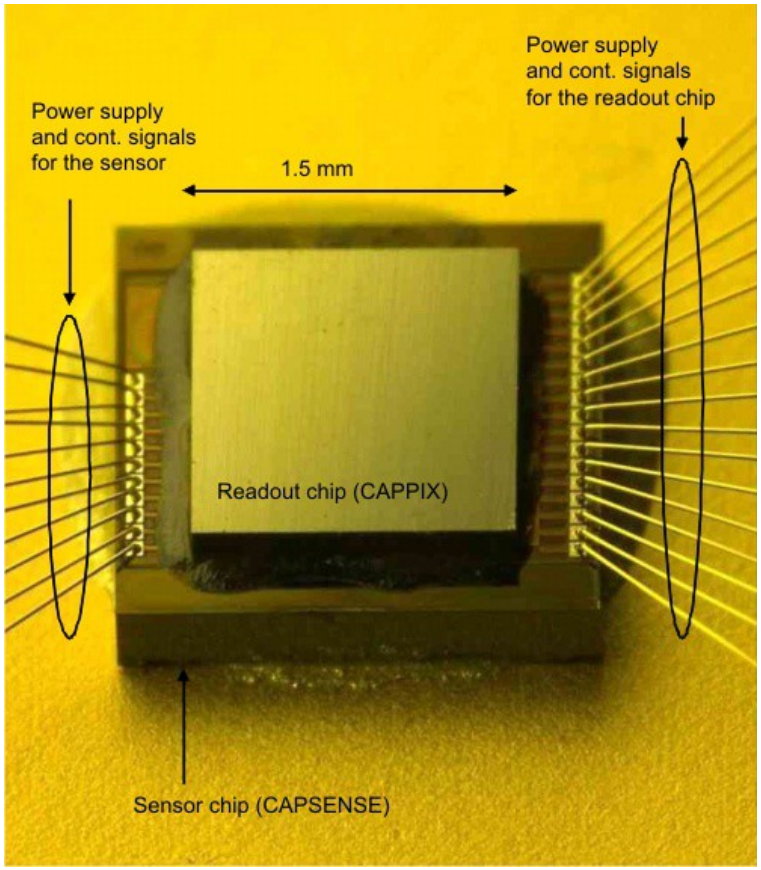


Spatial resolution: sigma=3.8µm, telescope resolution of 2.3 µm not subtracted

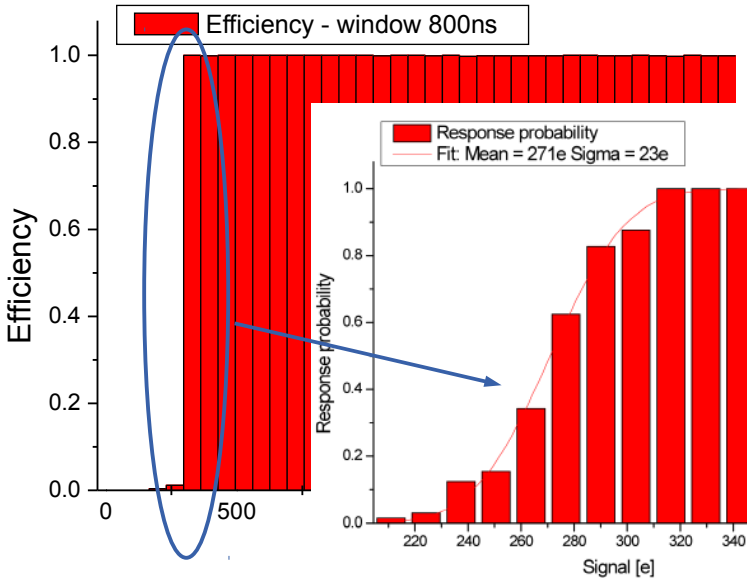
I. Peric

CPPD prototype results

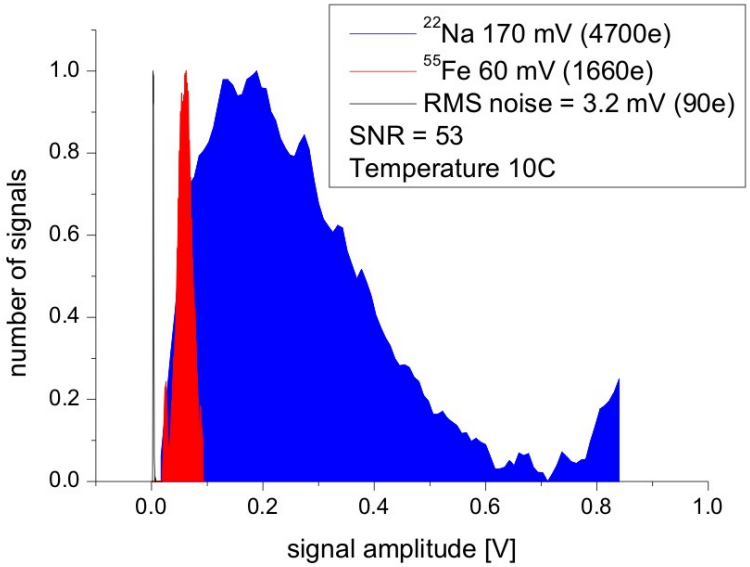
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



CAPPIX/CAPSENSE edgeless CCPD
50x50 µm pixel size



Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.

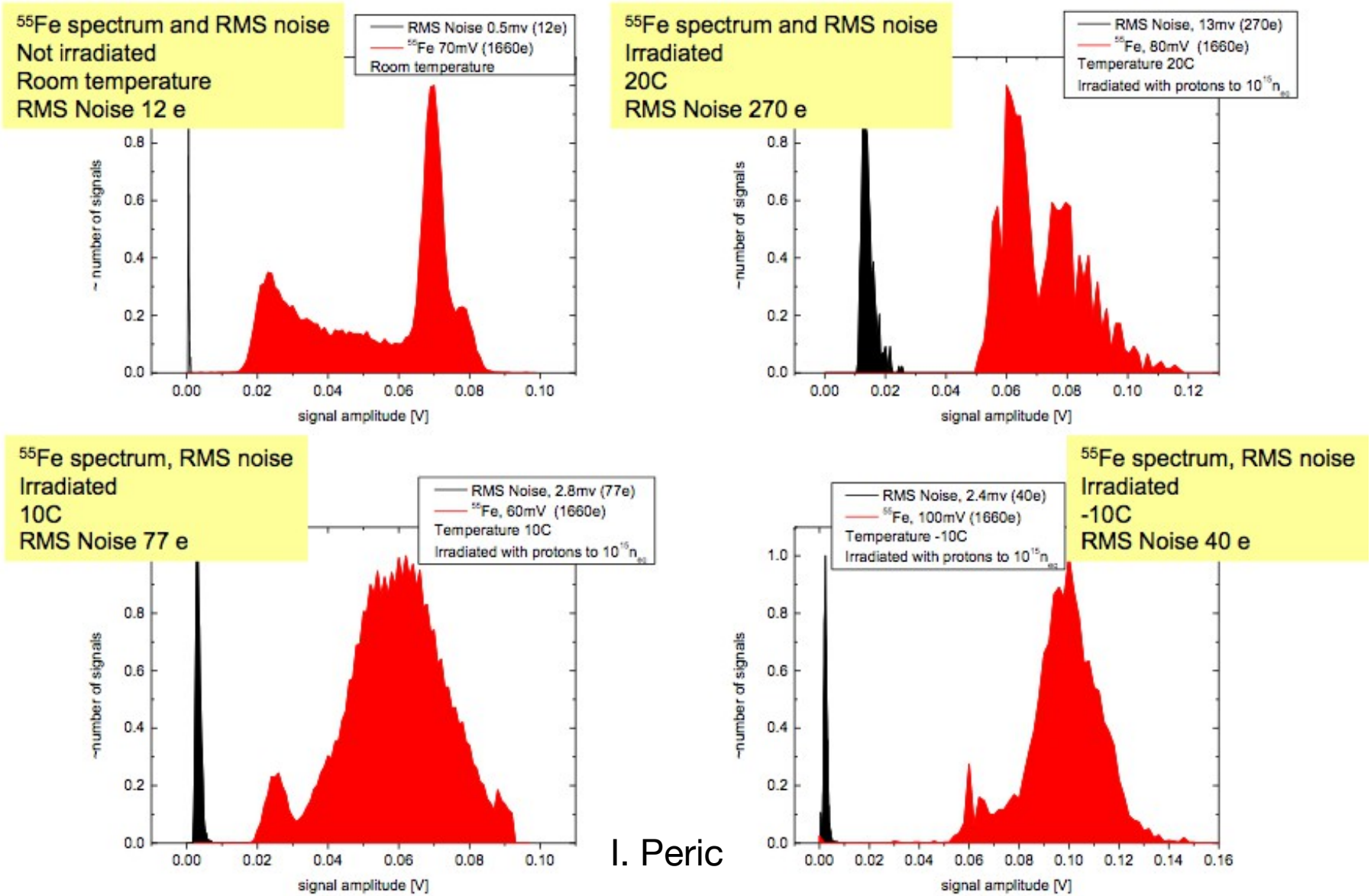


Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

I. Peric

CPPD prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling



I. Peric