SOI Pixel Development at KEK

June, 11, 2008 @BNL

Yasuo Arai (KEK)

KEK Detector Technology Project : [SOIPIX Group, http://rd.kek.jp/project/soi/]

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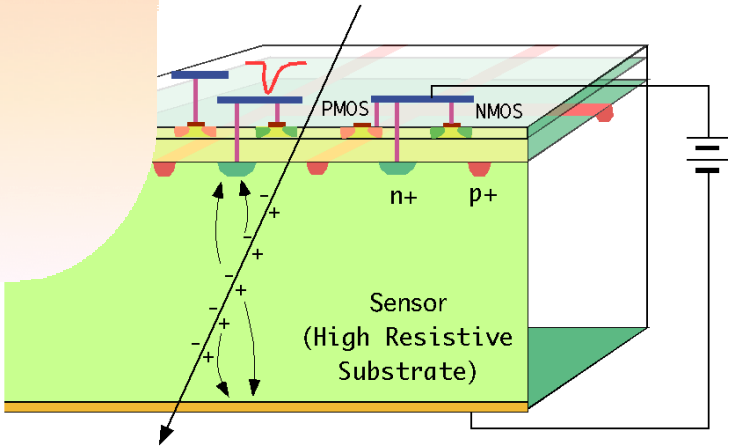
(and JASRI, RIKEN)

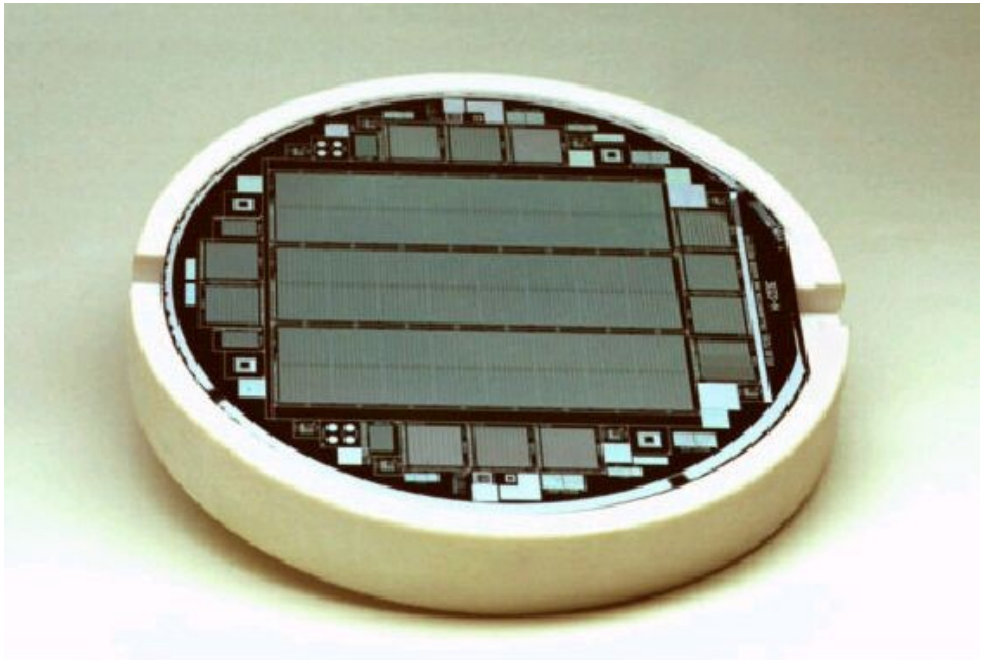
OUTLINE

- Introduction
- SOI Technology
  - Bulk and SOI Si
  - Features of FD-SOI
- SOI Pixel Detector R&D
  - SOI Pixel Process
  - KEK MPW run
  - Test Results
  - TCAD Simulations
- Summary

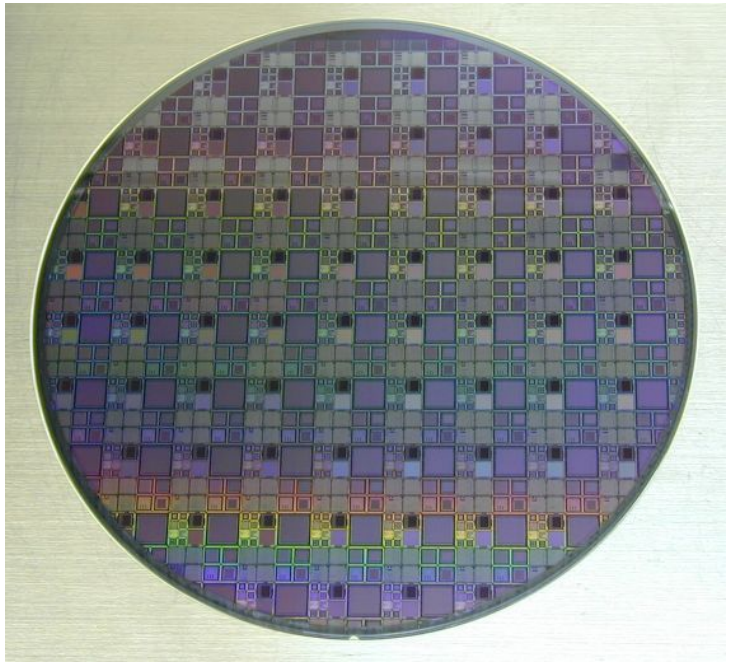


Introduction

Si Radiation Sensor



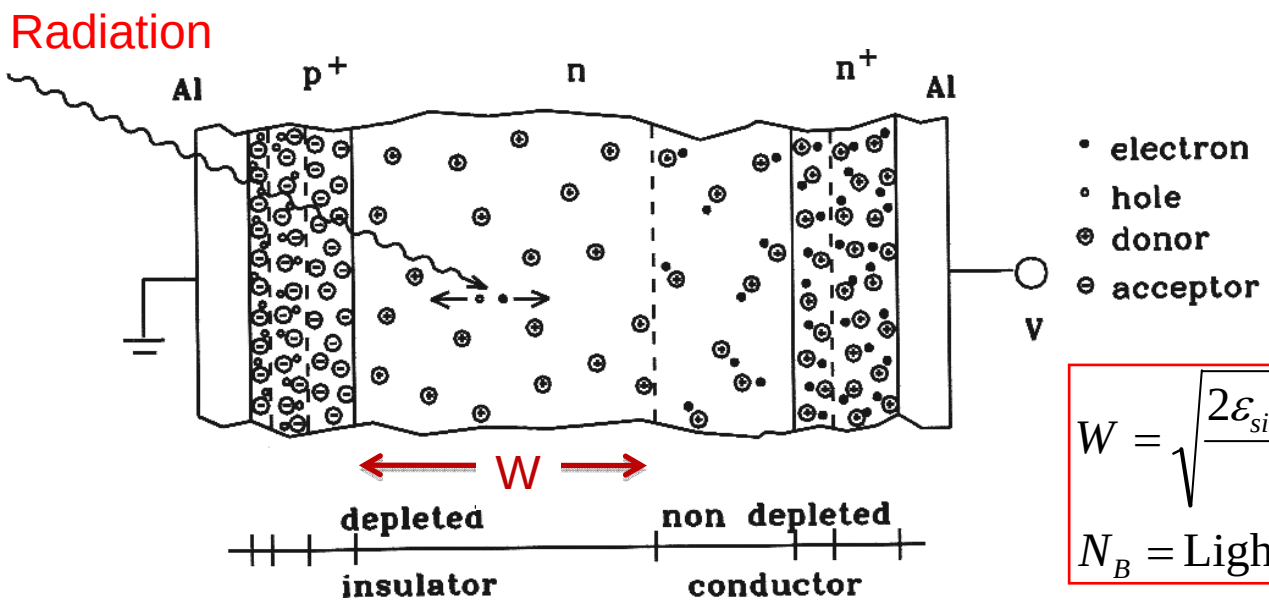
Si Readout LSI



Why these are not combined into one Si Wafer?

Why there was no monolithic detector which implements 100% fill-factor sensor and full readout circuit?

- Radiation Sensor needs Thick Depletion Region
  → Use High-resistivity Si wafer.
- CMOS LSI circuits are built on low-resistivity Si wafer with many impurities.
- To combine the sensor and circuit in a wafer, two different Si layer must be created.

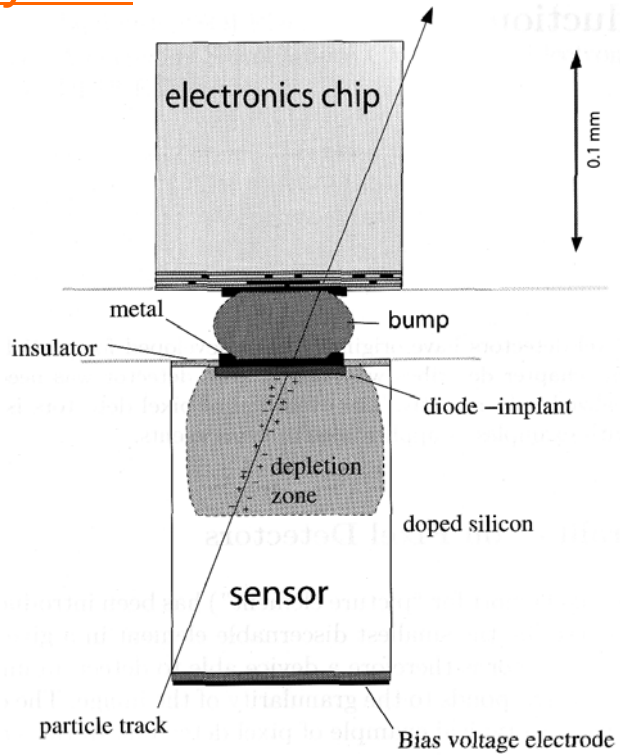


$$W = \sqrt{\frac{2\varepsilon_{si}(V_{bi} - V_{bias})}{qN_B}}$$

N_B = Lightly doped bulk concentration

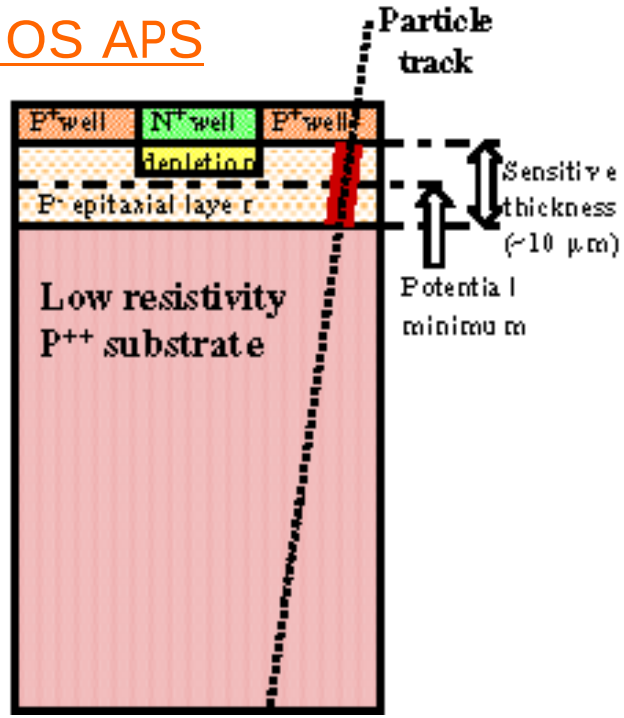
Issues in Present Pixel Detectors

Hybrid



- Position resolution is limited by bump size.
- Many unwanted materials.
- High parasitic capacitance.

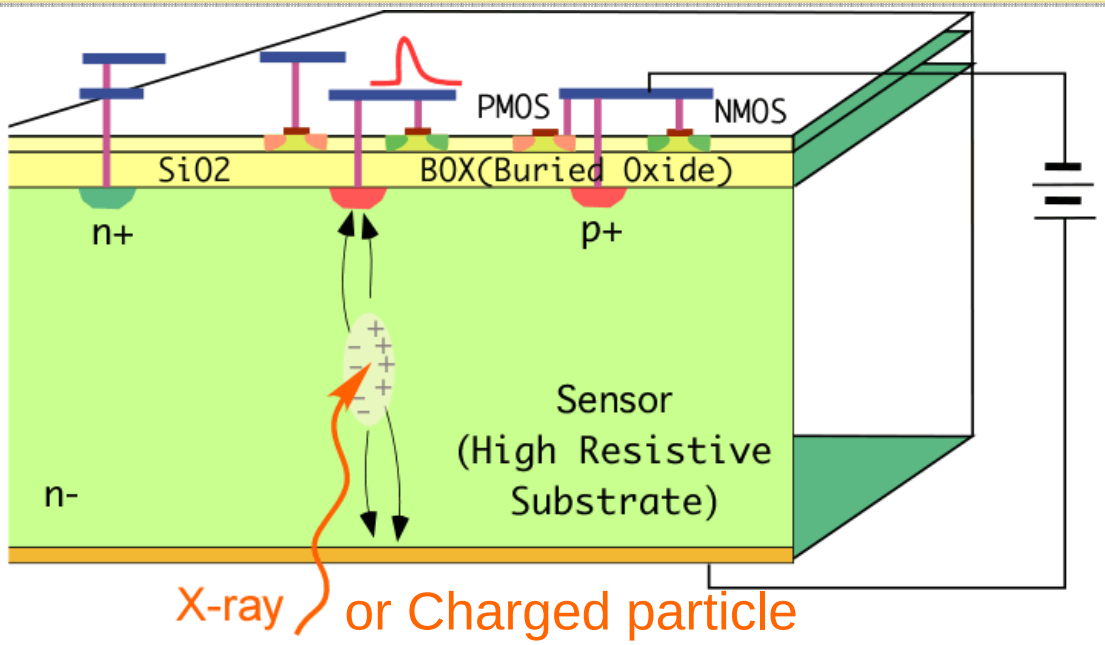
CMOS APS



- Sensitive area is very thin epitaxial layer (~10um).
- Charge collection is slow due to thermal drift.
- NMOS Tr. only. No PMOS.

Monolithic Pixel with SOI (Silicon-On-Insulator) Technology

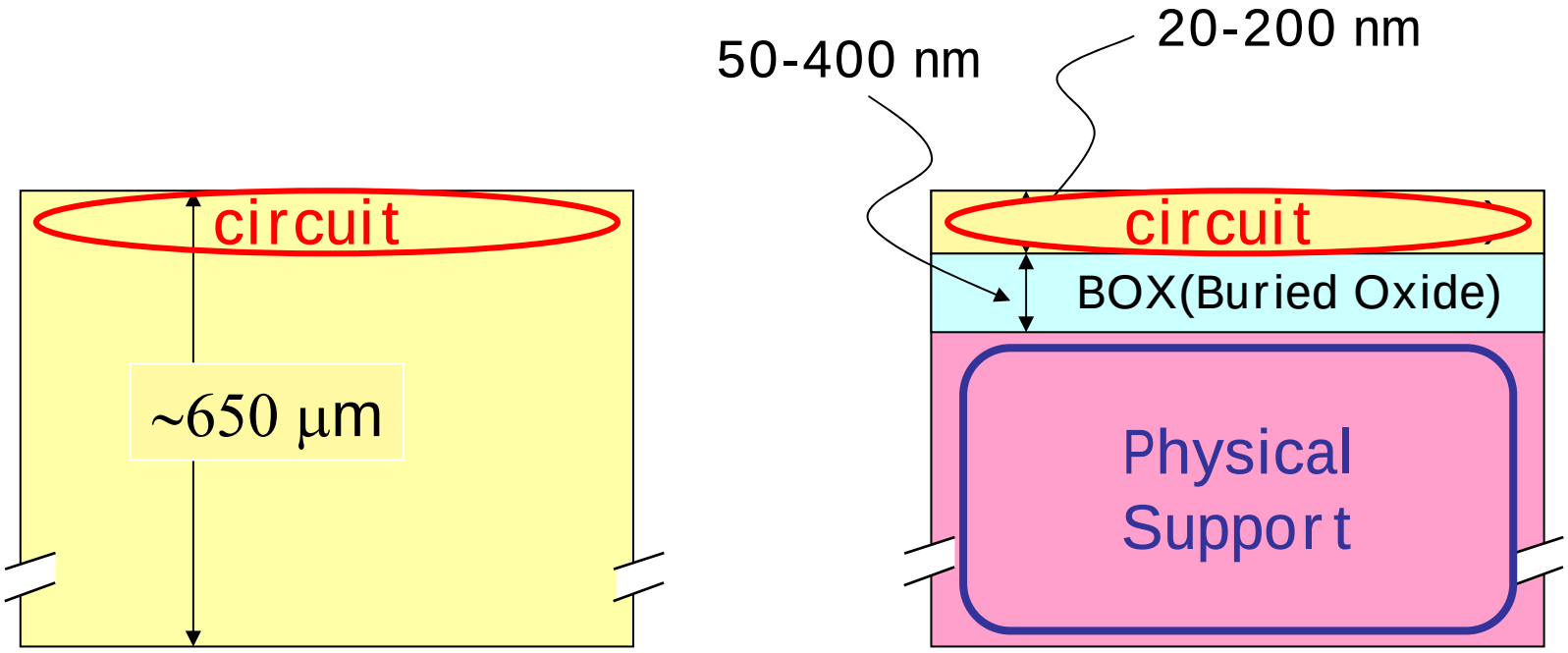
- In SOI technology, Two different Si Wafers (Hi-R & Lo-R) can be bonded via Oxide.
- It become popular in late 90's, and regarded as a main stream technology in near future.



SOI is also an ideal technology to implement Monolithic Radiation Sensor!

Features of SOI Technology

Bulk and SOI Wafer

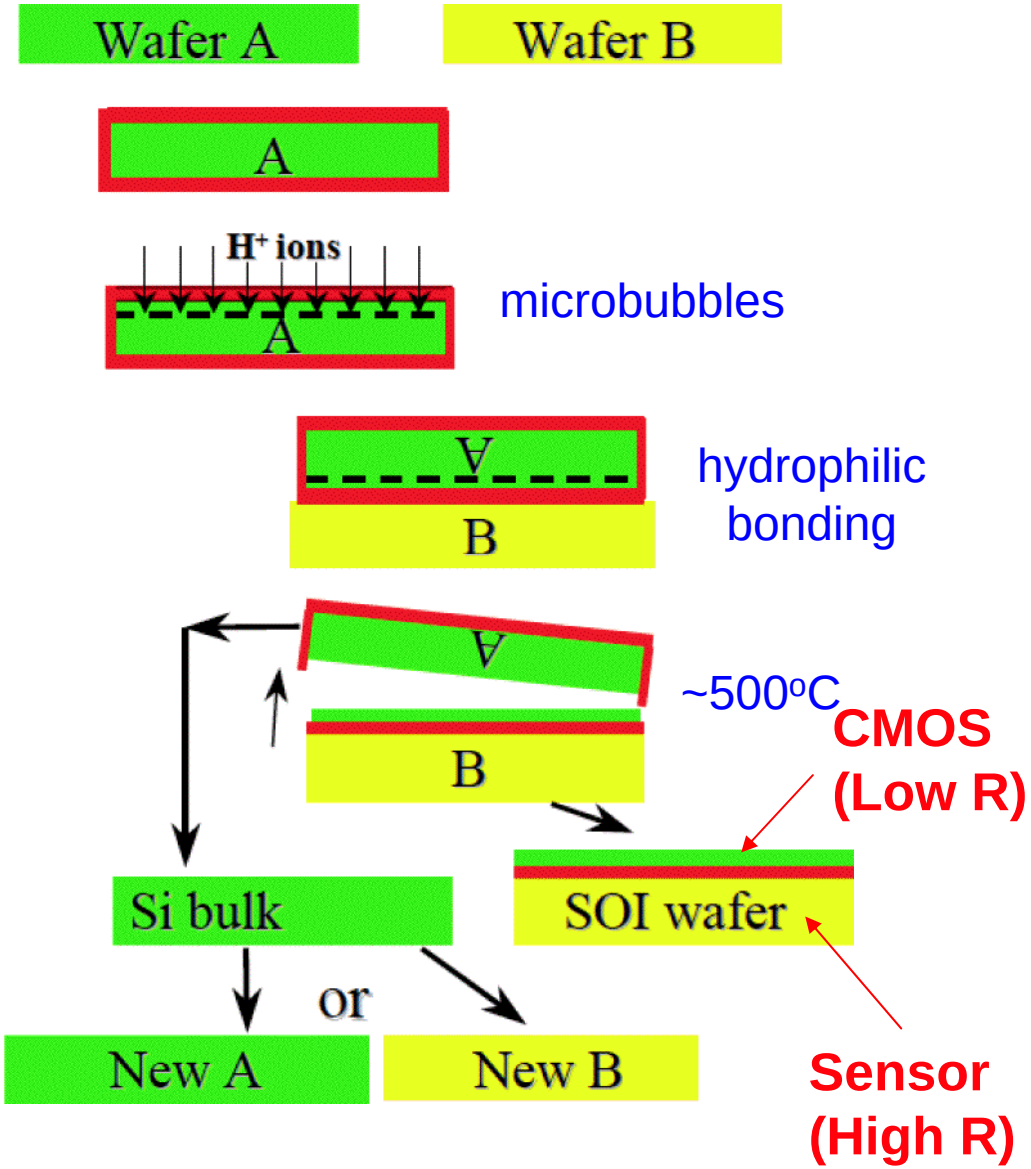


Bulk Wafer

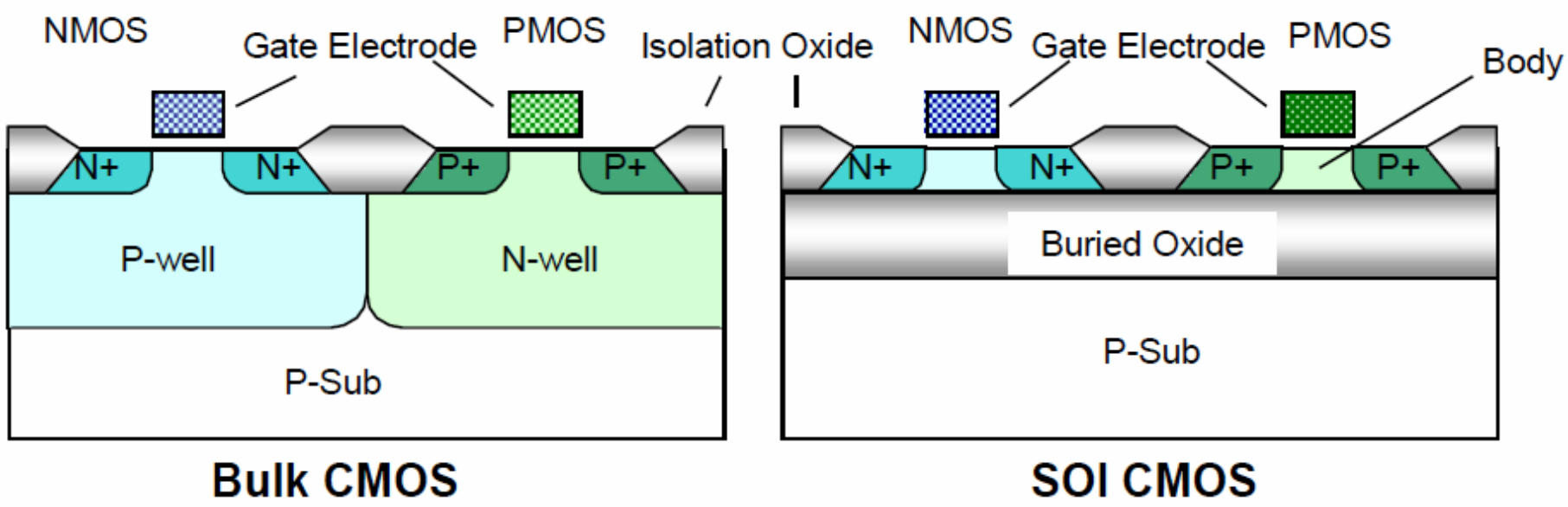
SOI Wafer

UNIBOND™ Process (1995, France LETI) -> SOITEC

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B

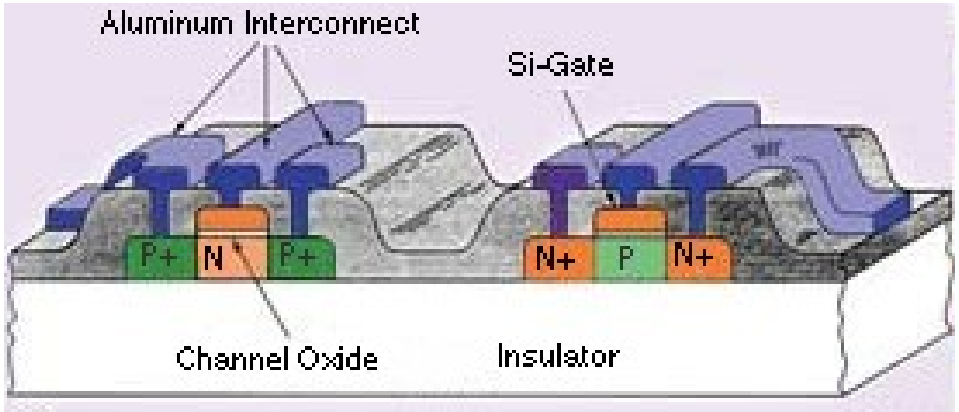


Bulk CMOS vs. SOI CMOS



In SOI, Each Device is completely isolated by Oxide.

No well structure.



PD-SOI vs. FD-SOI

PD-SOI (Partially Depleted)

◆Thick SOI thickness（T_{SOI}）
～100-200nm

◆Depletion layer < T_{SOI}

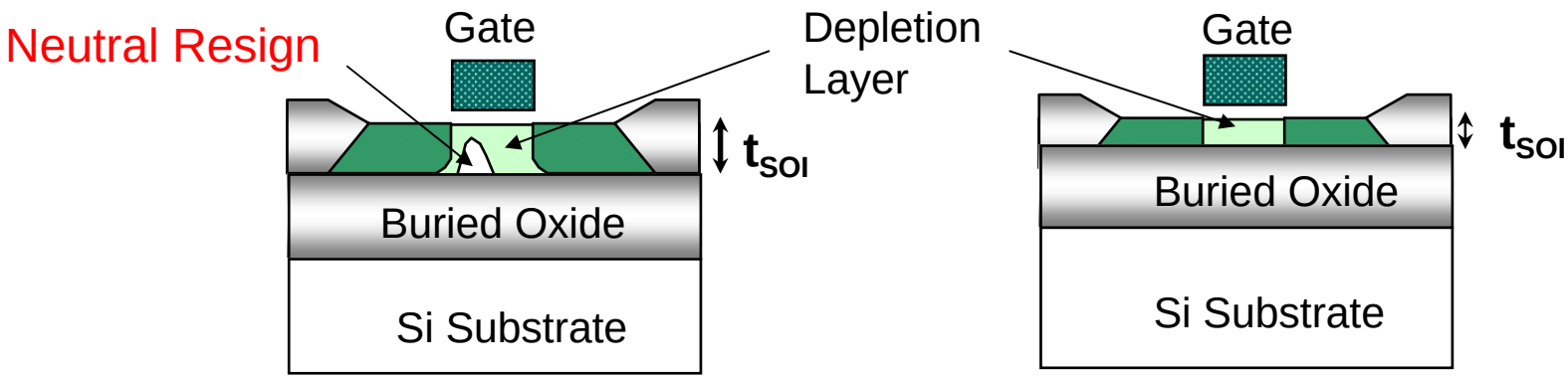
◇Large floating body effect
◇High drive Current by kink effect
→ High speed application

FD-SOI (Fully Depleted）

◆Thin SOI thickness（T_{SOI}）
< 50nm

◆ Depletion layer > T_{SOI}

◇Less floating body effect
◇Steep subthreshold slopes
→ Low power application



FD-SOI has advantage in performance under very low voltage operation.

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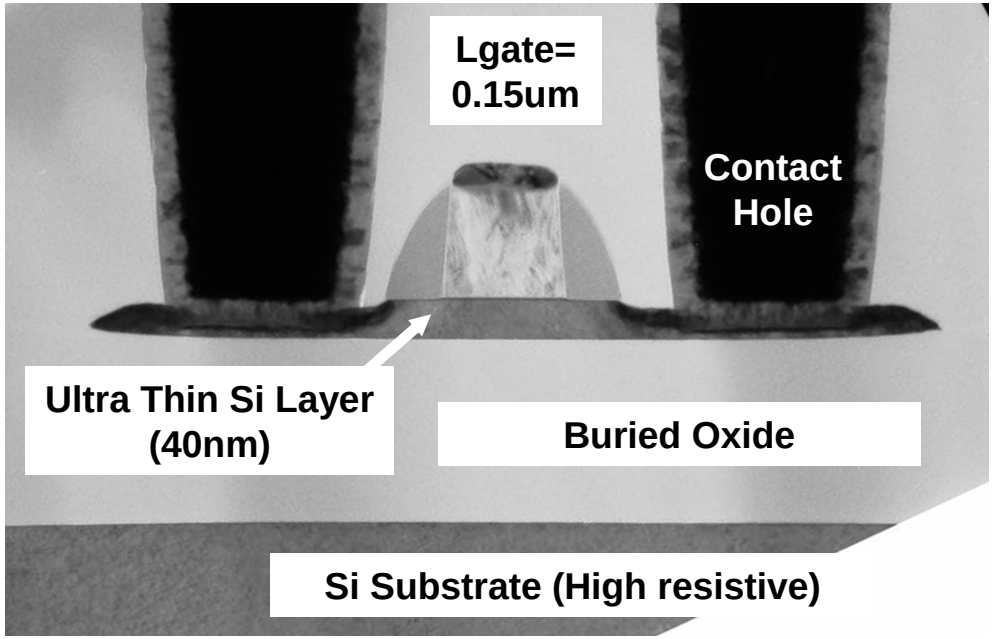
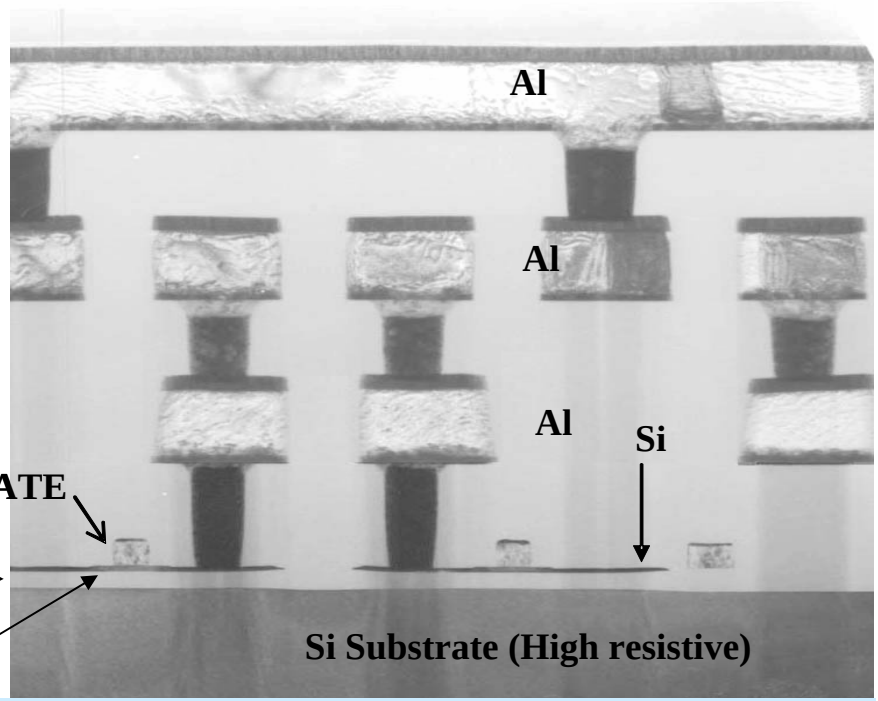
FD-SOI Structure



Close up of MOSFET

Cross Sectional SEM Photograph



Cross Sectional View of FD-SOI Device

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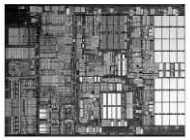
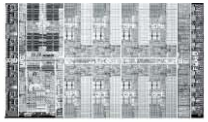
Current Status of PD-SOI and FD-SOI



◆ **PD-SOI (Partially Depleted)**

High-speed microprocessors

- **IBM: PowerPC , mainframe CPU's, Wii(Nintendo), Xbox**
- **Free scale: PowerPC**
- **AMD: Athlon processors**
- **Sony (with IBM and Toshiba) : Cell, PS3**



◆**FD-SOI (Fully Depleted)**

Low-power application

- **Oki: solar cell watch, long-wave RF decoder**

Technology Node option beyond 32nm, Next 3D Tr. (R&D)

- **Intel, many major companies**

At present, only Oki has an experience of mass production of FD-SOI

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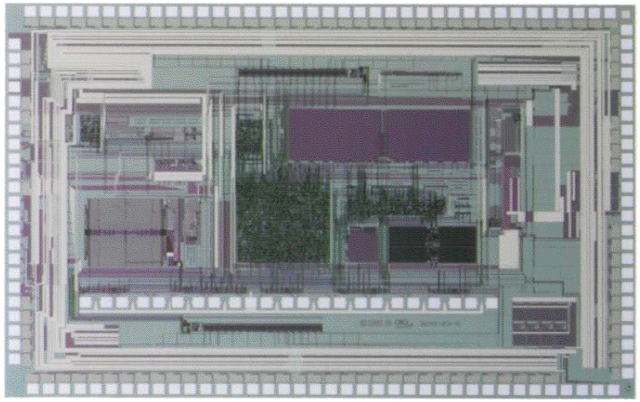
FD-SOI LSI Products for Consumer Market

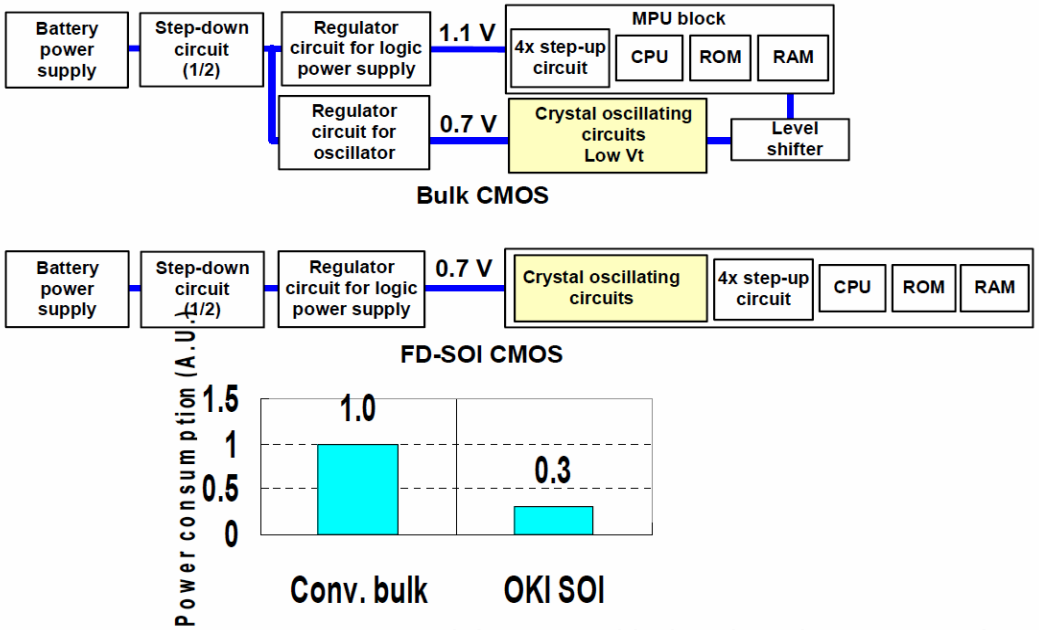
Radio Controlled Solar Watch



This Watch-LSI includes
MCU, SRAM, MROM, Power Unit,
LCD Driver etc in One-chip.

70% Power reduction compared with bulk device

http://www.casio.co.jp



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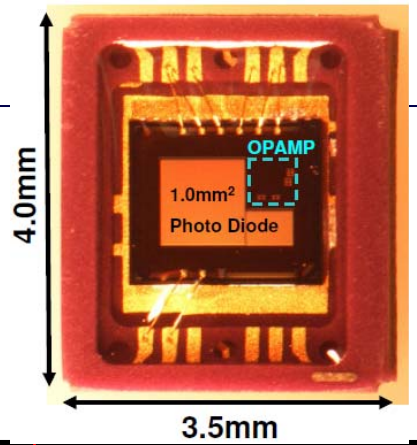
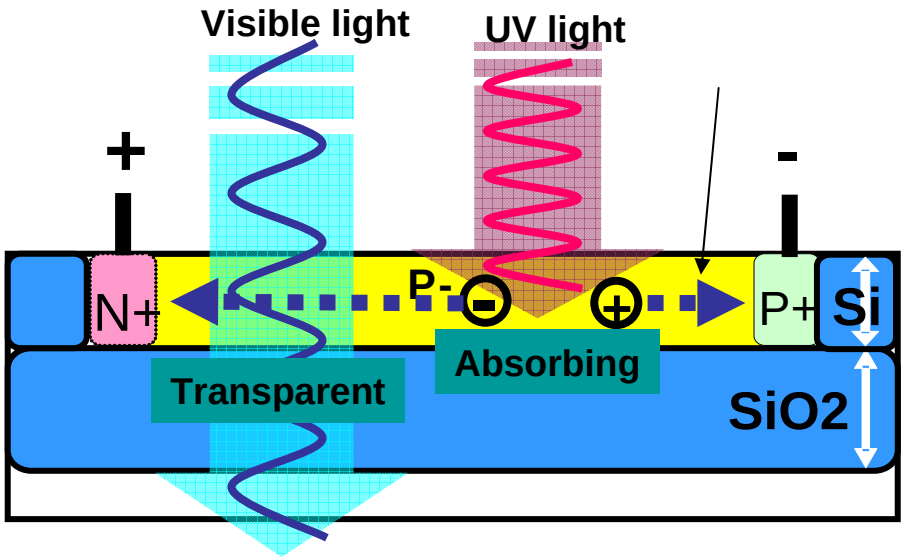
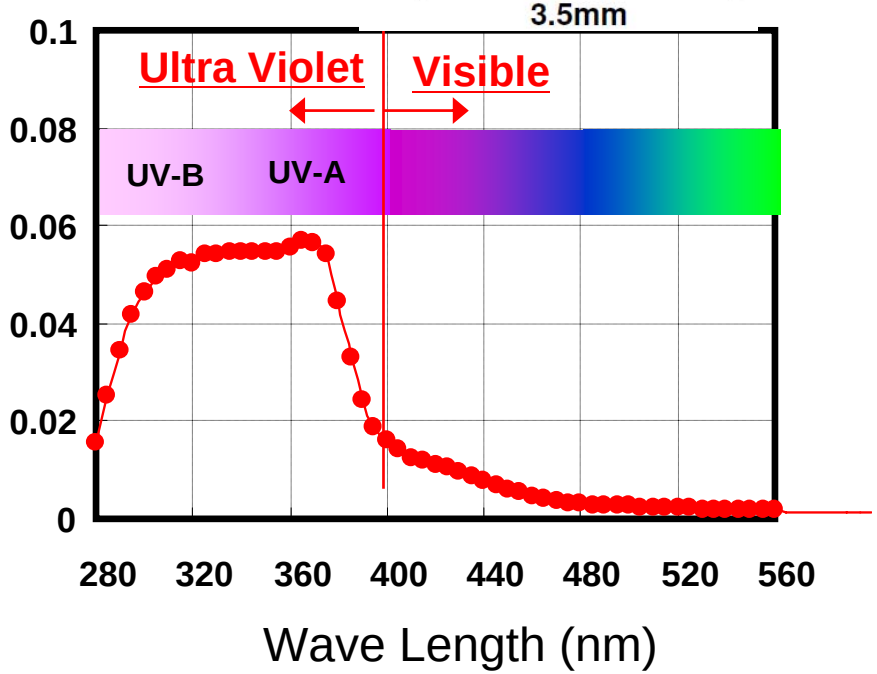
FD-SOI UV Sensor

- ✓UV selective without external filters
- ✓On chip analog / digital circuits
- ✓Very high uniformity





Principal Schema



Spectral of FD-SOI Photo-Diode

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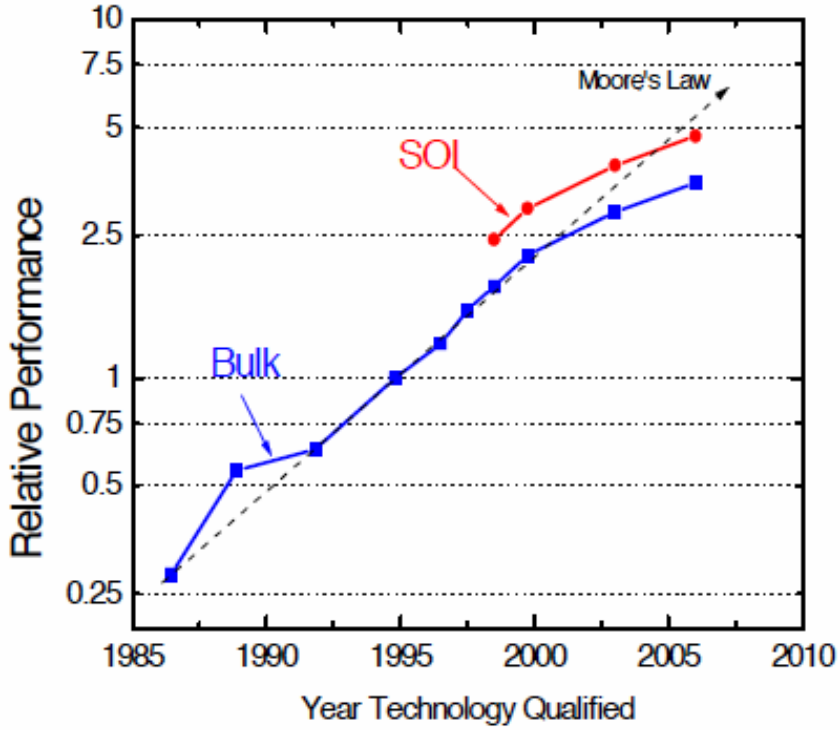
Features of (FD-)SOI

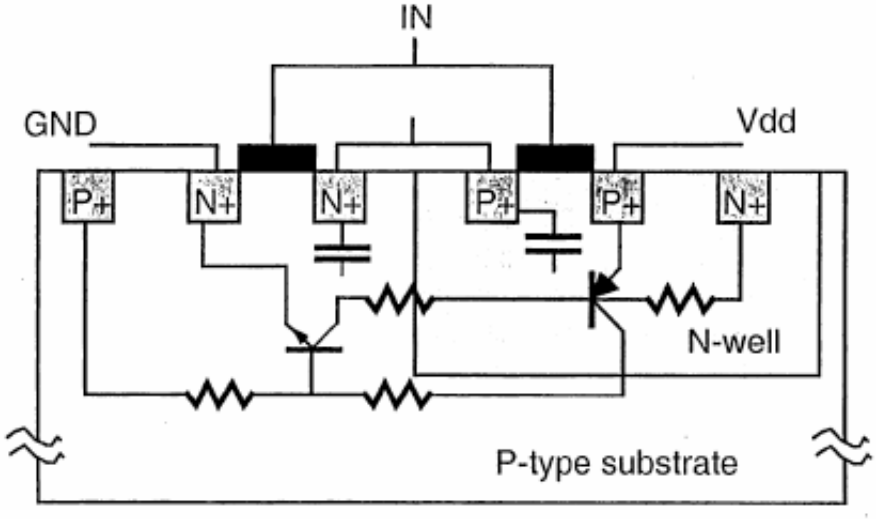
- Full Dielectric Isolation :
  Latchup Free, Small Area,
  Good Circuit Isolation
  No Body Bias Effect
- Low Junction Capacitance :
  High Speed
- Steep Sub-threshold Slope
  Low Power
- No Kink Effect
  Good for Analog Design
- Less Impurity in Body
  Good Vth Matching,
  Less 1/f Noise



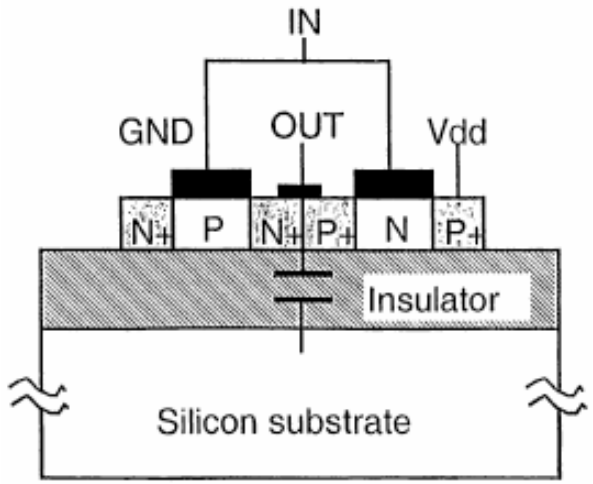
- No Well junction, Thin Film :
  Low Leak,
  Low Vth Shift (Temp. 4K - 300C).
- Small Active Volume :
  High Soft Error Immunity
- TID compensation by Back Bias

Latchup Free Structure

Bulk CMOS



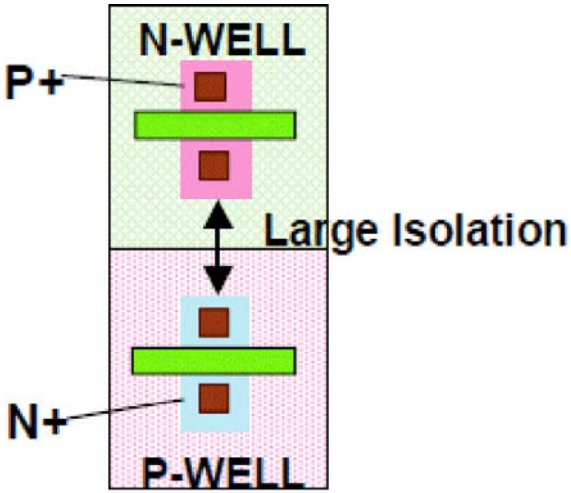
SOI CMOS

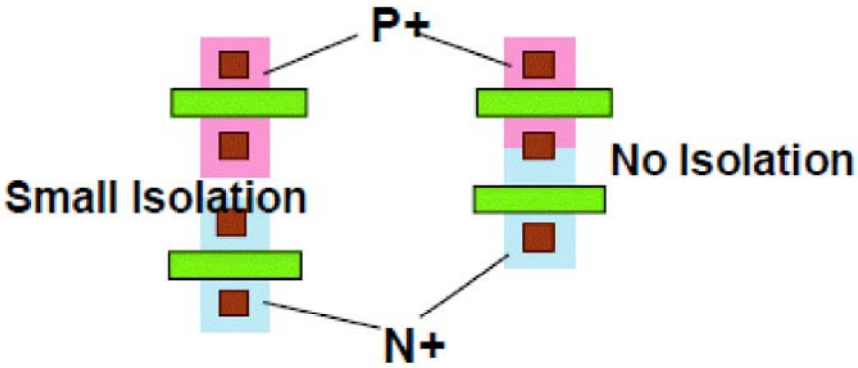


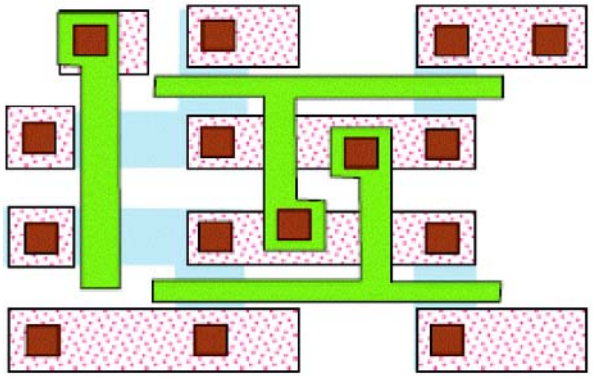
(Ref. 'SOI Technology' by Jean-Pierre Colinge, Springer)

No Parasitic PNPN Structure

Area reduction by SOI

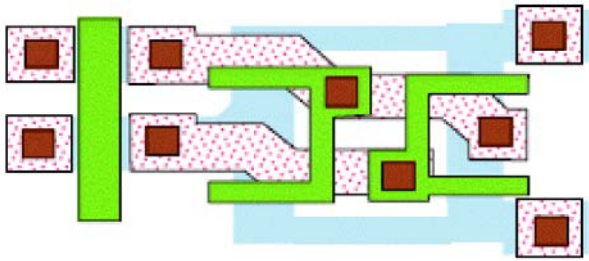






Area 1

Bulk



SRAM-Cell Layout

Area 0.67

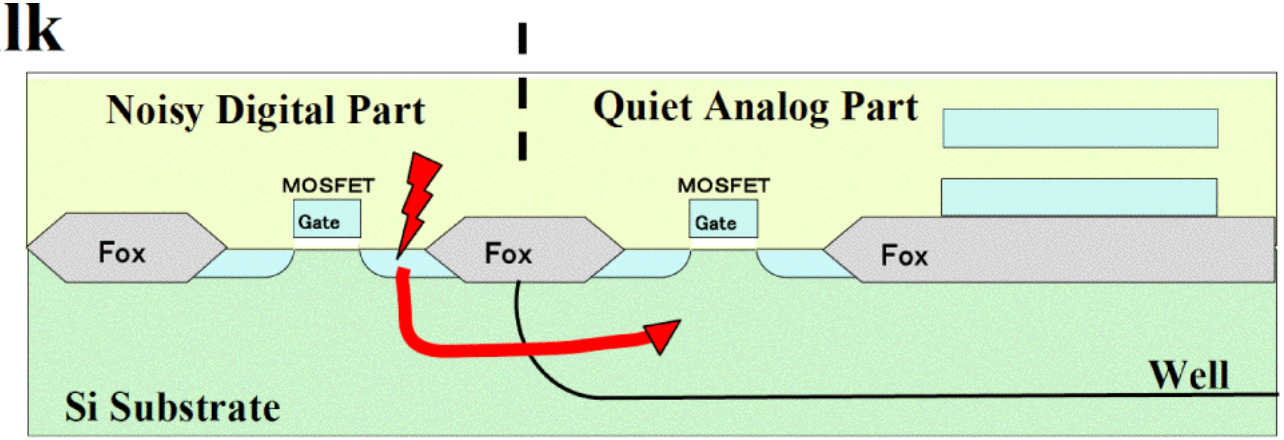
SOI

No Well Isolation

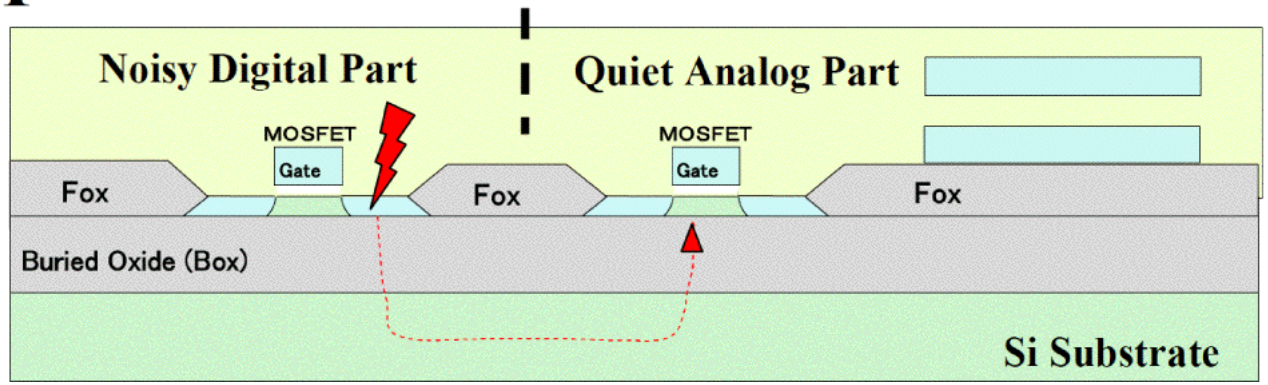
Isolation between Analog and Digital Part

10-40dB lower than Well isolation of Bulk, when High-Resistive Substrate is used

Bulk

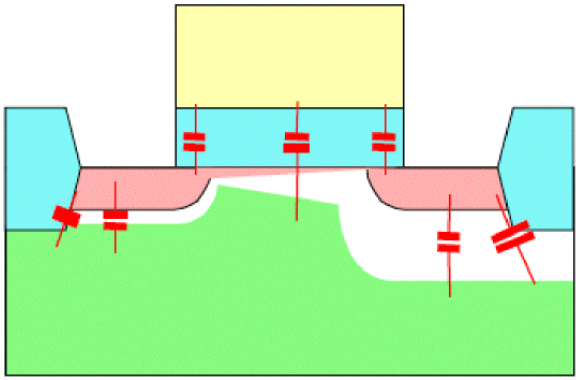


SOI

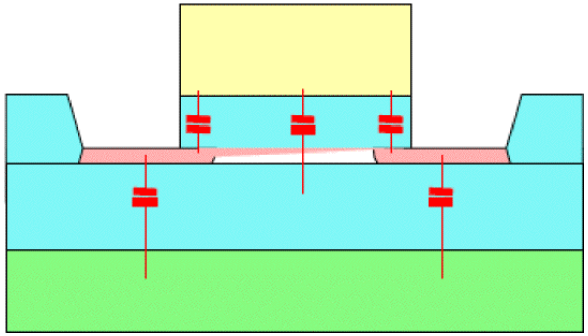


Smaller Junction Capacitance

Bulk



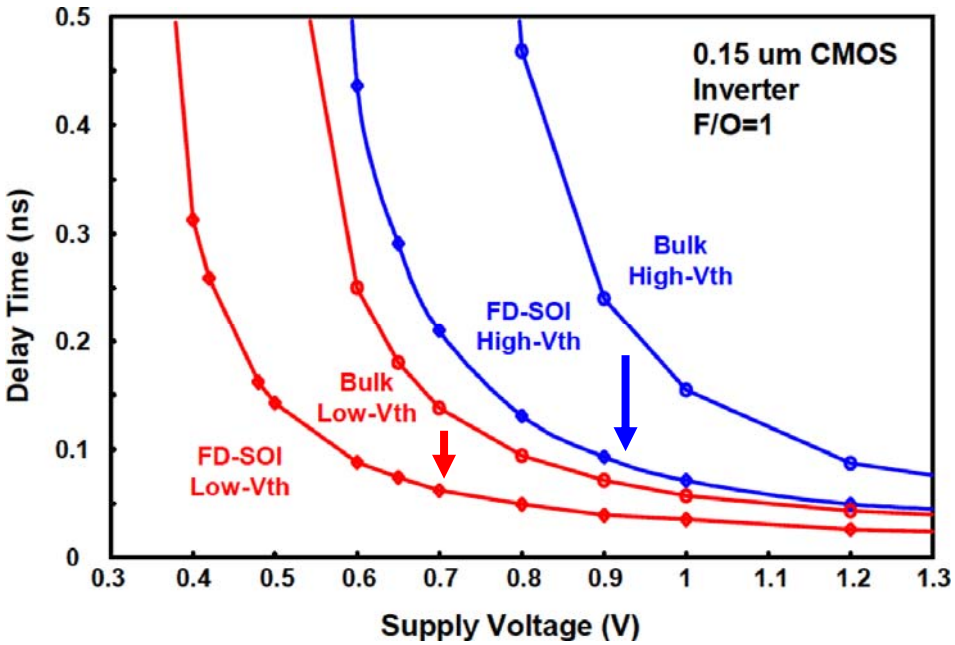
SOI



Cj is 1/10 of Bulk technology.

Gate Capacitance is 30-40% Lower.

High Speed / Low Power



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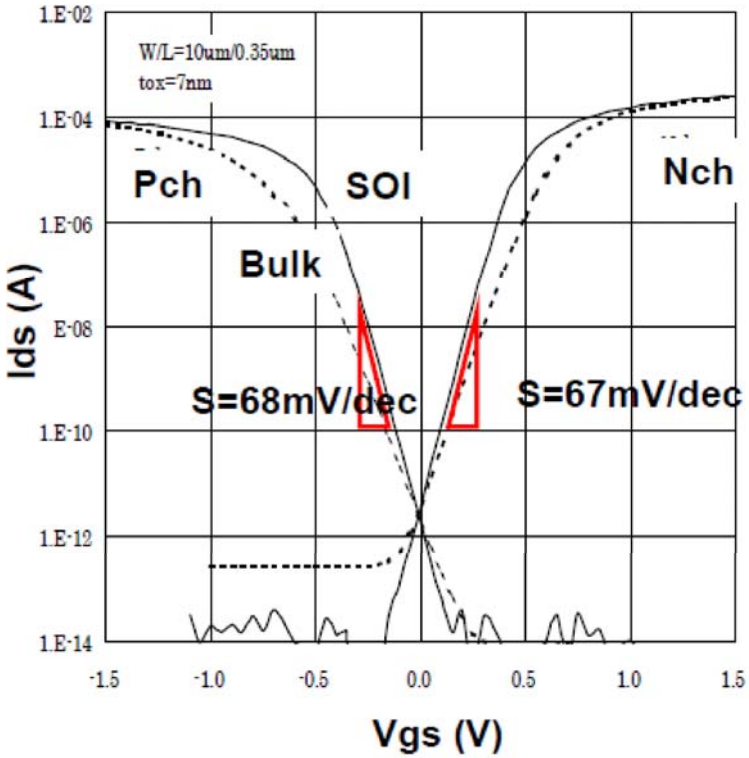
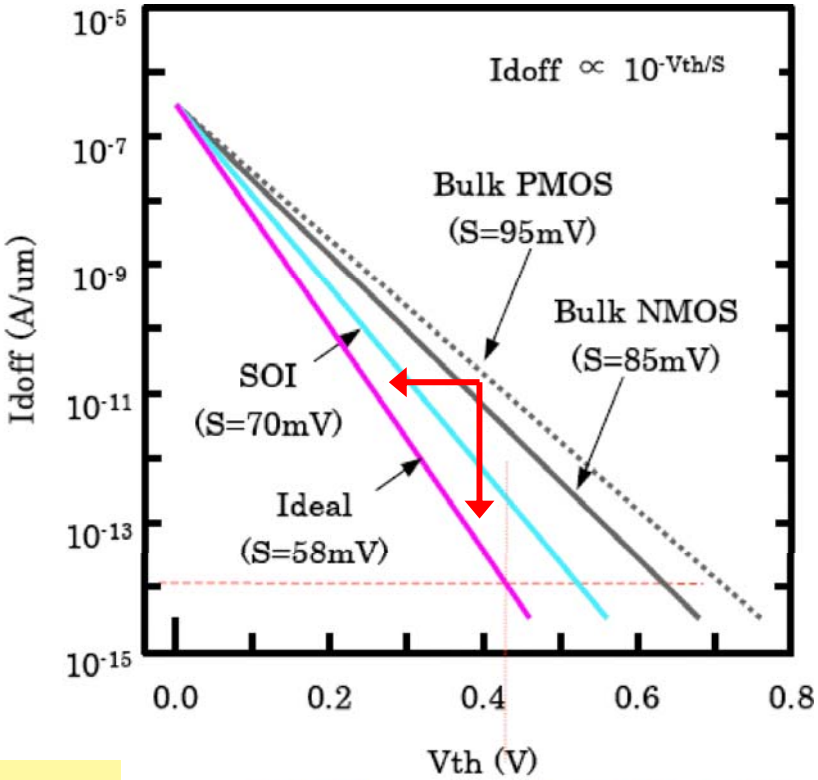
Steep Sub Threshold Slope





F.Ichikawa et al., SSDM, 2004

Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).

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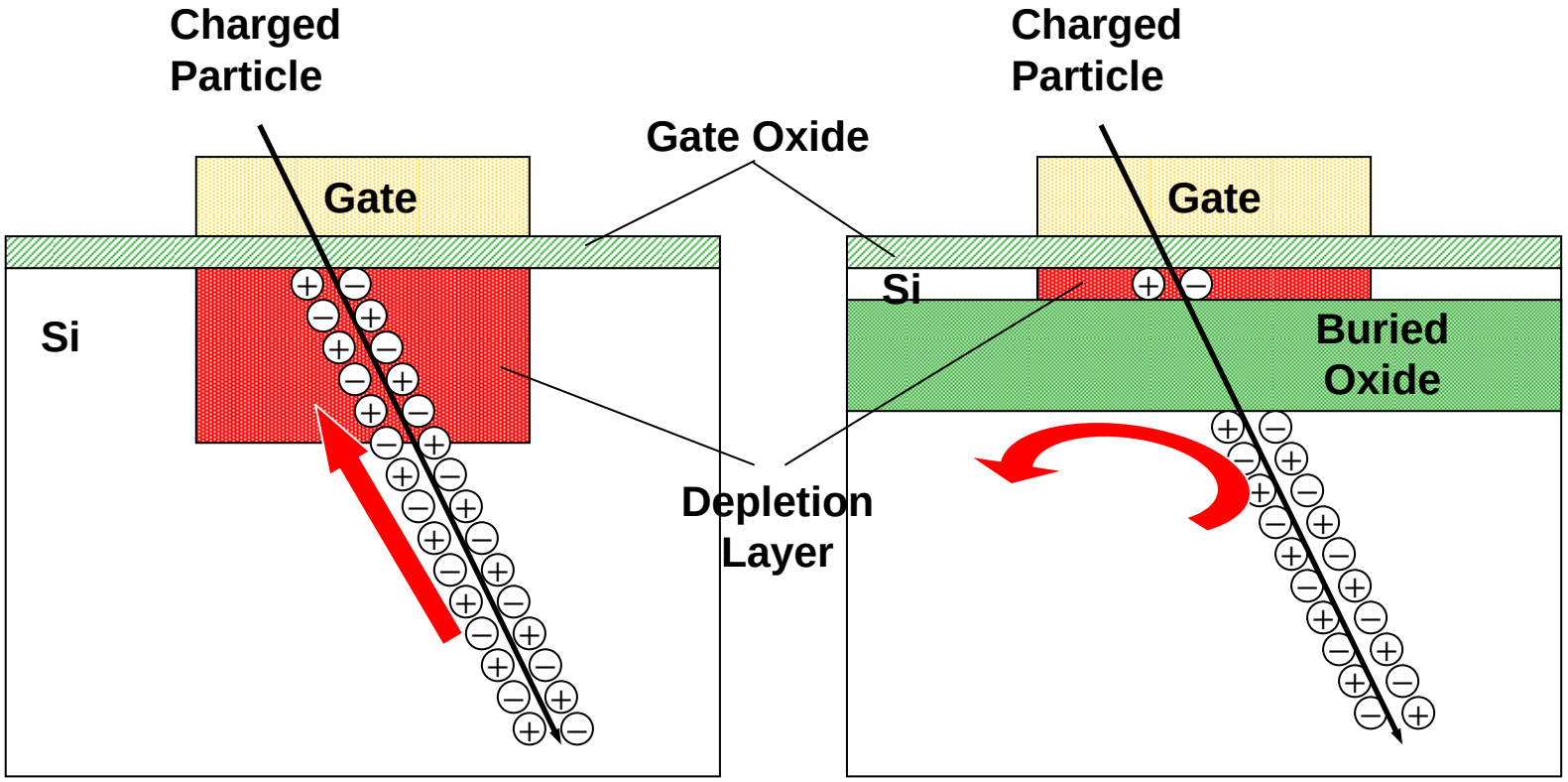
High Soft Error Immunity



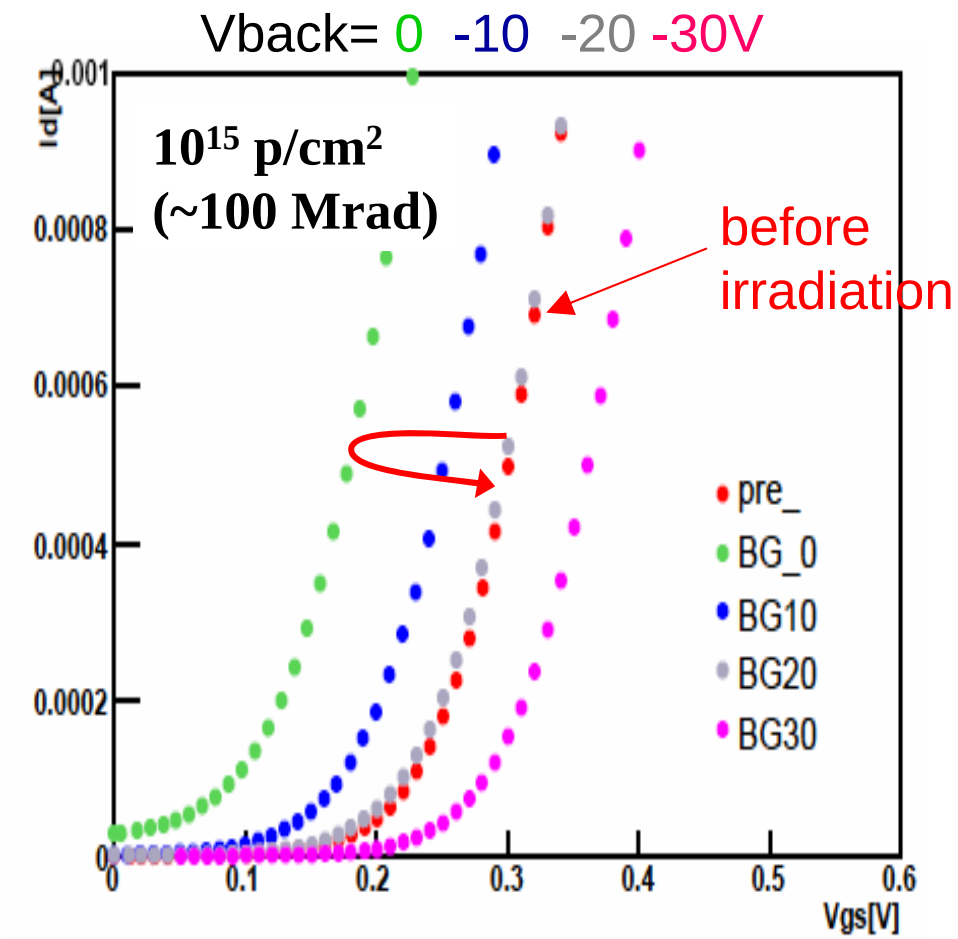
Bulk Device

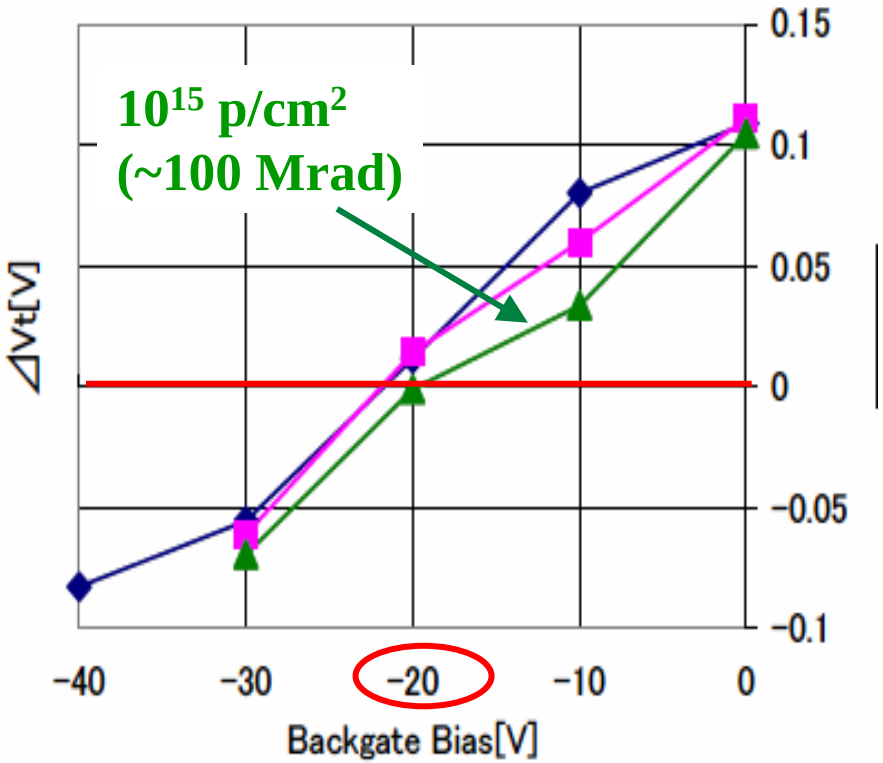
SOI Device

Higher soft error immunity due to ultra thin body Silicon.

Total Ionization Dose (compensation by back bias)

Leak Current and V_{Th} resumes to nearly original value by biasing back side even after 100Mrad.





Summary of this section

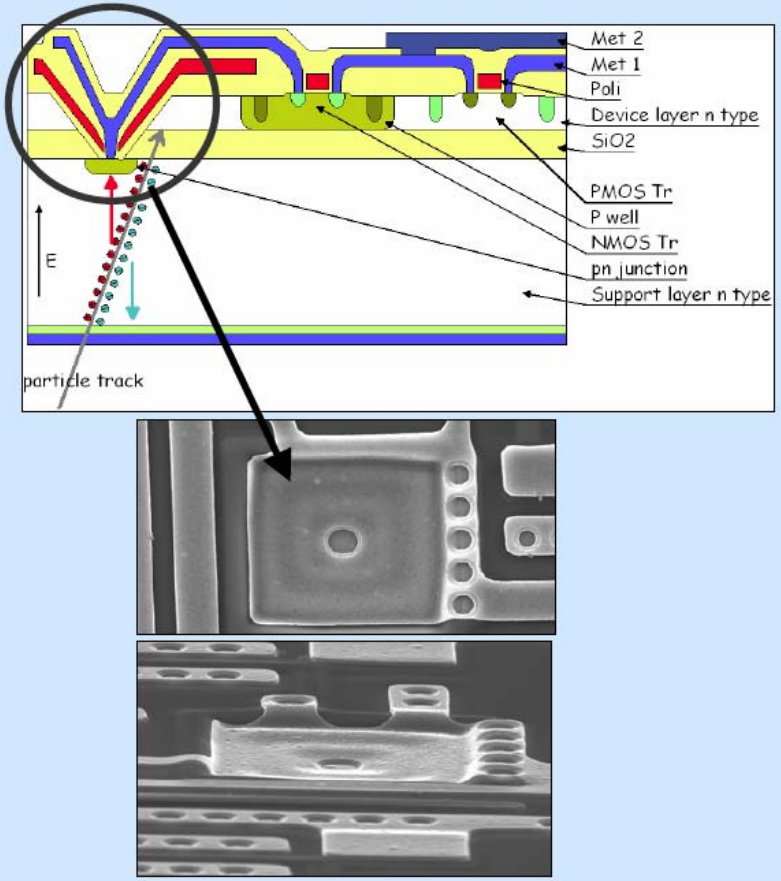
- FD-SOI technology has many attractive features:
  Latchup Free,
  Radiation Hardness,
  High Temperature Operation,
  Low Power, ...
  for use in High Energy and Space applications.

but the substrate Si is a simple physical structure until now.

→ Can we integrate Radiation Sensor at the bottom Si ?

Pioneering work by SUCIMA

Principle of SOI monolithic detector



The idea:

Integration of the pixel detector and readout electronics in the wafer-bonded SOI substrate

Electronics → Device layer

- Low resistive (9-13 Ωcm, CZ)
- 1.5 μm thick
- Standard CMOS technology

Detector → Support layer

- High resistive (> 4 kΩcm,FZ)
- 300 μm thick
- Conventional p^+-n
- DC-coupled

W.Kucewicz Vertex 2004 - Villa Vigoni, Menaggio – Como, 13 – 18 September 2004 3

Unfortunately technology is not so advanced (~3μm technology).

KEK SOIPIX R&D History

'05. 7: Start Collaboration with OKI Elec. Co. Ltd. for SOI Pixel detector R&D .

'05.10: FY05 TEG submission in OKI MPW (Multi Project Wafer) run with 0.15 um technology.

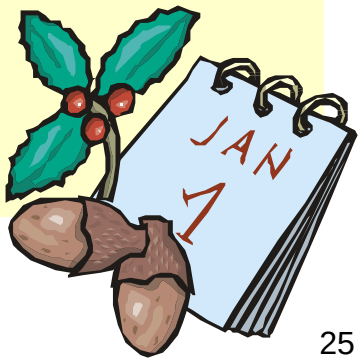
'06. 3: Fabrication was finished.

FY05 TEG chips are successfully tested.
Response to Light and β-ray is confirmed.

'06.12: First MPW run hosted by KEK with 17 designs which includes submissions from LBNL, FNAL, U of Hawaii.

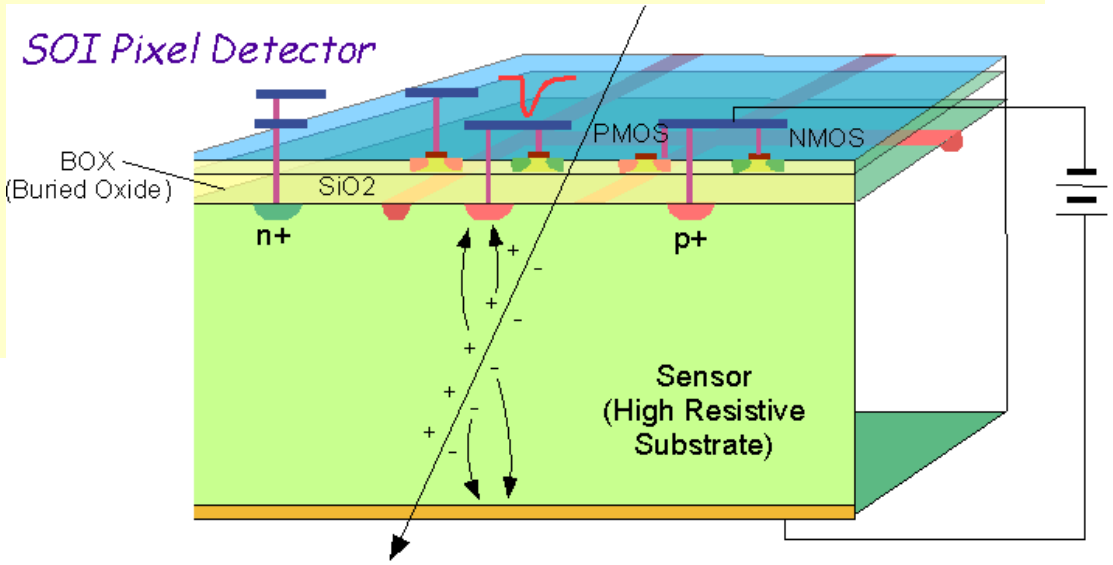
'07.6: Process is changed from 0.15 um to 0.2 um.

'08.1: Second KEK MPW run is submitted.



Features of SOI Monolithic Pixel Detector

- Monolithic Detector, No Bump Bonds (->Low material, Thin Device).
- Standard CMOS Electronics (-> Intelligent Pixel).
- Advanced Si Process (-> Small Pixel size of ~5um is possible).
- Fully depleted sensor with small capacitance of the sense node (~10fF, High gain V=Q/C, Low noise)
- Based on Industrial standard technology (-> Cost benefit and Scalability)
- No Latch Up, Rad Hard.
- Low Power
- Low/High Temp operation
- ...



Publications

- "First Results of 0.15um CMOS SOI Pixel Detector", Y. Arai, et al. , SNIC Symposium, Stanford, California, 3-6 April 2006, SLAC-PUB-12079, SLAC-R-842, eConf: C0604032, PSN-0016. http://www.slac.stanford.edu/econf/C0604032/papers/00
- "Development of a CMOS SOI Pixel Detector", Y. Arai, et al., Proceedings of 12th Workshop on Electronics for LHC and Future Experiments (LECC 2006), 25-29 September 2006, Valencia SPAIN.
- "Monolithic Pixel Detector in a 0.15mm SOI Technology", Y. Arai, et al., IEEE Nuclear Sci. Symposium, San Diego, Oct. 29 – Nov. 4, 2006, Conference Record, Vol. 3, Oct. 2006 Page(s):1440 – 1444.
- "Deep sub-micron FD-SOI for front-end application", Nucl. Instr. and Meth. .A, Vol. 579, Issue 2, 1 Sep. 2007, Pages 701-705, H. Ikeda, et al., Proceedings of the 11th Symposium on Radiation Measurements and Applications May, 2006.
- "Electronics and Sensor Study with the OKI SOI process", Y. Arai, Topical Workshop on Electronics for Particle Physics (TWEPP-07), 3-7 Sep. 2007, Prague, Czech Republic. CERN-2007-007, pp. 57-63.
- "R & D of a pixel sensor based on 0.15 μm fully depleted SOI technology", Toru Tsuboyama, et al., Sep. 2006, Perugia, Italy, Vertex 2006, Nucl. Instr. and Meth A 47545(2007).
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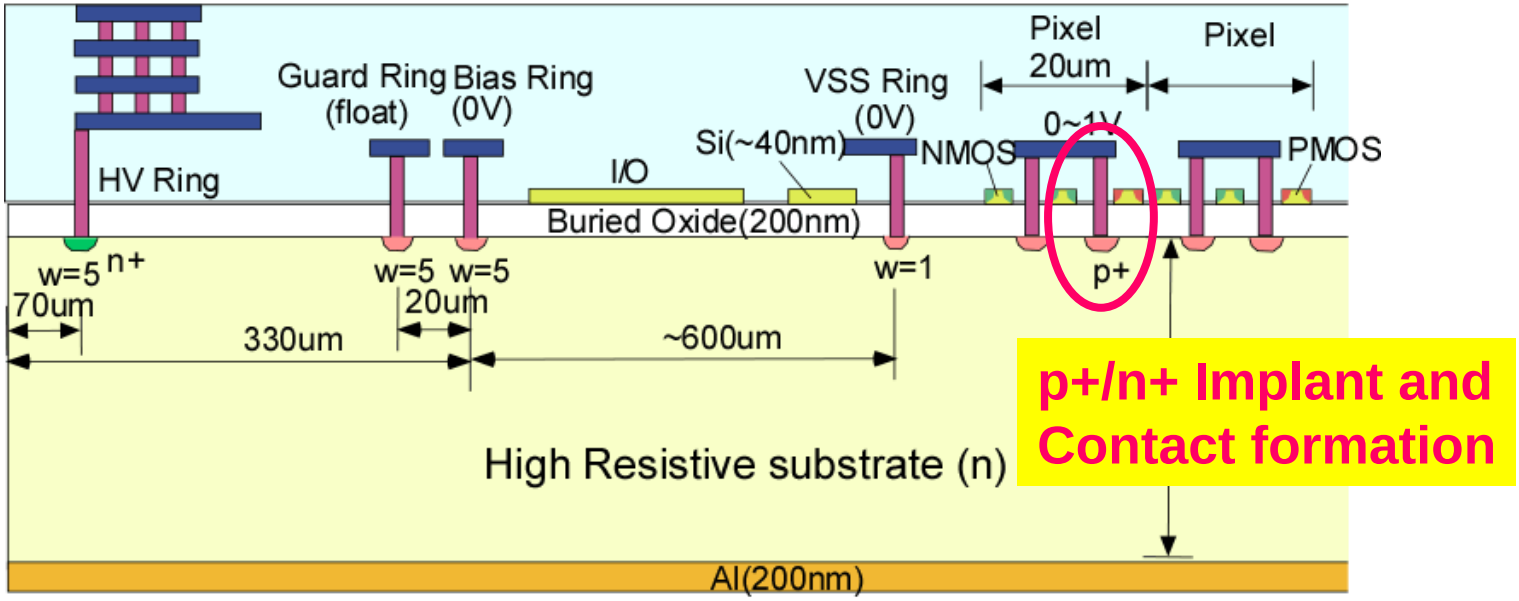
- "R&D of a monolithic pixel sensor based on 0.15 μmfully depleted SOI technology", Toru Tsuboyama, et al., Nucl. Instr. and Meth A 47566(2007).
- "SOI pixel developments in a 0.15μm technology", Arai, Y.; Ikegami, et al., IEEE Nucl. Sci. Sympo., Conf. Record, Vol. 2, 2007 pp. 1040 – 1046
- "Total Dose Effects on 0.15μm FD-SOI CMOS Transistors", Y. Ikegami, et al., 2007 IEEE Nuclear Science Symposium Conference Record, N44-6, pp. 2173-2177.
- "A monolithic pixel sensor in fully depleted SOI technology", Nucl. Instr. and Meth. A, Vol. 583, 2007, pp. 526-528, Marco Battaglia, Dario Bisello, Devis Contarato, Peter Denes, P. Giubilato, L. Glesener and C. Vu. (LBNL)
- "Perspectives for low noise detector readout in a sub-quarter-micron CMOS SOI technology", Re, V.; Gaioni, L.; Manghisoni, M.; Ratti, L.; Speziali, V.; Traversi, G. ; Yarema, Ray; IEEE Nucl. Sci. Sympo., Conf. Record, Vol. 3, 2007, pp. 1873 – 1877. (FNAL)

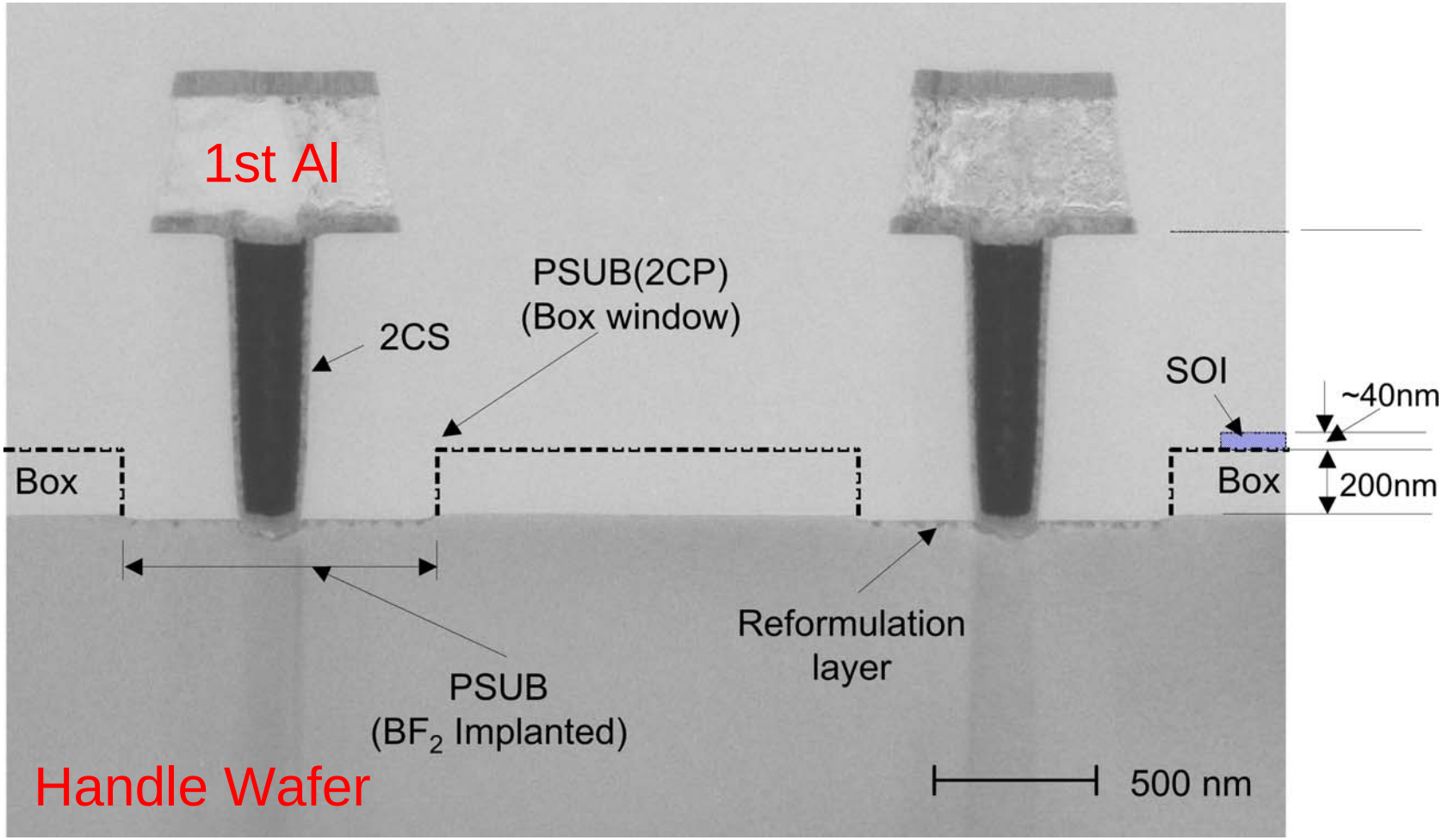
SOI Pixel Process

Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type)*, 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).



(This figure is not to scale)

Metal via contact & p+ implant



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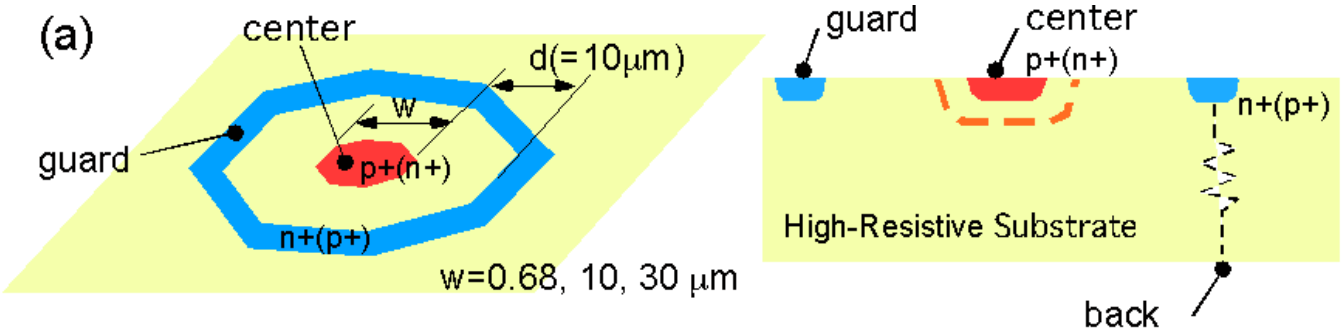
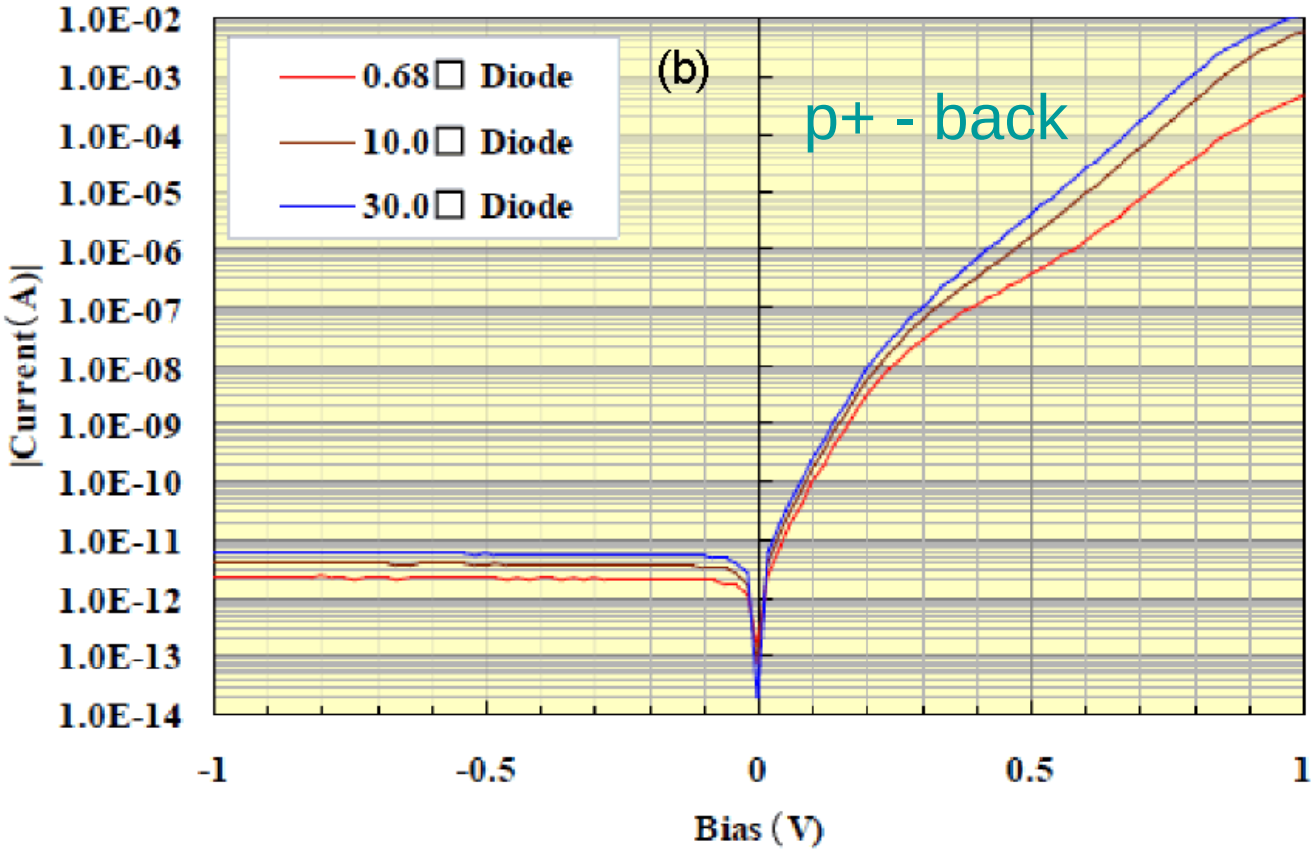
p-n junction I-V characteristics



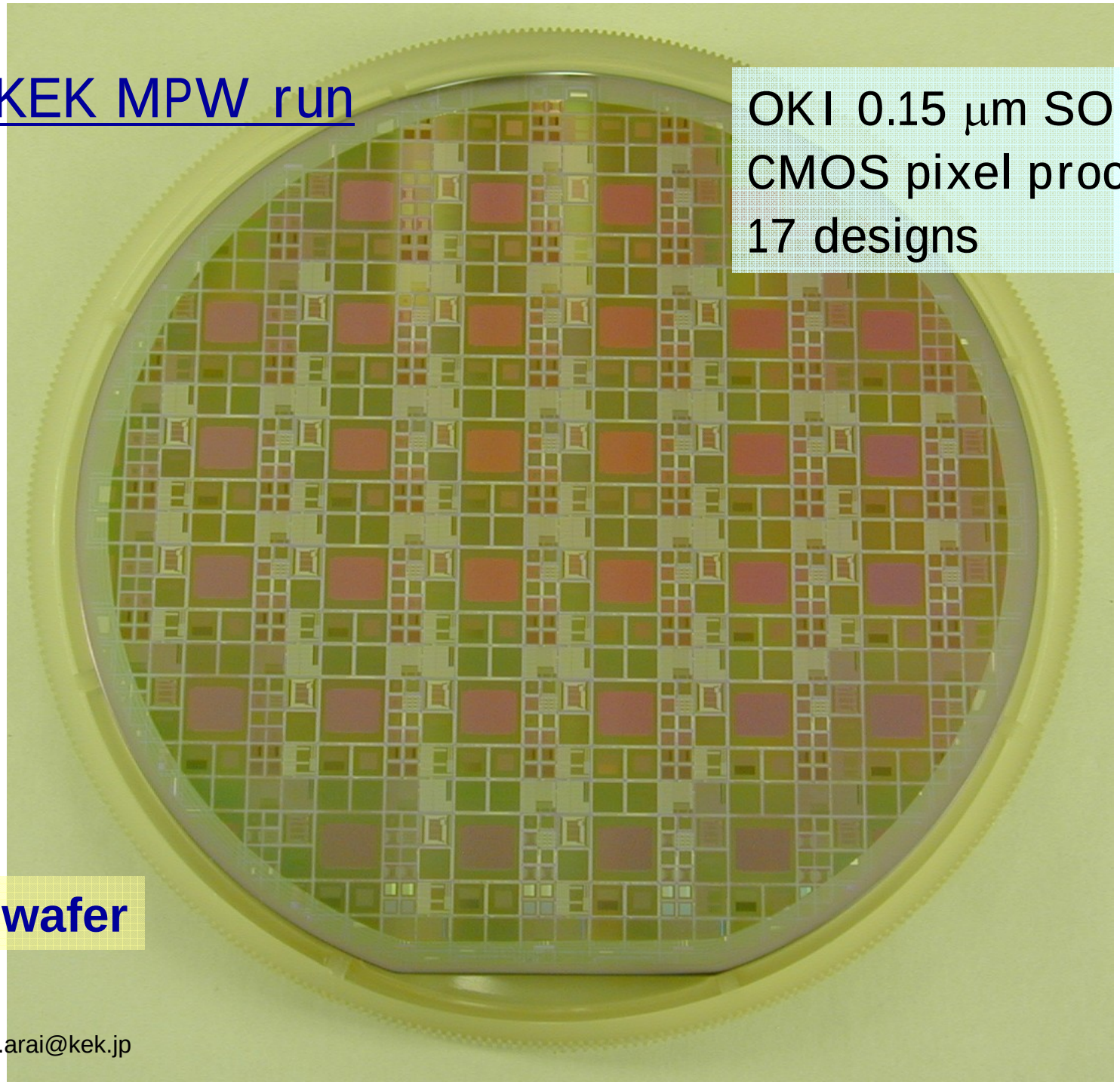


Confirm good diode characteristic.

Substrate is n type.
~700 Ω-cm
(~6 x 10^{12} cm^{-3})

1st KEK MPW run

OKI 0.15 μm SOI
CMOS pixel process
17 designs



6"ϕ wafer

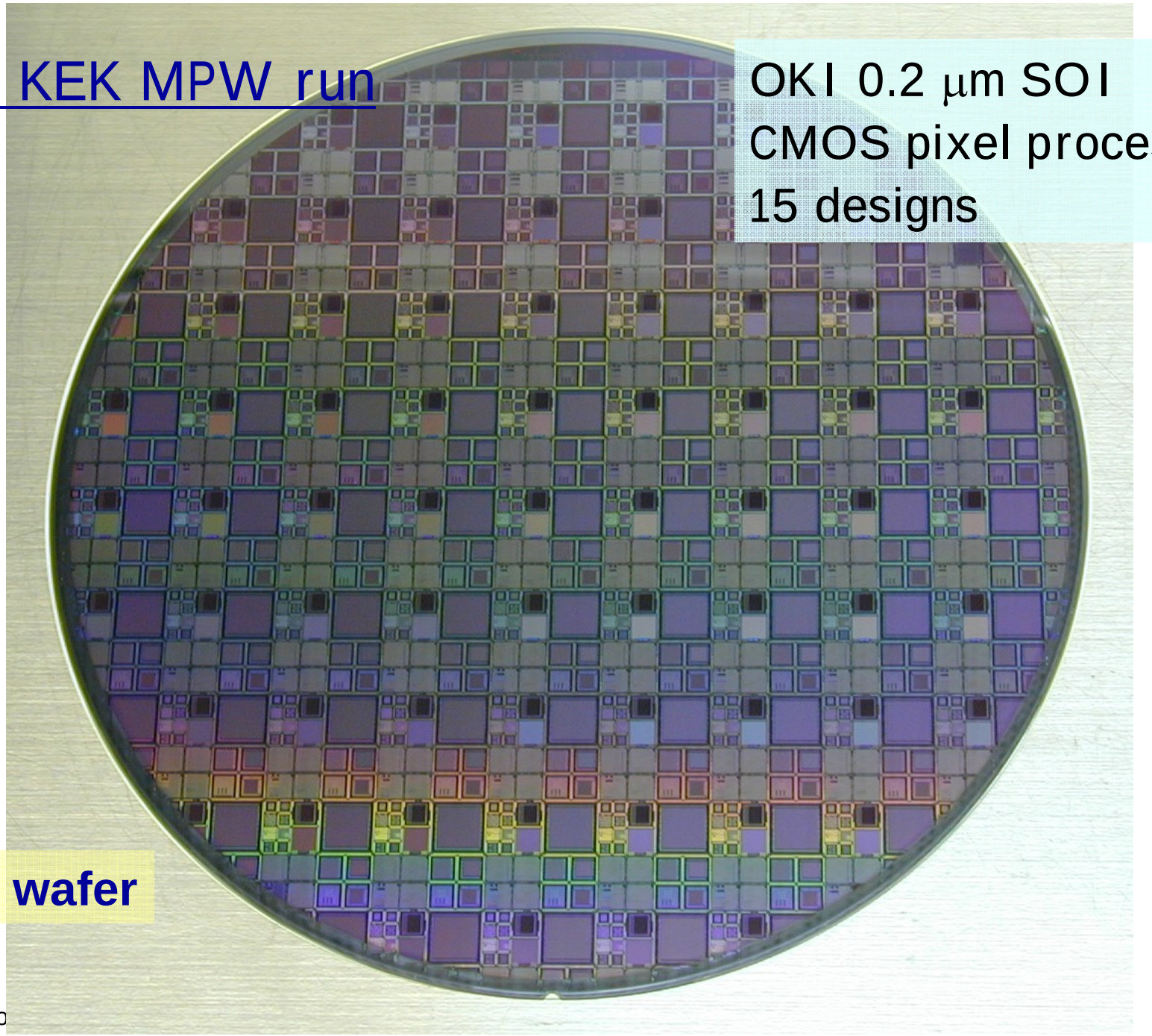
Process Change

- OKI 0.15μm Lab. line was closed in March 2007, then we moved to OKI 0.2μm Mass Production line.
- Although feature size is a little bit increased, 0.2um process looks more adequate to pixel due to its higher operating voltage and low leakage current.
- The 0.2μm process should have better quality due to mass prod. line.

	0.15 μm	0.2 μm
Wafer Diameter	6 inches	8 inches
Core (I/O) Voltage	1.0V (1.8V)	1.8V (1.8/3.3V)
Gate Length	0.14 μm	0.2 μm
Gate Oxide Thickness	2.5/5 nm	4.5/7 nm
BOX Thickness	200 nm	200 nm
Ioff	<100 pA/μm	<0.1 pA/μm

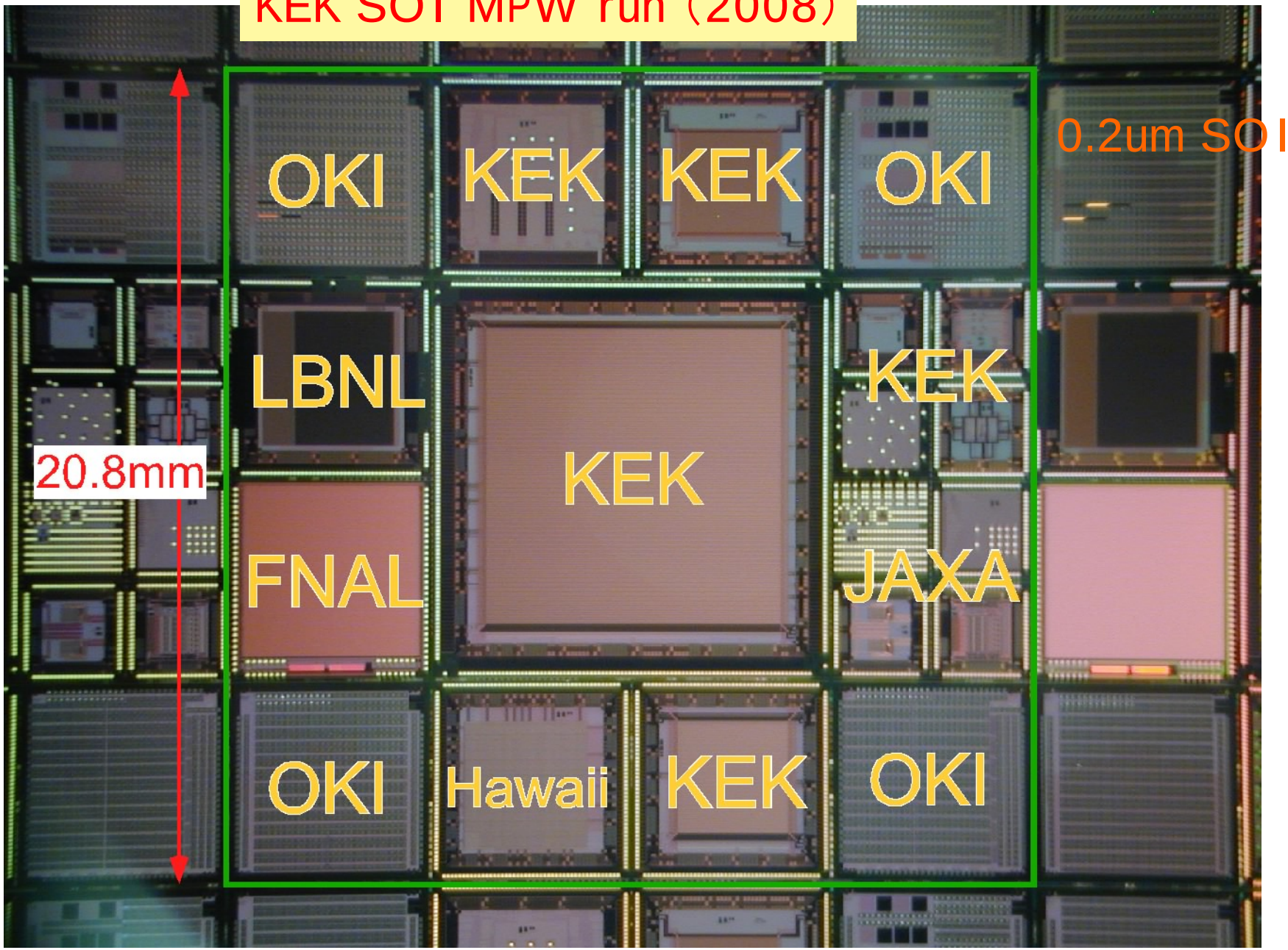
2nd KEK MPW run

OKI 0.2 μm SOI
CMOS pixel process
15 designs



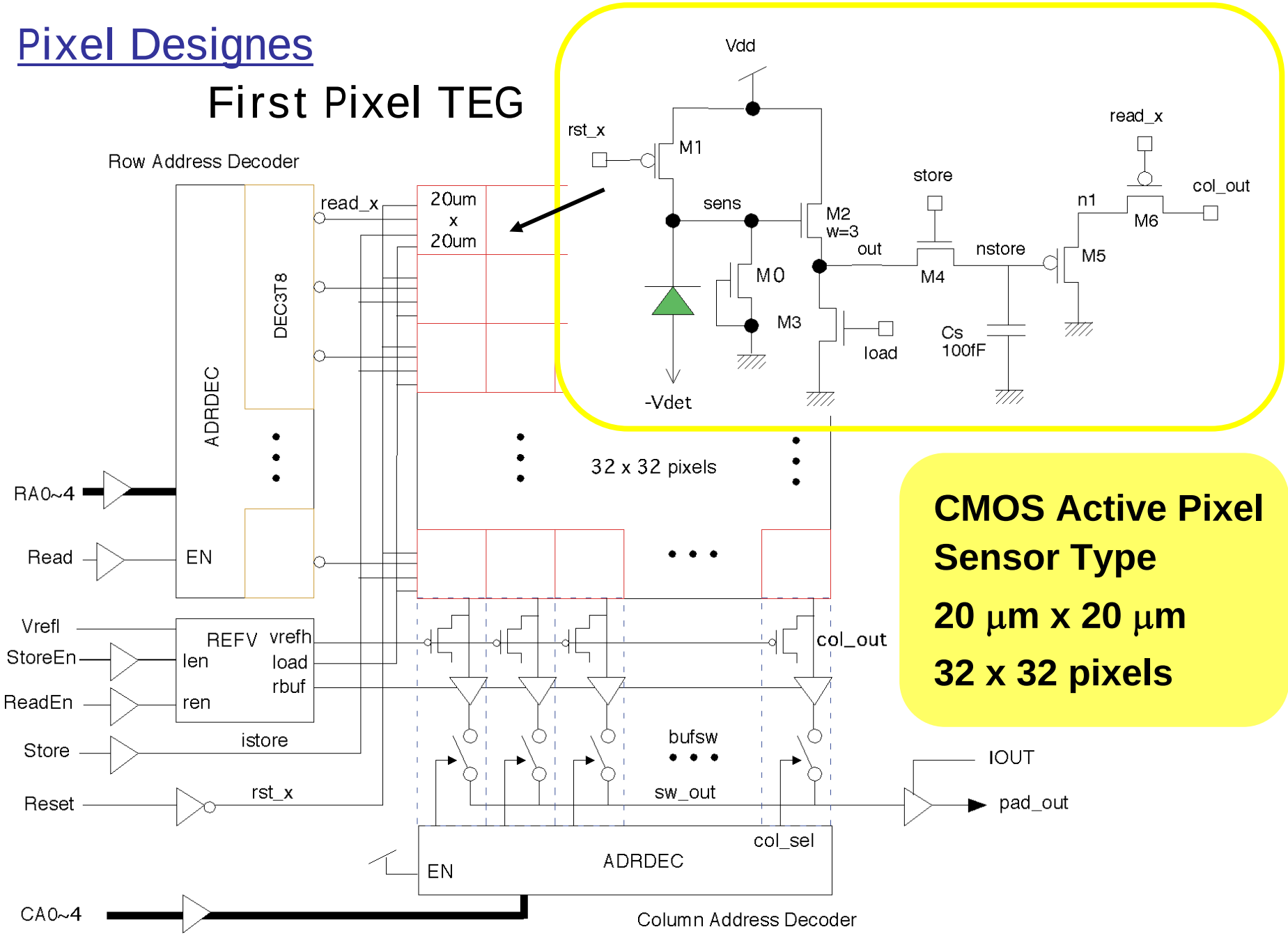
8"ϕ wafer

KEK SOI MPW run（2008）



Pixel Designes

First Pixel TEG

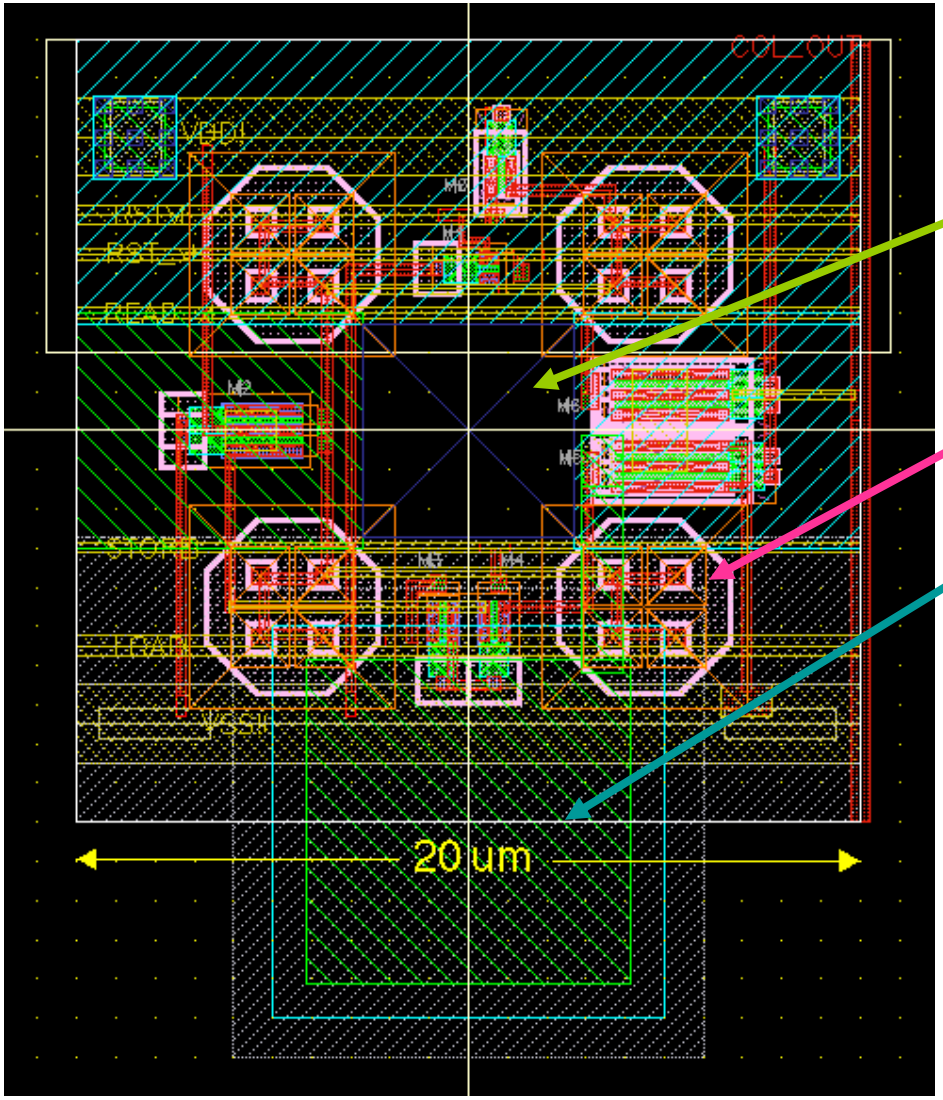


CMOS Active Pixel Sensor Type

20 μm x 20 μm

32 x 32 pixels

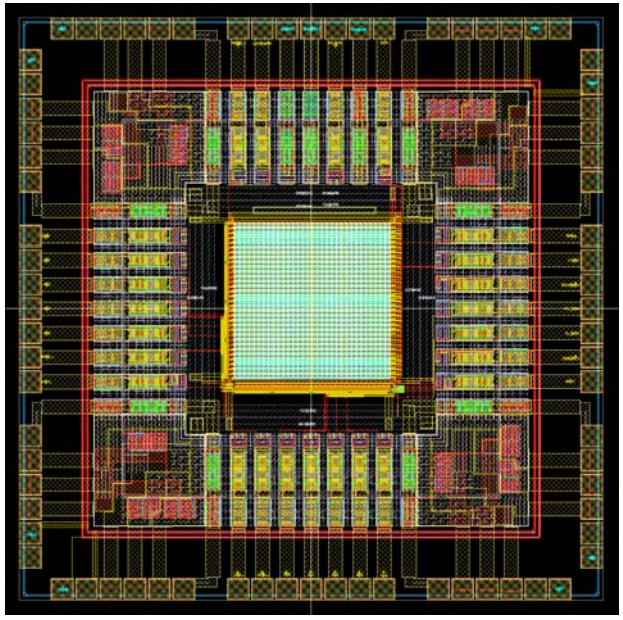
Pixel Layout



Window for Light Illumination (5.4 x 5.4 um^2)

p+ junction

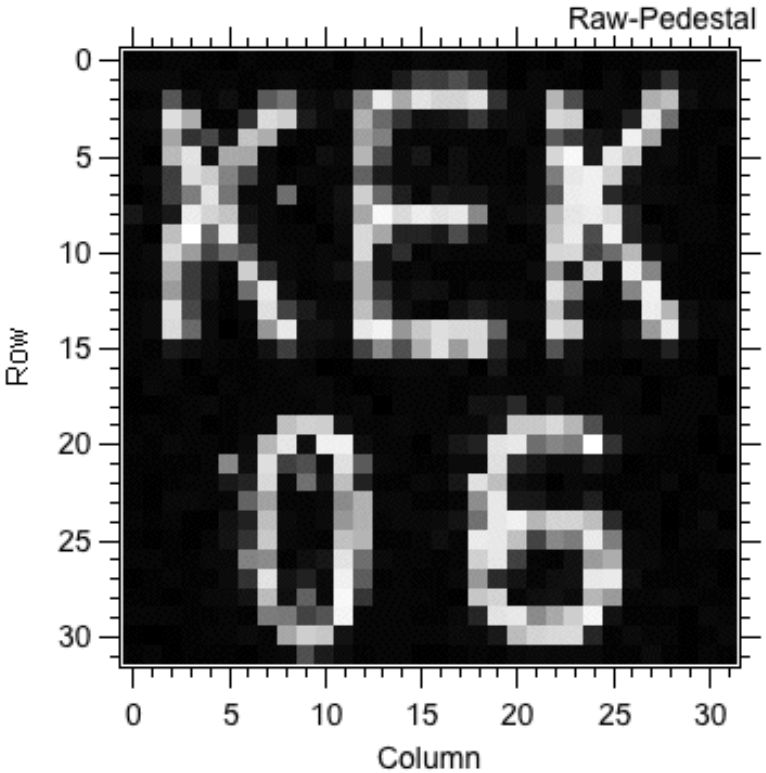
Storage Capacitance(100 fF)



2.5 x 2.5 mm^2

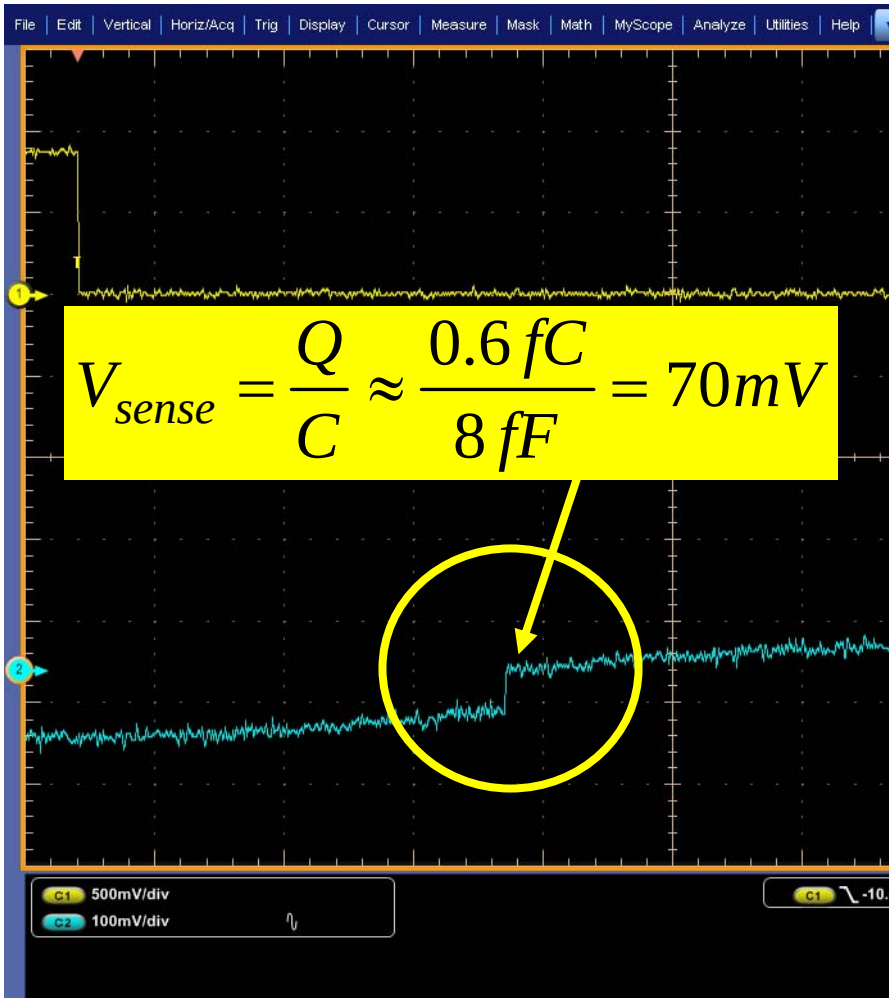
Laser Image

32x32 image view with 670nm Laser and plastic mask



Vdet = 10 V, Exposure Time = 7 ms

β-ray (^{90}Sr) Signal



KEK : I-V characterisitic of the detector

2.5 x 2.5 mm^2 chip

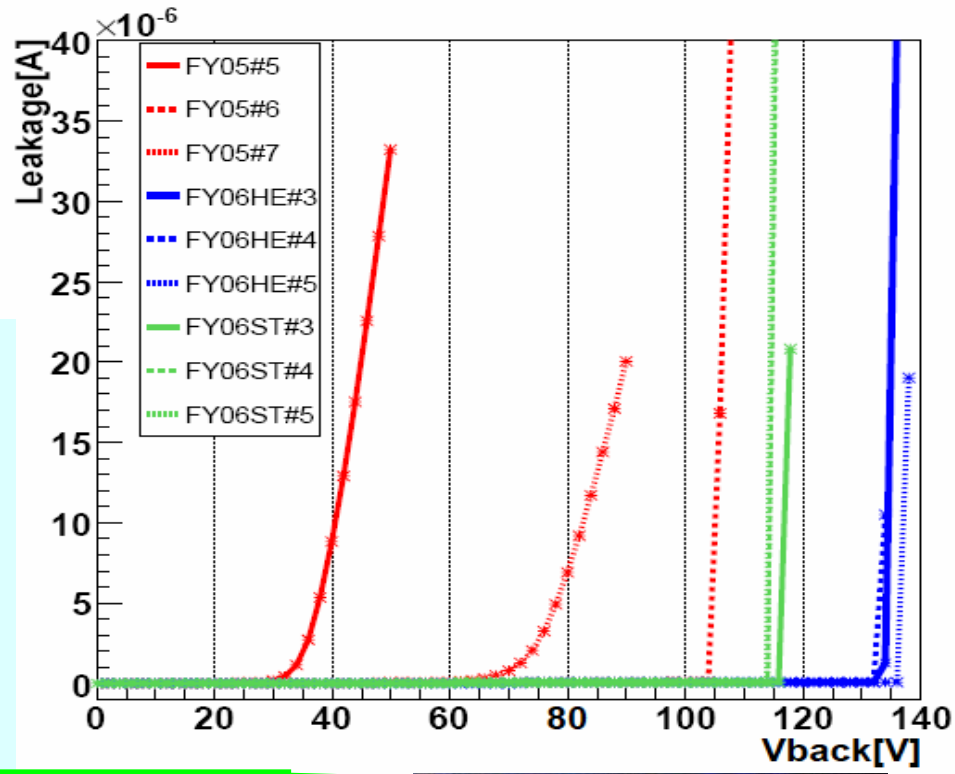
FY05

↓ Round the corner of bias ring.

FY06(Std.)

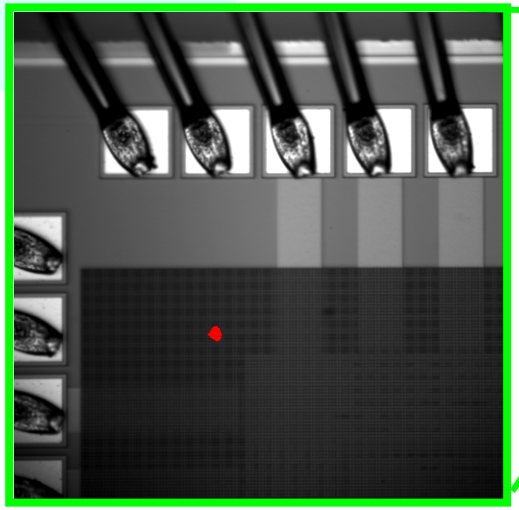
↓ p+/n+ implant with higher E (~x4.7 deep).

FY06(HE)

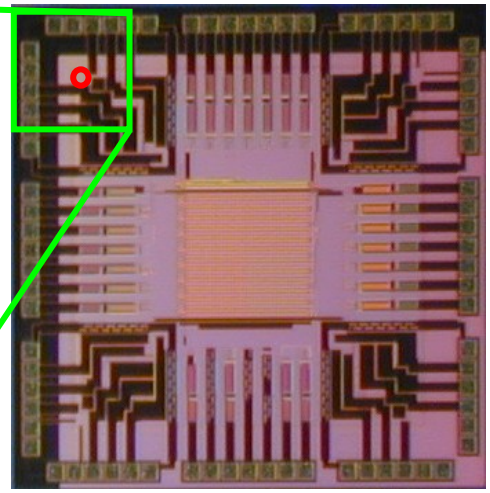


become better, and reached to ~140V.

Micro Discharges are observed with infrared camera



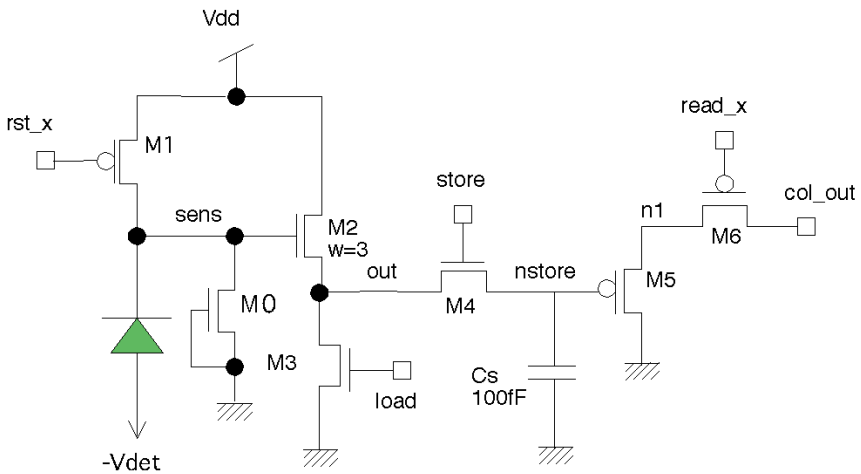
I = 40 μA, T = 1 min

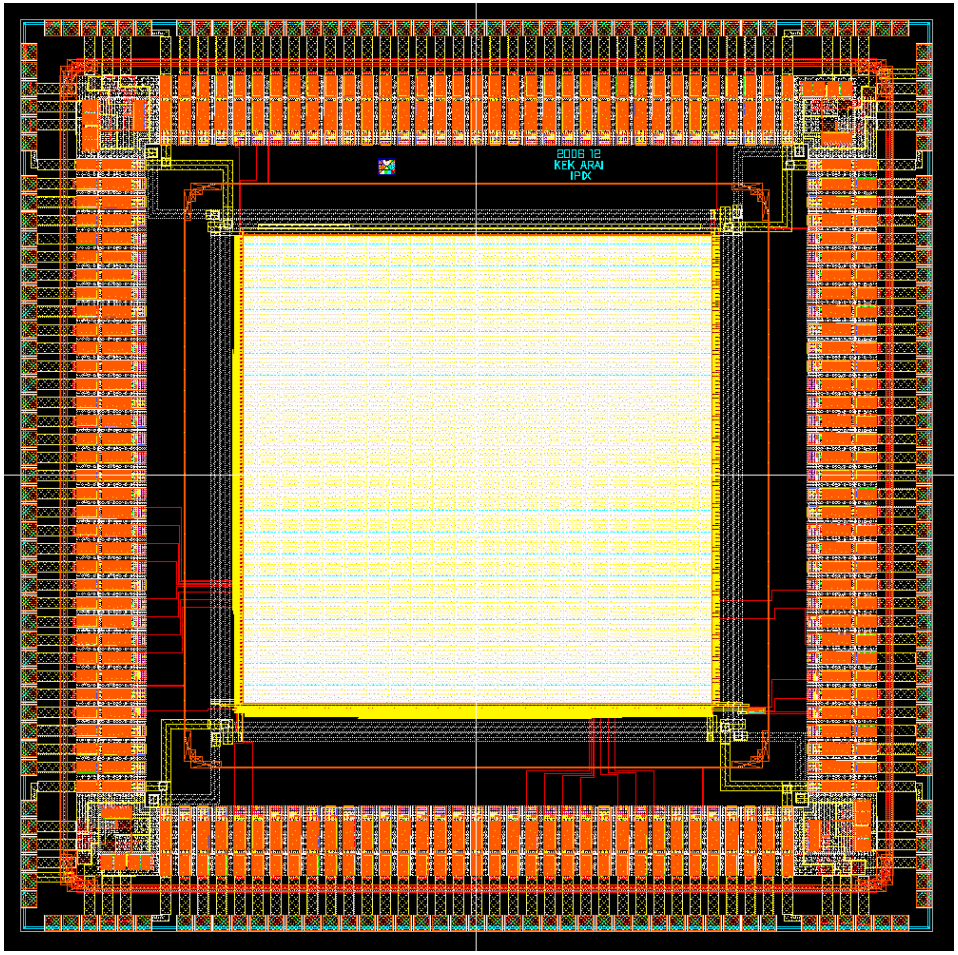


Corner of the bias ring

KEK : Integration Type Pixel (INTPIX)

- 20 μm x 20 μm pixel (same as FY05 design)
- 128 x 128 pixels
- 5x 5 mm^2 chip

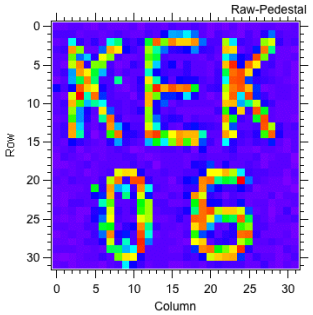




Laser Image

TOPPIXN

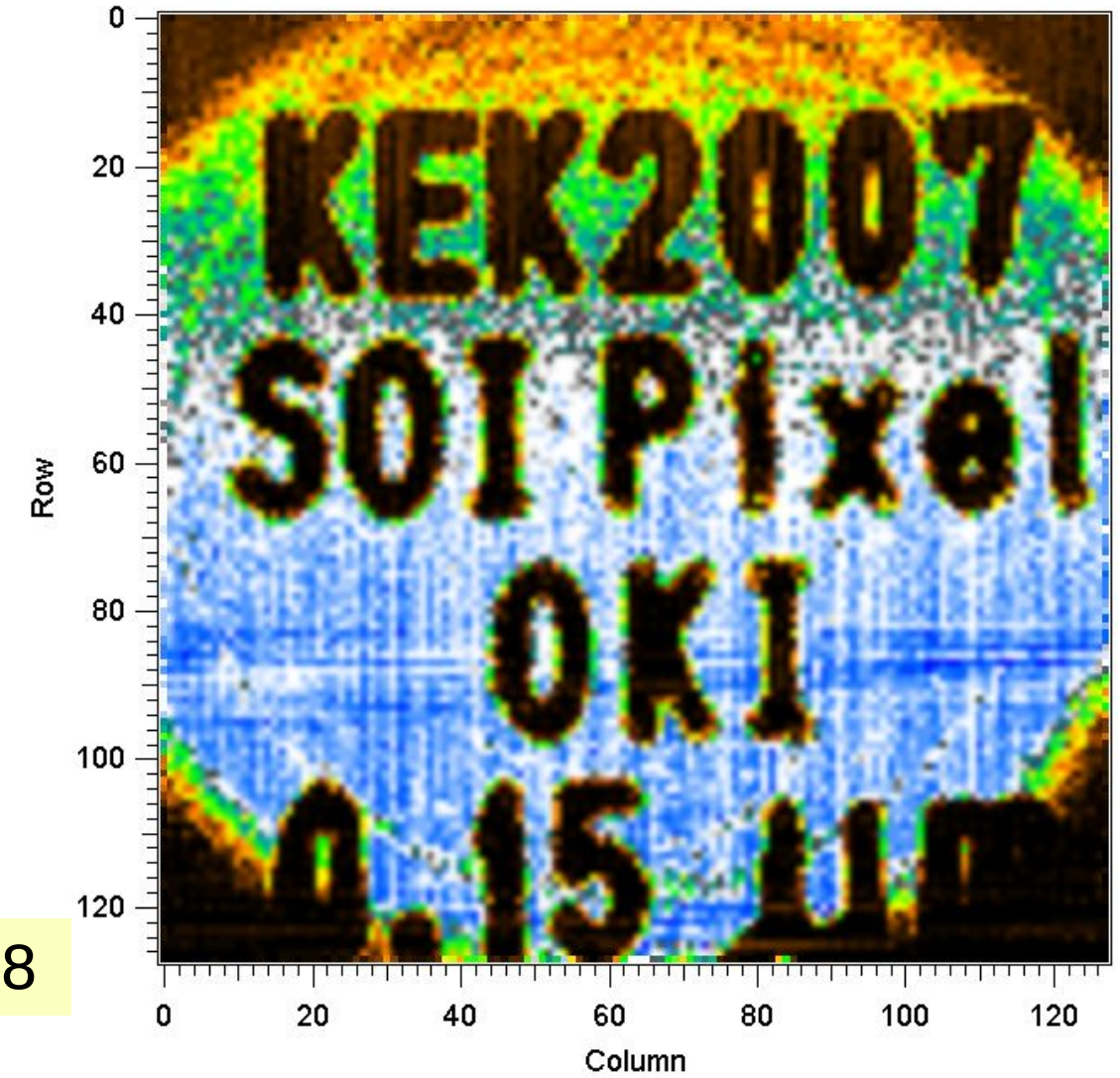
0.64 mm



32x32

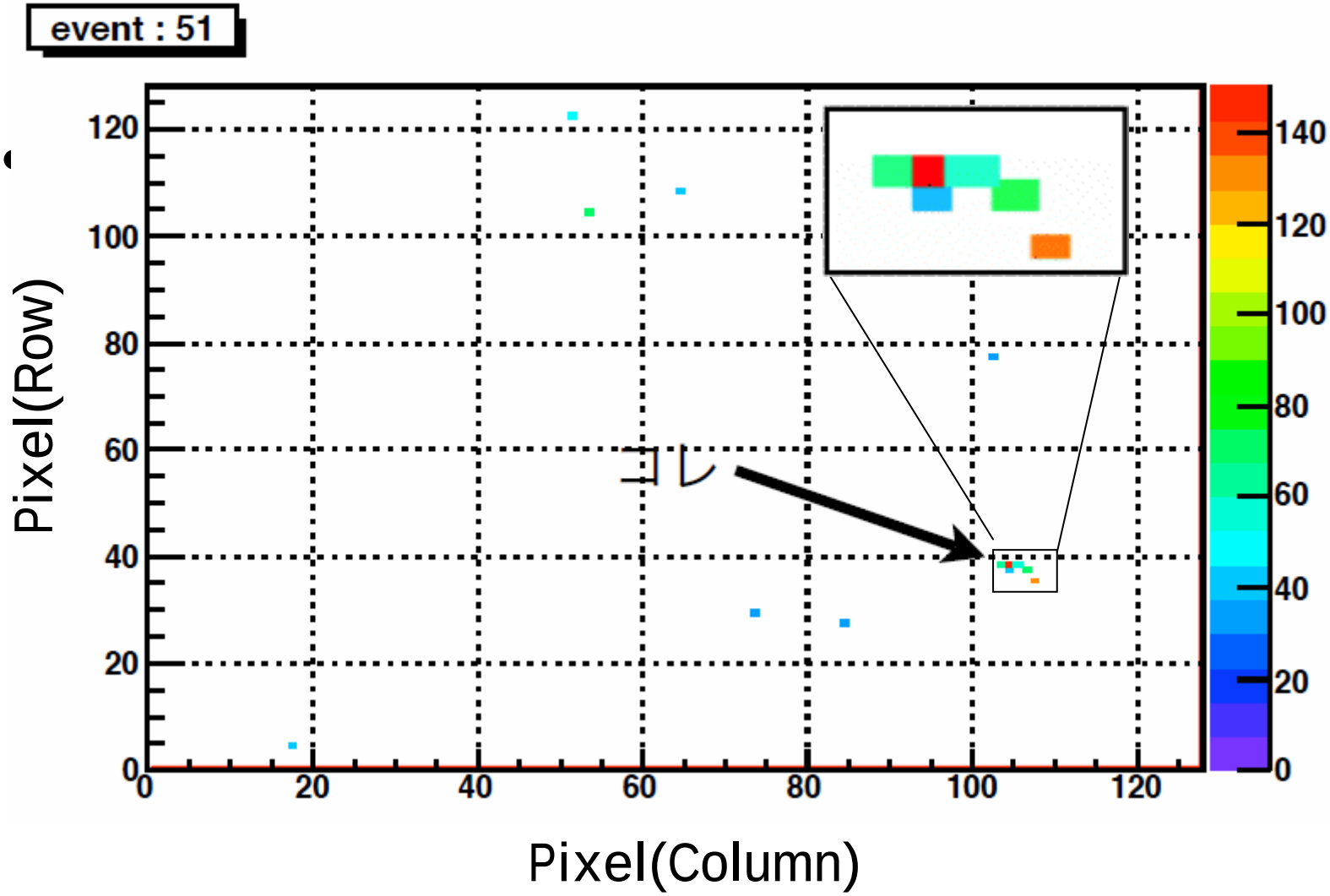
INTPIX1

2.56 mm



128x128

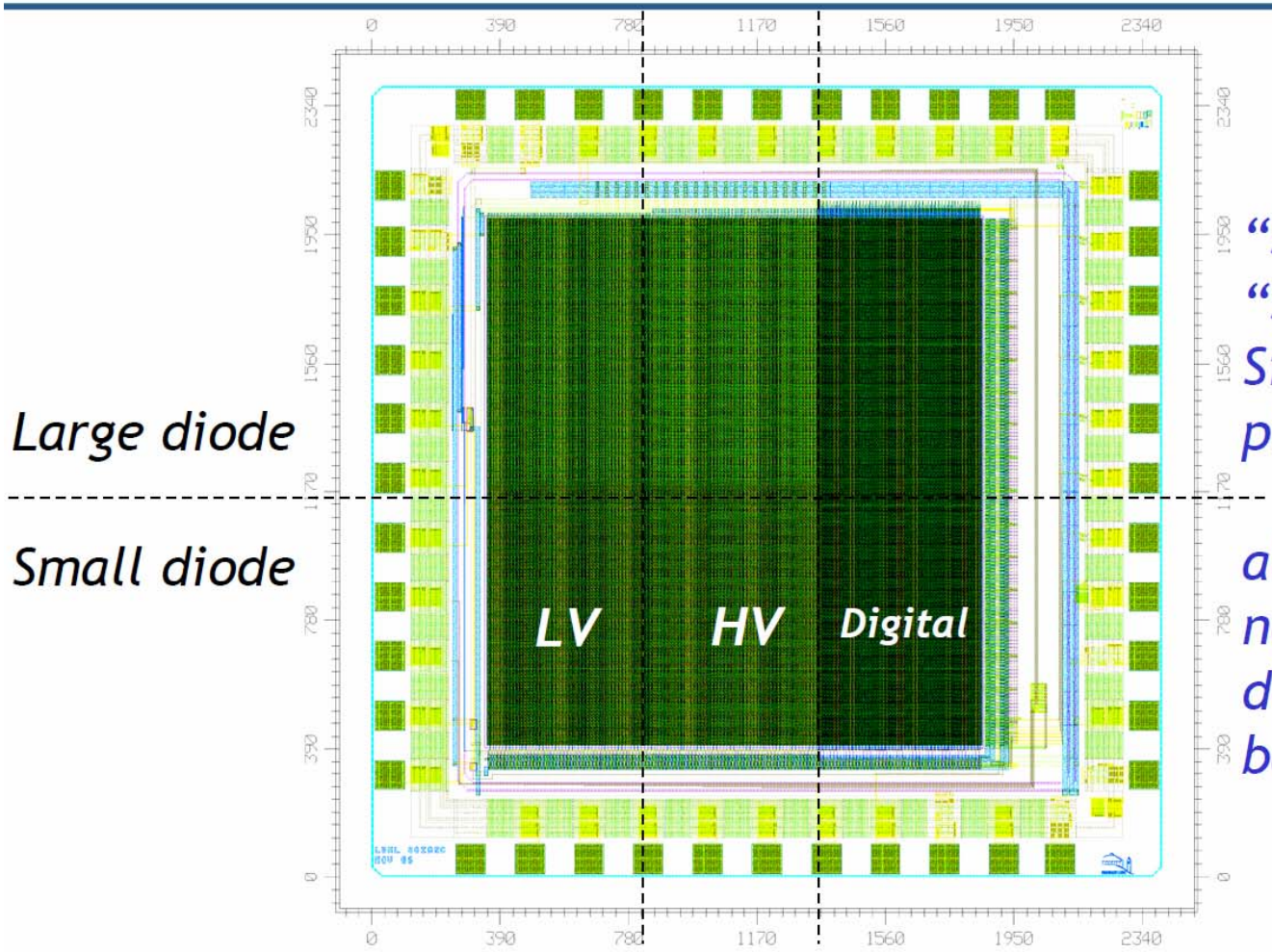
β-ray Detection



LBNL Pixel

Peter Denes

LBNL SOI Test Chip 12/06



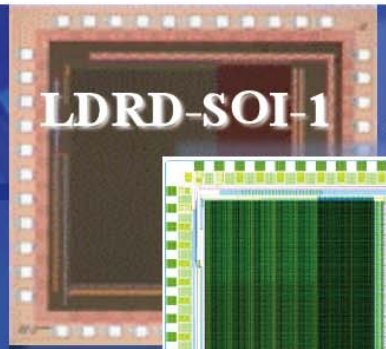
Large diode

Small diode

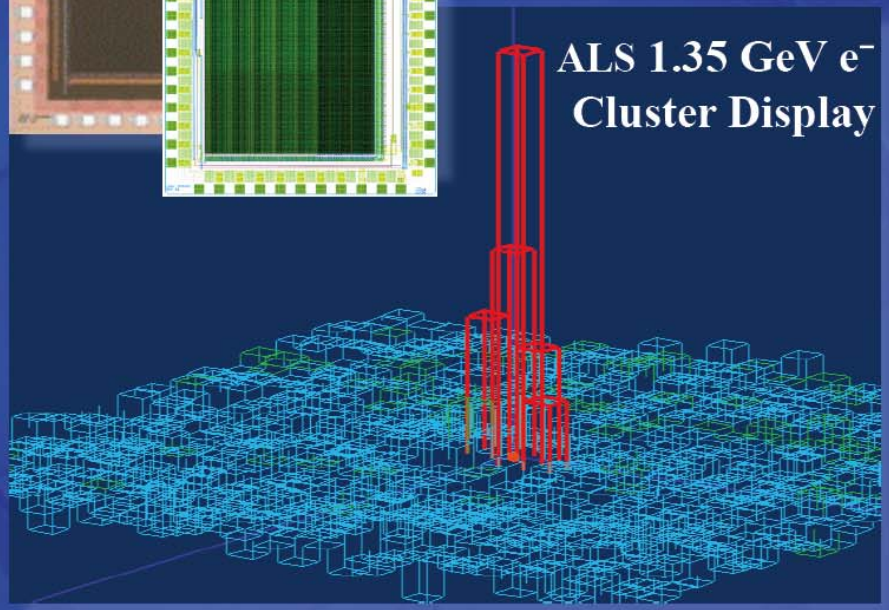
"3T" LV pixel
"3T" HV pixel
Simple digital pixel

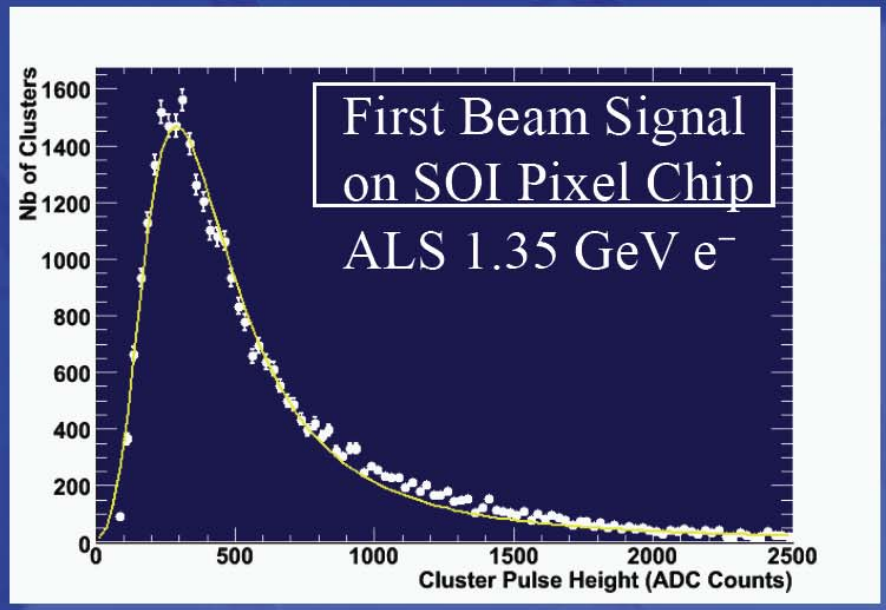
all work, but not as well as desired (due to backgating)

LAWRENCE BERKELEY NATIONAL LABORATORY



LDRD-SOI-1 Analog Pixels: Beam Test





V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>	Signal MPV (ADC)	S/N
1	9.7	0.05	3.31	132	8.9
5	14.0	0.12	3.39	242	14.9
10	7.8	0.20	3.31	316	15.0
15	3.9	0.01	2.45	301	13.6

to appear in NIM A (2007)

FNAL: MAMBO - Monolithic Active pixel Matrix wit Binary cOunters

Fermilab

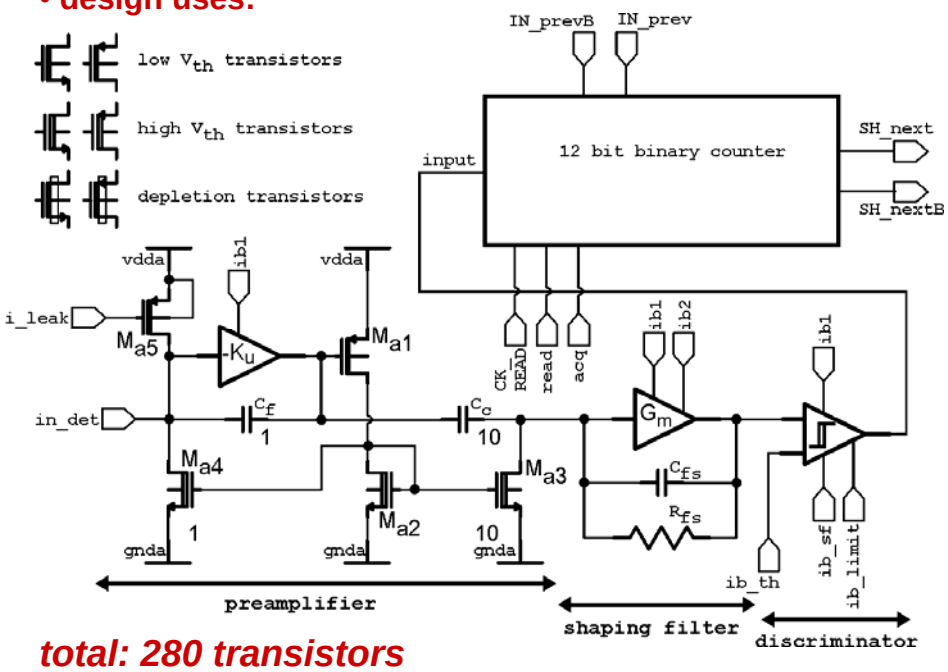
G. Deptuch

- applications
  - imaging detector for direct detection in electron microscopy (TEM), and soft X-rays,

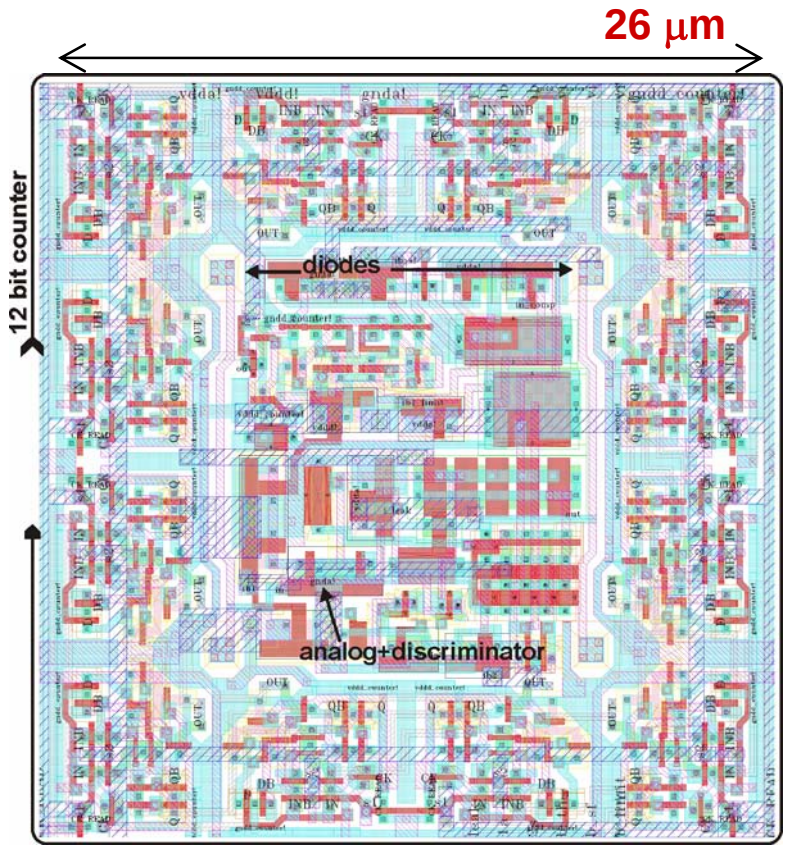
design:

- test prototype 64x64 pixels, pitch 26μm, 4 parallel diodes /pixel (distance ~13μm),
- each pixel: CSA, CR-RC^2 shaper, discriminator + 12 bit binary counter,
- counter reconfigurable to shift register – readout serial (caterpillar) through all pixels.

- pixel:
  - design uses:



total: 280 transistors



FNAL: MAMBO

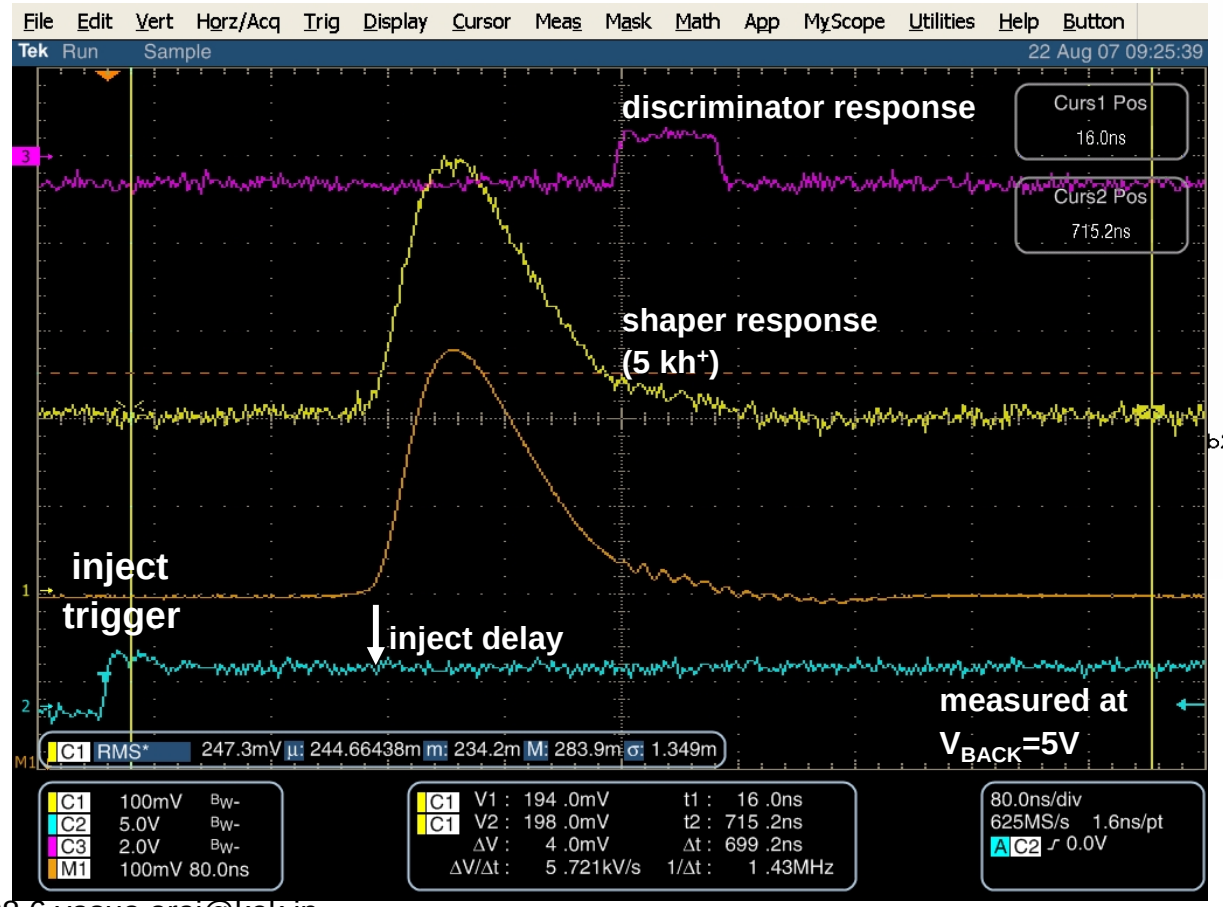
G. Deptuch

tests: ▸▸ performed till now: measurements on test structures

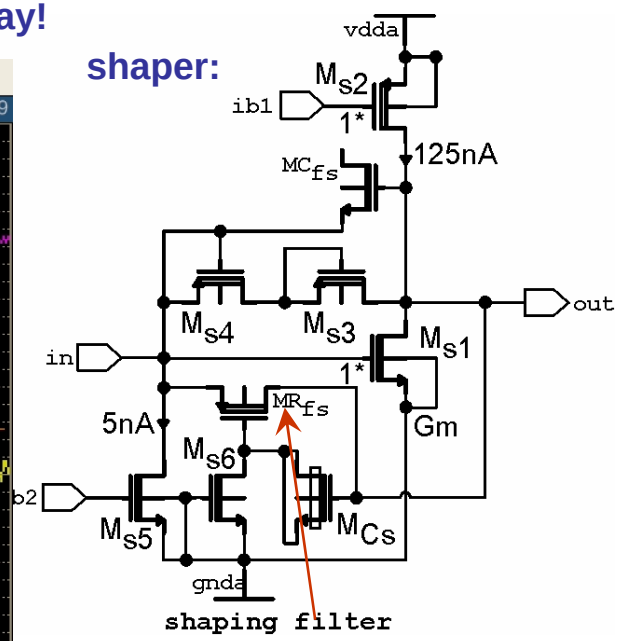
- analog channel with charge injection by pulse generator OK,
- counter/shift register OK, (proper operation requires back-gate voltage above certain level ~5V due to conflicting leakage of NMOS and PMOS transistors in OFF state)
- discriminator OK,

→ Gain significantly lower and shaping much faster – seems to be understood;

acquisition of full scale images is underway!



shaper:



feedback resistance PMOS in saturation @ V_{gs}=const

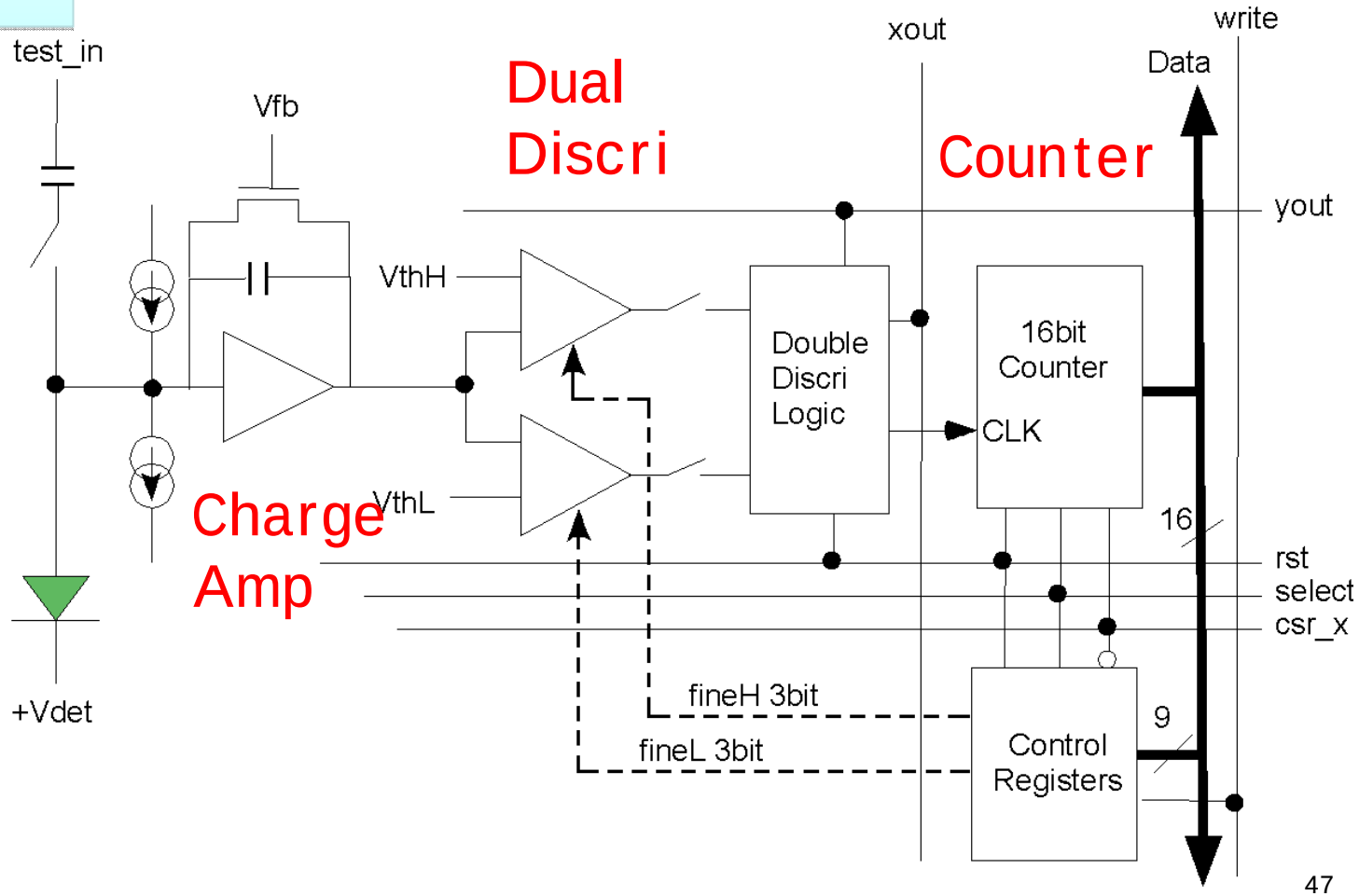
design: 90 MΩ

measurements suggest: 5-10 MΩ (L=150nm PMOS low VT)

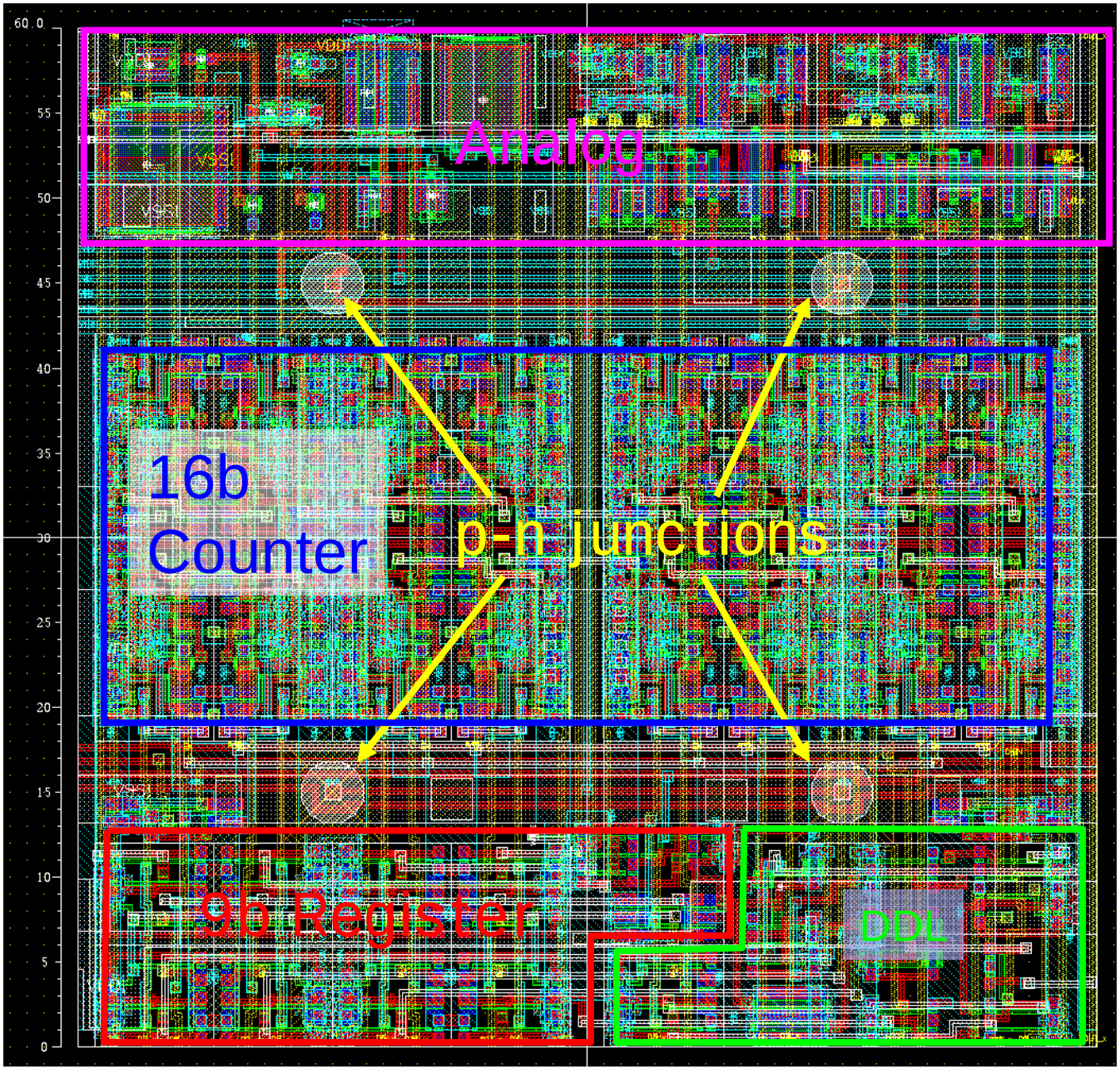
Counting Type Pixel (under development)

Energy window and counting in each pixel

10.4 mm□、128 x 128 pix



47

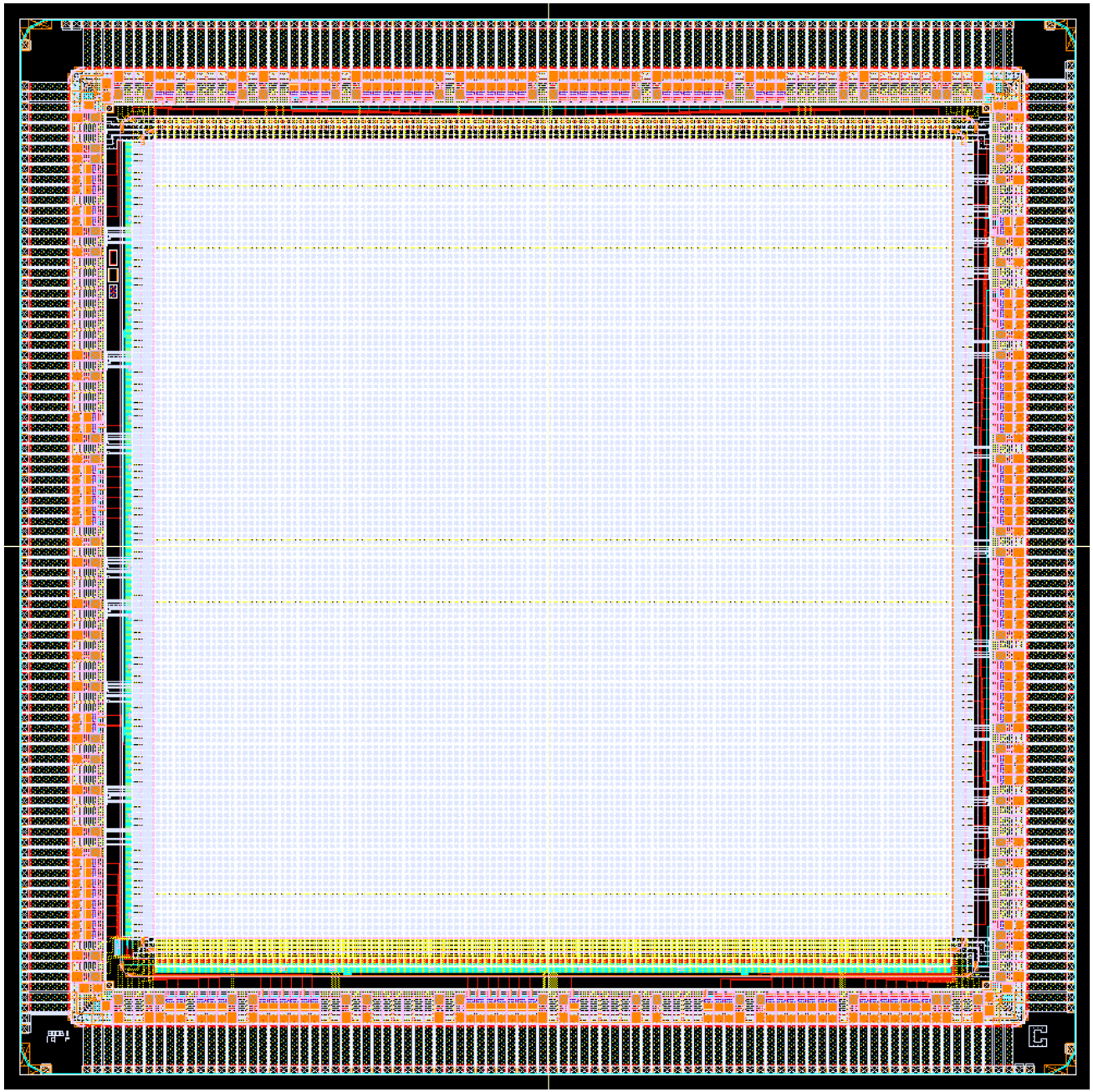


CNTPIX2

~600 Transistors
x 128 x 128
= 10,000,000 Trs

60x60 um^2

48



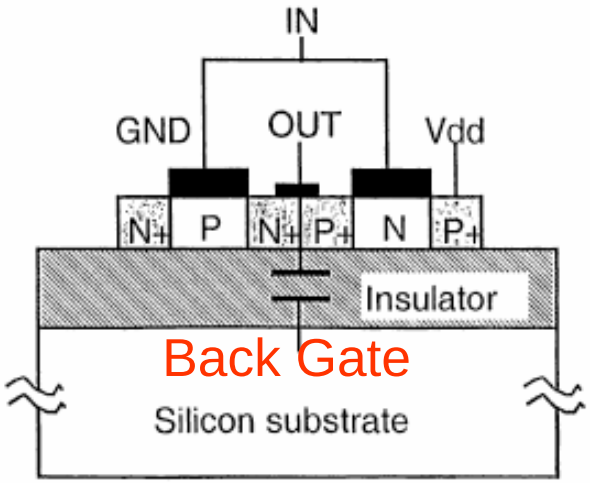
CNTPIX2

10.2x10.2 mm^2

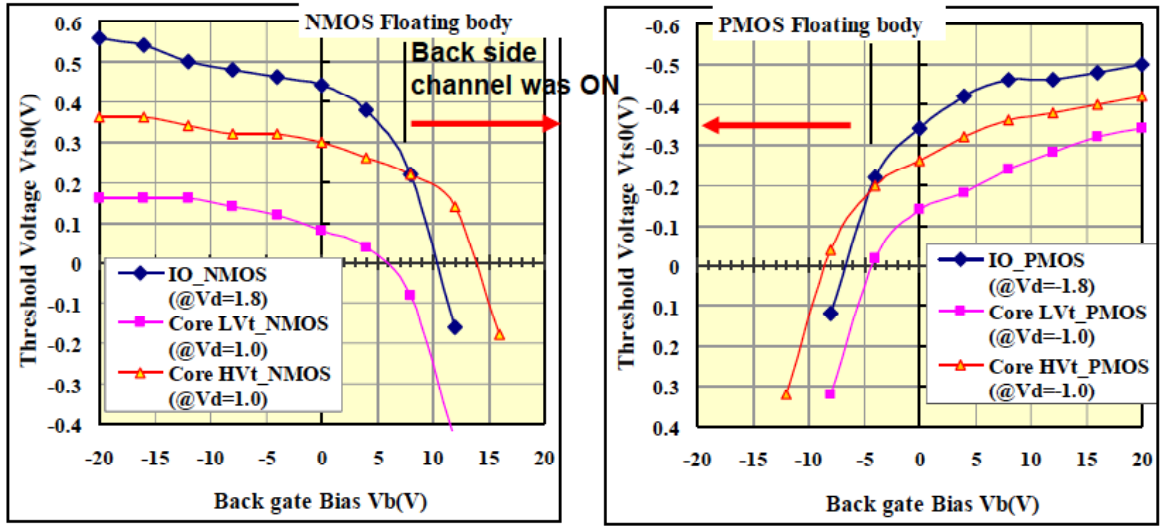
49

Issues in SOI Pixel

Back Gate Effect



NMOS Threshold Variation PMOS transistor



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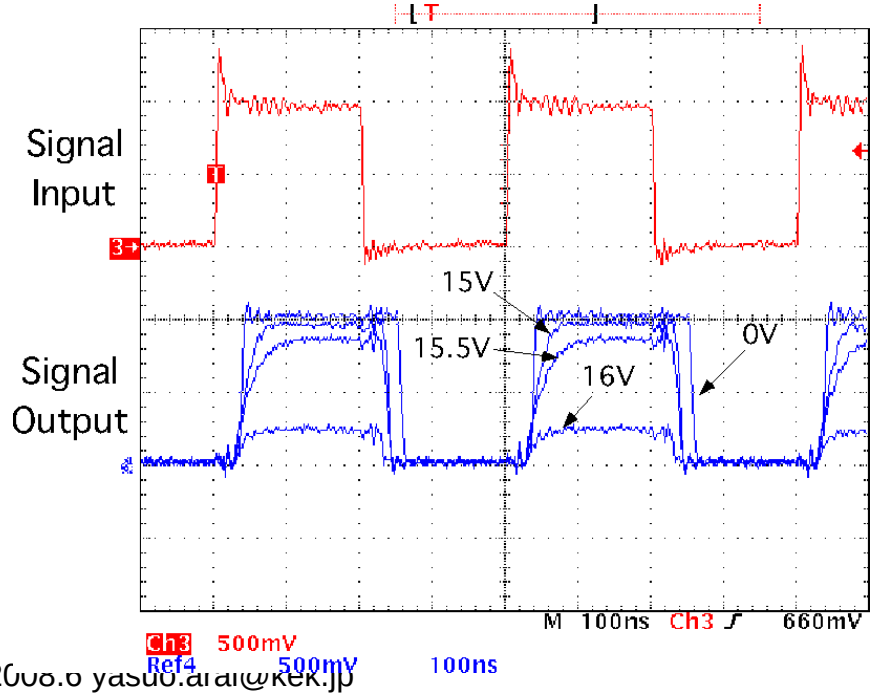


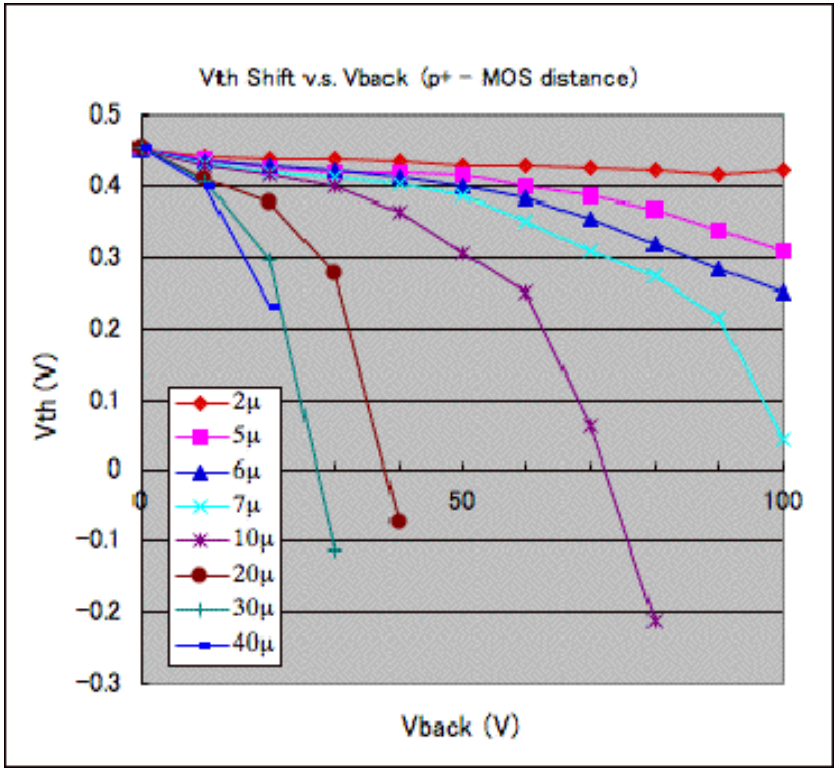
Substrate Voltage act as Back Gate, and change transistor threshold.

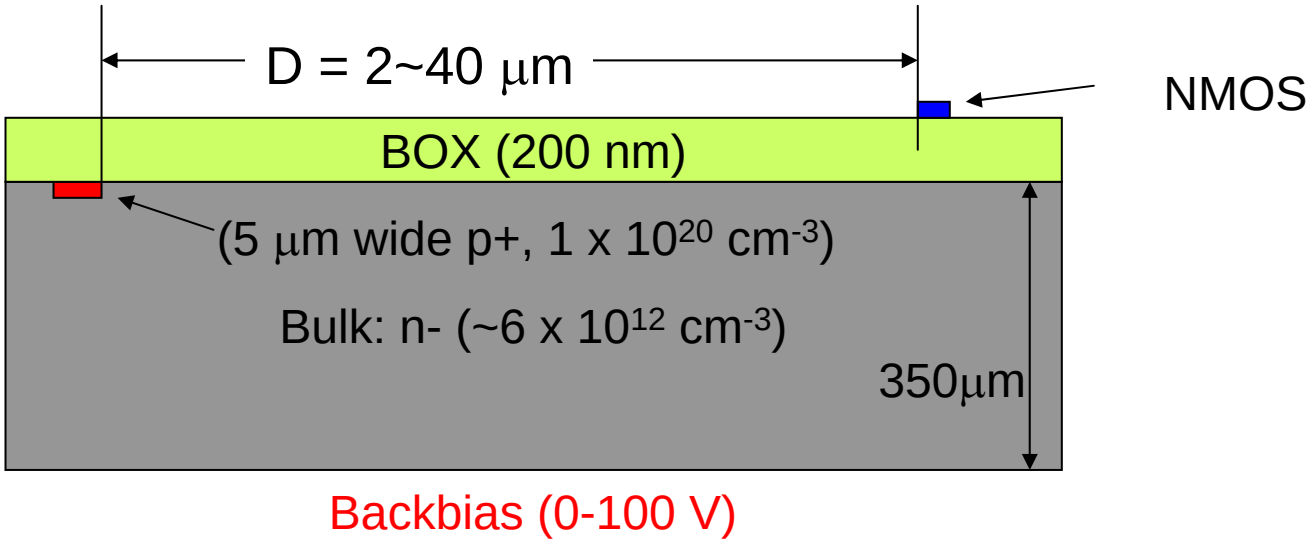
Signal disappeared at V_{det}=16V due to the back gate effect.

TCAD Simulations

ENEXSS :
3D TCAD Simulator developed by SELETE Consortium Japan.

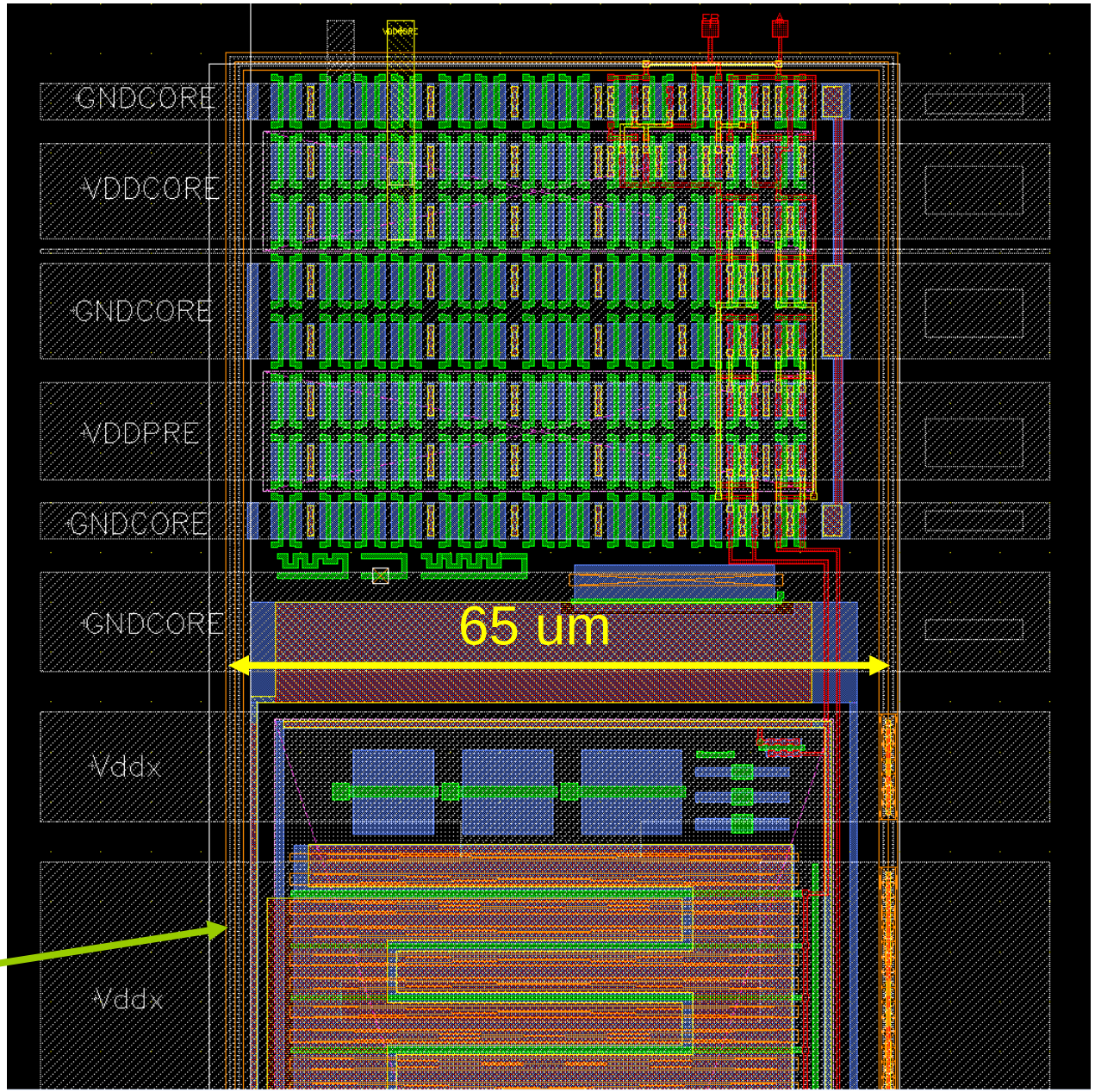
Back Gate effect can be reduced by placing p+ implant near transistors.





p+ Guard for I/O Buffer

It is hard to re-design I/O buffers, so we just surround the buffer with p+ ring.

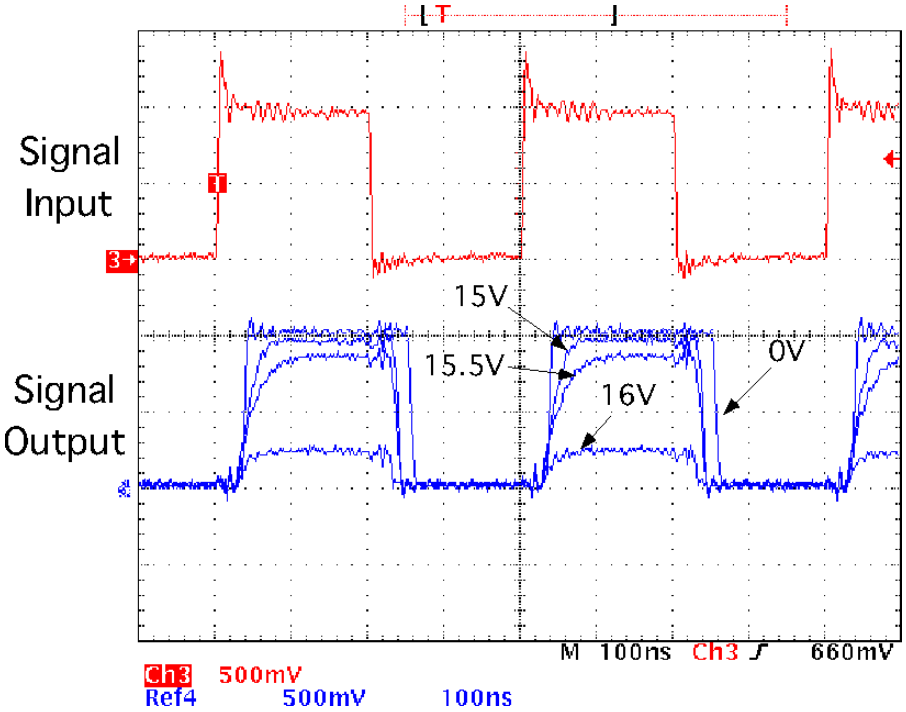


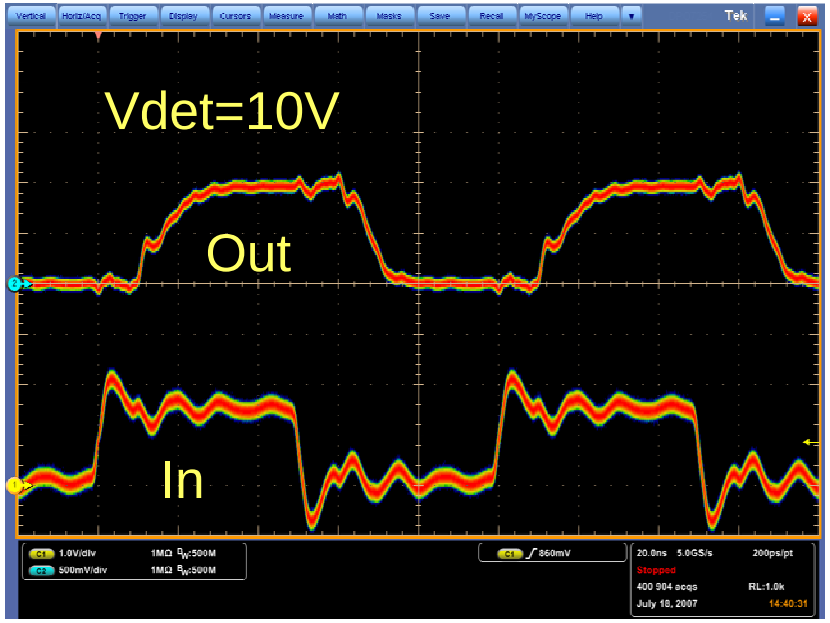
p+ ring

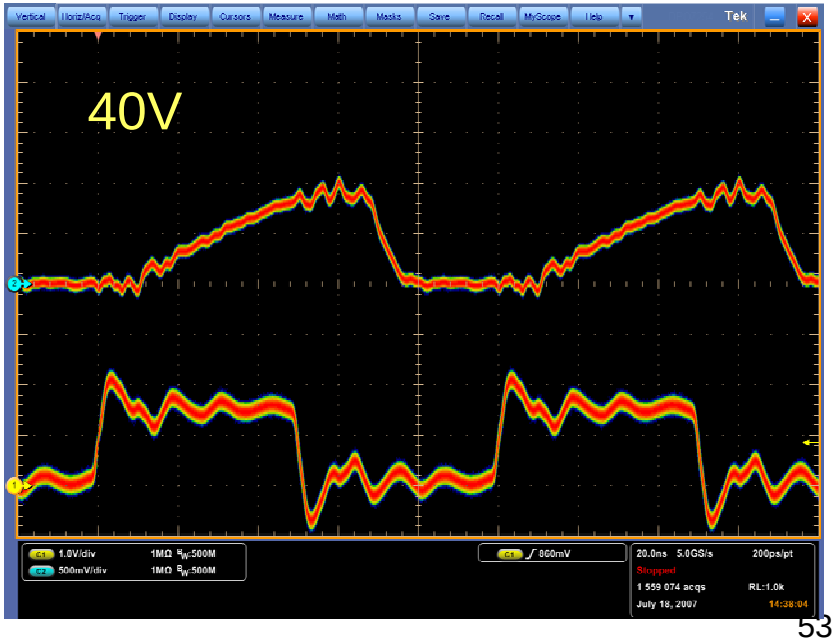
p+ ring = 0V

10MHz Clock

without p+ ring



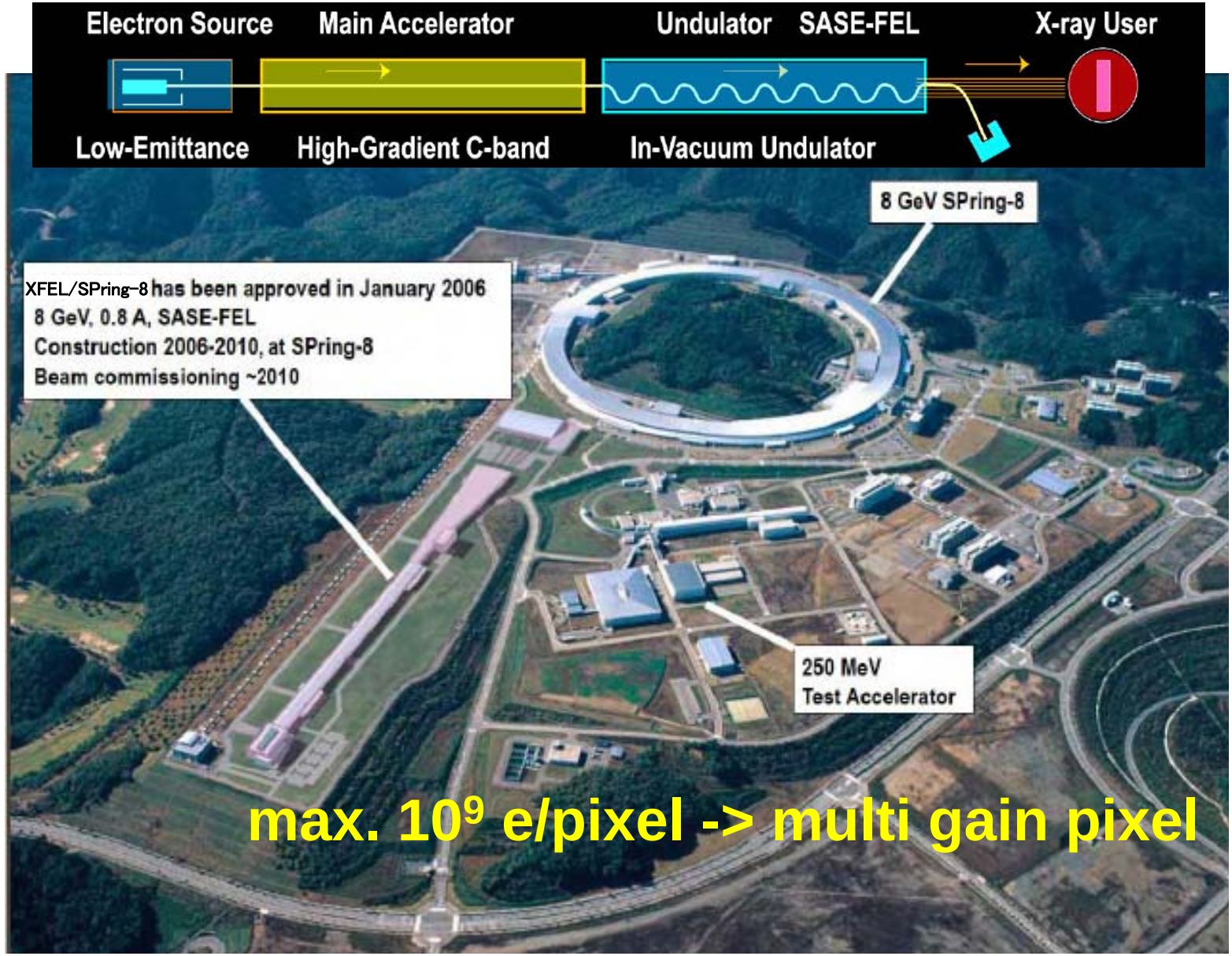




16V --> 40V

Future Applications

XFEL/SPring-8



max. 10^9 e/pixel -> multi gain pixel

Summary

- SOI device has many interesting features to use in HEP, Space, and Imaging at Synchrotron light sources.
- We confirmed the basic operation of SOI pixel detector with OKI 0.15 μm FD-SOI technology.
- In 2006-7, we submitted 1st KEK MPW run with 17 designs including US and Japan Univ./Labs.
- In 2008, we submitted 2nd KEK MPW run in 0.2 μm technology
- Our R&D proposal is approved as a new R&D program in JP-US cooperative program.
- People at Spring-8 also has strong interests in this technology for XFEL application.
- We welcome more people to join to use this technology.