

HIGHLIGHTS OF VITH INTERNATIONAL MEETING ON FRONT-END ELECTRONICS FOR HIGH ENERGY, NUCLEAR, MEDICAL AND SPACE APP.

- ▶ CMOS Technology
- ▶ New Facilities
- ▶ LHC and SLHC
- ▶ Medical Applications
- ▶ Radiation Effects
- ▶ Special Design and New Detectors
- ▶ MAPS
- ▶ Neutrino Experiments
- ▶ Space Applications
- ▶ 3D Electronics
- ▶ International Linear Collider

*Vith INTERNATIONAL MEETING
ON FRONT END ELECTRONICS
for High Energy, Nuclear,
Medical and Space Applications*

May 17th to 20th, 2006
Perugia , Italy

Organizing Committee
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Local Organizing Committee
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MICRON

Participation by invitation only <http://fee2006.pg.infn.it>



INTRODUCTION TO CONFERENCE

▶▶ International Meeting on Front End Electronics is a conference focused on advanced front-end electronics mainly for high energy physics applications. The first meeting was held in Yellowstone in 1992 and since then the meeting has gone back and forth between the US and Europe every 2 or 3 years, with the last one held in Snowmass in 2003. This year meeting took place in Perugia, Italy, from May 17th to May 20th.



▶▶ 42 talks 20' and 30' minutes

▶▶ No formal proceedings of the conference, CD with talks

▶▶ Talks available at

<http://fee2006.pg.infn.it/>

CMOS TECHNOLOGY

▶▶ **(Micron) Intoduction to Micron's Image Sensor Program ...**

no slides available

1.7 μm pixel pitch with 1.5 transistor per pixel

w.r.t. classical 3T/ pixel

1/4 " format 8Mpixel CMOS camera

▶▶ **Special session on MAPS ...**

M. Barbero, UH, USA

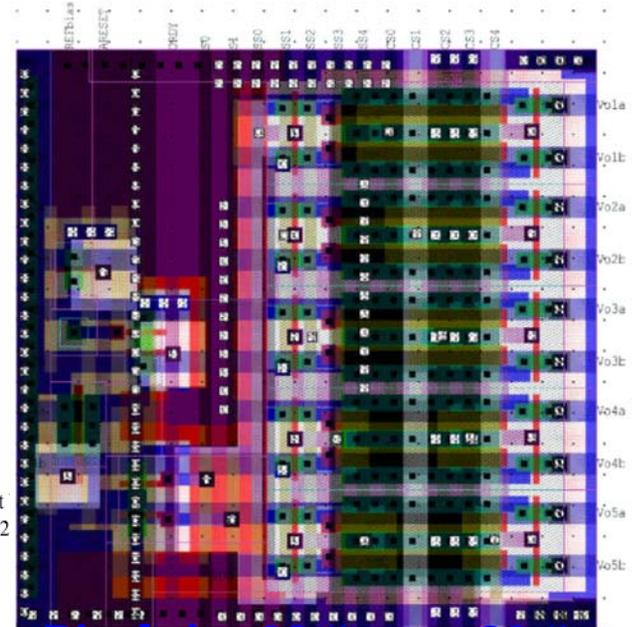
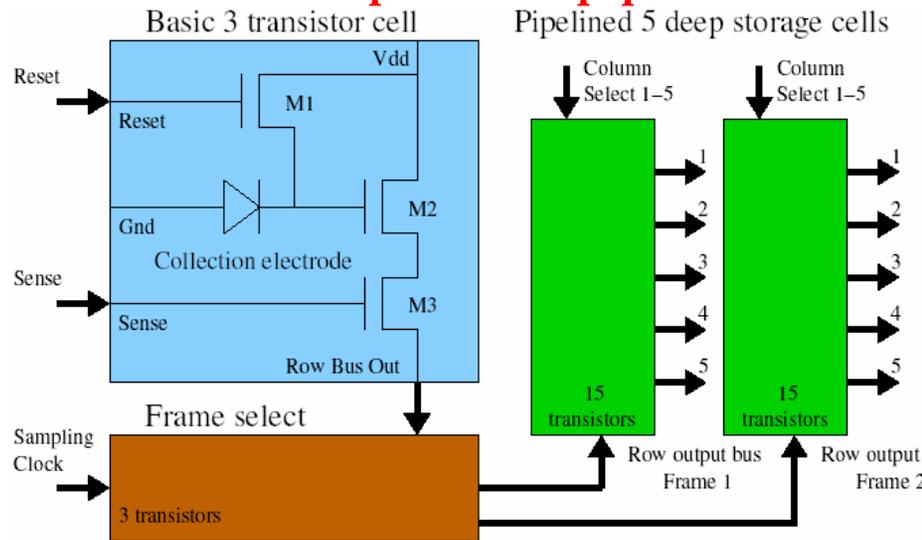
forceful development for KEKB Belle VxD



~120Kpixel sensor (128x928 pix)

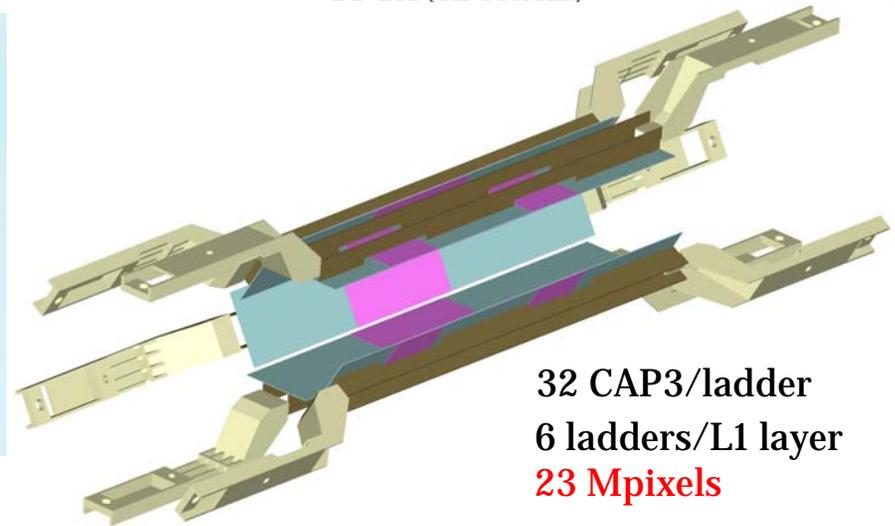
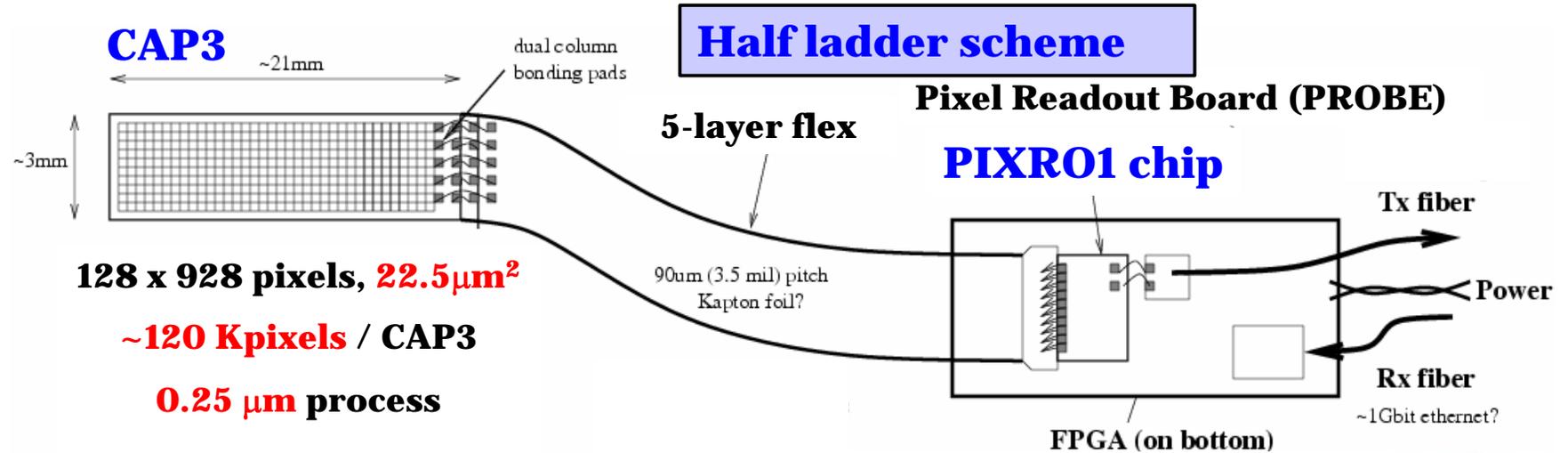
TSMC 0.25 μm Process

5-deep double pipeline



Pixel size 22.5 μm x 22.5 μm

5 metal layers

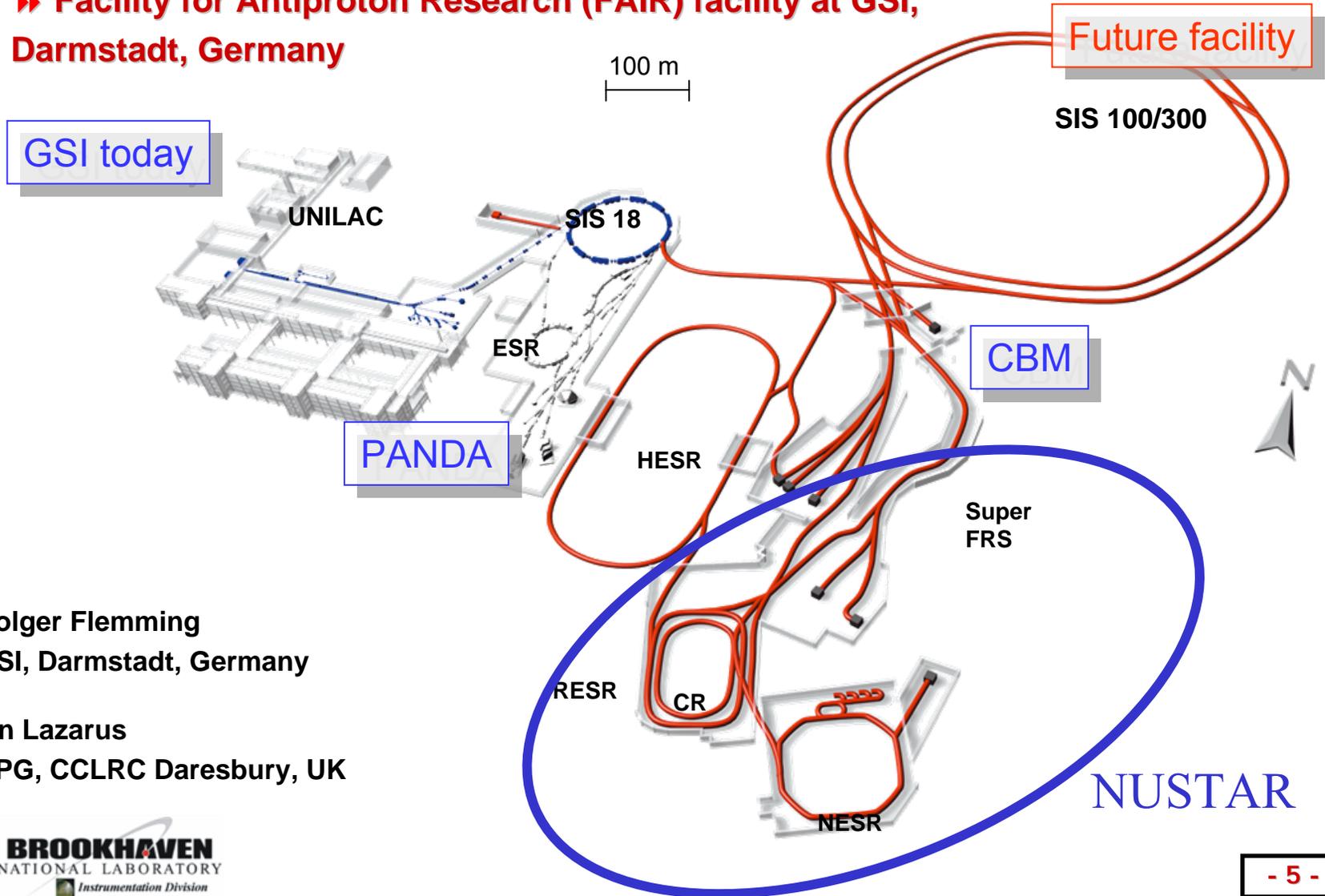


32 CAP3/ladder
 6 ladders/L1 layer
23 Mpixels



NEW FACILITIES

► Facility for Antiproton Research (FAIR) facility at GSI, Darmstadt, Germany



Holger Flemming
GSI, Darmstadt, Germany

Ian Lazarus
NPG, CCLRC Daresbury, UK



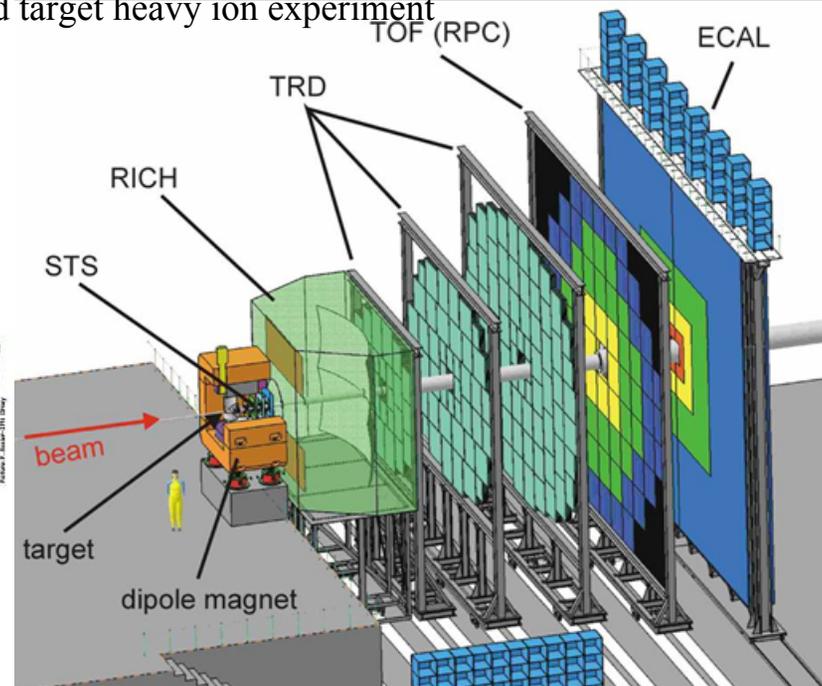
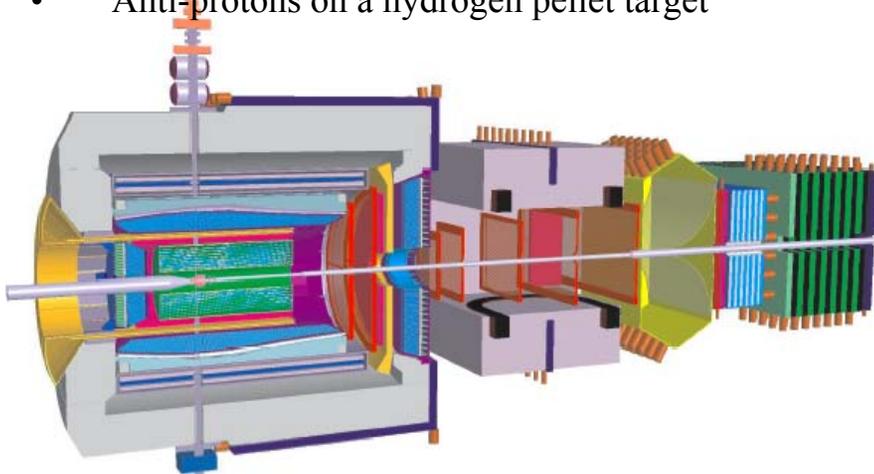
NEW FACILITIES

PANDA

- anti-Proton ANihilation at DArmstadt
- Physics Topics
 - Charmonium spectroscopy
 - Search for exotic hadrons in the charm sector
 - Charm mesons in nuclear matter
 - Open charm physics
 - Hypernuclei
- 4π detector
- Anti-protons on a hydrogen pellet target

CBM

- Condensed Barion Matter
- Physics Topics
 - In-medium modifications of hadrons
 - Strangeness in matter
 - Indications for deconfinement at high ρ_B
 - Critical point
- Fixed target heavy ion experiment





Improve the luminosity by a factor 10 : $10^{34} \rightarrow 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$

► Physics motivation

- Increased physics reach in most typical LHC physics channels
- It is not clear today if these improvements are absolutely crucial for new physics, or rather if they represent (gradually) better measurements and better exploitation of the LHC energy domain
- However, in either case upgrading the LHC seems very attractive and an obvious next step to plan for

► Pragmatic view

- The luminosity will increase as function of time at LHC, we will need to upgrade the detectors to take advantage of this
- Some parts of the detector systems might have performance problems or operational problems, and will therefore require interventions and improvements faster than foreseen today
- An impressive expertise about the construction has been accumulated and it is known today how to improve the detectors

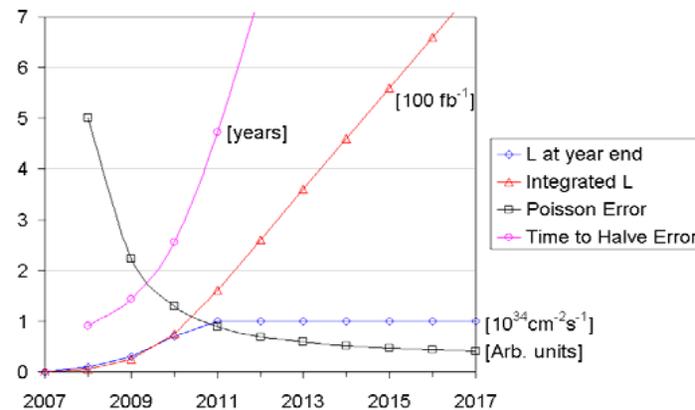
Philippe Farthouat, CERN



LHC AND SLHC

- ▶ The most relevant parameters for the detectors
 - ▶ BCO interval: 25ns, 15ns, 12.5ns, 10ns (or 75ns)
 - ▶ Forward area/beam pipe : Would like to move the closest machine element towards the IP
 - ▶ Timescales : assume 2014 ± 2 years

Driven by this plot, but also by lifetime of IR quads 700 fb^{-1}

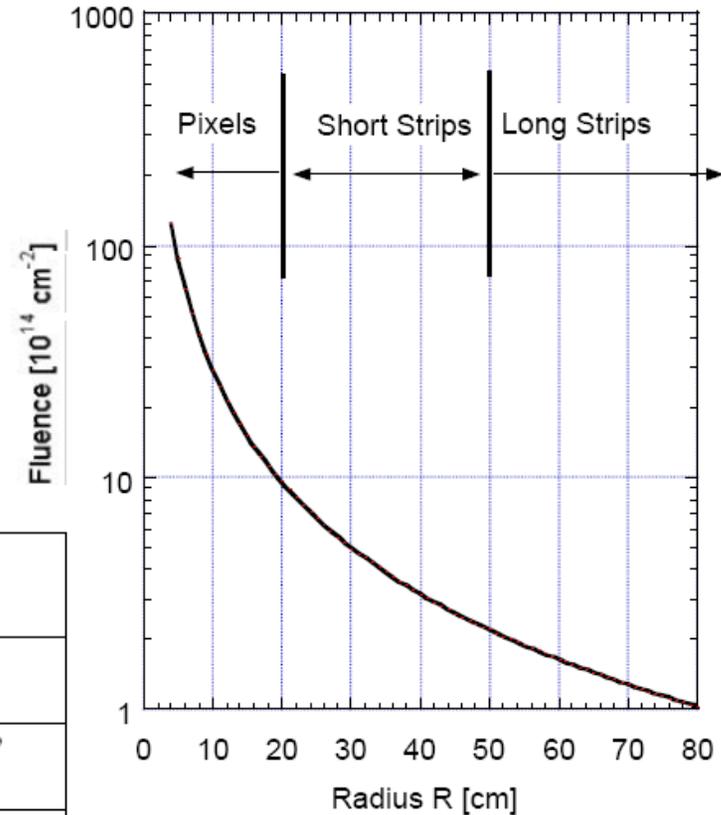


- ▶ Increased radiation levels (and resulting activation) : Need to improve shielding, moderators, access procedures, and safety in general – important constraint for any change considered

inner detector

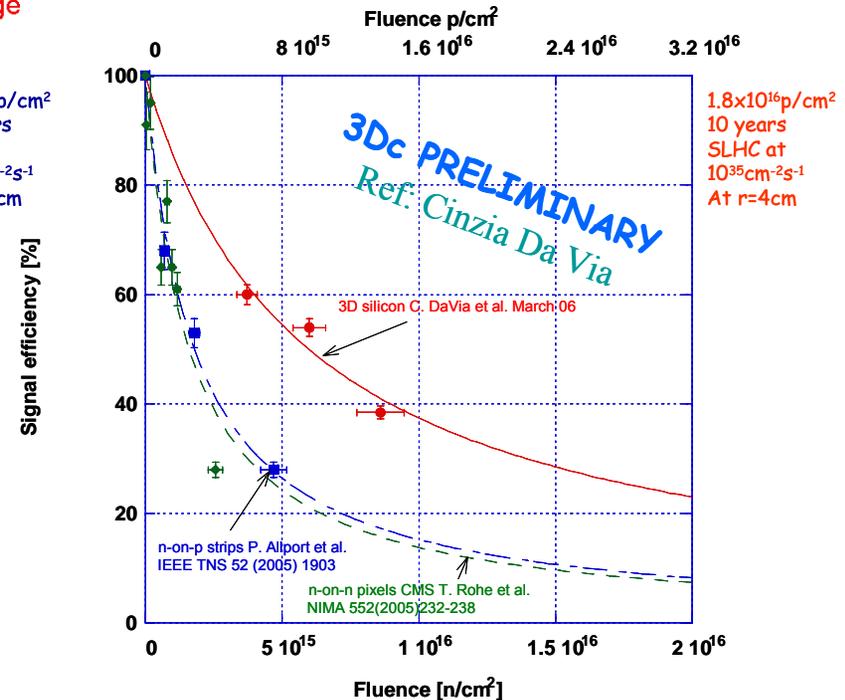
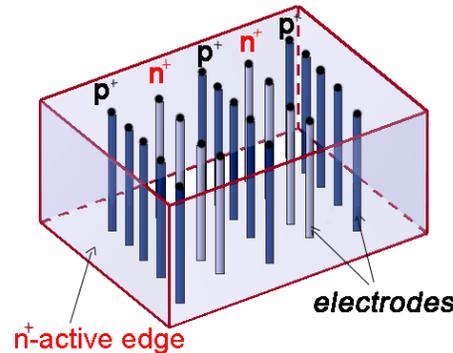
- ▶ Overall concept: **all silicon tracker**
- ▶ Replace
 - ▶ TRT by long silicon strips
 - ▶ SCT by short silicon strips
 - ▶ Pixel tracker by smaller silicon pixels
- ▶ Several ideas being developed now, no final decision made yet

Radius [cm]	Fluence [cm^{-2}]	Specification for Collected Signal (CCE in 300 μm)	Limitation due to	Detector Technology
> 50	10^{14}	20 ke^- (~100%)	Leakage Current	"present" LHC SCT Technology, "long" strips
20 - 50	10^{15}	10 ke^- (~50%)	Depletion Voltage	"present" LHC Pixel Technology ? "short" strips - "long" pixels
< 20	10^{16}	5 ke^- (~20%)	Trapping Time	RD50 - RD39 - RD42 Technology 3-D



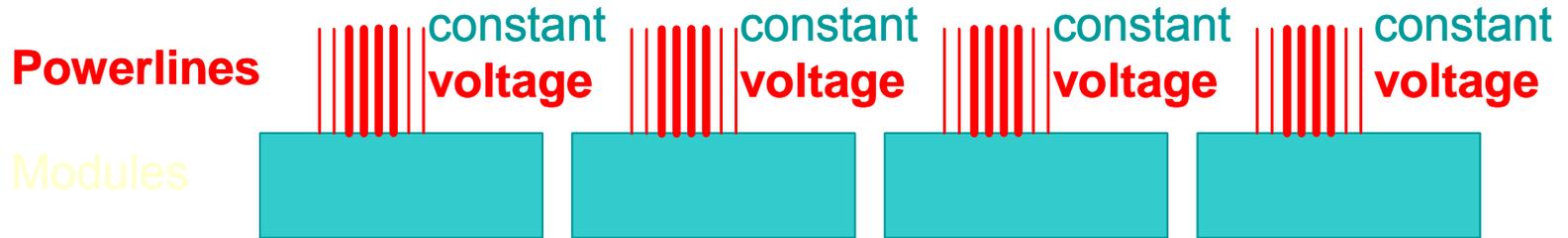
LHC AND SLHC

- ▶ Fast charge collection
- ▶ Lower V_{depl}
- ▶ But higher capacity
- ▶ Radhardness considerably better than standard silicon
- ▶ Until now fabricated on a small scale in house (Stanford)
 - ▶ Yield now 80%
- ▶ Arrangements for commercial production at SINTEF (still in early state)

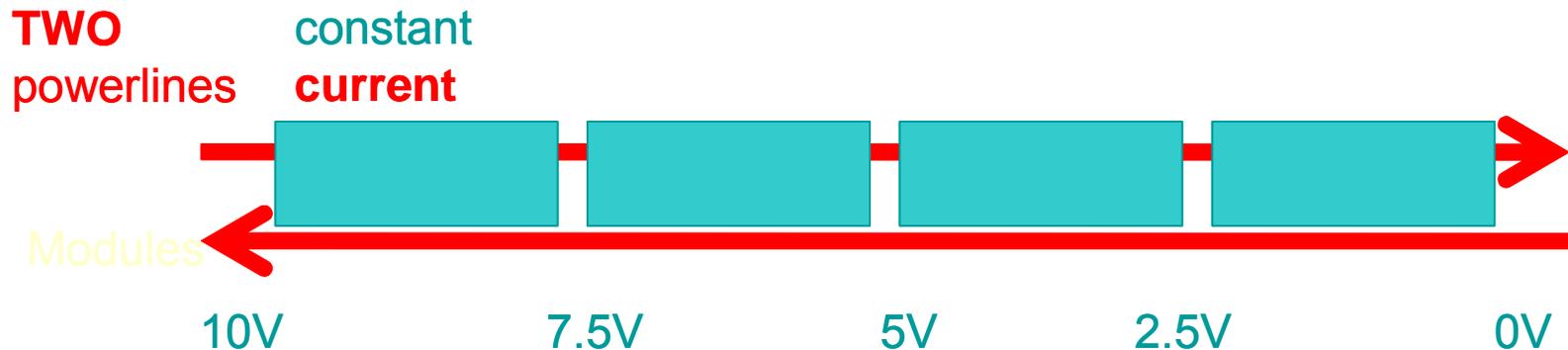


Ref: talk of Parker at Genova tracker upgrade workshop
<http://agenda.cern.ch/fullAgenda.php?id=a053875>

► Currently used **Parallel Powering:**



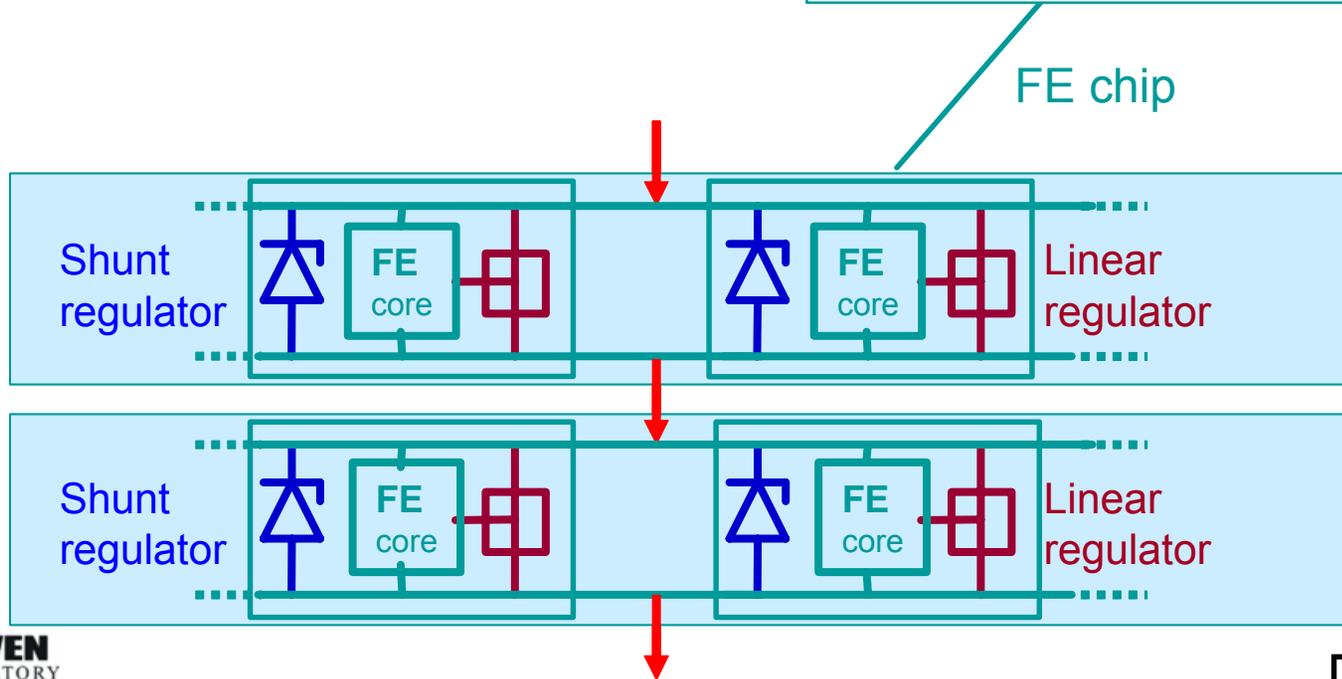
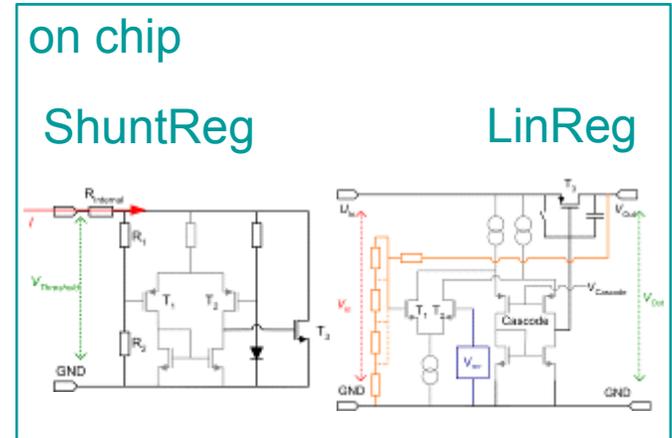
► Idea of **Serial Powering:**



LHC AND SLHC

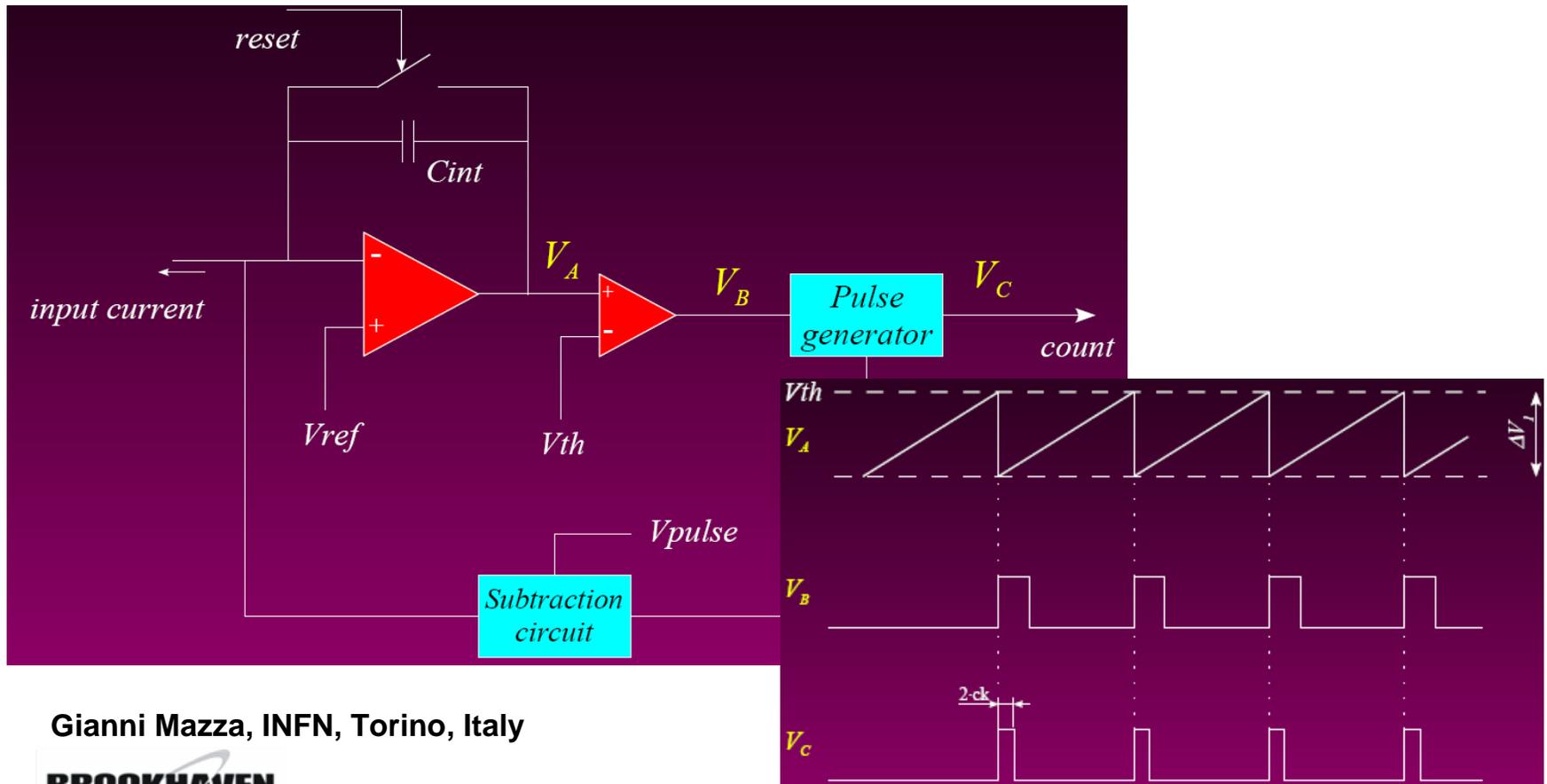
serial powering

- ▶ Basic principle:
 - ▶ Constant current through all modules
 - ▶ Voltages generated **on FE chip** by
 - ▶ Shunt regulators
 - ▶ Linear regulators





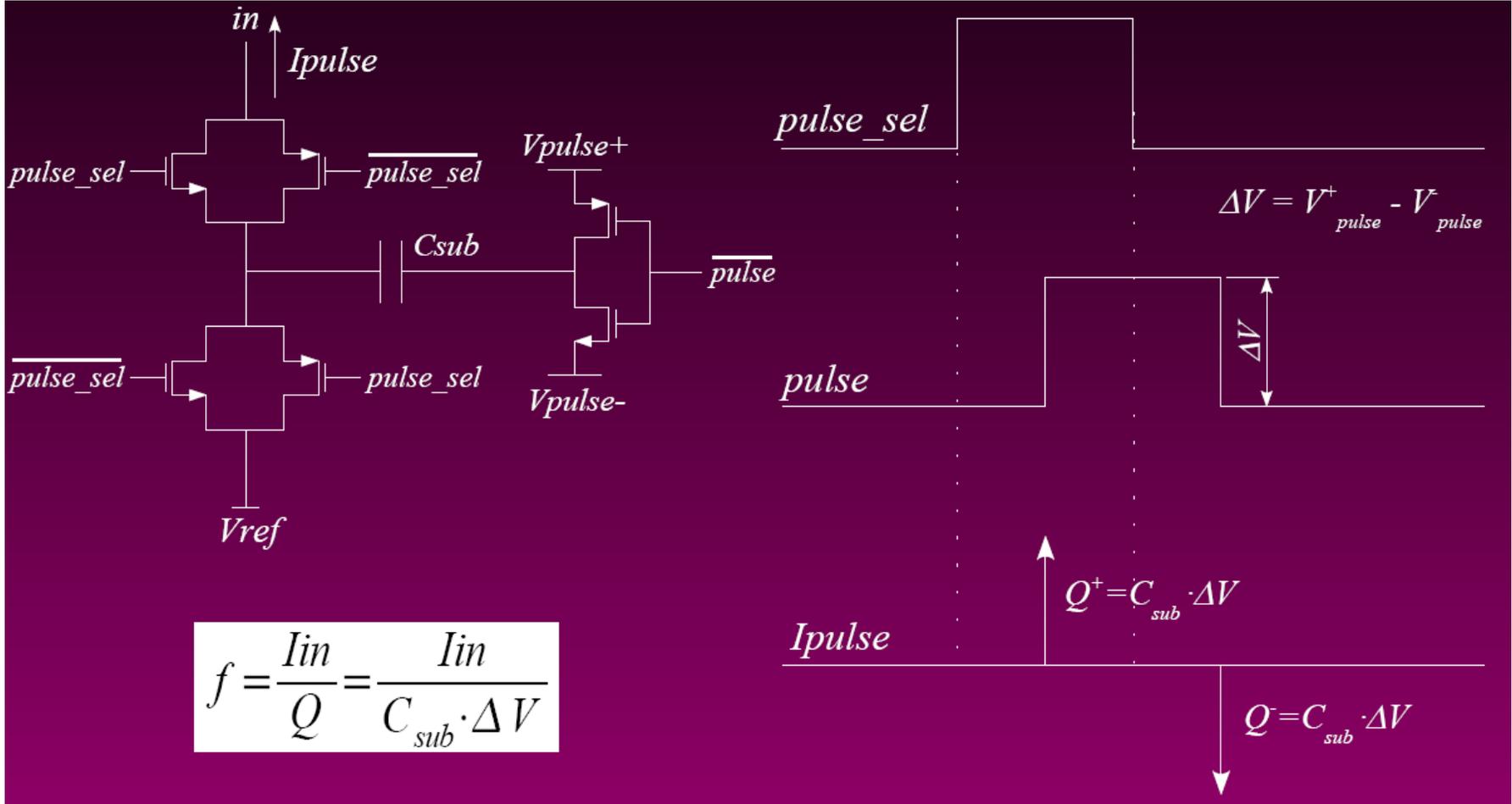
64 channel ASIC for the readout of gas detectors for hadron therapy
Beam Calibration (before treatment) – Beam monitoring (during treatment)
big dynamic range



Gianni Mazza, INFN, Torino, Italy

 MEDICAL APPLICATIONS

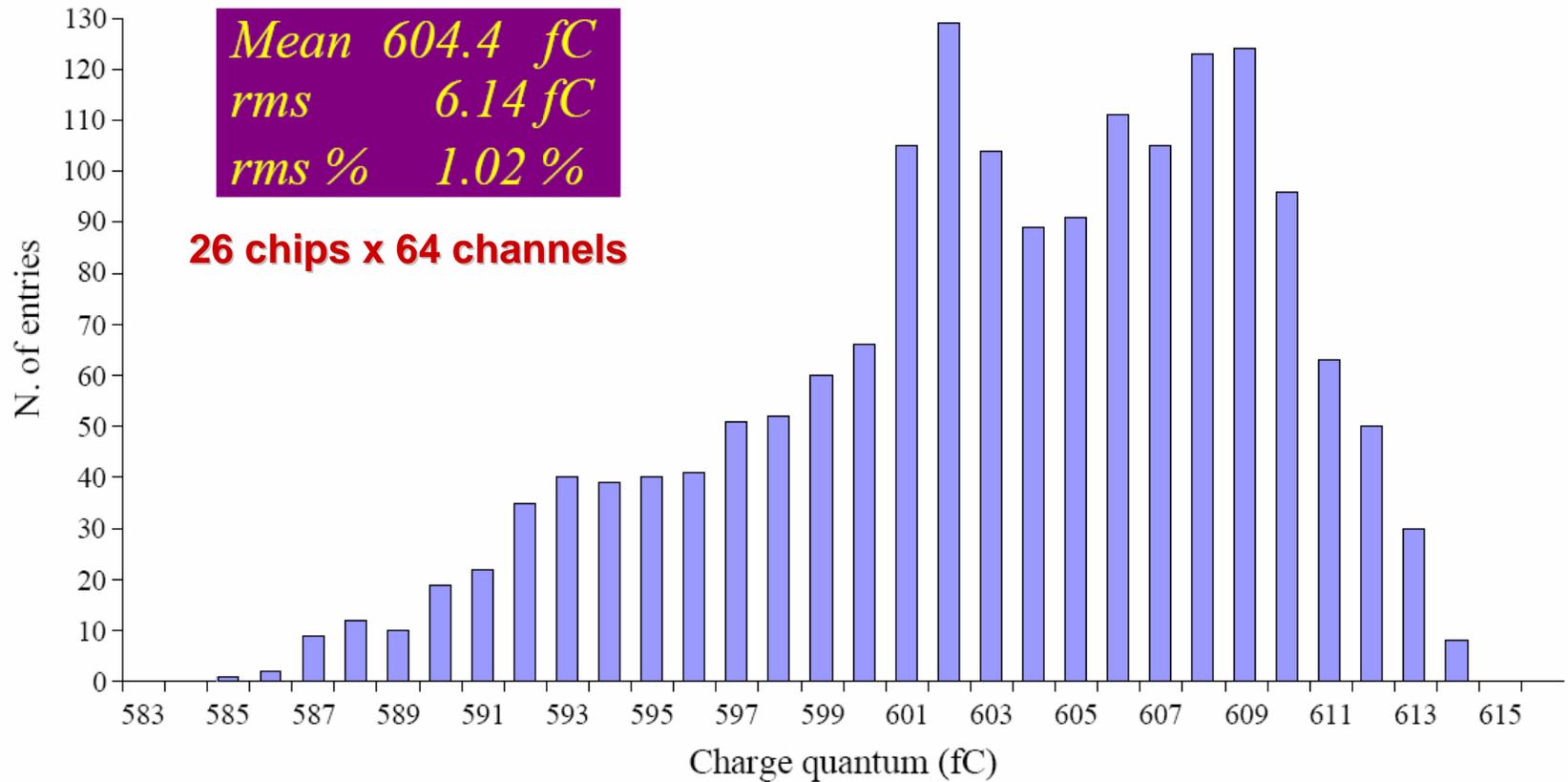
charge subtraction



$$f = \frac{I_{in}}{Q} = \frac{I_{in}}{C_{sub} \cdot \Delta V}$$



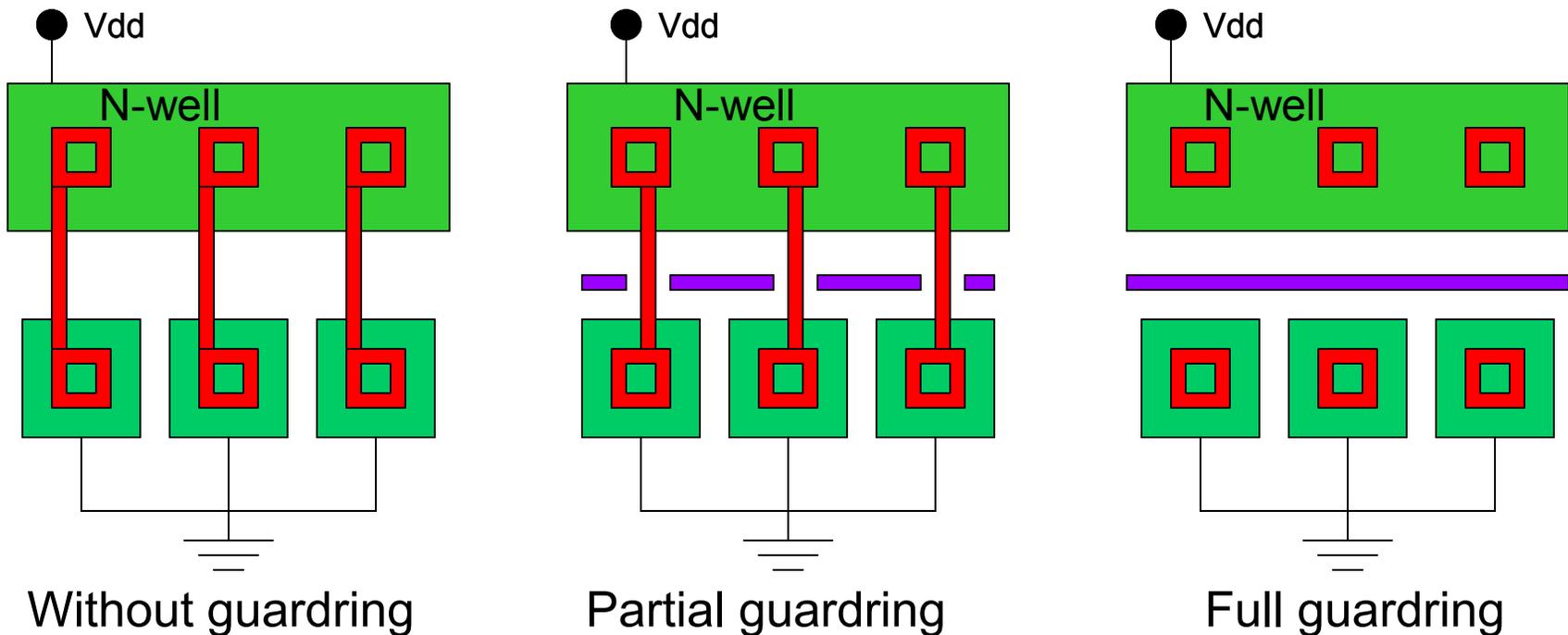
MEDICAL APPLICATIONS



simply and quite efficient

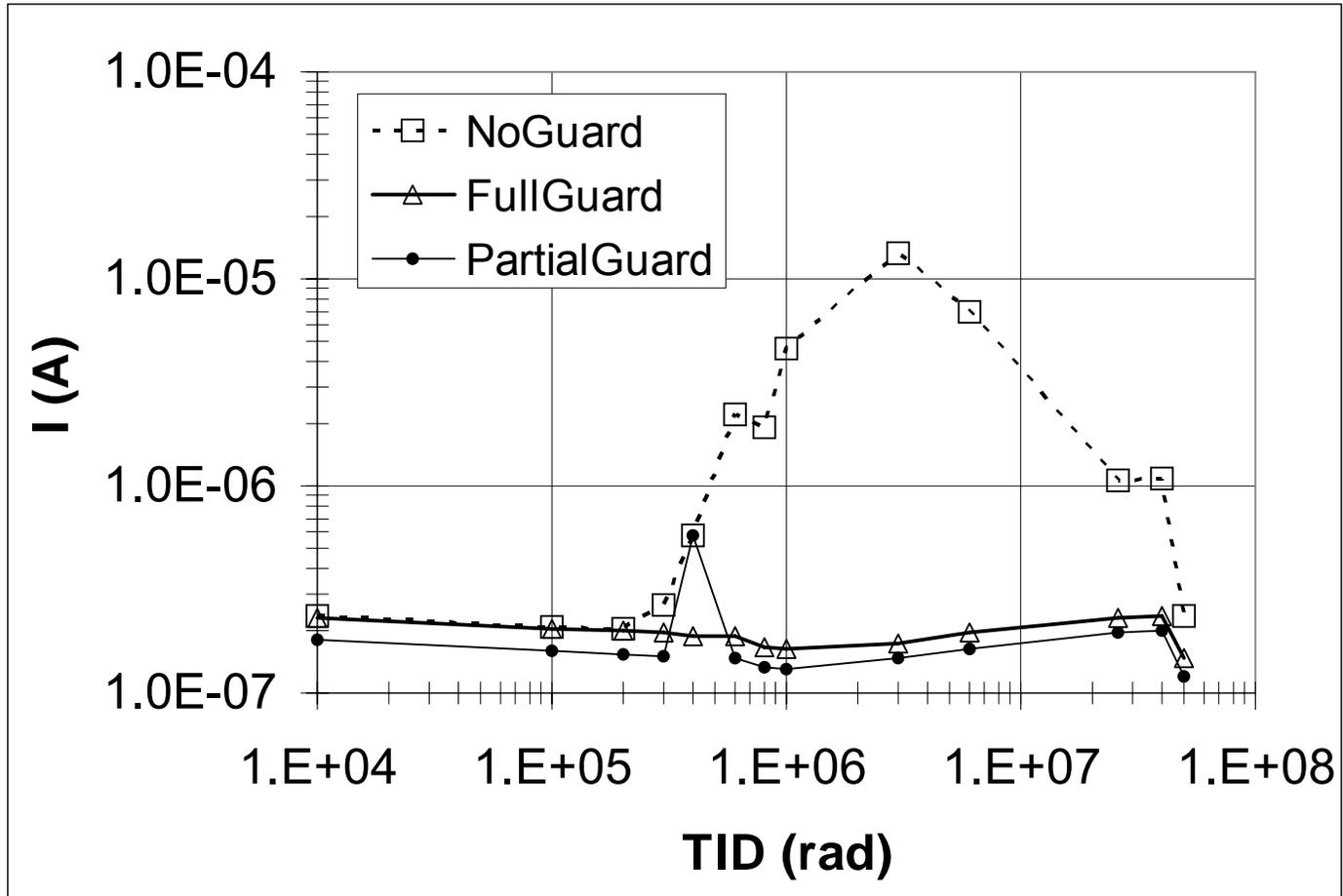


Realistic test structure with series of Inverters + DFF along 350um, and with different separation between n-well (PMOS logic) and NMOS:



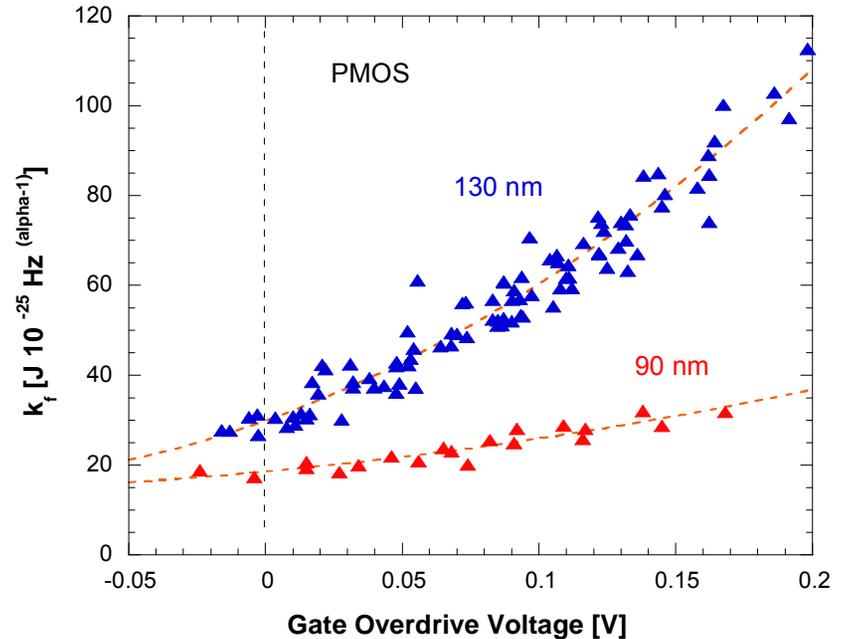
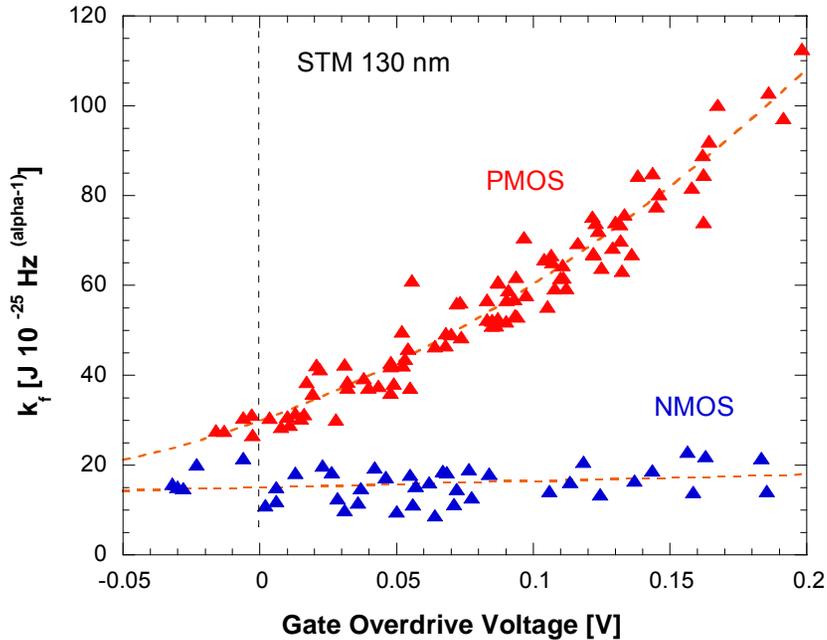


RADIATION EFFECTS





SPECIAL DESIGN AND NEW DETECTORS



In PMOS devices, flicker noise coefficient is clearly bias dependent (dependence is weaker in STM 90 nm technology)

In NMOS transistors k_f is to a large extent independent of the overdrive voltage V_{ov}

Ludovico Ratti, CERN

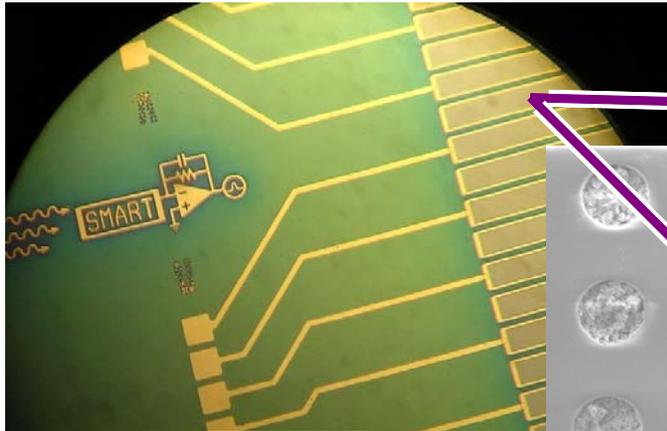
CMOS processes in the 100-nm minimum feature size range for applications to the next generation collider experiments



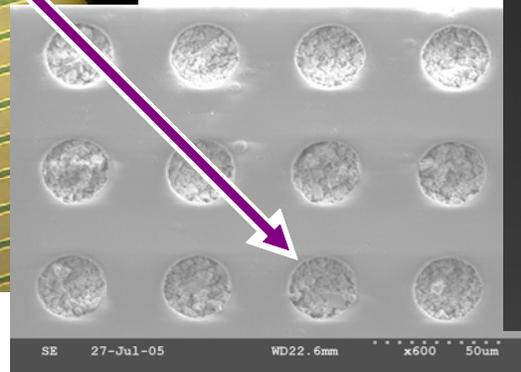
but presentation on neutron detection ...

High Efficiency Neutron Detector Array

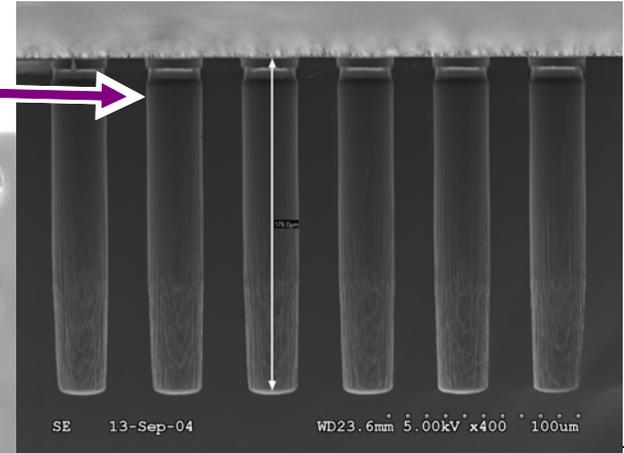
(HENDA)



Linear pixels and bonding pads



30 micron diameter holes with ${}^6\text{LiF}$



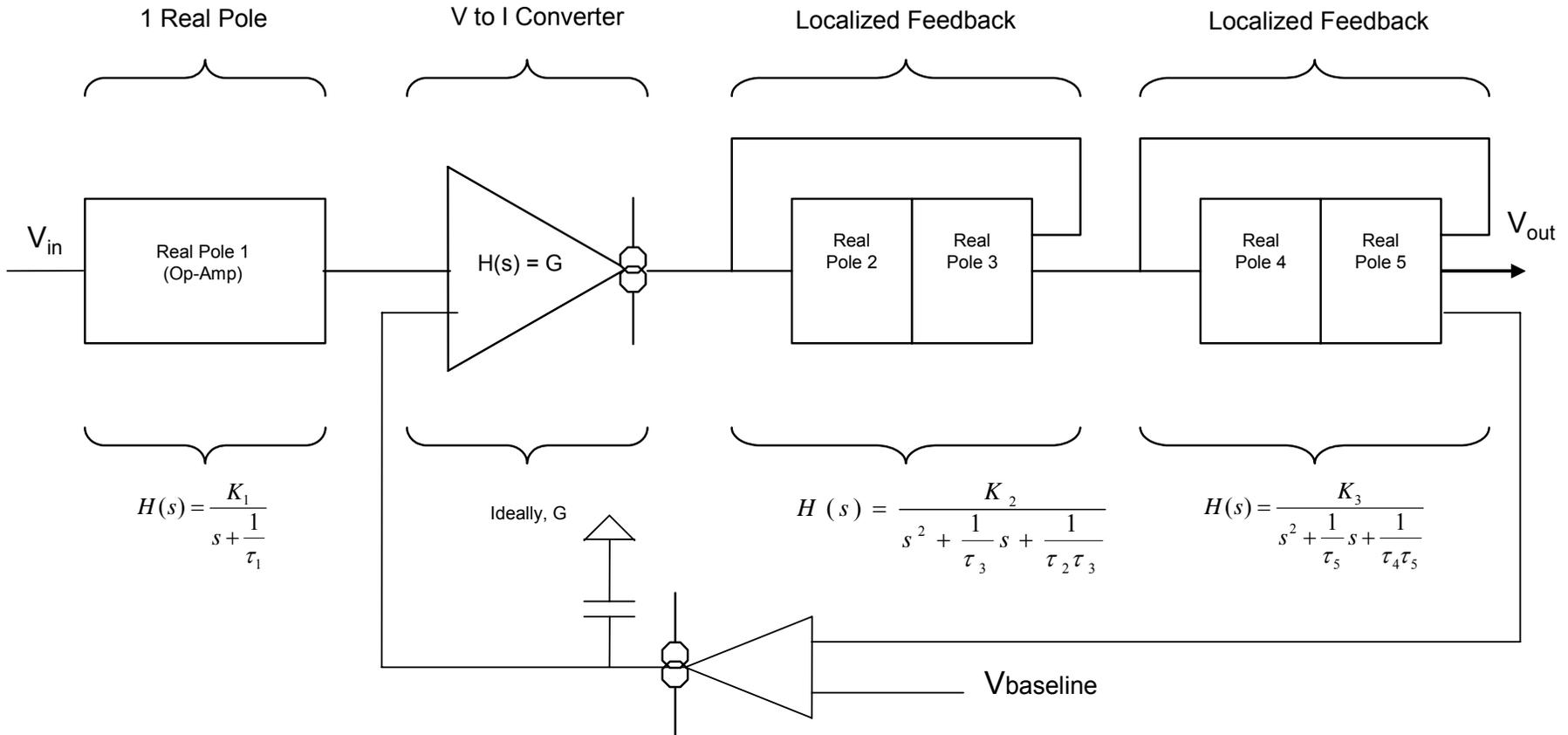
Etched holes >170 microns deep

- Semiconductor linear thermal neutron detection imaging array
- Reaction - $n + {}^6\text{Li} \rightarrow {}^4\text{He} + {}^3\text{H} + 4.79 \text{ MeV}$
- Pixel dimensions are 80 microns wide, and 4 cm long, with a 100 micron pitch
- Contains 1000 pixels, each with expected intrinsic thermal neutron detection efficiency of >20%
- Millions of holes filled with neutron reactive material increase the detector efficiency

Steven Bunch, University of Tennessee, USA



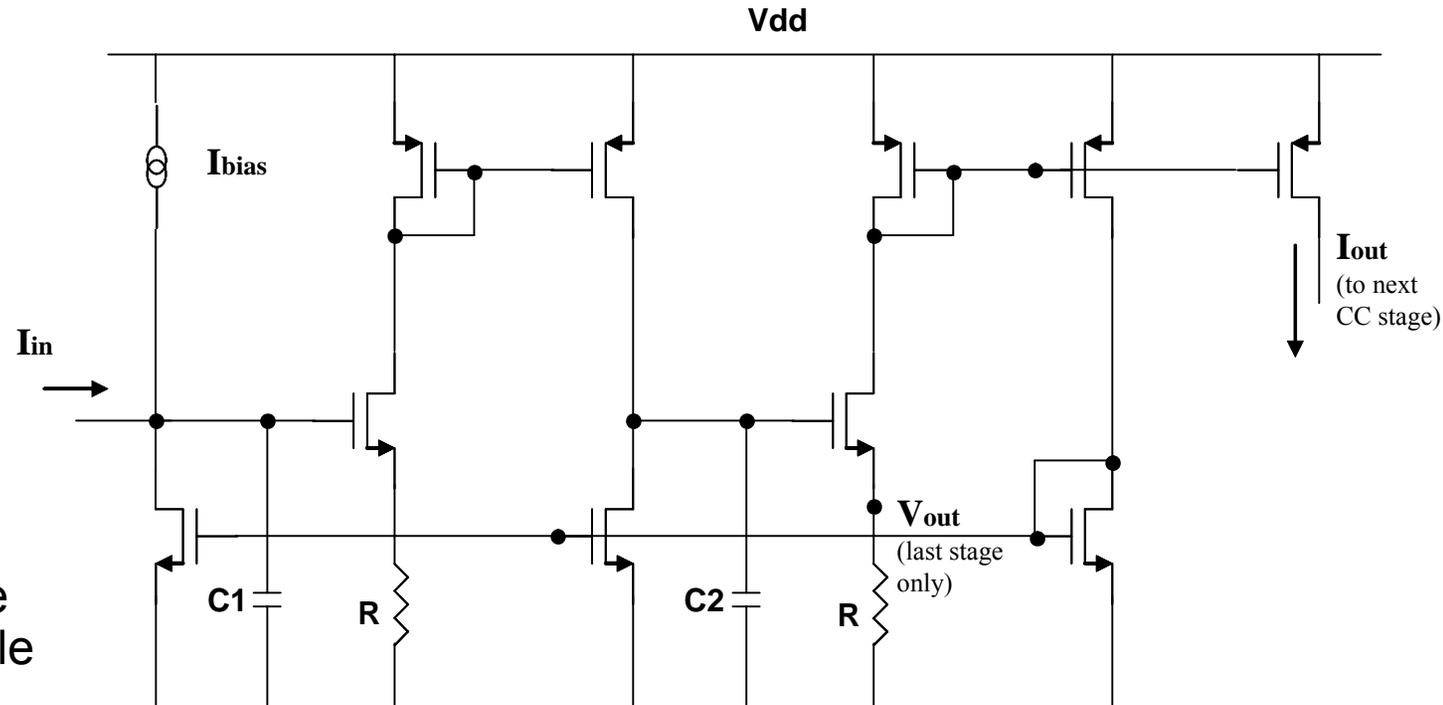
NEUTRINO EXPERIMENTS



- Semi-Gaussian pulse response with 1 real, 4 complex poles
- 1 μ -sec pulse-pair resolution with gated baseline restoration (SNS synchronous)
- Current-mode quasi-linear operation



current mode solution allowing R values easier achievable in ICs



- Modified R-lens magnification
- Intrinsically low-noise
- R magnification allows small physical R to give low-frequency pole

- At higher signal levels, circuit is dynamic, but magnified small physical R dominates $1/g_m$ for improved linearity over Gm-C filters

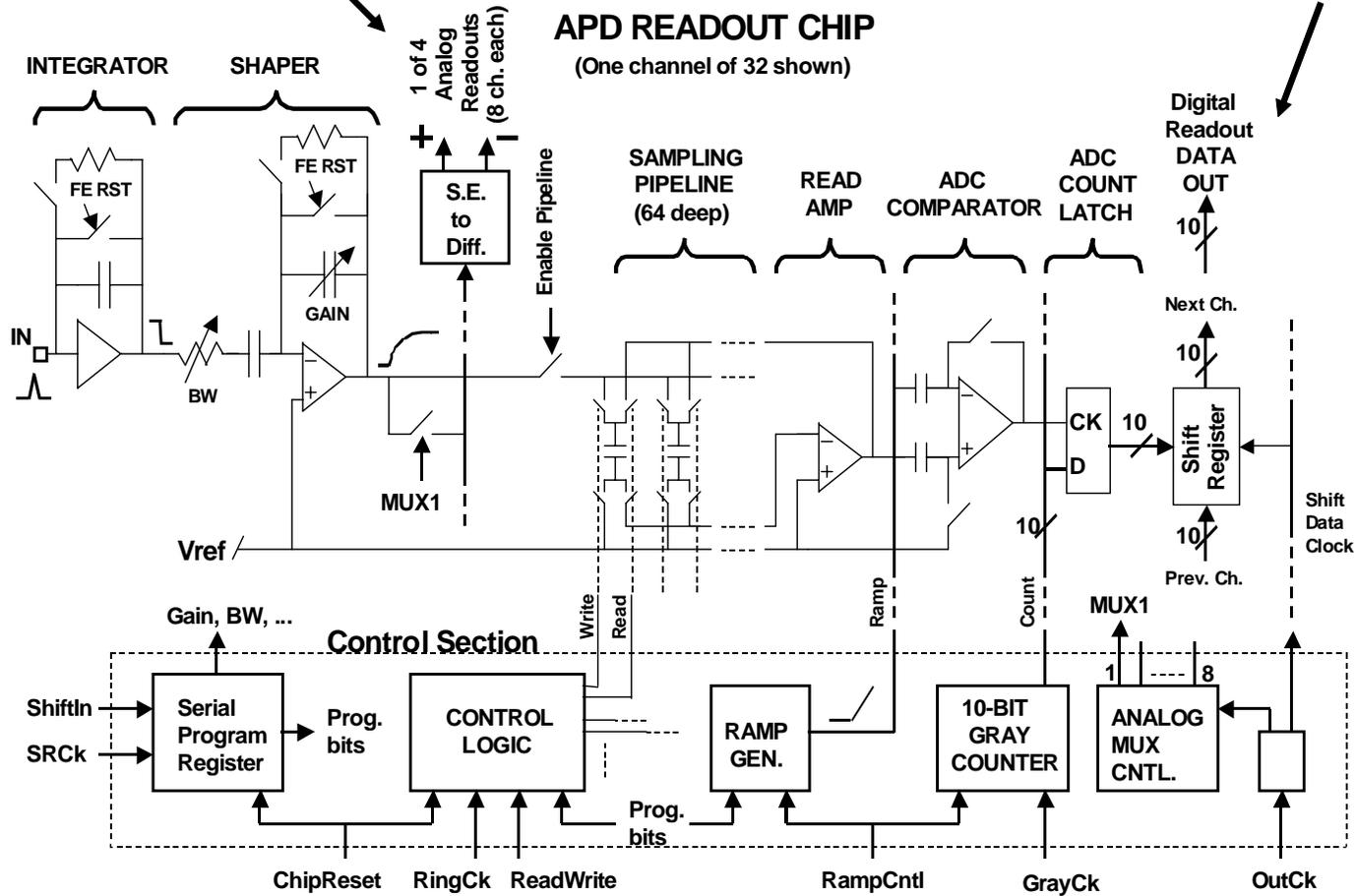
G. Bertuccio, *et al.*, "R-lens filter: An $(RC)^n$ current-mode lowpass filter," *Electronics Letters*, vol. 35, no. 15, 22nd July 1999.



NEUTRINO EXPERIMENTS

Mux version
analog output

Pipeline version
digital output



Tom Zimmerman, Fermilab, USA

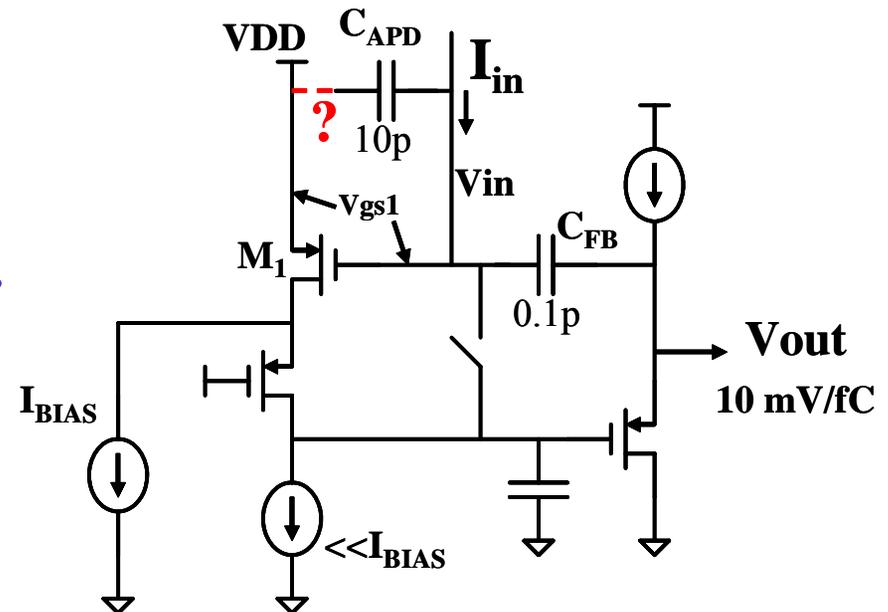
The NOvA APD readout chip



NEUTRINO EXPERIMENTS

- 1 LSB \sim 100e: use 10 mV/fC ($C_{FB} = 0.1$ pF), followed by shaper gain (x2-x10)
- 500 ns sample time: M_1 is PMOS to avoid significant 1/f noise contribution.
- M_1 (PMOS) source is referred to VDD, not ground.
- Where to refer APD capacitance for best PSRR?
- If I_{BIAS} is fixed, then V_{gs1} is constant, so $\Delta V_{in} = \Delta V_{DD}$. If C_{APD} grounded:
 $\Delta V_{out}/\Delta V_{DD} = \Delta V_{out}/\Delta V_{in} = C_{APD}/C_{FB} = \mathbf{100}$ (disaster!!)
- If C_{APD} is referred to VDD:
 - Tight input loop (minimizes pickup)
 - $\Delta V_{out}/\Delta V_{DD} = \mathbf{1}$ (better!!)

Integrator





NEUTRINO EXPERIMENTS

- But what about C_{STRAY} to ground (bond pad, bondwire, etc.)? Ruins PSRR.
- Use M_2 with $V_{gs} = VDD$ to generate I_{BIAS} .

Two advantages:

- 1. For a given I_{BIAS} , **max. V_{gs_2} yields min. g_{m_2} , lowest M_2 noise.**
- 2. I_{BIAS} changes with VDD . Now $\Delta V_{in} = (\Delta VDD)[1 - (g_{m_2}/g_{m_1})]$.

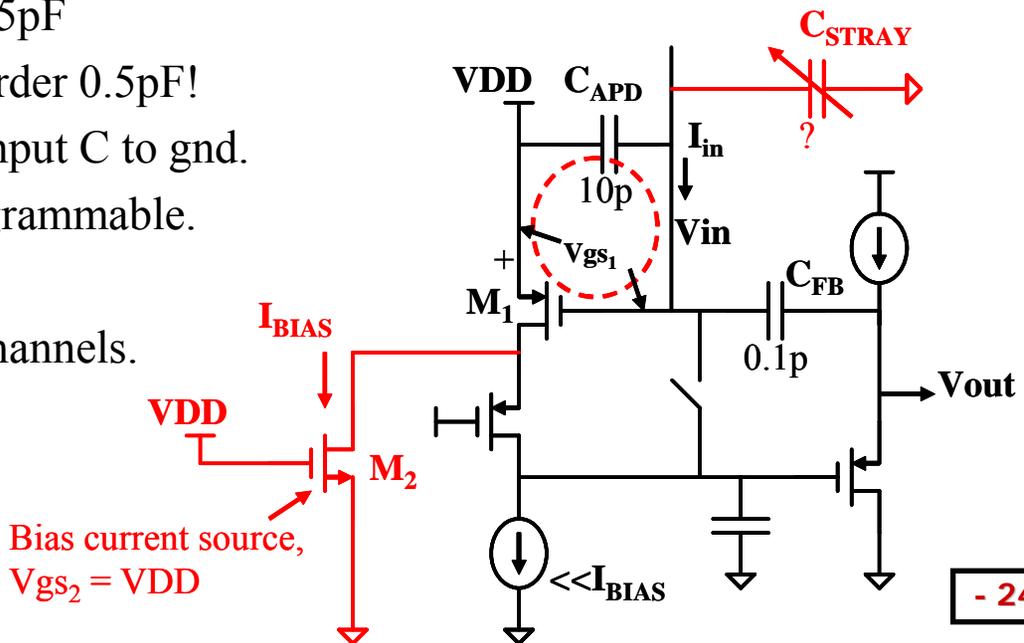
If $(C_{STRAY}/C_{APD}) = (g_{m_2}/g_{m_1})$, then $\Delta V_{out} = 0!!$ (to 1st order).

- Typically $(g_{m_2}/g_{m_1}) \sim 0.05$:

M_2 noise contribution $\sim 2\%$

Optimum $C_{STRAY} \sim 0.5\text{pF}$

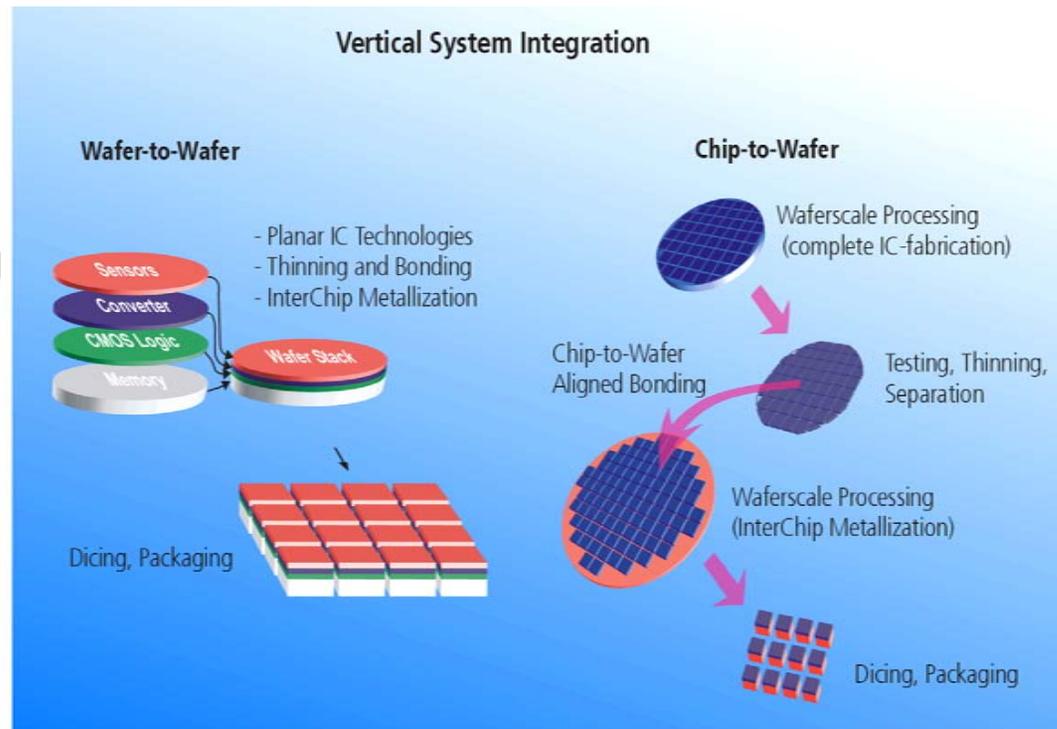
- Unavoidable C_{STRAY} is of order 0.5pF !
- Add small programmable input C to gnd.
- Make I_{BIAS} (M_2 width) programmable.
- Tweak for best PSRR!
- Assumes same C 's on all channels.



- » (FhG IZM-M – Aramin Klumpp) 3D System Integration
- » (Fermilab - Ray Yarema) 3D Integrated Circuits for HEP

Key applications and potential of 3D

- Mobile Systems
(minimum volume, low power, security)
- Systems for high parallel signal processing
(e.g. image sensor)
- Increased Integration density
- More Functionality
- Mixed Technologies: 3D SoC

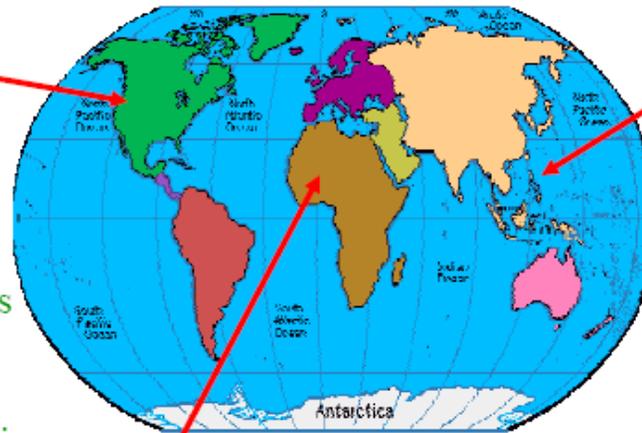




Who is Working on 3D ICs?

USA:

Albany Nanocenter
 U. Of Kansas,
 U of Arkansas
 Lincoln Labs, AT&T
 MIT, RPI, RTI, TI
 IBM, Intel, Irvine Sensors
 Micron, Sandia Labs
 Tessera, Tezzaron,
 Vertical Circuits, Ziptronix



Asia:

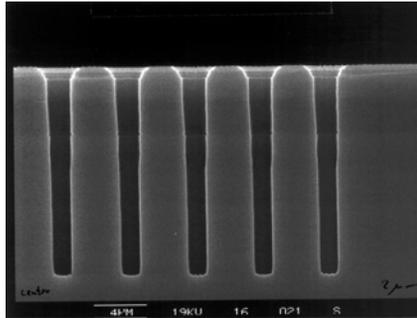
ASET, NEC, University of Tokyo,
 Tohoku University, CREST,
 Fujitsu, ZyCube, Sanyo,
 Toshiba, Denso, Mitsubishi, Sharp,
 Hitachi, Matsushita, Samsung

Europe: Fraunhofer IZM, IMEC Delft,
 Infineon, Phillips, Thales, Alcatel Espace,
 NMRC, CEA-LETI, EPFL, TU Berlin

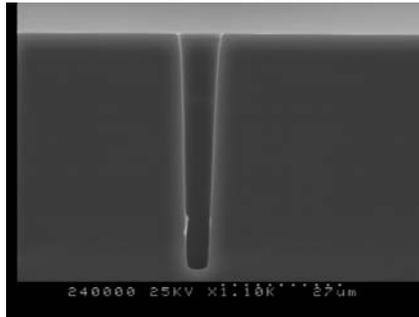


3D ELECTRONICS

1.0 2.0 3.0 5.0 10 100 Via-Diameter [μm]



16 μm ,
8:1



40 μm ,
4:1

Etch Capability
IZM-M

10 16 20 40 60 70 Via-Depth [μm]
10:1 8:1 7:1 4:1 6:1 Aspect Ratio

1.0 μm 3.5 μm 5 μm 10 μm 100 μm Via-Diameter

CVD of
- copper
- tungsten
- TiN

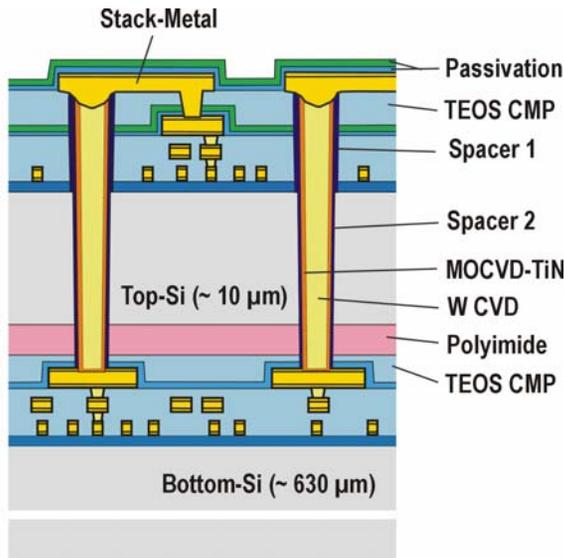
Electroplating of
- copper
PVD of Seedlayer
- Ti:W / Cu

Process for filling

10 μm 70 μm 100 μm Via-Depth
10:1 3:1 2:1 .. 7:1 1:1 Aspect Ratio

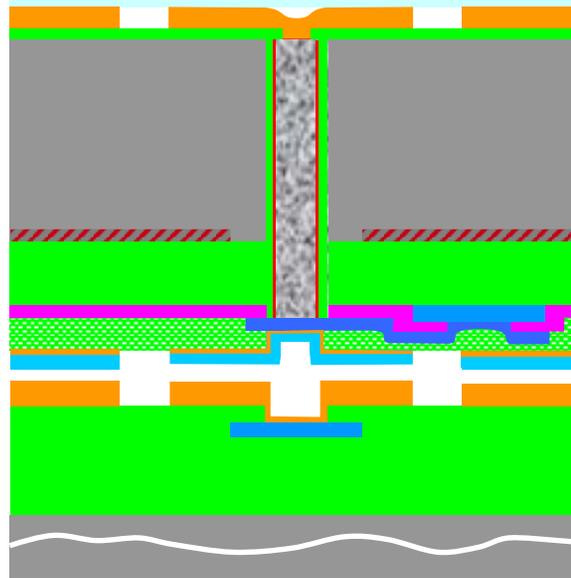
Vertical System Integration – Three relevant Concepts (IZM-M)

InterChip Via (ICV)



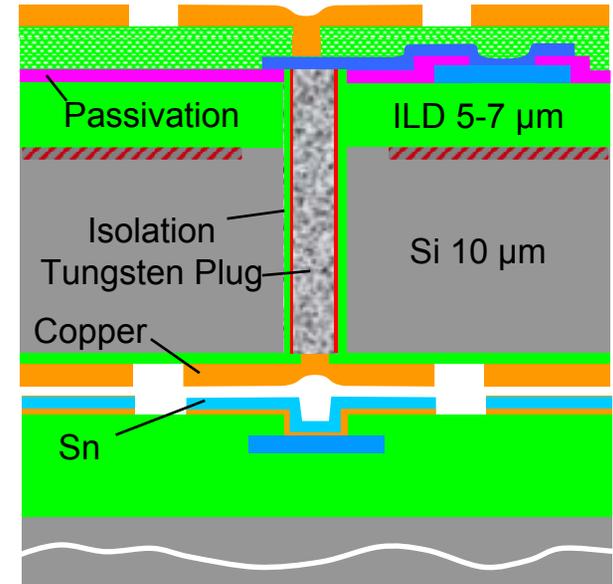
W-Plug / Polyimide

Face to Face modular (F2F-M)



W-Plug / Cu / Sn

ICV / SLID



W-Plug / Cu / Sn

Low resistance per Via:

1 Ohm, Pin only ($2.5 \times 2.5 \mu\text{m}^2$, 10 μm depth)

2.5 Ohm Via with SLID-Contacts

Electrical measurements

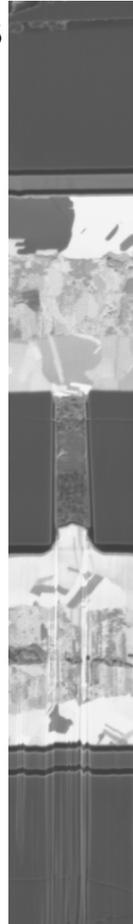
Measured values (from 240 element chain statistics):

Contact hole + soldering layers. ~0.43 Ohms

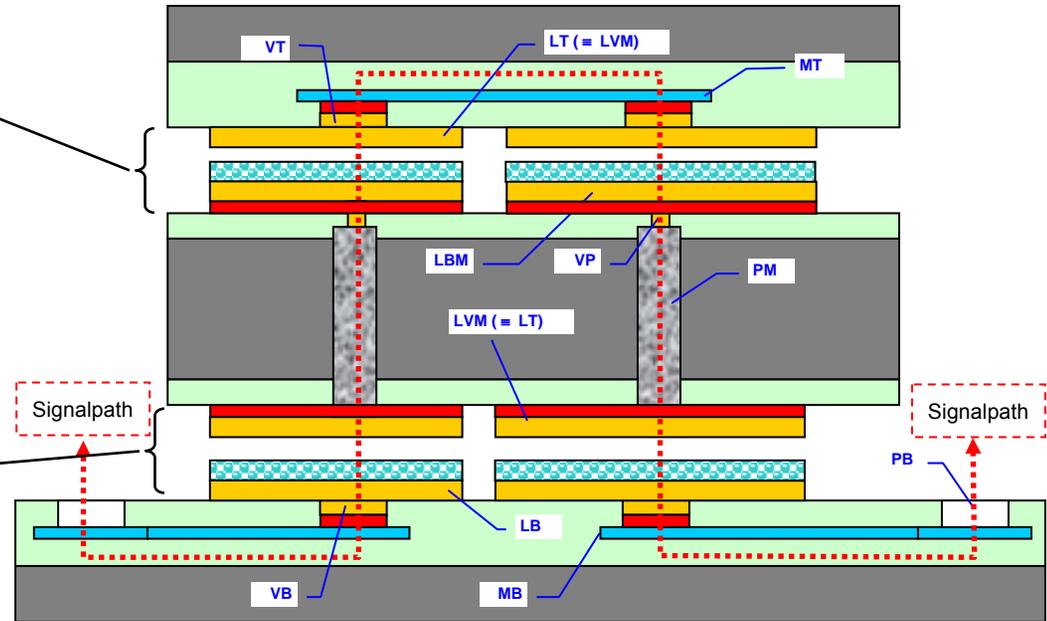
W-plug: ~ 1 Ohm

Contact hole + soldering layers. ~0.43 Ohms

Sum Value: 2.5 Ohm



Daisy Chains with up to 240 elements



- TiW:N
- Tin
- Copper

Contact under Pressure and Heat

~ 5 bar, 260 – 300 °C (Sn-melt)

Eutectic Alloy;

$T_{melt} > 600\text{ °C}$

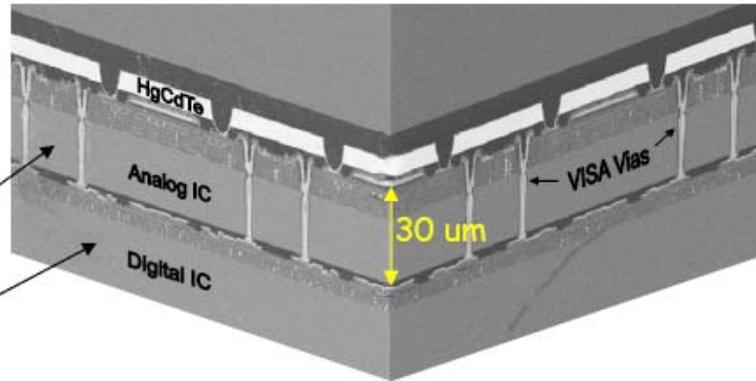
Chance: Increase of Performance

but: **Costs per Chip (or Interconnect) as Main Criteria**

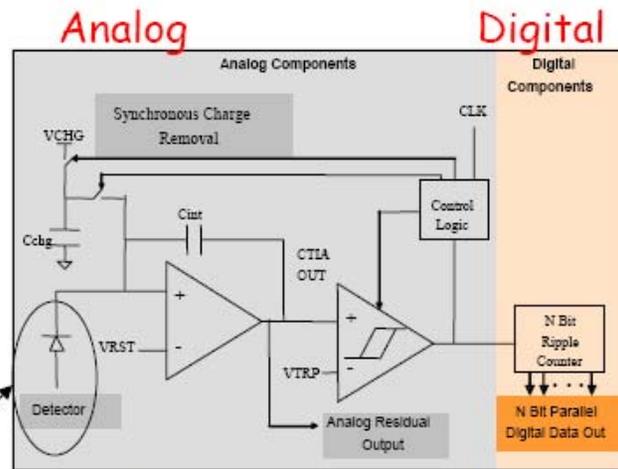
3D ELECTRONICS

3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
 - HgCdTe (sensor)
 - 0.25 μm CMOS (analog)
 - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- **High diode fill factor**



Array cross section



3 Tier circuit diagram

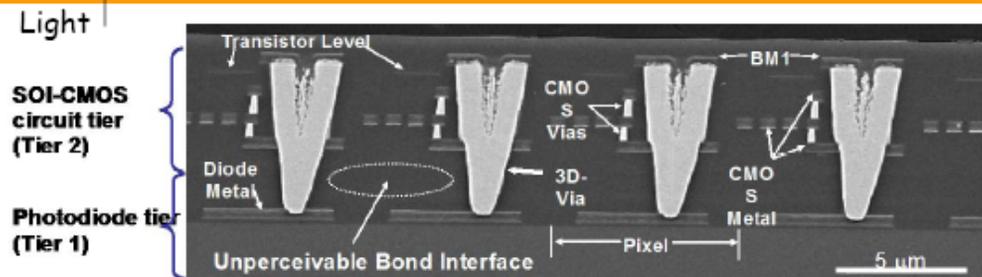
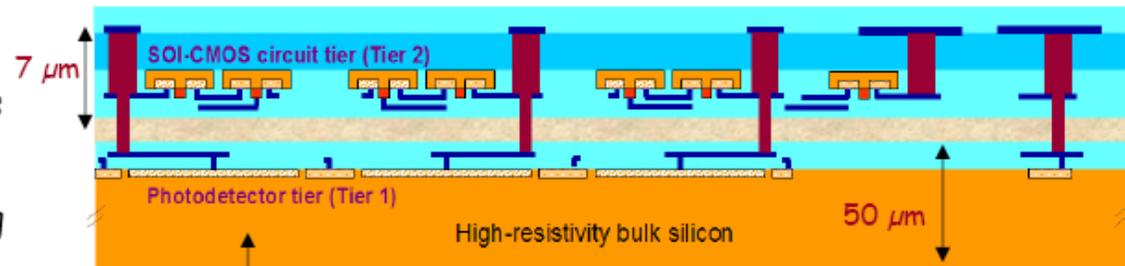


Infrared image

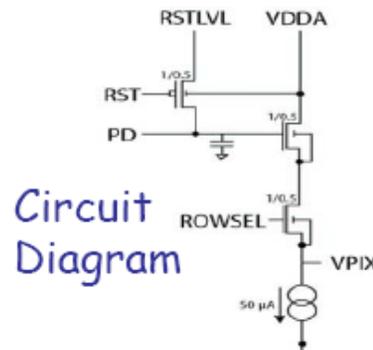

3D ELECTRONICS

3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- **2 tiers**
- Wafer to wafer stacking (150 mm to 150 mm)
- **100% diode fill factor**
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 - 0.35 μm SOI CMOS, **7 μm thick**
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- **1 million 3D vias**
- Pixel operability >99.999%
- 4 side abutable array



Drawing and SEM Cross section



Circuit Diagram

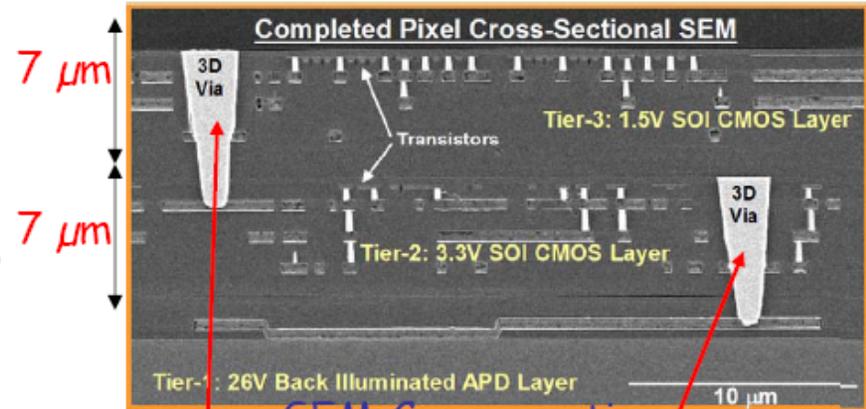


Image

3D ELECTRONICS

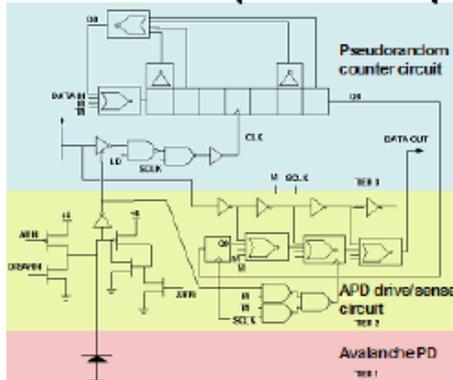
3D Laser Radar imager

- 64 x 64 array, 30 μm pixels
- 3 tiers
 - 0.18 μm SOI
 - 0.35 μm SOI
 - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel

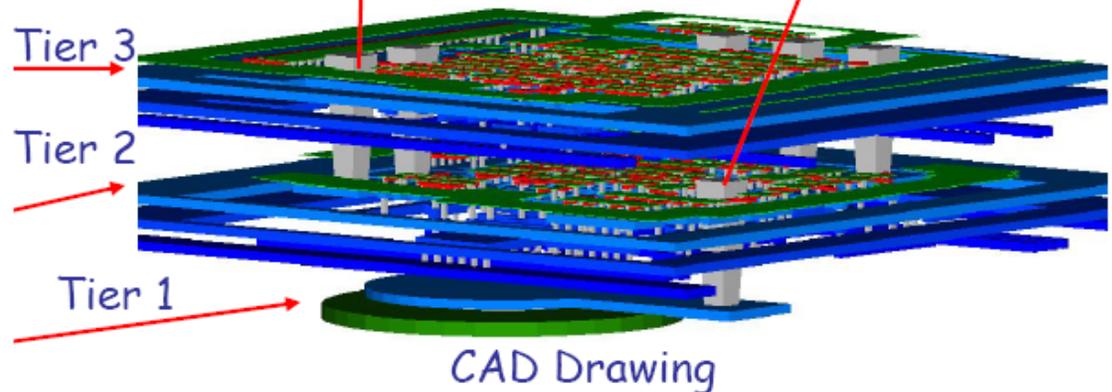


SEM Cross section

VISA APD Pixel Circuit (~250 transistors/pixel)



Schematic

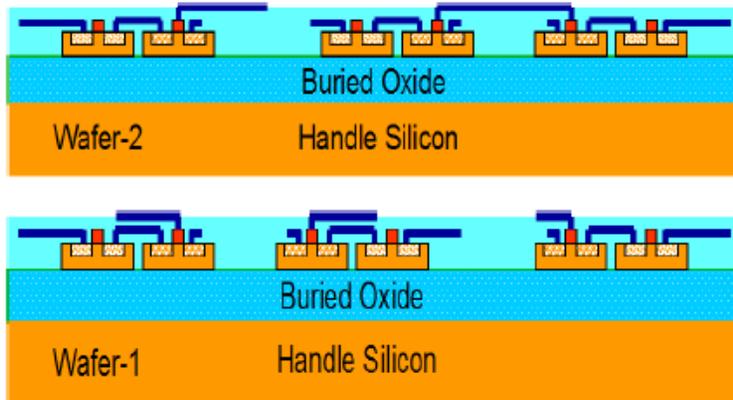


3D ELECTRONICS

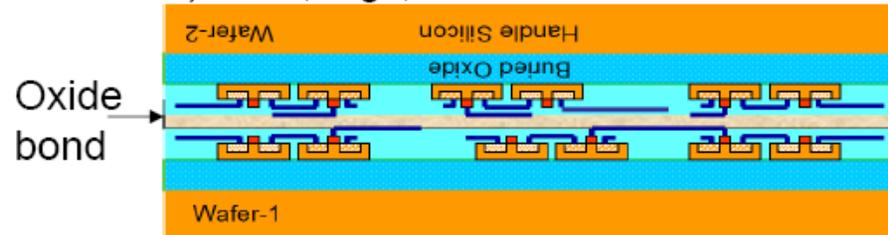
3D SOI

- 3 tier chip (tier 1 may be CMOS)
 - 0.18 um (all layers)
 - SOI simplifies via formation
- Single vendor processing

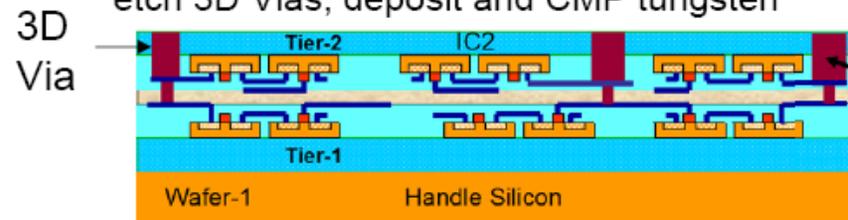
1) Fabricate individual tiers



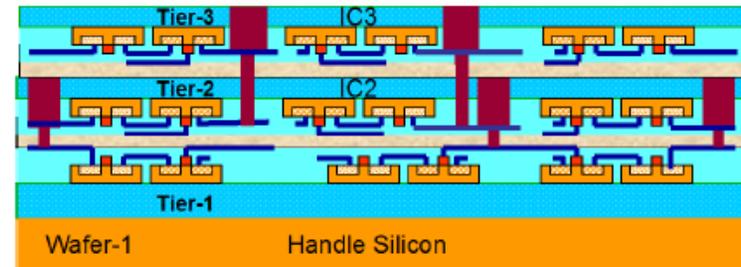
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



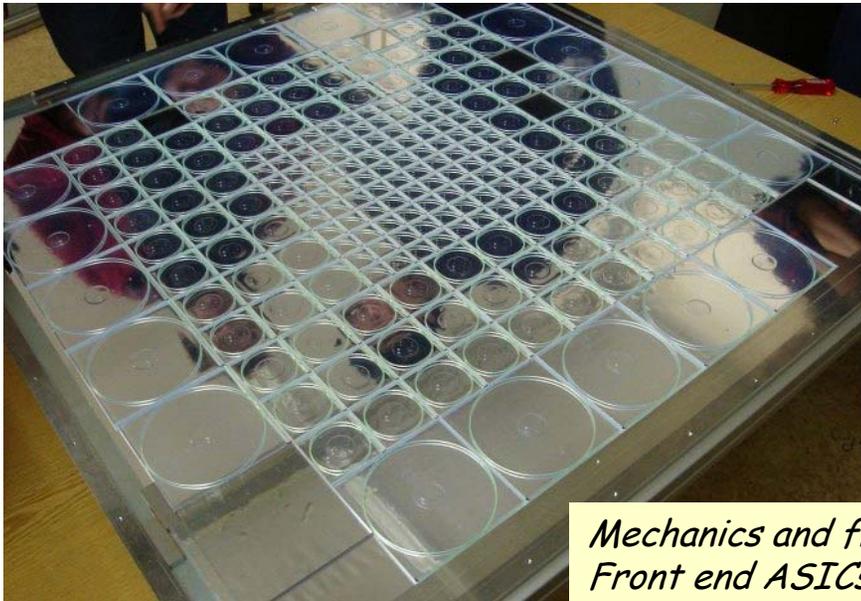
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



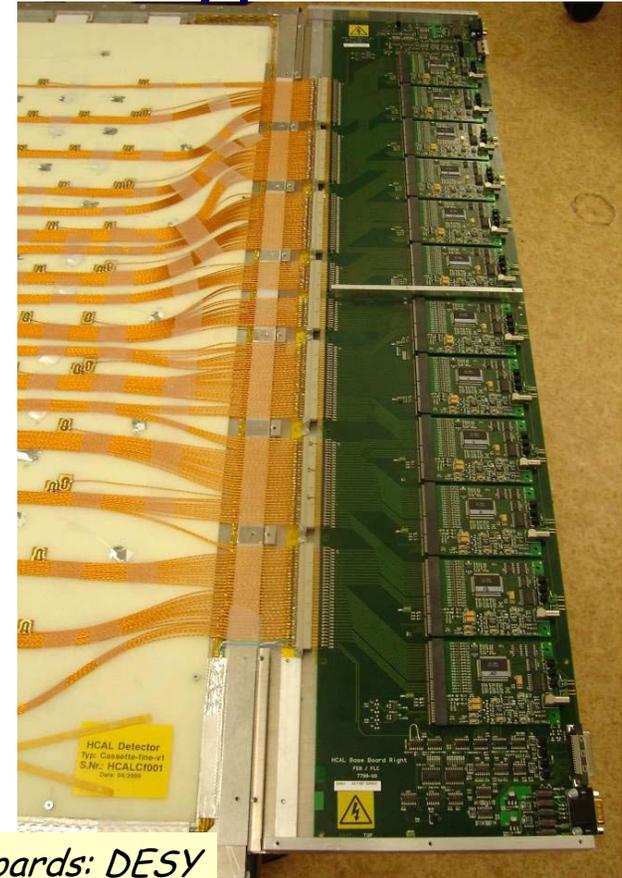


AHCAL testbeam prototype

- 1 cubic metre,
- 38 layers, 2cm steel plates
- 8000 tiles with SiPMs
- Electronics based on ECAL design



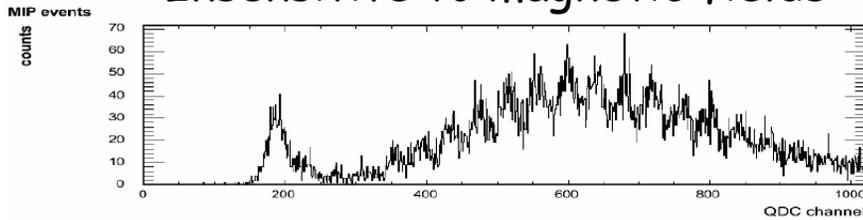
*Mechanics and front end boards: DESY
Front end ASICs: LAL*



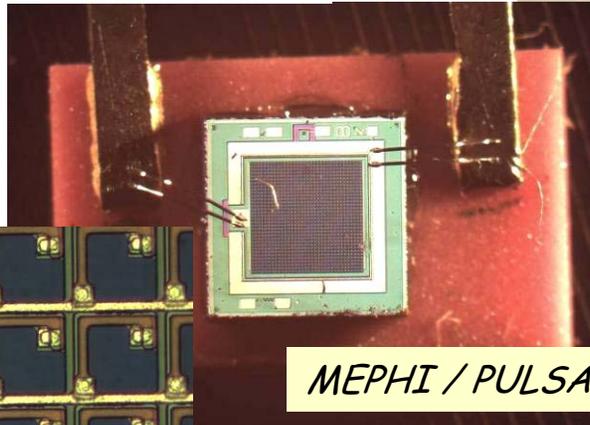


INTERNATIONAL LINEAR COLLIDER

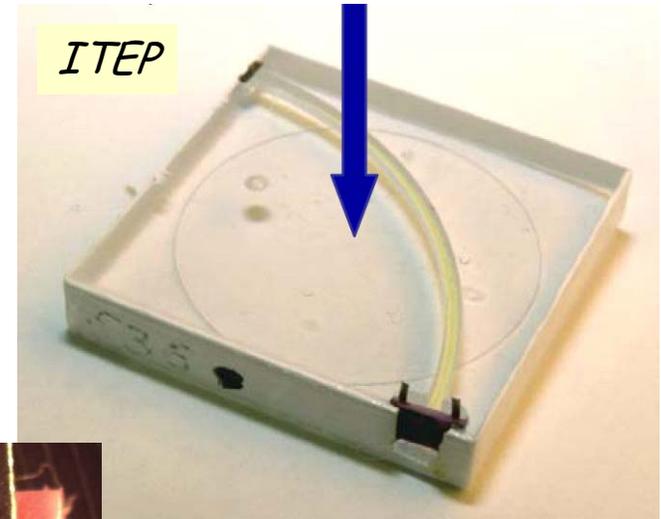
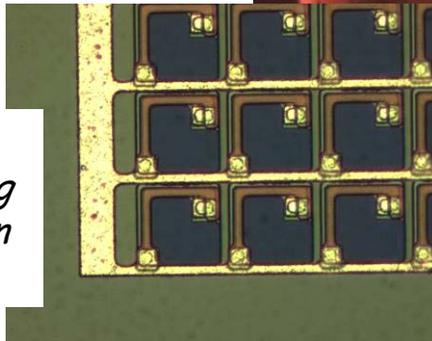
- Multipixel Geiger Mode APDs
 - Gain 10^6 , bias ~ 50 V, size 1 mm^2
 - Insensitive to magnetic fields



*Auto-calibrating
but non-linear*



*1156 pixels with
individual quenching
resistor on common
substrate*



*3x3 cm scintillator tile
with WLS fibre*

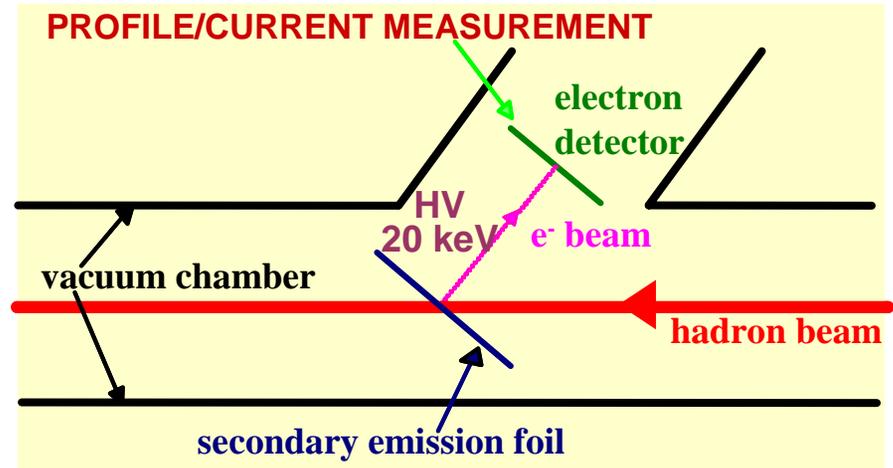
*New era for scintillator-
based detectors:
High granularity at
relatively low cost*


MAPS – MY PRESENTATION
HADRON THERAPY

- ▶ real time beam monitoring
- 60-250 MeV p, 120-400 MeV $^{12}\text{C}^{6+}$

Innovative Non-Destructive Beam Monitor for the Extraction Lines of a Hadrontherapy Centre

choice – dedicated MAPS sensor



- ▶ 10 kHz frame rate (<2% dose non-uniformity),
- ▶ beam $70 \times 70 \text{ mm}^2 \rightarrow$ demagnification $\times 5$,
- ▶ beam image granularity $\sim 1 \text{ mm} \rightarrow$ pixel pitch $\sim 200 \mu\text{m}$,
- ▶ active area matrix of minimum 5000 pixels,
- ▶ signal range single e^- to $9 \times 10^3 e^-/\text{pixel}$ every $100 \mu\text{s}$,
- ▶ sensitivity to 20 keV e^- ,
- ▶ no dead time.

SEM electrons from
0.1 – 0.4 μm thick
(Al- Al_2O_3 -Al) foils

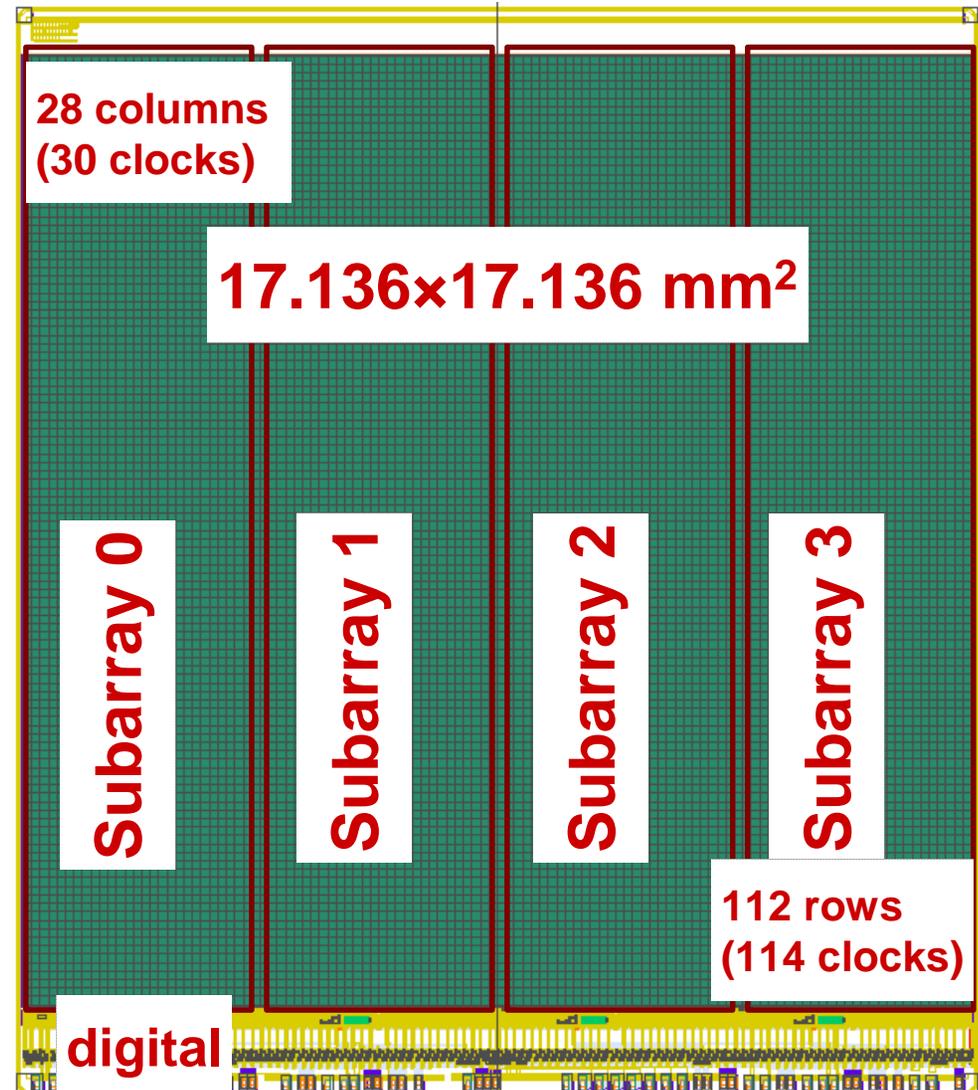
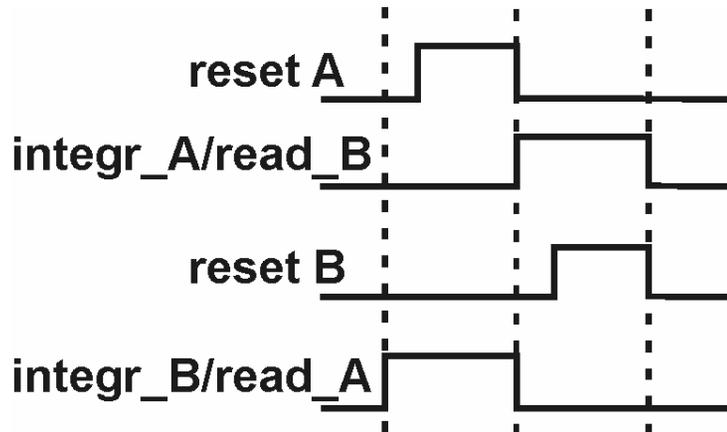
$5 \div 5000 \text{ rad/s}$ ($0.05 \div 50 \text{ Gy/s}$)

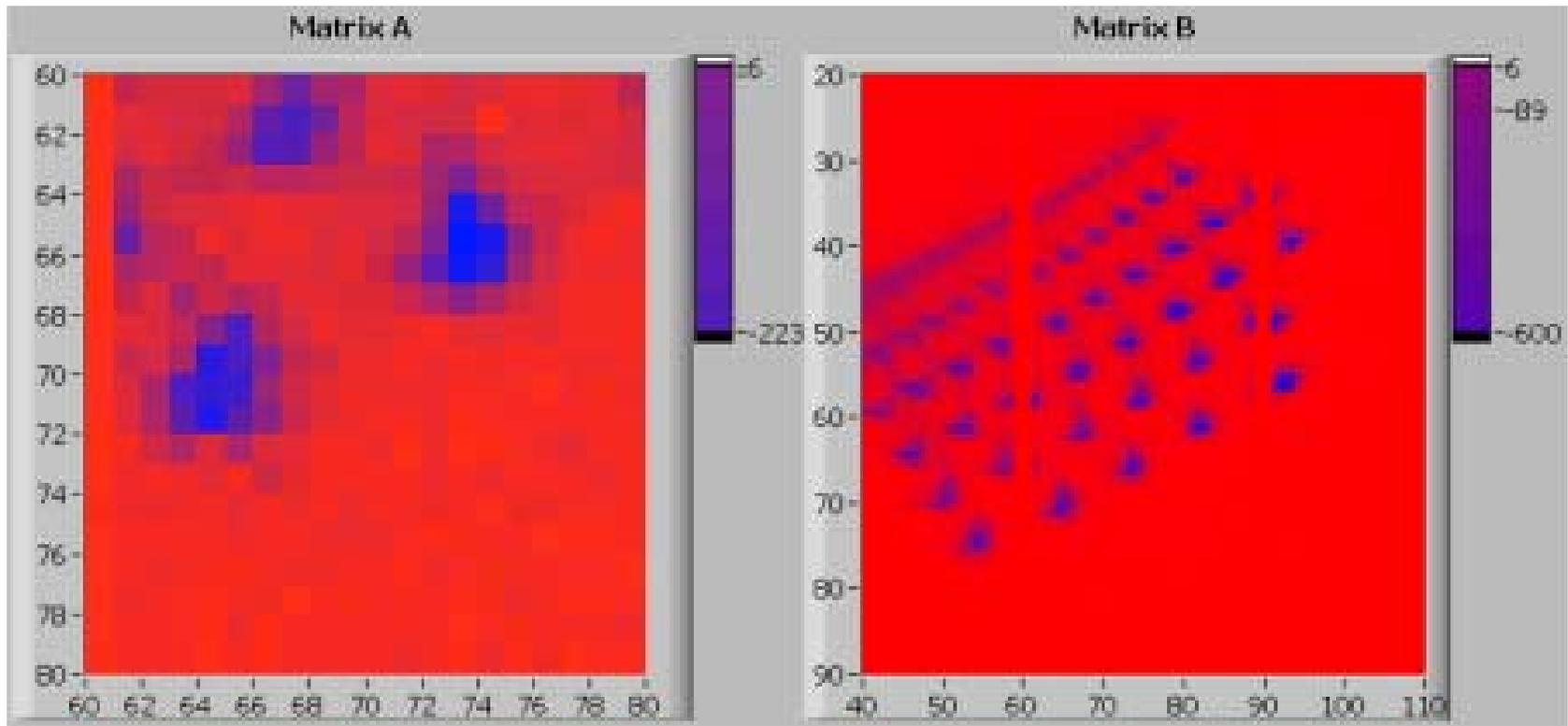
Thinned and back side illuminated detector required



MAPS – MY PRESENTATION

- ▶ AMS CUA 0.6 μm CMOS 14 μm epi,
- ▶ chip size: 17350 \times 19607 μm^2 ,
- ▶ array 112 \times 112 square pixels,
- ▶ four sub-arrays of 28 \times 112 pixels read out in parallel $w_{\text{read/integr}} < 100\mu\text{s}$,
- ▶ no dead time – alternate integration and readout in halves of pixels,



 **MAPS – MY PRESENTATION****▶▶ Tests on 17 MeV p beam in SLIM at JRC Ispra, Italy**

▶▶ nominal settings: 20.0 kV Al foil, 17.69 kV rings; the beam SLIM: un-measurably low (20 nA on the collimator).