Highlights of VIth International Meeting on Front-End Electronics for High Energy, Nuclear, Medical and Space App.

- CMOS Technology
- New Facilities
- LHC and SLHC
- Medical Applications
- Radiation Effects
- Special Design and New Detectors
- MAPS
- Neutrino Experiments
- Space Applications
- 3D Electronics
- International Linear Collider
Introduction to Conference

International Meeting on Front End Electronics is a conference focused on advanced front-end electronics mainly for high energy physics applications. The first meeting was held in Yellowstone in 1992 and since then the meeting has gone back and forth between the US and Europe every 2 or 3 years, with the last one held in Snowmass in 2003. This year meeting took place in Perugia, Italy, from May 17th to May 20th.

- 42 talks 20’ and 30’ minutes
- No formal proceedings of the conference, CD with talks
- Talks available at http://fee2006.pg.infn.it/
**CMOS Technology**

- **(Micron) Introduction to Micron’s Image Sensor Program**
  - no slides available
  - 1.7 µm pixel pitch with 1.5 transistor per pixel
  - ¼ " format 8Mpixel CMOS camera
  - w.r.t. classical 3T/ pixel

- **Special session on MAPS**
  - M. Barbero, UH, USA
  - Forceful development for KEKB Belle VxD

**~120Kpixel sensor (128x928 pix)**

- TSMC 0.25µm Process
- 5-deep double pipeline
- Pixel size 22.5 µm x 22.5 µm

- 36 transistors/pixel
- 5 sets CDS pairs
- 5 metal layers
CAP3
~21 mm
~3 mm
128 x 928 pixels, 22.5 μm²
~120 Kpixels / CAP3
0.25 μm process

Half ladder scheme
5-layer flex
Pixel Readout Board (PROBE)
PIXRO1 chip

32 CAP3/ladder
6 ladders/L1 layer
23 Mpixels

Brookhaven National Laboratory
Instrumentation Division
Facility for Antiproton Research (FAIR) facility at GSI, Darmstadt, Germany

Holger Flemming
GSI, Darmstadt, Germany

Ian Lazarus
NPG, CCLRC Daresbury, UK
New Facilities

- anti-Proton ANihilation at DArmstadt
- Physics Topics
  - Charmonium spectroscopy
  - Search for exotic hadrons in the charm sector
  - Charm mesons in nuclear matter
  - Open charm physics
  - Hypernuclei
- 4π detector
- Anti-protons on a hydrogen pellet target

Condensed Barion Matter
- Physics Topics
  - In-medium modifications of hadrons
  - Strangeness in matter
  - Indications for deconfinement at high $\rho_B$
  - Critical point
- Fixed target heavy ion experiment

R&D on front-end electronics for Fair just started
**LHC and SLHC**

*Improve the luminosity by a factor 10: $10^{34} \rightarrow 10^{35} \text{ cm}^{-2} \text{s}^{-1}$*

**Physics motivation**
- Increased physics reach in most typical LHC physics channels
- It is not clear today if these improvements are absolutely crucial for new physics, or rather if they represent (gradually) better measurements and better exploitation of the LHC energy domain
- However, in either case upgrading the LHC seems very attractive and an obvious next step to plan for

**Pragmatic view**
- The luminosity will increase as function of time at LHC, we will need to upgrade the detectors to take advantage of this
- Some parts of the detector systems might have performance problems or operational problems, and will therefore require interventions and improvements faster than foreseen today
- An impressive expertise about the construction has been accumulated and it is known today how to improve the detectors

Philippe Farhouat, CERN
LHC and SLHC

- The most relevant parameters for the detectors
  - BCO interval: 25ns, 15ns, 12.5ns, 10ns (or 75ns)
  - Forward area/beam pipe: Would like to move the closest machine element towards the IP
  - Timescales: assume 2014±2 years

Driven by this plot, but also by lifetime of IR quads 700 fb⁻¹

- Increased radiation levels (and resulting activation): Need to improve shielding, moderators, access procedures, and safety in general – important constraint for any change considered
inner detector

- Overall concept: **all silicon tracker**

- Replace
  - TRT by long silicon strips
  - SCT by short silicon strips
  - Pixel tracker by smaller silicon pixels

- Several ideas being developed now, no final decision made yet

<table>
<thead>
<tr>
<th>Radius [cm]</th>
<th>Fluence [cm(^2)]</th>
<th>Specification for Collected Signal (CCE in 300 um)</th>
<th>Limitation due to</th>
<th>Detector Technology</th>
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</thead>
<tbody>
<tr>
<td>&gt; 50</td>
<td>(10^{14})</td>
<td>20 ke(^{-}) (~100%)</td>
<td>Leakage Current</td>
<td>“present” LHC SCT Technology, “long” strips</td>
</tr>
<tr>
<td>20 - 50</td>
<td>(10^{15})</td>
<td>10 ke(^{-}) (~50%)</td>
<td>Depletion Voltage</td>
<td>“present” LHC Pixel Technology? “long” strips - “long” pixels</td>
</tr>
<tr>
<td>&lt; 20</td>
<td>(10^{16})</td>
<td>5 ke(^{-}) (~20%)</td>
<td>Trapping Time</td>
<td>RD50 - RD39 - RD42 Technology 3-D</td>
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Fast charge collection

Lower $V_{\text{depl}}$

But higher capacity

Radhardness considerably better than standard silicon

Until now fabricated on a small scale in house (Stanford)
  - Yield now 80%

Arrangements for commercial production at SINTEF (still in early state)

Ref: talk of Parker at Genova tracker upgrade workshop
http://agenda.cern.ch/fullAgenda.php?ida=a053875
Currently used **Parallel Powering:**

- Powerlines: constant voltage
- Modules: constant voltage

Idea of **Serial Powering:**

- TWO powerlines: constant current
- Modules with voltages: 10V, 7.5V, 5V, 2.5V, 0V
serial powering

- Basic principle:
  - Constant current through all modules
  - Voltages generated on FE chip by
    - Shunt regulators
    - Linear regulators
**Medical Applications**

**64 channel ASIC for the readout of gas detectors for hadron therapy**

Beam Calibration (before treatment) – Beam monitoring (during treatment)

big dynamic range

Gianni Mazza, INFN, Torino, Italy
charge subtraction

\[ f = \frac{I_{in}}{Q} = \frac{I_{in}}{C_{sub} \cdot \Delta V} \]

\[ \Delta V = V_{pulse}^+ - V_{pulse}^- \]

\[ Q^+ = C_{sub} \cdot \Delta V \]

\[ Q^- = C_{sub} \cdot \Delta V \]
Medical Applications

Mean 604.4 fC
rms 6.14 fC
rms % 1.02 %

26 chips x 64 channels

simply and quite efficient
Radiation effects

Realistic test structure with series of Inverters + DFF along 350um, and with different separation between n-well (PMOS logic) and NMOS:

- Without guardring
- Partial guardring
- Full guardring

Federico Faccio, CERN  
Radiation tolerance of commercial 130nm CMOS technologies for High Energy Physics Experiments
Radiation effects

I (A) vs TID (rad)

- □ - NoGuard
- △ - FullGuard
- ● - PartialGuard
In PMOS devices, flicker noise coefficient is clearly bias dependent (dependence is weaker in STM 90 nm technology).

In NMOS transistors $k_f$ is to a large extent independent of the overdrive voltage $V_{OV}$.
High Efficiency Neutron Detector Array (HENDA)

- Semiconductor linear thermal neutron detection imaging array
- Reaction: $n + ^{6}\text{Li} \rightarrow ^{4}\text{He} + ^{3}\text{H} + 4.79 \text{ MeV}$
- Pixel dimensions are 80 microns wide, and 4 cm long, with a 100 micron pitch
- Contains 1000 pixels, each with expected intrinsic thermal neutron detection efficiency of >20%
- Millions of holes filled with neutron reactive material increase the detector efficiency

Steven Bunch, University of Tennessee, USA

HENDA and Patara - A solid state neutron detector and a prototype readout chip for the SNS
Neutrino experiments

- Semi-Gaussian pulse response with 1 real, 4 complex poles
- 1 µ-sec pulse-pair resolution with gated baseline restoration (SNS synchronous)
- Current-mode quasi-linear operation
current mode solution allowing R values easier achievable in ICs

- Modified R-lens magnification
- Intrinsically low-noise
- R magnification allows small physical R to give low-frequency pole
- At higher signal levels, circuit is dynamic, but magnified small physical R dominates $1/g_m$ for improved linearity over Gm-C filters

Neutrino experiments

Tom Zimmerman, Fermilab, USA
The NOvA APD readout chip
Neutrino experiments

- 1 LSB ~ 100e: use 10 mV/fC ($C_{FB} = 0.1pF$), followed by shaper gain (x2-x10)
- 500 ns sample time: $M_1$ is PMOS to avoid significant 1/f noise contribution.
- $M_1$ (PMOS) source is referred to VDD, not ground.
- Where to refer APD capacitance for best PSRR?
- If $I_{BIAS}$ is fixed, then $V_{gs1}$ is constant, so $\Delta V_{in} = \Delta V_{DD}$. If $C_{APD}$ grounded: $\frac{\Delta V_{out}}{\Delta V_{DD}} = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{C_{APD}}{C_{FB}} = 100$ (disaster!!)
- If $C_{APD}$ is referred to VDD:
  - Tight input loop (minimizes pickup)
  - $\frac{\Delta V_{out}}{\Delta V_{DD}} = 1$ (better!!)
**Neutrino experiments**

- But what about $C_{\text{STRAY}}$ to ground (bond pad, bondwire, etc.)? Ruins PSRR.
- Use $M_2$ with $Vgs = VDD$ to generate $I_{\text{BIAS}}$.

Two advantages:
  
  - 1. For a given $I_{\text{BIAS}}$, \textbf{max. $Vgs_2$ yields min. $gm_2$, lowest $M_2$ noise.}
  - 2. $I_{\text{BIAS}}$ changes with $VDD$. Now $\Delta Vin = (\Delta VDD)[1 - (gm_2/gm_1)]$.
    
    If $(C_{\text{STRAY}}/C_{\text{APD}}) = (gm_2/gm_1)$, then $\Delta Vout = 0!!$ (to 1st order).

- Typically $(gm_2/gm_1) \sim 0.05$:
  
  M2 noise contribution $\sim 2$

  Optimum $C_{\text{STRAY}} \sim 0.5pF$

- Unavoidable $C_{\text{STRAY}}$ is of order $0.5pF$!
- Add small programmable input C to gnd.
- Make $I_{\text{BIAS}}$ ($M_2$ width) programmable.
- Tweak for best PSRR!
- Assumes same C’s on all channels.

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Bias current source, $Vgs_2 = VDD$
Key applications and potential of 3D

- Mobile Systems (minimum volume, low power, security)
- Systems for high parallel signal processing (e.g. image sensor)
- Increased Integration density
- More Functionality
- Mixed Technologies: 3D SoC
Who is Working on 3D ICs?

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT, RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix

Europe:
Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung
### 3D Electronics

<table>
<thead>
<tr>
<th>Via-Diameter [µm]</th>
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<tbody>
<tr>
<td>1.0</td>
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</table>

#### Etch Capability

<table>
<thead>
<tr>
<th>IZM-M</th>
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<tbody>
<tr>
<td>10:1</td>
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<tr>
<td>8:1</td>
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#### Via-Depth [µm]

<table>
<thead>
<tr>
<th>Aspect Ratio</th>
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<tbody>
<tr>
<td>40</td>
</tr>
<tr>
<td>4:1</td>
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</tbody>
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#### Process for filling

- **CVD of**
  - copper
  - tungsten
  - TiN
- **Electroplating of**
  - copper
  - Ti:W / Cu
- **PVD of Seedlayer**

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<td>1.0 µm</td>
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<table>
<thead>
<tr>
<th>Via-Depth</th>
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<tbody>
<tr>
<td>70 µm</td>
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<tr>
<td>7:1</td>
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- **Brookhaven National Laboratory**
- Instrumentation Division
**Vertical System Integration – *Three relevant Concepts (IZM-M)***

**InterChip Via (ICV)**
- Stack-Metal
- Top-Si (~ 10 µm)
- Bottom-Si (~ 630 µm)
- Passivation
- TEOS CMP
- Spacer 1
- Spacer 2
- MOCVD-TIN
- W CVD
- Polymide
- TEOS CMP

**Face to Face modular (F2F-M)**
- W-Plug / Polyimide
- W-Plug / Cu / Sn
- ICV / SLID

**ICV / SLID**
- Passivation
- Isolation
- Tungsten Plug
- Si 10 µm
- ILD 5-7 µm
- Copper
- Sn

**Low resistance per Via:**
- 1 Ohm, Pin only (2.5 x 2.5 µm², 10 µm depth)
- 2.5 Ohm Via with SLID-Contacts
Electrical measurements

Measured values (from 240 element chain statistics):

- Contact hole + soldering layers: ~0.43 Ohms
- W-plug: ~1 Ohm
- Contact hole + soldering layers: ~0.43 Ohms

Sum Value: 2.5 Ohm

Daisy Chains with up to 240 elements

Contact under Pressure and Heat
~5 bar, 260 – 300 °C (Sn-melt)
Eutectic Alloy; \( T_m \) > 600 °C

Chance: Increase of Performance

but: Costs per Chip (or Interconnect) as Main Criteria
3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor

Array cross section

Infrared image

3 Tier circuit diagram
3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p'n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 - 0.35 μm SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array
3D Laser Radar imager

- 64 x 64 array, 30 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel
3D SOI

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers

2) Invert, align, and bond wafer 2 to wafer 1

3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3
AHCAL testbeam prototype

- 1 cubic metre,  
- 38 layers, 2cm steel plates  
- 8000 tiles with SiPMs  
- Electronics based on ECAL design

Mechanics and front end boards: DESY  
Front end ASICs: LAL

Christophe de la Taille, IN2P3/LAL, Orsay, France  
Front End Electronics for Calorimetry at ILC
• **Multipixel Geiger Mode APDs**
  - Gain $10^6$, bias ~ 50 V, size 1 mm$^2$
  - Insensitive to magnetic fields

**Auto-calibrating but non-linear**

1156 pixels with individual quenching resistor on common substrate

**3x3 cm scintillator tile with WLS fibre**

**New era for scintillator-based detectors:**
*High granularity at relatively low cost*
Hadron Therapy

- real time beam monitoring
  - 60-250 MeV p, 120-400 MeV $^{12}$C$^{6+}$

Innovative Non-Destructive Beam Monitor for the Extraction Lines of a Hadrontherapy Centre

choice – dedicated MAPS sensor

- 10 kHz frame rate (<2% dose non-uniformity),
- beam 70×70 mm$^2$ ➔ demagnification ×5,
- beam image granularity ~1 mm ➔ pixel pitch ~200 μm,
- active area matrix of minimum 5000 pixels,
- signal range single e$^-$ to 9×10$^3$ e$^-$/pixel every 100 μs,
- sensitivity to 20 keV e$^-$,
- no dead time.

5 ÷ 5000 rad/s (0.05 ÷ 50 Gy/s)

Thinned and back side illuminated detector required

Design and test results of MAPS for a novel technique of hadron therapy beam monitoring
- AMS CUA 0.6 µm CMOS 14 µm epi,
- chip size: 17350×19607µm²,
- array 112×112 square pixels,
- four sub-arrays of 28×112 pixels read out in parallel $\tau_{\text{read/integr}}<100\mu$s,
- no dead time – alternate integration and readout in halves of pixels,
MAPS – my presentation

- Tests on 17 MeV p beam in SLIM at JRC Ispra, Italy

- nominal settings: 20.0 kV Al foil, 17.69 kV rings; the beam SLIM: un-measurably low (20 nA on the collimator).