Highlights of 5-th International Symposium of Semiconductor Tracking Detectors
14-17 June 2004, Hiroshima
Series of symposia dedicated to large tracking systems

• History of tracking semiconductor detectors
• High Energy Physics Experiments LHC (ATLAS, CMS), B-factories (BABAR, BELLE), NLC?
• NASA Projects AMS, GLAST
Semiconductor Tracking Detectors
historical overview

M. Turala
Pre-history


P.J. van Heerden et al., *The Crystal Counter*, Physica 16, (1950), 505


![Image of pulses from alpha-particles](image.png)

*Fig. 3. Photograph of pulses from sixteen alpha-particles striking the n−p barrier.*
Pre-history

1960-80

Si detectors in particle physics

- Cross-section measurements, JINR Dubna (V. Nikitin et al.)
- Active targets, CERN (G. Bellini et al.)
- Neutrino/ muon flux monitoring, CERN (E. Heijne et al.)
- BOL experiment at the Synchrocyclotron in Amsterdam
Si strip detectors technology

J. Kemmer et al.,
First HEP experiments

Identification (tagging) and measurements of particles with short lifetimes:

• charm lifetime: longer for mesons, e.g. $D^\pm (10.51\pm0.13) \times 10^{-13}$s
  shorter for baryons, e.g. $\Lambda_c (2.06\pm0.12) \times 10^{-13}$s
• average beauty hadron lifetime:  $(15.64\pm0.14) \times 10^{-13}$s
• $\tau$ lepton lifetime:  $(2.906\pm0.011) \times 10^{-13}$s

1981

decay length $l = \gamma \beta ct$, so typically the decay vertex is at a distance of single millimeters from the interaction vertex
First HEP experiments

NA11 experiment at CERN

1981

Fig. 5. Block diagram of the readout electronics.
First CCDs for HEP

Silicon drift chambers

VLSI readout


VLSI readout

Next generation of VLSI readout chips


Si vertex detectors for $e^+e^-$

First vertex detector for Mark II experiment at SLC

A. Litke et al., A Silicon Strip Vertex Detector for the Mark-II Experiment at the SLAS Linear Collider, Nucl. Instr. Meth., A265 (1988)

Fig. 1. Layout of the silicon strip vertex detector.

Fig. 2. Plan for a silicon detector module.
Microvertex DELPHI

1986-2000

1989-1990
192 detectors (all s-s)
55296 readout channels

1991-1993
288 detectors (all s-s)
73728 readout channels

1994-1995
288 detectors (96 s-s, 192 d-s)
125952 readout channels

1996-2000
888 detectors,
1399808 readout channels:
736 strip detectors with
174080 readout channels
1225728 pixels

From A. Zalewska

Si vertex detectors at LEP


<table>
<thead>
<tr>
<th>ALEPH VDETII</th>
<th>DELPHI Si Tracker</th>
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<table>
<thead>
<tr>
<th>OPAL µVTX3</th>
<th>L3 SMD</th>
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</table>
SLD vertex detector

Vertex detectors for SLD spectrometer at SLC


Fig. 47 Cross-section (XY view) of SLD upgrade vertex detector.

Fig. 48 Cross-section (RZ view) of SLD upgrade vertex detector.
Vertex detectors of BaBar

B. Aubert et al., The BaBar detector, Nucl. Instr. Meth A479 (2002)

Fig. 16. Fully assembled SVT. The silicon sensors of the outer layer are visible, as is the carbon-fiber space frame (black structure) that surrounds the silicon.

Fig. 17. Schematic view of SVT: longitudinal section. The roman numerals label the six different types of sensors.
Vertex detector of Belle

A. Abashian et al., The Belle Detector, Nucl. Instr. Meth A479 (2002)

SVD used in the Level 1.5 Trigger for rejection of beam gas background.
Pixel detectors

First Pixel Detectors


Fig. 1. Schematic representation of a hybrid detector.

Fig. 6. A photograph of a 10×64 readout chip bump bonded to a germanium PIN diode array.
Pixel detectors

Monolithic Active Pixel Sensors (MAPS)


From W. Dulinski
Pixel detectors

Monolithic Active Pixel Sensors (MAPS)


Measured CMOS MAPS tracking performance (20 µm pitch)

ENC: 10–20 e⁻, S/N_{seed, mean Landau} > 20–30

Efficiency (5σ seed cut): ε_{MIP} > 99 %

Spatial resolution: σ = 1.4 - 2.4 µm

Demonstrated on several devices in various submicron CMOS processes:

- AMS 0.6 µm, 14 µm epi
- Alcatel 0.35 µm, 4 µm api
- AMS 0.35 µm, no(!) epi
- TSMC 0.25 µm, 8 µm epi (LBL team)

From W. Dulinski
Towards high luminosities

R&D programme for LHC

- RD2 Proposal to Study a Tracking/ Preshower Detector for LHC
- RD8 Proposal to Develop GaAs Detectors for Physics at the LHC
- RD19 Development of Hybrid and Monolithic Silicon Micropattern Detectors
- RD20 Development of High Resolution Si Strip Detectors for High Luminosity at LHC
- RD29 A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Applications
- RD39 Development of Superconducting Strip Detectors
- RD41 Development of Diamond Tracking Detectors for High Luminosity Experiments at the LHC
- RD48 (Radiation Hardening of Silicon Detectors - \textit{ROSE})
- RD49 (Studying Radiation Tolerant ICs for LHC - \textit{RADTOL})
Radiation damage

**First observations in 1958**


**First observations in HEP**

Radiation damage

Beginning of systematic studies


- Donor removal and acceptor creation: \( N_{\text{eff}}(\Phi) = N_0 e^{-\phi} - \beta \Phi \)
- Type inversion @ fluences 0.4 – 3 x 10^{13} \text{ cm}^{-2} depending on the resistivity
- Anti-annealing → increase of the depletion voltage by ~ 30% in 2 years

Fig. 2. \( C-V \) curves of one photodiode measured at several intermediate proton fluences.

Fig. 3. Depletion voltage for photodiodes during proton irradiation. The line is the best fit according to eqs. (1) and (2). Type inversion occurs at \( \Phi = 1.1 \times 10^{13} \text{ cm}^{-2} \).

Fig. 10. Post-irradiation behaviour of the depletion voltage for photodiodes. The diodes were irradiated in 1990 (full symbols) and 1989 (open symbols).
Radiation damage

Submicron CMOS process

N. S. Saks et al., IEEE Trans NS-31 (1984), 1249


Si vertex-trackers for LHC

CMS - 210 m² of silicon sensors!

Full Silicon Tracker
210 m² of silicon sensors, $10^7$ strips, $6.7 \times 10^7$ pixels
Si vertex-trackers for LHC

CMS - Si strip detector modules/ pixel electronics

**Sensors:** Production batches received from Hamamatsu (excellent quality) and ST (improvement needed)

**Problems solved:** packaging of ASICs, bondability of pitch adaptors, ordering CF frames

**Hybrids:** latest batch good, 4700 ordered, awaiting bulk order (delivery in Oct 03)

**15’000 modules**

**15’000 hybrids**

Reliable, high yield Industrial hybrid Fabrication and assembly

**25,000,000 Bonds**

Automated module assembly

**Readout Chip:** 0.25μm ROC received Aug-03. Works very well (first iteration!). Performance superior to DMILL chip. Chip irradiated to 25 Mrad works fine.

0.25μm ROC, IBM_PSI146
Tracking in space

**AMS (ALPHA Magnetic Spectrometer)**

Y-H. Chang, The AMS Silicon Tracker

- Rigidity \( (dR/R \approx 2\% \) for 1 GeV Protons) with Magnet
- Signed Charge \( (dE/dx) \)
- 8 Planes, \( \sim 6m2 \)
- Pitch (Bending): 27.5\( \mu \text{m} \)
- Pitch (Non-Bending): 104\( \mu \text{m} \)
Tracking in space

GLAST Si tracker (1999 beam tests)

From R. Johnson
Production at HAMAMATSU

• 75% to 90% of the market (my estimate)
• 4 inch line since 1986
• 6 inch line since 1998
• Excellent quality control & feedback
• 6 inch line for Single Sided Strips only
• 0.6µm process O.K.

• FUTURE “PLANS”
• No large scale production for HEP
• Pixel & Drift Detectors
• Extend the Detector thickness up to 2 mm for higher energy X-rays
Position sensing in high energy heavy ion experiments

- NA45 (CERES) Experiment at SPS at CERN
  a) 3” cylindrical drift detector
  b) 4” cylindrical detector (past)
- STAR Experiment at RHIC at BNL (present)
- ALICE Experiment at LHC at CERN (future)
Innovations in CERES cyl. Det.

- Collection of leakage current generated at the Si-SiO interface at a sink anode
- Interlaced anodes (Nyquist filtering in linear dimension)
STAR Drift Detector
Silicon Drift Detectors

Tot. No. channels \(133 \cdot 10^3\)
Tot. No. detectors 260

Total area 1.37 m²

<table>
<thead>
<tr>
<th></th>
<th>Layer 3</th>
<th>Layer 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radius (mm)</td>
<td>14.9</td>
<td>23.8</td>
</tr>
<tr>
<td>Ladders</td>
<td>14</td>
<td>22</td>
</tr>
<tr>
<td>SDDs per ladder</td>
<td>6</td>
<td>8</td>
</tr>
</tbody>
</table>
ALICE Silicon Drift Detector

**Wafer**: 5”, Neutron Transmutation Doped (NTD) silicon, 3 kΩ·cm resistivity, 300 μm thickness

**Active area**: $7.02 \times 7.53 \text{ cm}^2$ (83% to total)
Detector design features

Charge collection zone

- guard cathodes (32 µm pitch)
- 292 drift cathodes (120 µm pitch)
- implanted HV voltage dividers
- 256 collection anodes (294 µm pitch)

injector lines

injector line bonding pad
MOS injector (every 8th anode)
Beam Tests in 2003 – Position resolution

Exhaustive test of the front-end parameters performed in beam test: gain, sampling & ADC frequencies...
The Controlled-Drift Detector (CDD)*

(*) Patents: US 6,249,033 EP0862226

- 2D position sensing (100-200µm)
- low capacitance (~100fF) and integrated JFET ⇒ high energy resolution
- low no. of channels (n instead of n×n)
- integrate-readout mode

The X-ray position along the drift is obtained from the electrons' drift time

The X-ray energy is obtained from the electron charge collected at the anodes
The BaBar Silicon Vertex Tracker: lessons learned

Giovanni Calderini, INFN Pisa

5th Internation Symposium on Semiconductor Tracking Detectors
Hiroshima, Japan
Constraints from the integration with PEP-II:
- Permanent (B1) dipole magnets restrict polar acceptance: $17.2^\circ < \theta < 150^\circ$
- Bunch crossing period: 4.2 ns (almost continuous interactions!)
- Radiation hardness
- Microstrip silicon detector; 5 double-sided layers
- Layer 1-3 (barrel-shaped) for a precise measurement of track impact parameter
- Layer 4-5 (arch shaped) for pattern recognition and low pt tracking
- Resolution dominated by multiple scattering
- 150 k channels, 340 wafers (6 different models)

Integration with PEP-II is a complex technical choice
- Double-sided, AC-coupled Si
- Integrated polysilicon bias resistors
- 300 µm n-type (4-8 kΩcm)
- P+ and n+ strips perpendicular to each other
The AToM Chip
(A Time over threshold Machine)

- 128 Ch’s/chip
- Rad-Hard bulk 0.8 µm CMOS process
  (HONEYWELL 4”)

- Capable of simultaneous:
  • Acquisition
  • Digitization
  • Sparsified Readout

- No common mode noise:
  • separation analog/digital parts in the chip layout
  • proper system shielding

- Info from AToM: Timestamp $T_0$ and TOT
- Internal charge injection
- Digital-based diagnostics
SVT High Density Interconnect

Functions:
- Mounting and cooling for readout ICs.
- Mechanical mounting point for module.

Features:
- AlN substrate.
- Double sided.
- Thermistor for temp. monitor.
- 3 different models.
Observed failure modes
(what could we repair and how?)

BaBar SVT not accessible and a shutdown to extract it requires at least four months!
Reliability of every part is critical.
Redundancy whenever possible!

A) Connectors

Never careful enough with cables and connectors.
Connectors on hybrid rather delicate
Several iterations on insertion tools and procedures.
Still one of the most critical issues
Redundancy and robustness more important than sophistication.

- Two redundant signal and control paths: used in several modules
- Must carefully balance the pros and cons of permanent vs. breakable connections

Connectors were one of the main sources of failure during and immediately after the installation

Improved insertion procedure during 2002 shutdown
Additional strain reliefs added

At least 3 half modules fixed in this way!
C) Cooling system: stability

Modest power dissipation: 4mW/ch = 600 W total

Nonetheless cooling issues have been driving several design issues:

- Material of hybrids
  AlN as a compromise between Al₂O₃ and BeO

- Mechanical structure
  Integrated cooling lines

- Complexity of interlock system to HV
  Degree of protection vs. possibility of fake alarms
  A glitch in the interlock system can trip the power and cost several minutes of data-taking!

General principles

Below atmospheric pressure – can’t leak.

And we’re happy we did it !!!
Conclusions

The SVT Detector of the BaBar experiment is working very well

Never been replaced since the beginning
Only 3 sections out of 208 not readout
Physics performance as expected

As in any system, some small imperfections: small details in the design that with the present wisdom we would do in a different way

I think at this stage of development of silicon detectors, we should analyze more critically the performance of our systems, and to share experience for the benefit of future designs.
Overview of the SCT

- The SCT forms part of the ATLAS Inner Detector.
- It is constructed using 4088 silicon micro-strip modules arranged as 4 barrels in the central region and 2 x 9 annular wheels in the forward region.
• The modules are arranged to provide 4 space points per track 
\[-2.5 < \eta < 2.5\]
• Each module measures two coordinates 
  – Detector pitch is 80 \( \mu \text{m} \) and \( \pm 20 \text{ mrad} \) stereo
Support structures

• All support structures, cylinders and discs, are produced using a sandwich material constructed with carbon fibre skins and a Korex core in industry.

• Cu/Ni cooling pipes, precision mounts for modules, power tapes, opto-fibre harnesses + DCS and alignment components are added.
Lessons learned

• The progression from prototyping components to full production can introduce some problems and cause delays
  – e.g. Forward hybrid de-lamination problem
• Do not underestimate the time required to optimise techniques and commission equipment
  – e.g. Module assembly techniques
• Take care in defining specifications
  – Achieving the same quality in multiple sites is not straightforward
• Expect unexpected production problems and allow for the time required to solve them
  – Start with a proper contingency to allow for unexpected problems
  – Rigorous prototyping and QA will minimise unexpected problems
SUMMARY

• The ATLAS SCT is in full production
  – Module production is well advanced (13% forward and ~75% barrel completed)
  – Most of the support structures have been delivered
  – Population with services is underway
  – The macro-assembly of completed barrels and discs is beginning
• Several problems have been solved
  – No show stoppers
• The schedule for completion is very tight but the collaboration is making every effort to achieve it.
The AMS-02 Detector

- **TRD**: e/p separation
- **TOF**: \( \beta \) and \(|Z|\), \text{sign}(Z)
- **Star tracker**: pointing
- **Magnet**: 0.8 T, \text{sign}(Z)
- **Si tracker**: p, \(|Z|\), \text{sign}(Z)
- **ACC**: anticoincidence system
- **RICH**: \( \beta \) and \(|Z|\), \text{sign}(Z)
- **ECAL**: e/p separation
The AMS-02 Tracker

- Localization of charged particle by double sided silicon sensors
- Eight layers (L1 ... L8) of \( \sim 1 \text{m}^2 \) each on five ultra-light support planes (P1 ... P5)
- Total of \( \sim 2500 \) double-sided sensors
- Resolution \( \sim 10 \mu\text{m} \) in bending direction, \( \sim 20 \mu\text{m} \) in non-bending direction

- Measures rigidity \( p/Z \) up to a few tens of TeV
- Measures specific energy loss \( dE/dx \sim |Z^2| \) for identification of elements
- Measures direction and energy of converted photons
Tracker Thermal Control System

AMS-Tracker Cooling System
(Mechanically pumped CO₂-Loop)

Wake heat pipe radiator
Evaporator rings
Passive pre-heater
Condensers
Ram heat pipe radiator
Condenser lines
Fluid component box

Collaboration with Dutch Aerospace Laboratory NLR and ZSU.
Tracker Performance:
1) spatial resolution

\[ \sigma_p \sim 8.5 \, \mu m \]

\[ \sigma_n \sim 30 \, \mu m \]
Conclusions

- No major problems encountered with the silicon tracker during AMS-01:
  Electrically and mechanically the tracker was unaffected by launch, landing and in orbit operations.

- For AMS-02, the number of independent measurement points and the issue of temperature control needed to be reconsidered.

- The tracker performance on the n-side of the silicon sensors had to be improved.

- In 2005, the new tracker for AMS-02 will be ready for system tests.
Basic Technology: Standard CMOS

Key Features:
- q collection via thermal diffusion (no HV)
- NO bump bonding
- “System on Chip” possible

Standard CMOS:
- Low Power
- Excellent Transistors
- Tight Process Control
- Excellent Uniformity
- High volume, low cost
- Large ADC, DSP base

Because of large Capacitance, need Thick DSSDs -- APS can be VERY Thin
Development Efforts

LEPSI, RAL, Strassbourg
Linear Collider
DESY/Hamburg

World’s Highest
$L=10^{34}$

Super-Belle: $\leq 10 \mu s$

See T. Tsuboyama’s talk

Apologies to those not mentioned:
Easy access will bring others

Belle Detector

LBNL, UC Irvine

STAR $\mu$-vertex detector
1. First upgrade (x4 present luminosity, 2006):
   10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):
   2 – 5 ms readout (integration) time
Operating principles

Need good CTI: $10^{-4}$ produces 25% signal loss after 5 cm charge transport
3.2 M-shell plasmons per µm (17 eV)
0.6 L-shell plasmons per µm (120 eV)
0.01 K-shell plasmons per µm (1.5 keV)

~4 primary collisions/µm with wildly fluctuating energy loss
Final thermalisation yields one e-h pair per 3.6 eV deposited
Conclusions

• CCDs have since 20 years been the *only* pixel devices used as sensors in vertex detectors for heavy flavour physics.

• This is of course about to change, with ATLAS, CMS, ALICE, BTEV, STAR, …

• The CCD architecture appears to be well matched to the TeV-scale linear collider. The discovery potential of this machine will be orthogonal to the LHC due partly to
  ▪ Ultra-thin and precise gigapixel vertex detector
  ▪ multi-Megavoxel calorimeter allowing sophisticated energy flow
### Status of radiation-hard materials for tracking detectors at SLHC

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>Diamond</th>
<th>Diamond</th>
<th>4H SiC</th>
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<tbody>
<tr>
<td>Material Quality</td>
<td>Cz, FZ, epi</td>
<td>Polycrystalline</td>
<td>single crystal</td>
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<td>(E_g) [eV]</td>
<td>1.12</td>
<td>5.5</td>
<td>5.5</td>
<td>3.3</td>
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<td>(E_{breakdown}) [V/cm]</td>
<td>(3\cdot10^5)</td>
<td>10'</td>
<td>10'</td>
<td>(2.2\cdot10^6)</td>
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<td>(\mu_e) [cm²/Vs]</td>
<td>1450</td>
<td>1800</td>
<td>&gt;1800</td>
<td>800</td>
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<tr>
<td>(\mu_h) [cm²/Vs]</td>
<td>450</td>
<td>1200</td>
<td>&gt;1200</td>
<td>115</td>
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<td>(v_{sat}) [cm/s]</td>
<td>(0.8\cdot10^7)</td>
<td>(2.2\cdot10^7)</td>
<td>(2.2\cdot10^7)</td>
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<td>(Z)</td>
<td>14</td>
<td>6</td>
<td>6</td>
<td>14/6</td>
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<tr>
<td>(\varepsilon_r)</td>
<td>11.9</td>
<td>5.7</td>
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<td>e-h energy [eV]</td>
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<td>13</td>
<td>13</td>
<td>7.6</td>
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<tr>
<td>Density [g/cm³]</td>
<td>2.33</td>
<td>3.515</td>
<td>3.515</td>
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<td>Displacem. [eV]</td>
<td>13-20</td>
<td>43</td>
<td>43</td>
<td>25</td>
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<td>e-h/(\mu_m) for mips</td>
<td>89</td>
<td>36</td>
<td>36</td>
<td>55</td>
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<tr>
<td>Max initial ccd [(\mu_m)]</td>
<td>&gt;500</td>
<td>280</td>
<td>550</td>
<td>40 (= thickness)</td>
</tr>
<tr>
<td>Max wafer (\phi) tested</td>
<td>6”</td>
<td>6”</td>
<td>6mm</td>
<td>2”</td>
</tr>
<tr>
<td>Producer</td>
<td>Several</td>
<td>Element-Six</td>
<td>Element-Six</td>
<td>Cree-Alenia, IKZ</td>
</tr>
<tr>
<td>Max fluence [cm²]</td>
<td>(7\cdot10^{15}) 24GeV p</td>
<td>(2\cdot10^{15}) n, (\pi), p</td>
<td>Not reported</td>
<td>(10^{16}) in progress</td>
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<td>CERN R&amp;Ds</td>
<td>RD50, RD39</td>
<td>RD42</td>
<td>RD42</td>
<td>RD50</td>
</tr>
</tbody>
</table>

See H. Kagan Talk  
See Kinoshita Talk
Radiation Induced Microscopic Damage in Silicon

$\text{particle} \rightarrow S_i S \rightarrow \text{Vacancy + Interstitial}$

$E_K > 25 \text{ eV}$

$E_K > 5 \text{ keV}$

Point Defects (V-V, V-O .. )

Influence of defects on the material and device properties

Charged defects $\Rightarrow N_{\text{eff}}, V_{\text{dep}}$

e.g. donors in upper and acceptors in lower half of band gap

Trapping (e and h) $\Rightarrow $ CCE

shallow defects do not contribute at room temperature due to fast detrapping

generation leakage current $\Rightarrow$

Levels close to midgap most effective
Leakage Current

$\Phi_{eq}[cm^{-2}]$

$\Delta I / V \[A/cm^3\]$

- **Damage parameter $\alpha$ (slope)**
  
  $$\alpha = \frac{\Delta I}{V \cdot \Phi_{eq}}$$

- $\alpha$ independent of $\Phi_{eq}$ and material kind

$V_{dep}$, $N_{eff}$

$U_{dep} \[V\]$ (d = 300 $\mu m$)

$|N_{eff}| \\left[ 10^{11} \text{ cm}^{-3} \right]$
Cz-Si as Detector Material

• High resistivity Cz-Si previously not available because lack of commercial applications

• Available in large diameters (up to 300mm) and in large quantities if necessary

• Oxygen content can be adjusted by crystal pulling speed within the range from few ppma above the O solid solubility in Si

• Homogenous impurity distribution in crystal can be achieved if a magnetic field is applied during the growth

• N and P-type high resistivity Cz-Si available
Thermal Donor generation (experimental results)
Thermal Donor generation

\[ N_{TD} = \left( \frac{a}{b} \right) C_{io}^\chi \frac{1}{|N_d - N_A|^2} \left\{ 1 - e^{-bD_{io}C_{io}t} \right\} \]

\[ D_i = 0,13 e^{-\frac{E_A}{kT}} \quad 2,4 \leq \chi \leq 2,6 \]

Cz-Si, \( O_i \approx 8 \times 10^{17} \text{ cm}^{-3} \)

MCz-Si, \( O_i \approx 4 \times 10^{17} \text{ cm}^{-3} \)

Oxygenated Fz-Si, \( O_i \approx 1 \times 10^{17} \text{ cm}^{-3} \)
Conclusions

- We have demonstrated first full-sized particle detectors ever made of Cz-Si
- Cz-Si shows very promising radiation hardness properties in proton beams
- High O content p⁺/n⁻/n⁺ detectors can be processed with p-type boron doped Cz-Si wafers by inverting p → n with TD’s
- It is low temperature, low cost process >> feasible solution for large scale experiments
- Resistivity range is very wide in p → n TD-process 500Ωcm < σ < ~10 kΩcm
- O content should be within some limits (3ppma < Oᵢ < 6ppma). Magnetic field may be required in crystal growth.
SiC Properties

Silicon carbide (SiC) is expected to be applied to high-power and high-frequency devices.

• Bandgap
  – $\times$ 2–3
• Break-down field
  – $\times$ one order
• Saturation velocity of electron
  – $\times$ 2
• Thermal conductivity
  – $\times$ 3
• High operation temperature
  – 500–600°C (Si:150°C)
• Radiation tolerance
  – $\times$ 1~2 order (MOSFET, γ)

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SiC</th>
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<tr>
<td>Bandgap</td>
<td>1.12 eV</td>
<td>2.2–3.3 eV</td>
</tr>
<tr>
<td>Break-down field</td>
<td>3 x 10^5 V/cm</td>
<td>3 x 10^6 V/cm</td>
</tr>
<tr>
<td>Saturation velocity of electron</td>
<td>1 x 10^7 cm/s</td>
<td>2 x 10^7 cm/s</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.5 W/cm K</td>
<td>4.9 W/cm K</td>
</tr>
<tr>
<td>High operation temperature</td>
<td>150 °C</td>
<td>500–600 °C</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
Summary

- We have evaluated electrical characteristics and detector performance for alpha particle before and after irradiations ($\gamma$, $\beta$).
  - I-V characteristics
    - Forward $\eta$ is no significant difference
    - Reverse Leakage current increase
  - C-V characteristics
    - $N_{\text{eff}}$ Neff decrease
  - CCE
    - CCE-V $\eta$ is changed so as to Neff
    - Life time $\tau$ is no significant difference
- The results of measurement for irradiated Si indicate that SiC has the possibility of radiation hardness as compared with Si.
The SCT Module

• Built with 2 pairs of identical single-sided silicon sensors
  – 768 AC-coupled p-strips on n-type silicon
  – 80 μm strips pitch
  – Glued back to back
    • with 40 mrad stereo angle
    • on a mechanical core of Thermal Pyrolitic Graphite (TPG)

• Each pair of sensors wire bonded to form long strips of 126 mm
The ATLAS SCT Readout Electronics

- Handled by ASICS realized in the radiation hard DMILL technology (ABCD3T)
- Custom IC designed by the ATLAS-SCT design team (W. Dabrowski et al.)
- 128-channel analog front-end consisting of amplifiers and comparators
- Digital readout circuit (pipeline)
- Operating at the LHC bunch crossing frequency (40 MHz)
- Utilizes the “binary” scheme
  - Signals from the silicon detector are amplified and then compared to a threshold
  - Only the result of this comparison (hit or no-hit logic)
The Wafer production testing and IC grading

- 6 inch wafer (fabricated by ATM, Nantes, France)
- 256 IC’s
- Wafer testing shared between CERN, RAL, SCIPP
- Design and implementation of a sophisticated tester
  - verify the analog front-end performance (gain & noise)
  - digital functions (control register, addressing, communication, pipeline, and output buffer)
  - the power consumption
SCT Hybrid Testing

- An extensive suite of both hardware and software has been developed to facilitate hybrid and module testing.
- The readout system is based on custom designed VME boards including Low Voltage and High Voltage boards developed specifically for SCT production testing.
- Two automated series of tests have been designed to simplify the testing procedure:
  - *Characterization Sequence* aimed to perform a full characterization of a hybrid or a module for both digital and analog performance
Conclusion

• By developing diagnostic tools during SCT module production we were able to reduce the rate of ASIC replacements on hybrids with defective ASICs and increase the number of working modules.

• The studies have demonstrated the importance of the capability to adjust the FE parameters and the importance of
Prototype results (1)

- Prototypes tested at the bench and in beam tests connected with SDD sensors.
- Results with PASCAL32

Corrections applied:
- doping inhomogeneity map
- voltage divider residual non-linearity
- drift velocity T-dependence
- drift-dependent non-linearity of centroid due to diffusion widening

**Along the drift-time axis**

**Along the anode axis**
Prototype results

- Prototypes tested at the bench and in beam tests connected with SDD sensors: results with full-size prototypes

- Resolution along the anode direction

- Resolution along the drift direction

Resolution along the drift direction

Resolution along the anode direction
BUMP BONDING + CMOS PROCESSOR

SPECIAL FEATURES
GLOBAL ADJUSTMENT for COMPARATOR TESTING / MASKING of EACH PIXEL
DELAY 6 ns rms DIGITAL TUNING in EACH PIXEL
DARK CURRENT COMPENSATION / COLUMN

LHC1 CHIP  CERN 1996
16 COLUMNS x 256 ROWS
pixel  50µm x 500 µm

PRESENTED in HIROSHIMA 1996
SYSTEM INTEGRATION

• CAN BE USED for IMAGING
3D ELECTRONICS : IMEC

- THINNING of WAFERS
- INSERTION of Epoxy or Silicon Interposer LAYERS
- 3D connectivity (8 chips shown)
- already in production (e.g. Bluetooth)
- typical cost: ~ 10 $ per package in volume production
HIGH DENSITY BONDING

0.25 µm CMOS CHIP
CERN 2001
CAMPBELL & LLOPART
256 COLUMNS x 256 ROWS
pixel 55µm x 55 µm

BUMP DEPOSITION
& SEM PHOTOS
COURTESY MCNC-RDI DURHAM NC

PITCH 55 µm x 55 µm

HIGH RESISTIVITY Si SENSOR MATRIX
CANBERRA SEMICONDUCTOR
INDUSTRIAL BUMP BONDING • BECOMING MAINSTREAM

AMKOR
with UNITIVE PITCH 200 µm

INTERPOSIERS
MULTILAYER CHIP PACKAGE
INTEGRATED CHIP ASSEMBLIES

- Ravi Mahajan, Johanna Swan, Nasser Grayeli
- Assembly Technology Development
- Technology Manufacturing Group Technology

NEW PACKAGING TECHNOLOGIES
CONNECTIONS beyond BUMP-BONDING

Z-AXIS PINS
CEA-LETI Gasse et al.

PITCH 10 µm -30 µm
TRACK VECTOR DETECTOR

3D MULTILAYER ASSEMBLY

PROVIDES $X$, $Y$, $\Theta_X$, $\Theta_Y$

intersecting position + angular direction
AMBITIOUS MULTI-LAYER
Gamma-ray Large Area Space Telescope

GLAST Mission
- High-energy gamma-ray observatory with 2 instruments:
  - Large Area Telescope (LAT)
  - Gamma-ray Burst Monitor (GBM)
- Launch vehicle: Delta-2 class
- Orbit: 550 km, 28.5° inclination
- Lifetime: 5 years (minimum)

GLAST Gamma-Ray Observatory:
- LAT ~20 MeV - 300 GeV
- GBM 20 keV to 20 MeV
- Spacecraft bus (Spectrum Astro)
GLAST LAT Overview

Si Tracker
- $8.8 \times 10^5$ channels, <160 Watts per 16 tower units
- 16 tungsten layers, 36 SSD layers per one tower
- Strip pitch = 228 µm
- Self triggering

CsI Calorimeter
- Hodoscopic array
- $8.4 \times X_0$, 8 × 12 bars
- 2.0 × 2.7 × 33.6 cm
  - ⇒ cosmic-ray rejection
  - ⇒ shower leakage correction

ACD
- Segmented scintillator tiles
- 0.9997 efficiency
- Minimal self veto

Mega-channel particle-physics detector
- in orbit:
  - ⇒ Low power (<650 W)!
  - ⇒ Extensive data reduction on orbit!
  - ⇒ No maintenance!
Overview of Silicon Tracker (TKR)

- Pair-conversion telescope
- Advantage of silicon tracker, comparing with EGRET spark chamber
  - Self trigger
  - High density optimal packing of converters and detectors enabled.
  - Fine strip pitch
    - Fine track

- Multiple-scattering limits angular resolution
- Gamma
- Veto counters
- E+ E-
Front-end Electronics MCM (Multi-chip Module)

- Two custom ASICs implemented by Agilent 0.5μm process
  - GTFE: 64-channel amplifier-discriminator, 24/layer
  - GTRC: read-out controller, 2/layer

- Power consumption
  - Analog: 1.5V and 2.5V lines, 120mW/layer = 78µW/channel
  - Digital: 2.5V, 126mW/layer

- GTFE (Front-End) ASICs: 24
  64 channels/chip * 24 = 1536 channels/layer

- GTRC (Read-out Controller) ASICs: 2

Pitch adapter
'Tray'

GTFE (Front-End) ASICs: 24
64 channels/chip * 24 = 1536 channels/layer
EM (Engineering Model) Mini Tower

- 6 SSD layers (3 x and 3 y) and 3 tungsten-converter layers:
  minimum configuration to test trigger condition
Summary (Current Status)

• To launch in early 2007, productions and tests of flight TKR towers are now going.
  – Fabrication of front-end electronics MCM (Teledyne LA in USA)
  – Burn-in tests of MCM (SLAC in USA)
  – Kapton flex-circuit cable fabrication (UCSC, SLAC, in USA)
  – Tray assembly and test (in Italy)
  – Composite tray panels (in Italy)
  – Sidewall fabrication (in Italy)
    Tower assembly and test (in Italy)