VECTORS and SUBMICRON TRACKING in SILICON DETECTORS

INSTRUMENTATION DIVISION SEMINAR
BROOKHAVEN NATIONAL LABORATORY

ERIK H.M. HEIJNE
CERN Genève
25 June 2008
NUCLEAR EMULSION

SPECIAL, THICK FILM  AgBr  3D, sub µm PRECISION

CHARM DECAY

ENERGY TRANSFERS TO GRAINS  CREATE LATENT IMAGE OF TRACKS

Emulsion Event WA59  ~ 1985

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
CERN H6 beam 120 GeV PIONS

SILICON PIXEL ASSEMBLY
256x256  55um pixels
EXPOSURE TIME  50 ms

BEAM HODOSCOPE &
TARGET &
DETECTOR

14.08 mm
256 pixels
BUMP BONDING Medipix2

BUMP DEPOSITION & SEM PHOTOS
COURTESY MCNC-RDI DURHAM NC

PITCH 55 µm

HIGH RESISTIVITY
Si SENSOR MATRIX
CANBERRA SEMICONDUCTOR

0.25 µm CMOS CHIP
CERN 2001
CAMPBELL & LLOPART
256 COLUMNS x 256 ROWS
pixel 55µm x 55 µm
DISCUSS SEVERAL DEVICES from MEDIPIX FAMILY

MEDIPIX2
TIMEPIX
MEDIPIX3

INTENDED for 2D X-RAY IMAGING
MAIN FUNCTIONALITY

SIGNAL PROCESSING in EACH PIXEL
TUNABLE THRESHOLD SETTINGS
13 bit REGISTER in EACH PIXEL
ADJUSTABLE FRAME EXPOSURE TIME $\mu$s - min

**MEDIPLEX2** COUNTING SIGNALS between LOWER/UPPER THRESHOLD

**TIMEPIX** CLOCK 10 MHz - 100 MHz to EACH PIXEL:
COUNTS from FIRST SIGNAL ARRIVAL TIME DRIFT TIME
COUNTS TOTAL TIME of SIGNAL(S) over THRESHOLD TOT

**MEDIPLEX3** SPECTROSCOPIC MODE,
SUMMING of COINCIDENT SIGNALS in ADJACENT PIXELS
MEDIPIX2 PARTNERS

- U INFN Cagliari
- CEA-LIST Saclay
- CERN Genève
- U d'Auvergne Clermont
- U Erlangen
- ESRF Grenoble
- U Freiburg
- U Glasgow
- IFAE Barcelona
- Mitthoeugskolan
- MRC-LMB Cambridge
- U INFN Napoli
- NIKHEF Amsterdam
- U INFN Pisa
- FZU CAS Prague
- IEAP CTU in Prague
- SSL Berkeley

Erik HEIJNE  CERN PH Dept

SPOKESMAN Michael CAMPBELL
Deputy Jan VISSCHERS

Instrumentation Division Seminar, BNL 25 June 2008

http://medipix.web.cern.ch/MEDIPIX/
THANKS TO

R&D, DESIGN WORK by the CERN MEDIPIX team

MICHAEL CAMPBELL, team leader
XAVI LLOPART
LUKAS TLUSTOS
RAFA BALLABRIGA
WINNIE WONG
EH

& CERN-MICROELECTRONICS GROUP

8-YEAR R&D EFFORTS by MEDIPIX COLLABORATION

WORK in the BEAM

2006: RYAN FIELD, SUMMER STUDENT NCSU
2007: JOHN IDARRAGA, MONTREAL, DOMINIC GREIFFENBERG, FREIBURG
2008: DAAN BOLTJE, NIKHEF
SCHEMATIC LHC
Underground
CERN LHC COOLING DOWN
LOW NOISE
(relative to microstrips)
ELECTRONICS READOUT
accepts positive and negative input _ different detector materials
charge sensitive preamplifier with individual leakage current compensation  CSA
2 discriminators with globally adjustable threshold
3-bit local fine tuning of the threshold per discriminator
1 test and 1 mask bit
external shutter activates the counter
13-bit pseudo-random counter/ shift register

Analogue

Digital

CERN

Instrumentation Division Seminar, BNL 25 June 2008
Medipix2 PIXEL CELL LAYOUT

CMOS technology 0.25μm
6 metal layers
pixel cell has ~500 transistors ⇒
chip ~33 million transistors

Static power consumption:
~8μW/channel @ 2.2 V

Amplifier Gain: ~11 μV/e⁻
Electronic Noise: ~100 e⁻ rms.
Medipix2 PIXEL CELL LAYOUT

CMOS technology 0.25μm
6 metal layers
pixel cell has ~500 transistors ⇒
chip ~33 million transistors

Static power consumption:
~8μW/channel @ 2.2 V

Amplifier Gain: ~11 μV/e-
Electronic Noise: ~100 e⁻ rms.
EVEN SMALL SIGNALS CAN BE USED

TRIMMED THRESHOLD DISPLACED to 'LOW' VALUE

1100 e\textsuperscript{-} or 4 keV in Si

IN BEAM TEST 800 e\textsuperscript{-} to 1000 e\textsuperscript{-}

SMALL PIXEL CELL
55\(\mu\)m x 55\(\mu\)m

THRESHOLD TRIMMING

GENERATED by M.I.P. in ~16 \(\mu\)m Si

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
TRUE 3D TRACKING INFORMATION from Si VOLUME
SETUP in H6 BEAM CERN

ACTIVE AREA SENSOR
14.08x14.08 mm²
256x256 PIXELS

BEAM AXIS H6

PERIPHERAL CHIP FUNCTIONS

WIREBOND CONNECTIONS
ASSEMBLY SUPPORT PCB

FLAT CONNECTOR

USB PROCESSOR MODULE

SENSOR 45 DEGREES
READOUT CHIP

beam
x (rows)
y (thickness)
z (columns)
SETUP in H6 BEAM CERN

ACTIVE AREA SENSOR
14.08x14.08 mm²
256x256 PIXELS

PERIPHERAL CHIP FUNCTIONS
WIREBOND CONNECTIONS
ASSEMBLY SUPPORT PCB

FLAT CONNECTOR
USB PROCESSOR MODULE

SENSOR 45 DEGREES
READOUT CHIP

BEAM AXIS H6

beam
x (rows)
y (thickness)
z (columns)
SETUP in H6 BEAM CERN

ACTIVE AREA SENSOR
14.08x14.08 mm²
256x256 PIXELS

BEAM AXIS H6

PERIPHERAL CHIP FUNCTIONS

WIREBOND CONNECTIONS
ASSEMBLY SUPPORT PCB

FLAT CONNECTOR

USB PROCESSOR MODULE

x (rows )
y (thickness)
z (columns)
SETUP in H6 BEAM CERN

ACTIVE AREA SENSOR 14.08x14.08 mm
256x256 PIXELS

PERIPHERAL CHIP FUNCTIONS
SENSOR 45 DEGREES
READOUT CHIP
ASSEMBLY SUPPORT PCB
WIREBOND CONNECTIONS
USB PROCESSOR MODULE
FLAT CONNECTOR

beam
x (rows) y (thickness) z (columns)
H6 120 GeV PIONS

EXPOSURE 1 s

14.08 mm
256 pixels

PARTICLE 'TRAILS'
~ PARALLEL

Parallel Medipix2  P-02-0668
120 GeV PIONS

INTERACTION in Medipix DETECTOR
Si 'EMULSION'

DECAY of NEUTRAL K ?

WHICH DIRECTION HAS TRAIL ?
PROJECTION CAUSES
AMBIGUITY : TOWARDS/AWAY

BEAM

1 mm

↓ 500 µm

July 2006 Parallel Medipix P-05-0583
120 GeV PIONS

ALL TRAILS in SAME DIRECTION

3-D RECONSTRUCTION

INTERACTION
190μm behind SENSOR

Parallel Medipix2 0016

inar, BNL 25 June 2008
MUONS from $\pi$, K DECAy

MEASUREMENTS MEDIPIX 2006

VECTORS & SUBMICRON PRECISION
H6 BEAM DECAY MUONS + BACKGROUND

ELECTRONs

ALPHA or NEUTRON

3 MUONS

(a few dead pixels)
H6 DECAY MUONS : EFFICIENCY

A FEW DEAD PIXELS

NO EFFECT on EFFICIENCY

Parallel Medipix M-01-0013
H6 DECAY MUONS : EFFICIENCY

TOTAL ENERGY/CHARGE in a TRAIL
3.4 MeV or \( \sim 1 \text{ M e}^- \)
CAN BE USED FOR TIMING/TRIGGER

A FEW DEAD PIXELS
NO EFFECT on EFFICIENCY

Parallel Medipix M-01-0013
SMALL-PIXEL CHARGE SHARING

CHARGE-SHARING & SINGLE - QUANTUM PROCESSING

MULTIPLE HITS for BINARY OPERATION if
SMALL PIXEL DIMENSIONS
THICK SENSOR    MORE DIFFUSION DURING DRIFT
LOW TRESHOLD

EFFECTS on ENERGY SPECTRAL DISTRIBUTION
REDUCTION of PEAK
INCREASE    LOW - ENERGY TAIL

TO BE SIGNIFICANTLY REDUCED in MEDIPIX3
CHARGE COLLECTION & LATERAL DIFFUSION

GROUND

DRIFT

+100V

DIFFUSION width shown EXAGGERATED

a PARTICLE ~ MIDDLE of PIXELS
TOP ROW

b PARTICLE CLOSE to REAR
MIDDLE ROW

ERIK HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
CHARGE SHARING

a and b SHARE SIGNAL CHARGE

COMPARATOR SIGNAL if \( > \sim 800 \) e\(^-\)

\[ > \frac{800}{3800} e^- > 20\% \text{ PARTITION} \]

DIFFUSION PRODUCES DOUBLE HITS

~8µm

DIFFUSION PRODUCES DOUBLE HITS
MUON TRAILS : 'CLOSED' SEGMENTS

VECTOR MEASUREMENTS from 'CLOSED SEGMENTS'

BOUNDED by SEQUENCES of DOUBLE HITS

ROW TRANSITION POINTS

Parallel Medipix M-01-0013
HIGH RECONSTRUCTION PRECISION with MUONS

DOUBLE HITS ---→ PRECISE ROW TRANSITION POINTS
CONSTRAIN TRAJECTORY to~ 0.05 µm  (??)

HOW to DEAL with SUCH DATA

Parallel Medipix M-01-0013
H6 DECAY MUONS

HIGH PRECISION at OVERLAP POINTS

VECTOR MEASUREMENTS

ANGULAR DISTRIBUTIONS

Parallel Medipix M-01-0013
### MUON VECTORS

Comparison of Tilt Angles for segments of Trail #4 in frame M01-013

<table>
<thead>
<tr>
<th>SEGMENT</th>
<th>SINGLE HIT PIXELS</th>
<th>INCL. OVERLAP</th>
<th>TILT mradian</th>
</tr>
</thead>
<tbody>
<tr>
<td>open left 1</td>
<td>37</td>
<td>38.5</td>
<td>26.0</td>
</tr>
<tr>
<td>2</td>
<td>43</td>
<td>48.5</td>
<td>20.6</td>
</tr>
<tr>
<td>3</td>
<td>37</td>
<td>45.5</td>
<td>22.0</td>
</tr>
<tr>
<td>4</td>
<td>41</td>
<td>48.5</td>
<td>20.6</td>
</tr>
<tr>
<td>5</td>
<td>41</td>
<td>49.5</td>
<td>20.2</td>
</tr>
<tr>
<td>open right 6</td>
<td>20</td>
<td>25.5</td>
<td>39.2</td>
</tr>
<tr>
<td>FIT on 5 pts</td>
<td></td>
<td></td>
<td>20.92</td>
</tr>
<tr>
<td>PIXELS 1-256</td>
<td>219</td>
<td>256</td>
<td>23.4</td>
</tr>
</tbody>
</table>

### VECTOR MEASUREMENTS

Parallel Medipix M-01-0013

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
H6 MUON ANGULAR DISTRIBUTION

ANGULAR DISTRIBUTION
VERTICAL PLANE
CONE of 15 mrad

ANGULAR DISTRIBUTION
HORIZONTAL PLANE
+ and - mixed
CONE of > 40 mrad
+ wide background
USE MUON TRAIL SEGMENTS TO PREDICT POSITIONS in ROW OVERLAP POINTS (TAKE ALWAYS MIDDLE OF SEQUENCE)

RESIDUAL DISTRIBUTION

RANGE ± 2.5 µm $\sigma = 0.8$ µm
TIMEPIX-TOT in H6 PION BEAM

NOTE:
+ DELTA RAYS
+ BRAGG PEAK in ENERGY DEPOSIT at END of TRAILS

JOHN IDARRAGA
DOMINIC GREIFFENBERG
ERIK HEIJNE
DELTA ELECTRONS in SILICON

June 2007

INCIDENT from RIGHT

BEAM

TIMEPIX MODE TOT

JOHN IDARRAGA
DOMINIC GREIFFENBERG
ERIK HEIJNE
MEASUREMENTS with MIPs in Si TIMEPIX (2007)

MUONS H6 in EHN1

June 2007

INCIDENT from RIGHT

BEAM

ANALYZED TRAIL

JOHN IDARRAGA
DOMINIC GREIFFENBERG
ERIK HEIJNE
TIMEPIX-TOT in H6 PION BEAM

SAME FRAME ENLARGED, DIFFERENT FULL SCALE

M.I.P. TYPICALLY DEPOSITS 200 - 300 eV per um
11-16.5 keV in PIXEL  TOT RANGE  70-95 (1 keV~6)
ARE THERE APPLICATIONS?
3D TECHNOLOGY* MULTILAYER ASSEMBLY

PROVIDES $X$, $Y$, $\Theta_X$, $\Theta_Y$

intersecting position + angular direction
STACKED CUBE

COMPONENTS 'EXIST'

3-D TECHNOLOGY ALREADY APPLIED at LOS ALAMOS

14 mm

40 CHIP LAYERS

700 µm

ELECTRICAL CONNECTIONS + READOUT

SENSOR

COOLING and SUPPORT

25 µm  30 µm

COOLING SHEET

DIAMOND ?

READOUT CHIP

14 mm

14 mm

14 mm

300 µm
3D STACKING
MAJOR EFFORTS in INDUSTRY
3D STACKING TECHNOLOGY

16 Chip Stacking Technology

- 16 Same Die Stack Package Development

- Pad Relocation using WLI
- 30 um Wafer Thinning
- Laser Sawing
- Damage-less Die Pick-up
- 250um Overhang
- 50um Loop Height

SAMSUNG at ISSCC 2007
SUPER ADVANCED TECHNOLOGY

TSUKUBA  ASET  K. Takahashi et al, Microel. Rel. 2003

Fig. 2. 3D LSI chip stacking structure.

INCREASE of FUNCTIONAL DENSITY  REQUIRES 3D STRUCTURES
MEDIPIX STACKING & TILING: FIRST TRY

- Printed Circuit Board (PCB)
- Cover mounting screws
- Medipix2-sensor assembly
- Wirebonds
- Bias cable
- USB interface

(a) The stacked prototype

JAN VISSCHERS
DAAN BOLTJE
NIKHEF

NIKHEF

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
223  3 beam  1 cosmic
223  3 beam  1 cosmic

E

I flipped
223  3 beam  1 cosmic

E

I flipped
223     3 beam 1 cosmic

E

I flipped
223  3 beam 1 cosmic

E  I flipped
223 3 beam 1 cosmic

E

I flipped
THE ROLE of CMOS TECHNOLOGY STEPS
TRANSISTORS

SMALLER

FASTER

POWER

LITHO

PROPERTIES

WHICH TOOLS & TRICKS
SOI TRANSISTOR LETI

LETI-SOITEC 3.4

SOI TRANSISTOR 18 nm

Fig. 1- TEM cross section of 18nm gate length n-sSOI MOSFET.
SOI TRANSISTOR LETI

LETI-SOITEC 3.4

SOI TRANSISTOR 18 nm + EPITAXIAL Si GROWTH

Fig. 1- TEM cross section

Fig. 2- HRTEM cross-section showing the detail of the channel edge. The Si film thickness is 2.5 nm.
IBM PRODUCTION in 65 nm
TSMC 45 nm
INTEL 45 nm

SOME DATA from
IEEE - IEDM  Washington Dec 2007
TRANSISTORS SMALLER

ITRS ROADMAP NODES  65 - 45 - 32 - 22 - nm

IMPROVEMENT NEEDED

SOME ROADS TAKEN :

< 65 MOBILITY ENHANCEMENT by STRAIN
< 45 LEAKAGE REDUCTION by HIGH k + METAL GATE
< 22 MULTI GATE DEVICES
PROGRESS in LITHOGRAPHY
MASK TECHNOLOGY 130 nm - 35 nm

Optical view of masks (patterns)

<table>
<thead>
<tr>
<th>Year</th>
<th>180 nm</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1998</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2004</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2006</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- No OPC
- Rule/Model Based OPC
- Model Based OPC, SRAF
- AAPSM + trim
- Chromeless, SRAF

Next gen?
45 nm INTEL: BETTER LITHOGRAPHY

Mrs Kelin KUHN, INTEL 18.2

SRAM CELL

Fig. 7 Cell topology enhancements for mismatch improvement

90nm – tall 1.0 µm²
65nm – wide 0.57 µm²
45nm – wide w/ patterning enhancement 0.346 µm²
45 nm INTEL IN PRODUCTION: NEW GATE

'Effective Oxide Thickness'

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
45 nm INTEL IN PRODUCTION : DRIVE

1V

45 nm TRANSISTORS IMPROVED compared to 65 nm

Fig.11 NMOS $I_{DSAT} \text{ vs. } I_{OFF}$ shows 1.38mA/μm at 1.0V & 100nA

Fig.10 PMOS $I_{DSAT} \text{ vs. } I_{OFF}$ shows 1.07mA/μm at 1.0V & 100nA
45 nm INTEL IN PRODUCTION

Fig. 4 Diffusion and poly layers of 0.346 μm² 6-T SRAM cell

SRAM CELL

Fig. 16 Cross-section of 8 of the 9 Cu interconnect layers

9 METAL STACK
45 nm TSMC IN PRODUCTION

STRAIN, <110>

Fig. 3 Schematic illustration of strain-optimized CMOS structures, utilizing <110> channel, e-SiGe, SMT and d-CESL.

Fig. 5 The 45nm CMOS Ion-Ioff performance at 1.0V.

Fig. 6 N/P-MOS sub-threshold characteristic at Vd=1.0 & 0.05V.

Fig. 7 N/P-MOS output characteristic.

LOW LEAKAGE

1 V

Instrumentat 2008
45 nm TSMC IN PRODUCTION

SMALL SRAM CELL

Fig. 10 0.242 SRAM bit-cell top-view SEM

9 METAL STACK

Fig. 12 X-TEM of 7+2M BEOL process.
MEDIPIX3

ATTACKS CHARGE SHARING

NEED for MORE TRANSISTORS
CHARGE SPREAD

ANALOG SHARING
IEEE NSS 2006, San Diego

Erik HEIJNE  CERN PH Dept

Instrumentation Division Seminar, BNL 25 June 2008
# PROGRESS in Si SENSORS

DEPENDS on AVAILABLE INDUSTRIAL TECHNOLOGY

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Type</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-D</td>
<td>SINGLE DIODE</td>
<td>1955</td>
</tr>
<tr>
<td>1-D</td>
<td>SEGMENTED DIODE</td>
<td>1960</td>
</tr>
<tr>
<td>QUASI 2-D</td>
<td>DOUBLE-SIDED STRIPS</td>
<td>1965</td>
</tr>
<tr>
<td>TRUE 2-D</td>
<td>CCD/MOS MATRIX</td>
<td>1971</td>
</tr>
<tr>
<td></td>
<td>PIXELS MONO or HYBRID</td>
<td>1989</td>
</tr>
<tr>
<td></td>
<td>PILLARS '3D'</td>
<td>1998</td>
</tr>
<tr>
<td>TRUE 3-D</td>
<td>VOXELS</td>
<td></td>
</tr>
</tbody>
</table>
END