INFN
Sezione di Milano

POLITECNICO DI MILANO
Dipartimento di Elettronica e Informazione

DRAGO Chip:
A 8-channel low-noise CMOS readout circuit for silicon detectors with on-chip front-end FET

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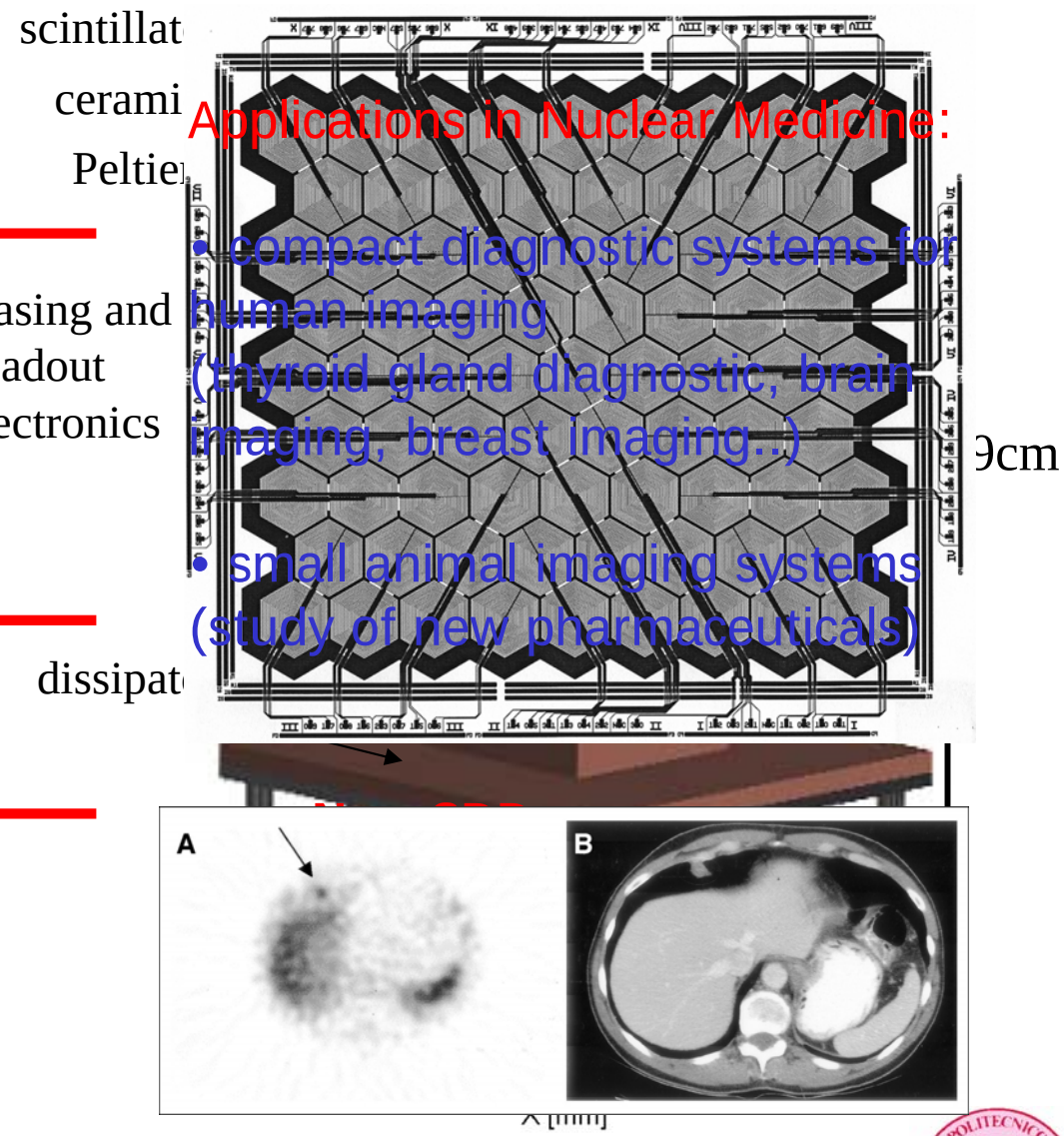
The DRAGO project

(DRift detector Array-based Gamma camera for Oncology)

Development of a new γ-camera with:

- High spatial resolution (<1mm)
- Extreme compactness, positioning ease and versatility
- Based on a 77 element matrix of Silicon Drift Detectors
- Applications in Nuclear Medicine

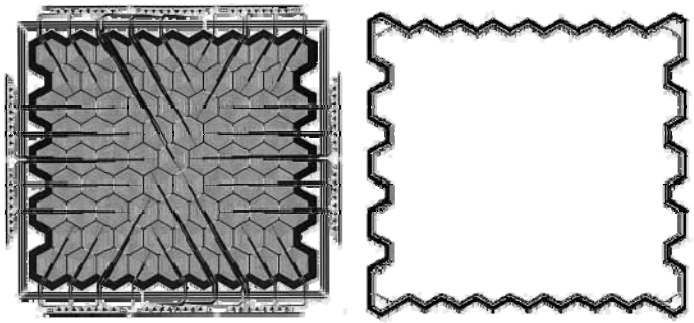


Applications in Nuclear Medicine:

- compact diagnostic systems for human imaging (thyroid gland diagnostic, brain imaging, breast imaging...)
- small animal imaging systems (study of new pharmaceuticals)

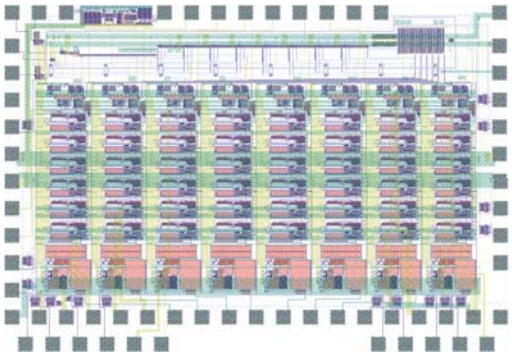
The DRAGO probe

Scintillator Crystal:
CsI(Tl) or $LaBr_3$

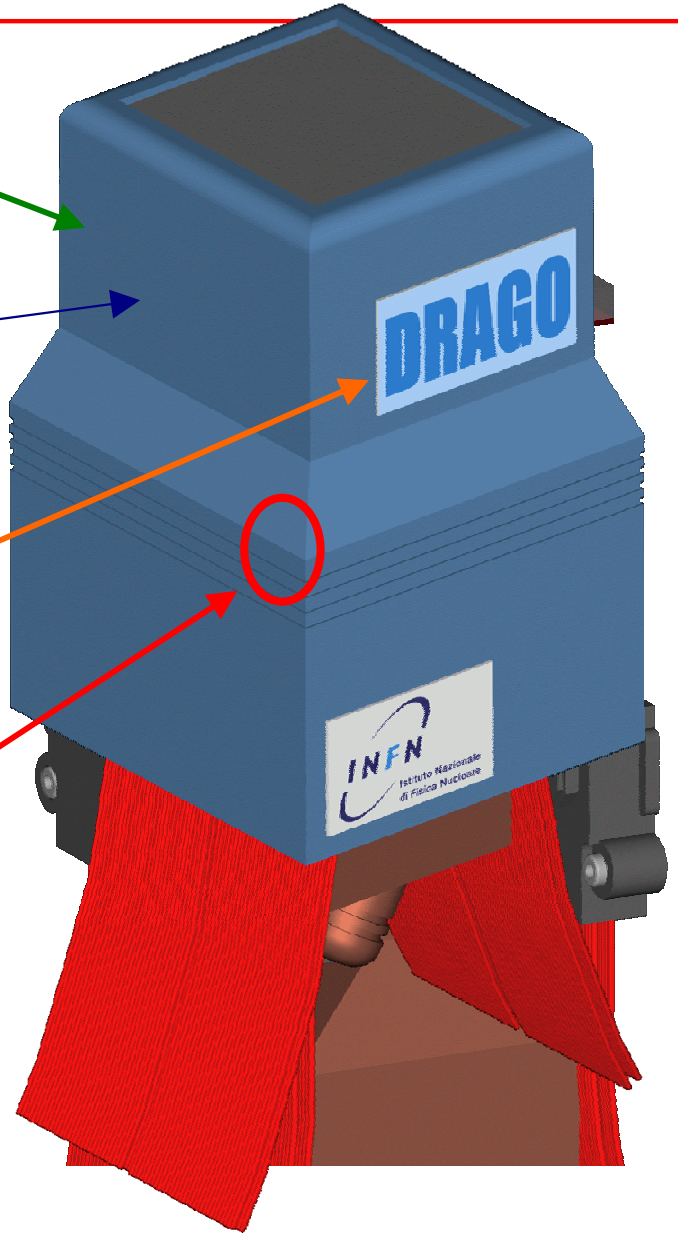


77 element SDD matrix

Peltier Cooler



ten 8-channel readout ASICs

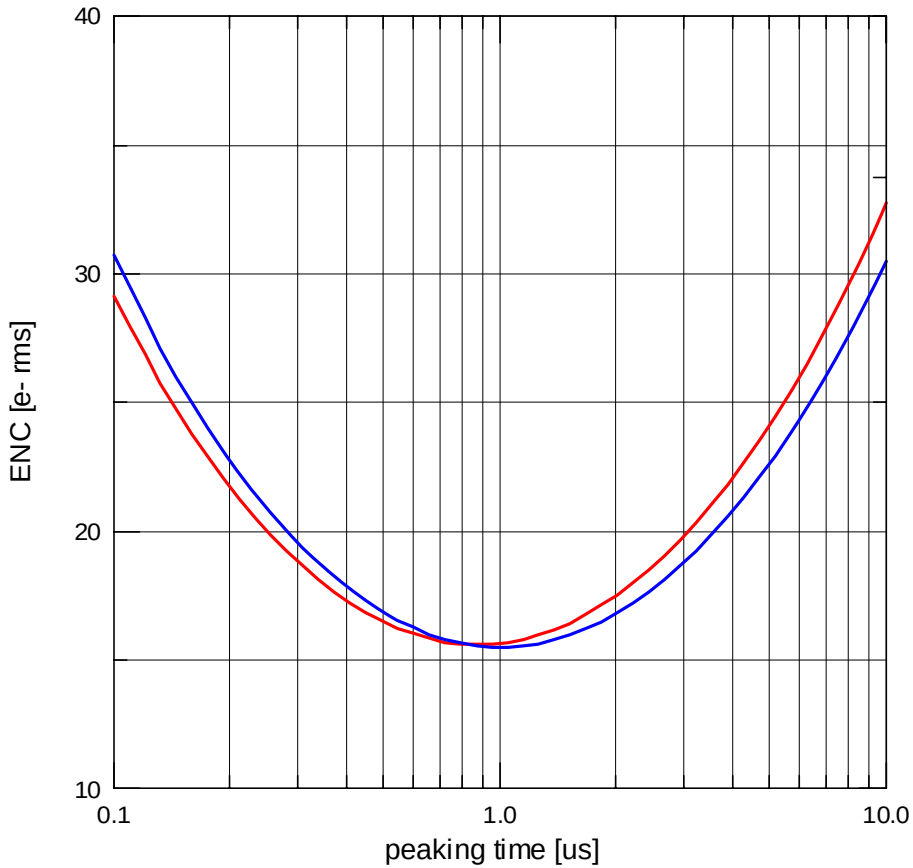


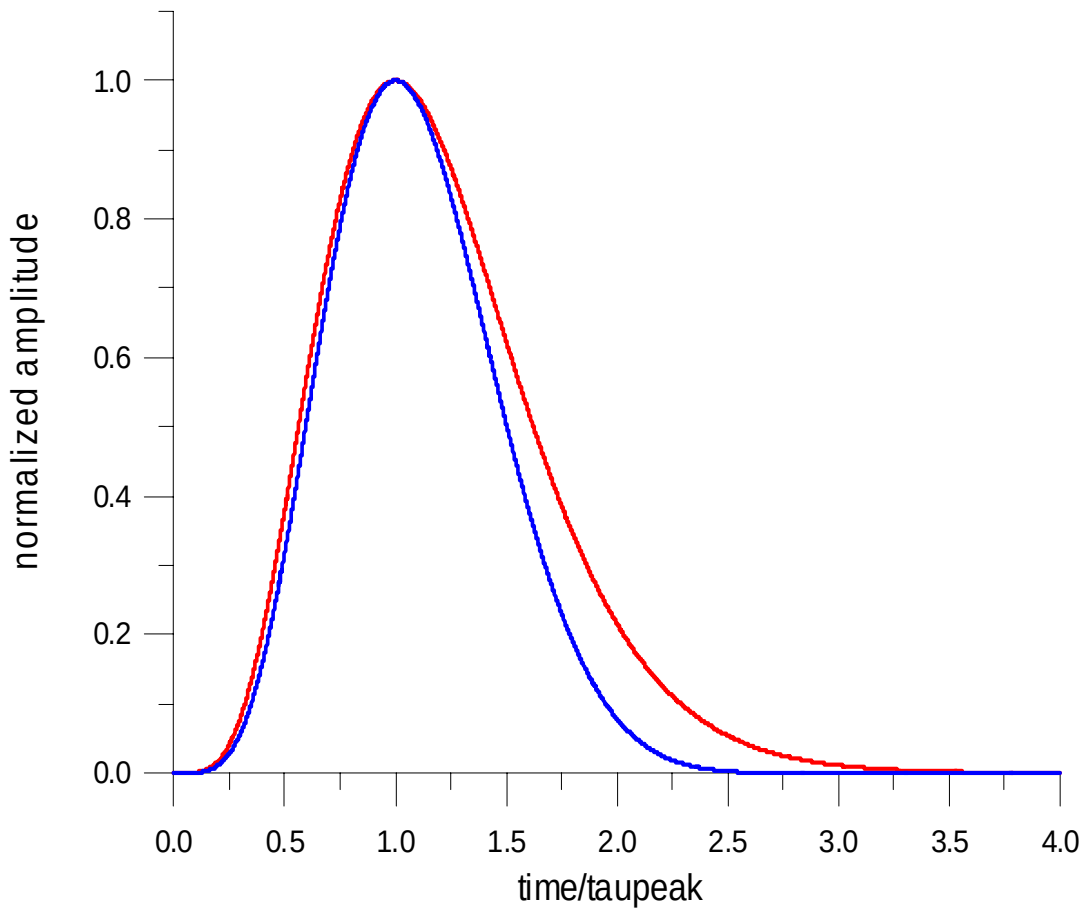
8cm

Drago Chip Specifications

- *8 channels per chip with MUX 8:1*
- *ENC<15 e- r.m.s.*
- *6th order shaper with real poles*
- *4 switchable peaking times τ (1.7-2-4-6μs) for different scintillators*
- *input dynamic range: 2700/5400 e- (2 gains selectable)*
- *linearity <1%*
- *compatibility with the input JFET integrated on the detector chip*
- *Synchronous MUX readout (10Mhz)*
- *self-triggerable, self-resettable*

Real Poles vs. Complex Conjugated Poles

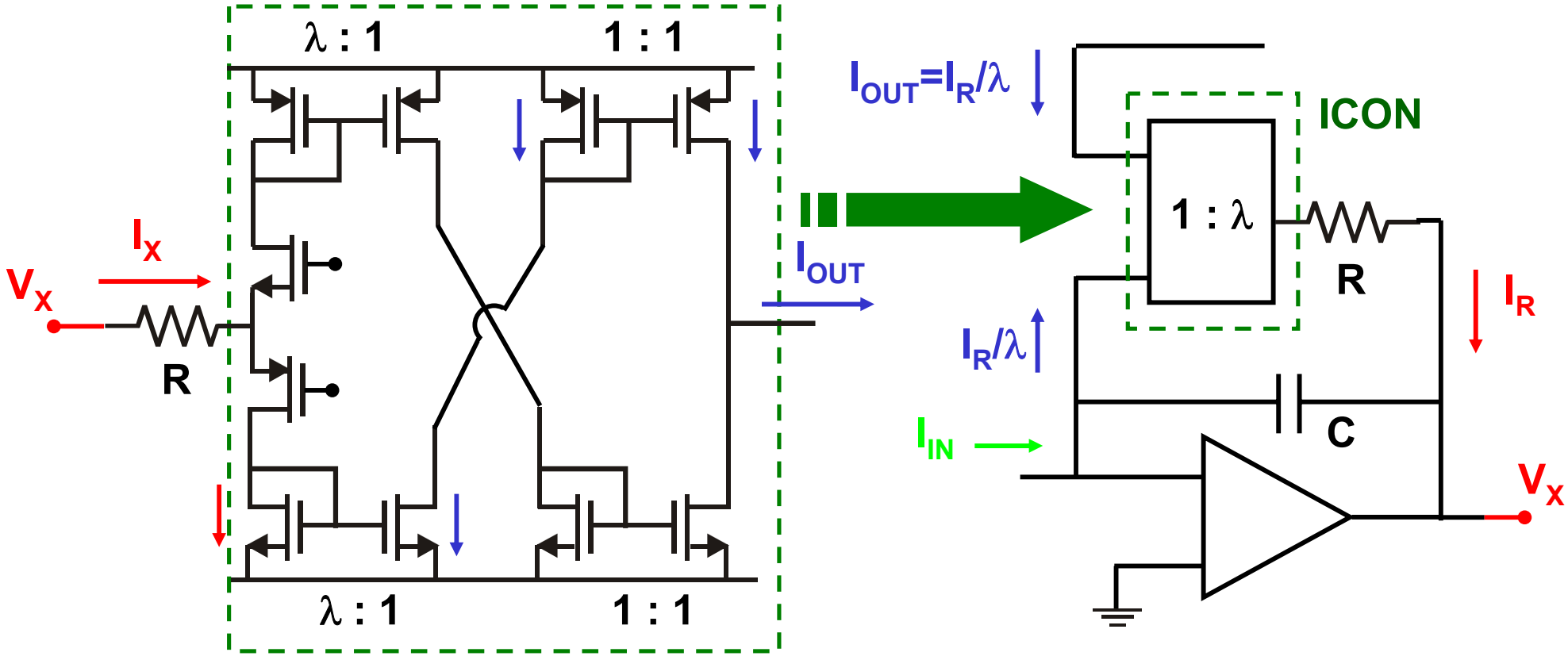




Real Poles

Complex Conjugated Poles

Basic RC Cell: ICON *



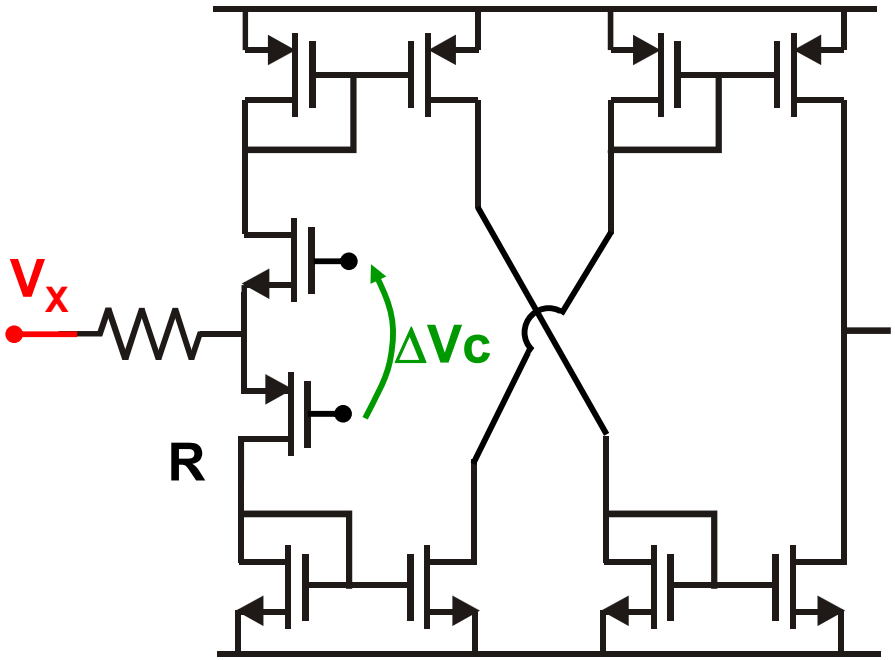
$$I_X = \frac{V_X}{R+1/gm} \approx \frac{V_X}{R}$$

$$\frac{V_X}{I_{IN}} = \frac{I_R}{\lambda} = \frac{V_X}{\left(R+1/gm\right)\cdot\lambda} \approx \frac{V_X}{R\cdot\lambda}$$

$$I_{OUT} = \frac{I_R}{\lambda} = \frac{\left(R+1/gm\right)\cdot\lambda}{1+s\cdot C\cdot\left(R+\frac{1}{gm}\right)\cdot\lambda} \approx \frac{R\cdot\lambda}{1+s\cdot C\cdot R\cdot\lambda}$$

*R.L. Chase, A. Hrisoho, J.P. Richer, *Nucl. Instr. Meth. A409*, pp. 328-331, 1998

Basic RC Cell: Pros and Cons



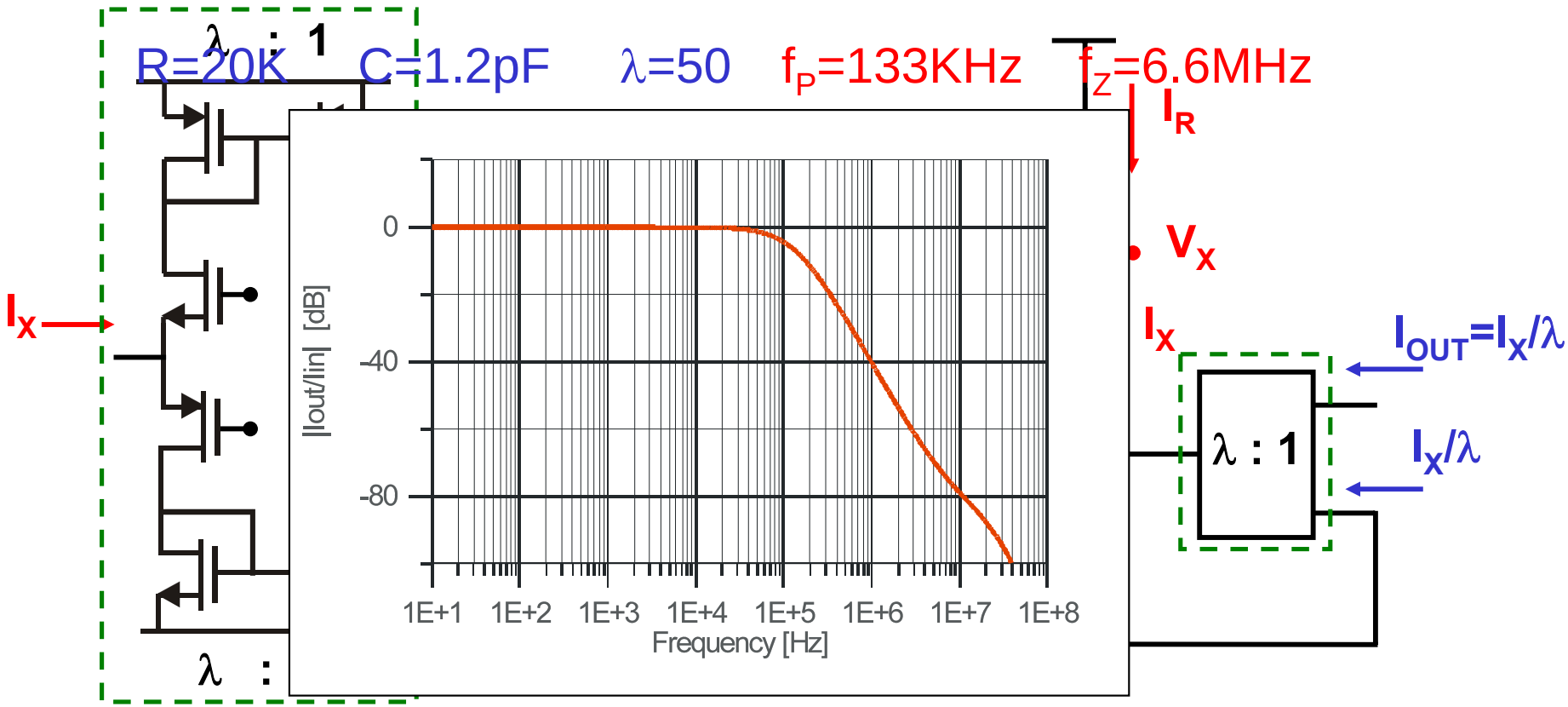
- ICON allows to obtain τ of the order of μs
- ICON accepts input signals of both polarities
- DC current in the mirrors depends only on **ΔVc**, when no signal is applied

it possible to bias the output mirrors with a *current < 100nA*, needed for *low noise applications*

If the DC current of the input MOSFETS is in the range of few μA, the 1/gm is of the order of few KΩ, as the physical resistor R

- It is not possible to design precise and stable time constants
- poor linearity

Proposed RC Cell



$$\frac{V_X}{I_{IN}} = -\frac{R \cdot \lambda}{1 + s \cdot C \cdot R \cdot (\lambda + 1)}$$

$$\tau_p = R \cdot (\lambda + 1) \cdot C$$

$$\frac{I_{OUT}}{I_{IN}} = \frac{1 + s \cdot C \cdot R}{1 + s \cdot C \cdot R \cdot (\lambda + 1)}$$

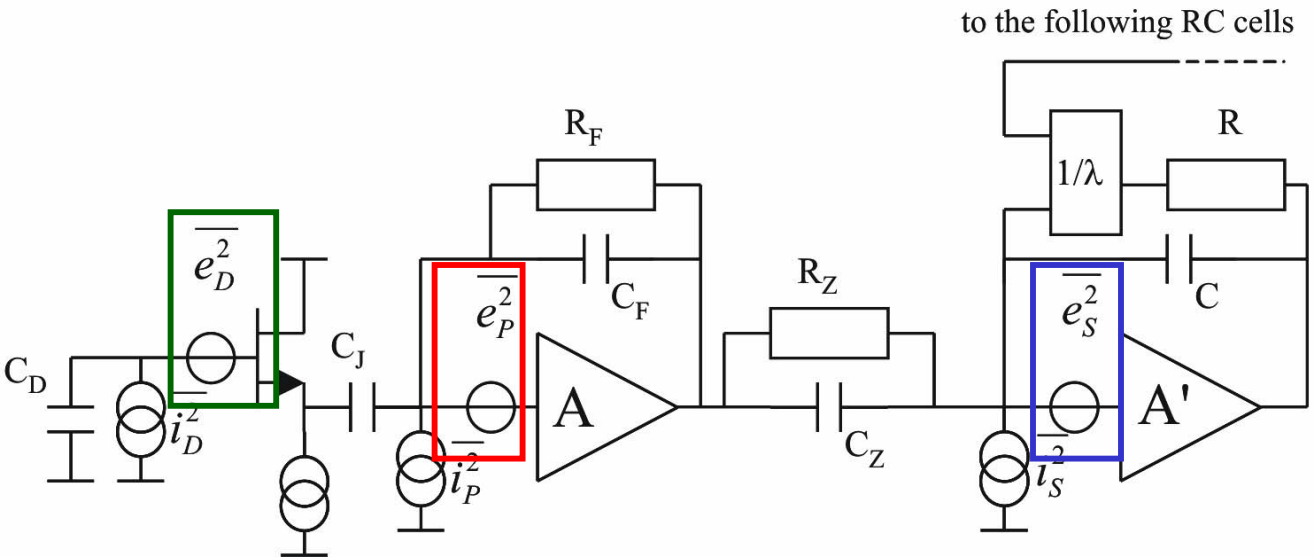
$$\tau_z = R \cdot C$$

Benefits

- time constants of the order of few μs
- Real pole or complex conjugate pole architectures are possible
- Very precise and stable time constants
- High linearity even at the low current needed for noise optimization
- Cascadability
- Compatibility with integrated preamplifier with pole-zero*

*G. De Geronimo, P. O'Connor, "A CMOS Fully compensated Continuous Reset System", *IEEE Trans. Nucl. Science, vol.47, n.4, 2000*

Noise Analysis: series contribution



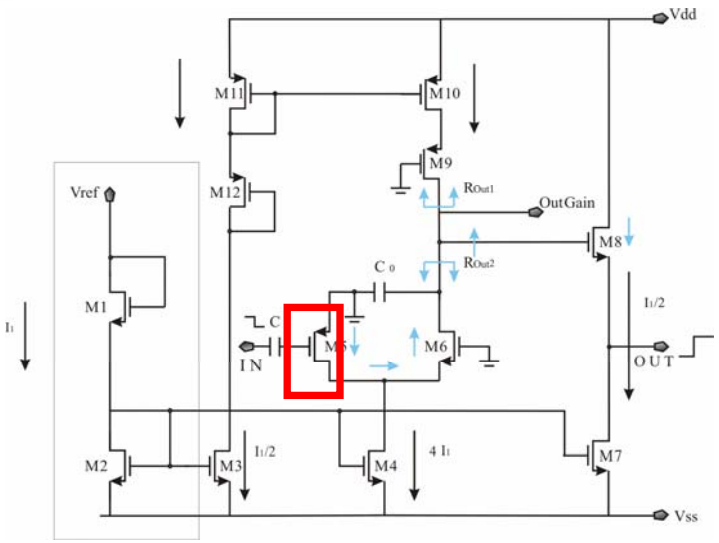
detector series noise

$$\overline{e_D^2} = \frac{2}{3} 4KT \frac{1}{gm} + \frac{A_F}{f}$$

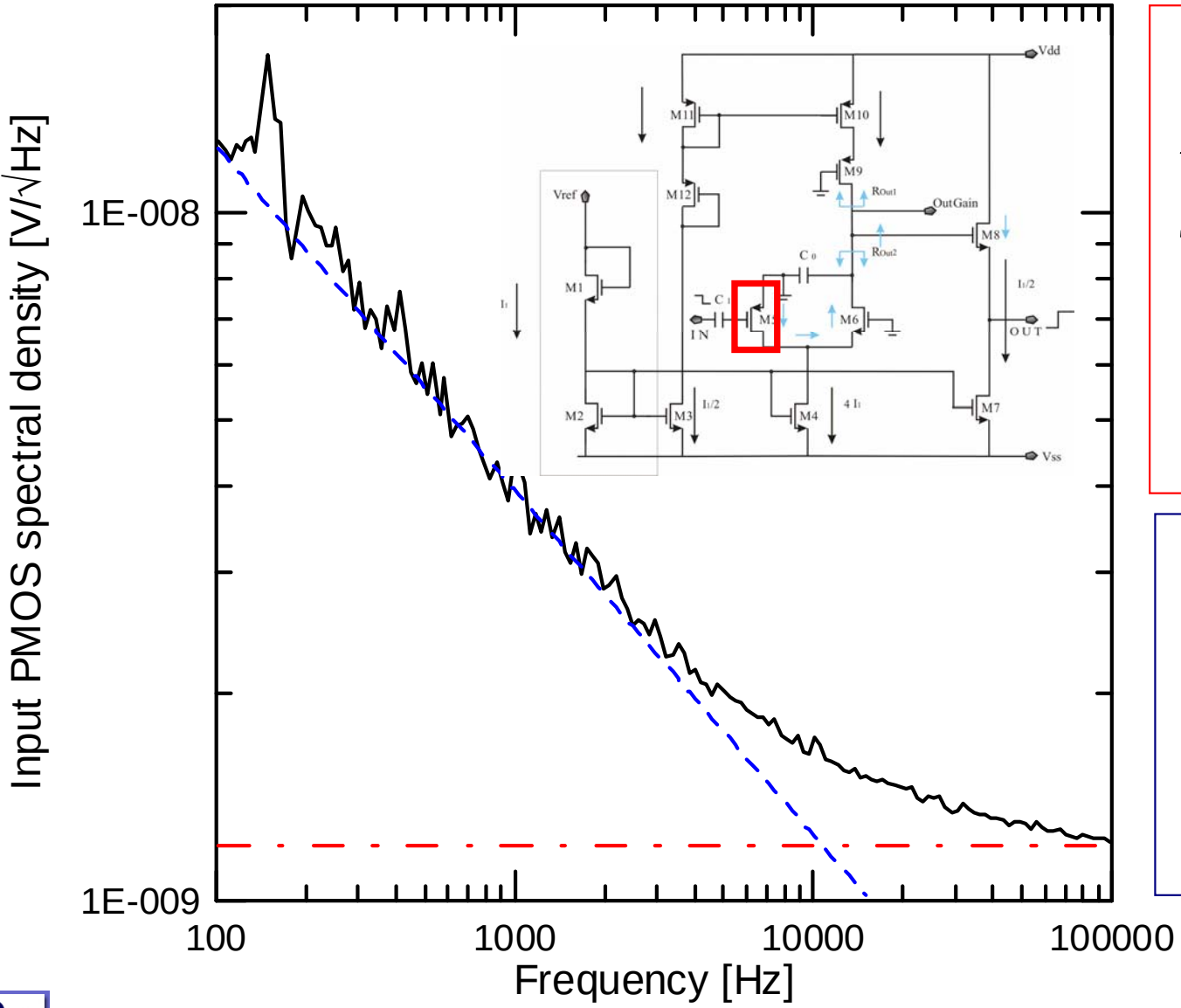
$$\overline{e_{TOT}^2} = \overline{e_D^2} + \overline{e_P^2} + \overline{e_S^2} (C_F / C_J)^2$$

an accurate sizing of the input PMOS is needed

less critical because $(C_F/C_J)^2=1/900$



Series noise



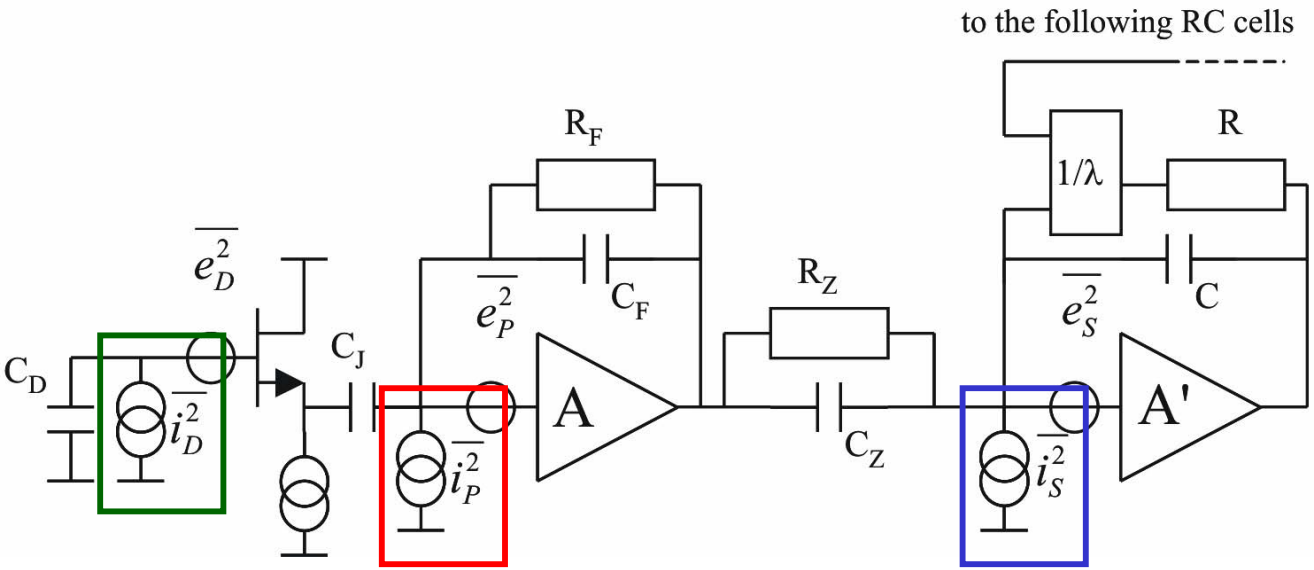
W/L=2000/0.7
Id=700 μA
gm=8.8 mS

$\sqrt{a}$=1.2 nV/√Hz
$\sqrt{a_f}$=1.24·10^{-7} V

JFET integrated on the SDD

$\sqrt{a}$=5.9 nV/√Hz
$\sqrt{a_f}$=2.2 ·10^{-6} V

Noise Analysis: parallel contribution



detector parallel noise

$$\overline{i_D^2} = 2qI_L$$

$$I_L \approx 1pA$$

cooled SDD

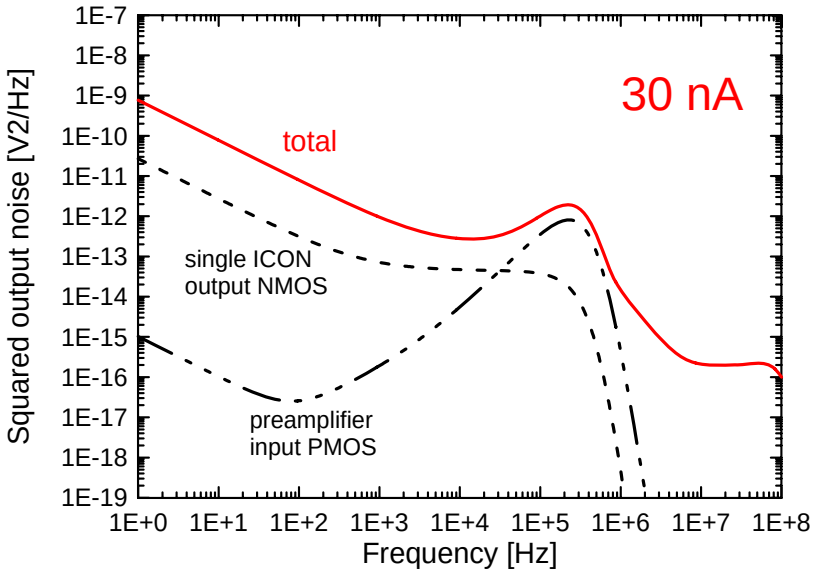
$$\overline{i_{TOT}^2} = \overline{i_D^2} + \overline{i_P^2}(C_D/C_J)^2 + \overline{i_S^2}(C_D/C_J)^2(C_F/C_Z)^2$$

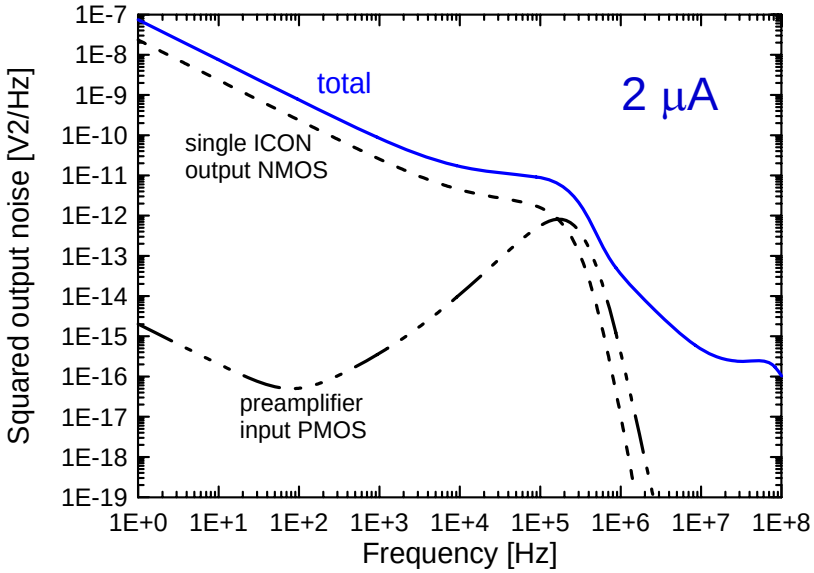
negligible because $R_F \sim (C_D/C_J)^2 \sim 10^{-4}$

$$\overline{i_S^2} \approx 2 \cdot 2qI_0 \qquad I_0 << \frac{I_L}{2}(C_J/C_D)^2(C_Z/C_F)^2 \qquad (C_Z/C_F)^2 \approx 600$$

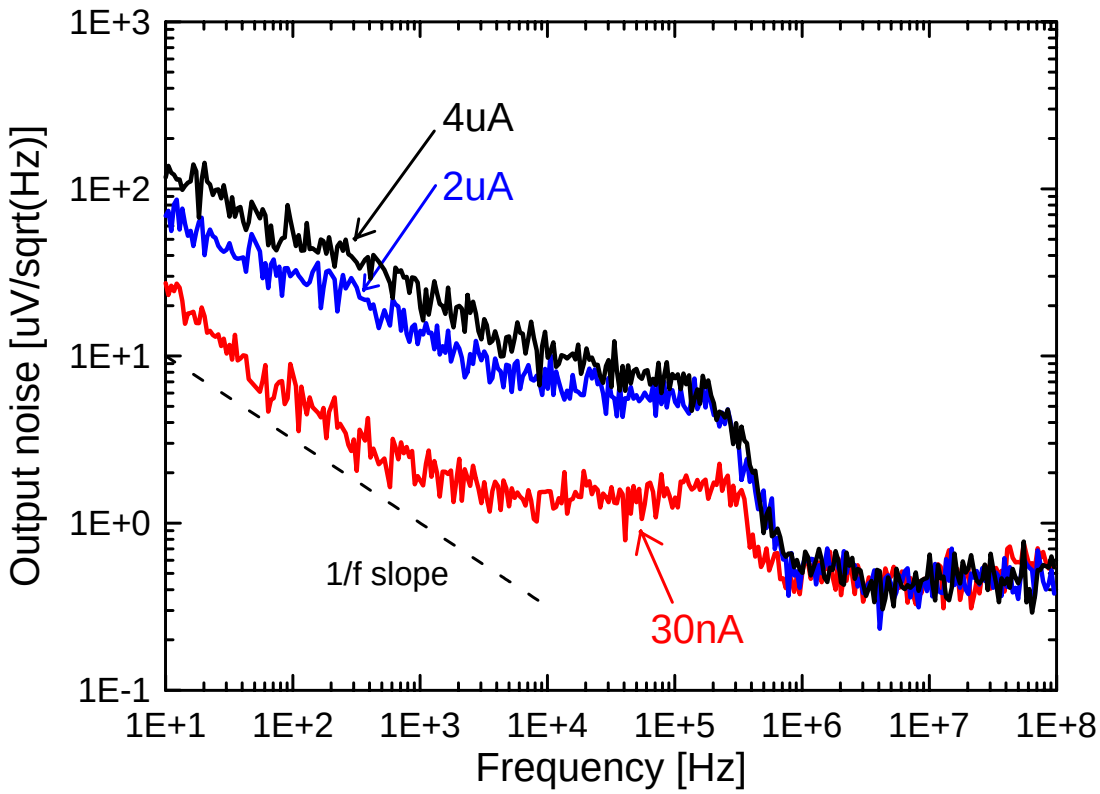
$I_0 << 3\mu A$ and with 6 stages: $I_0 << 250nA$

Noise power density



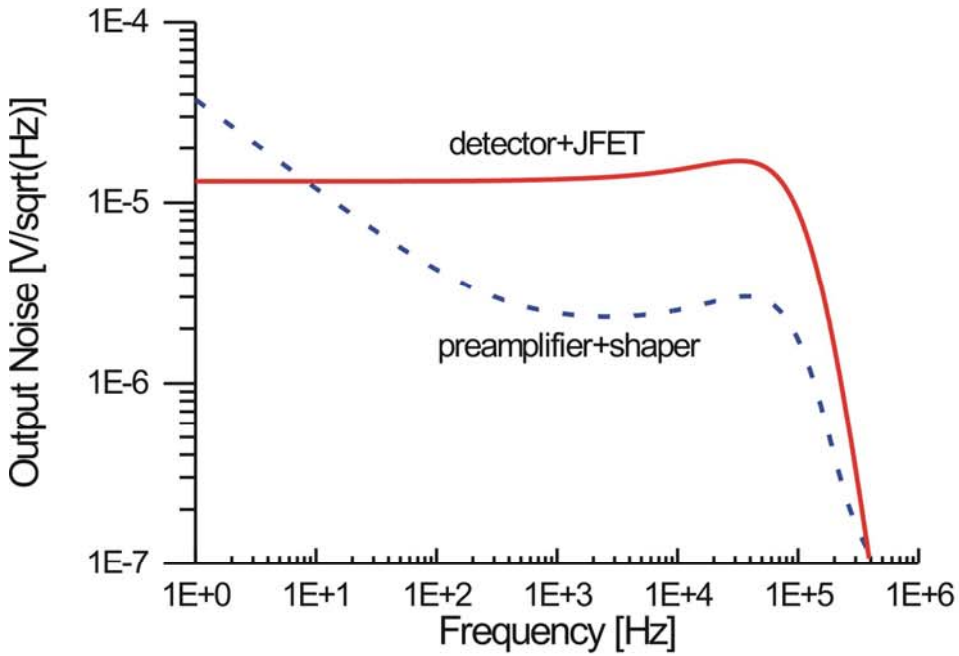


simulations for different values of *bias current of the output mirrors*

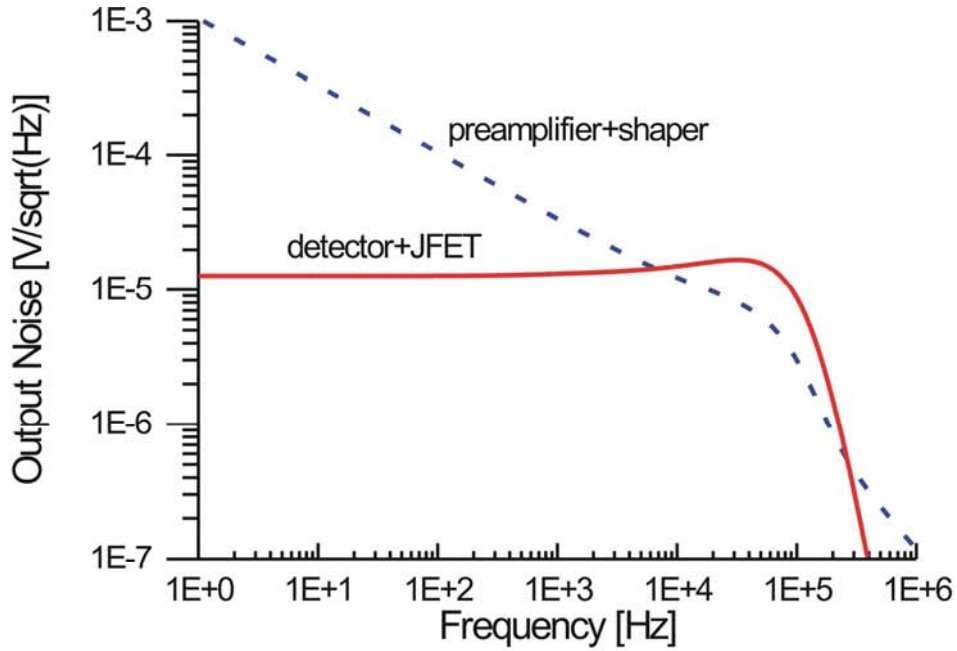


measurements confirm that it is necessary to operate at low current

Noise Analysis: simulation

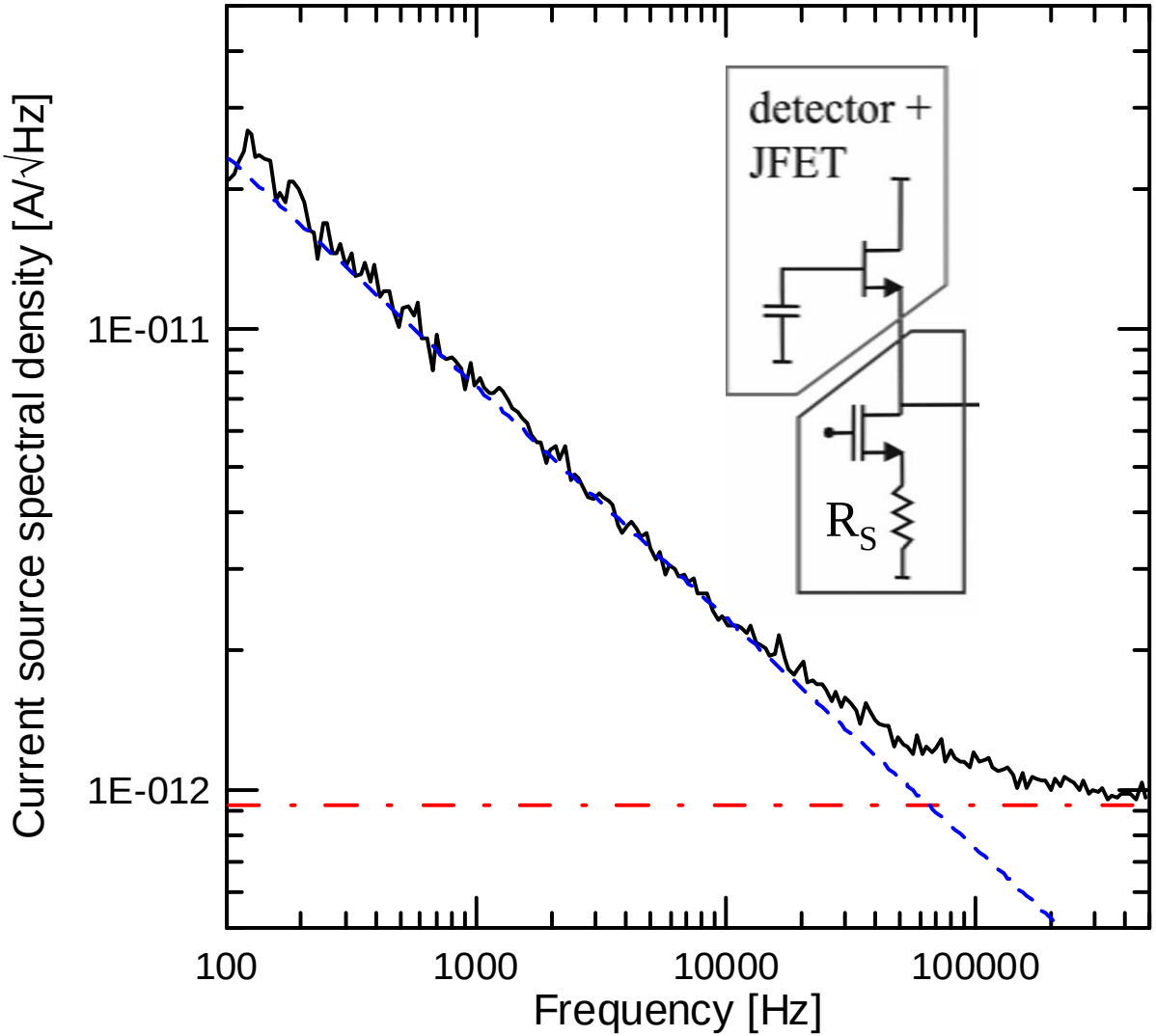


Peaking time = 6μs
I_{bias} output mirror = 30nA
ENC_{TOTAL}= 9.1 e- r.m.s.
$ENC_{DET+JFET}$= 9 e- r.m.s.
$ENC_{PRE+SHAPER}$= 1.7 e- r.m.s.



Peaking time = 6μs
I_{bias} output mirror = 2μA
ENC_{TOTAL}= 11.4 e- r.m.s.
$ENC_{DET+JFET}$= 8.8 e- r.m.s.
$ENC_{PRE+SHAPER}$= 7.2 e- r.m.s.

Current source



$\sqrt{i}=9.1 \cdot 10^{-13}$ A/√Hz

$\sqrt{i_f}=2.36 \cdot 10^{-10}$ A

$\sqrt{4KT/R_S}=9 \cdot 10^{-13}$ A/√Hz

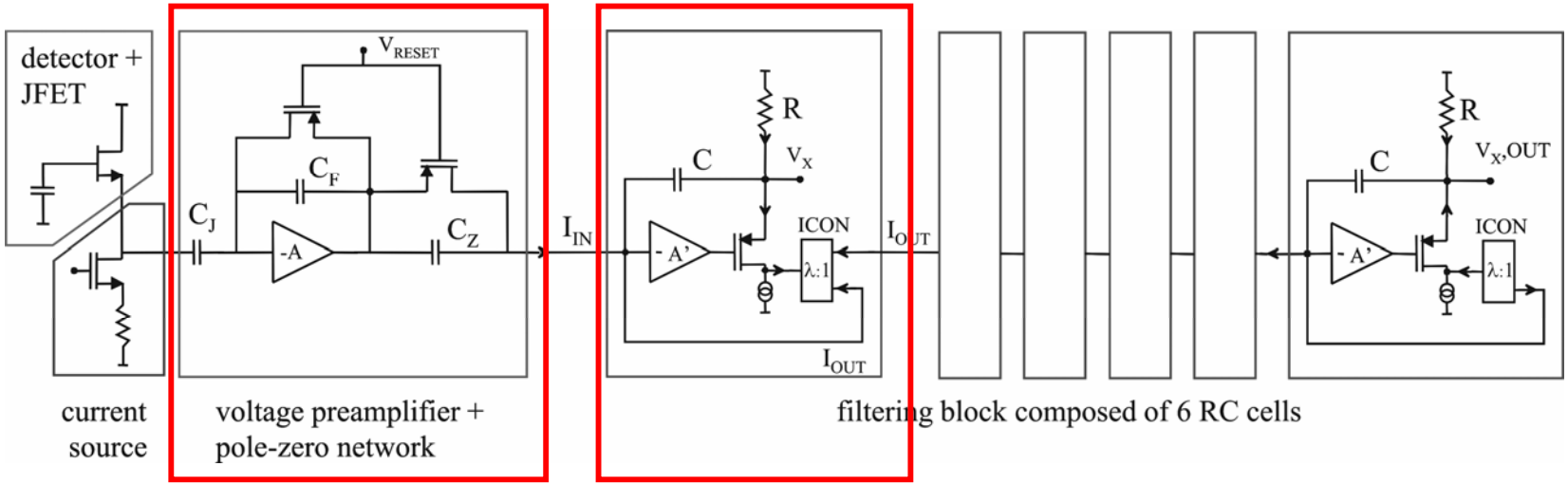
$R_S=20K\Omega$

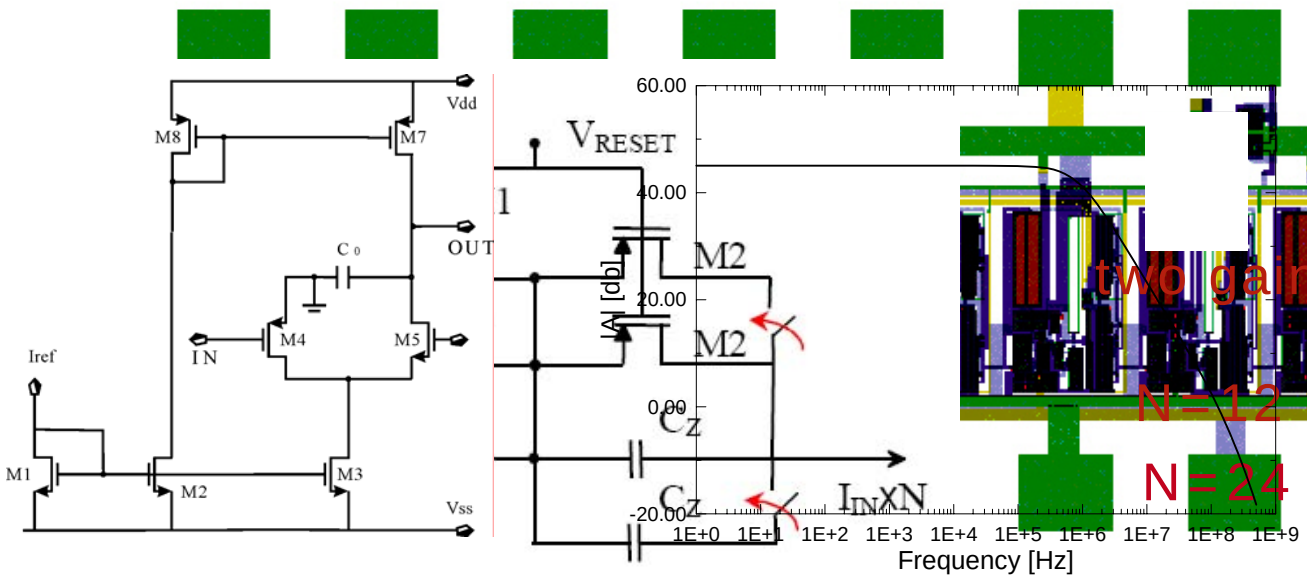
integrated JFET

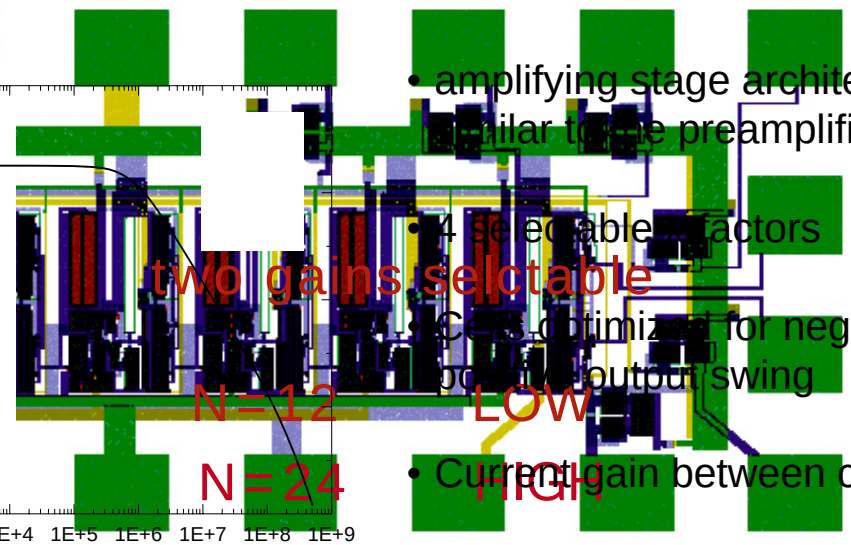
$\sqrt{i}=1.79 \cdot 10^{-12}$ A/√ Hz

$\sqrt{i_f}=6.7 \cdot 10^{-10}$ A

Single channel structure





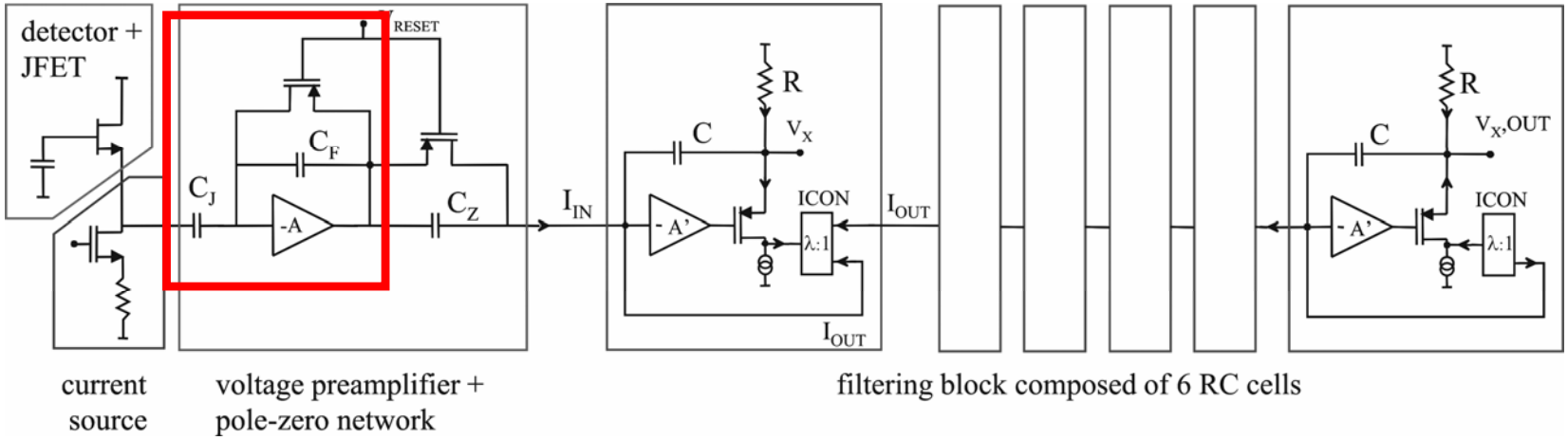


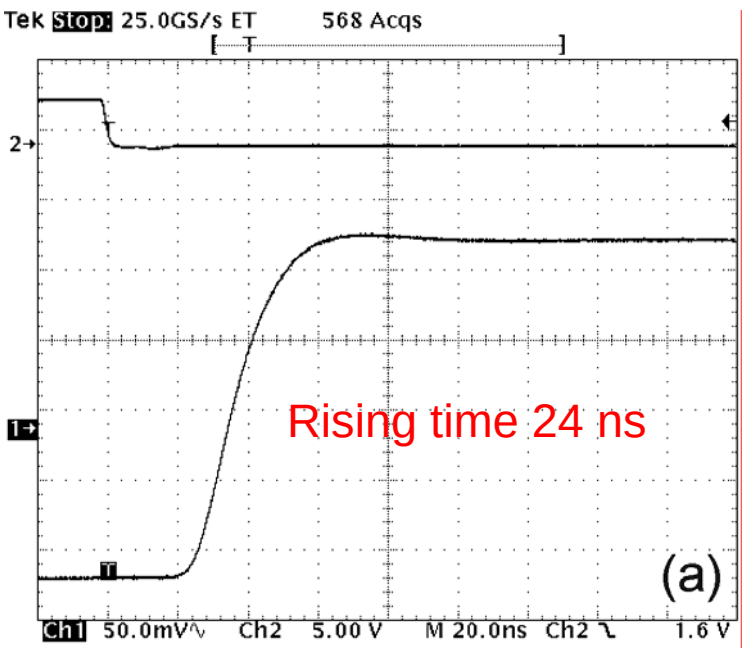
- amplifying stage architecture is similar to the preamplifier
- 4 selectable factors
- Cz's optimized for negative or positive output swing
- Current gain between cells

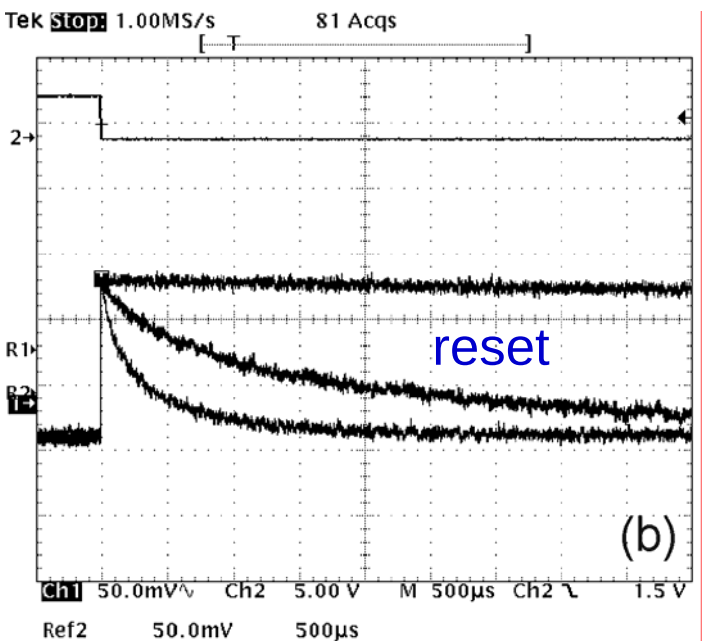
0.35μm 3.3 V CMOS AMS

Gain=110

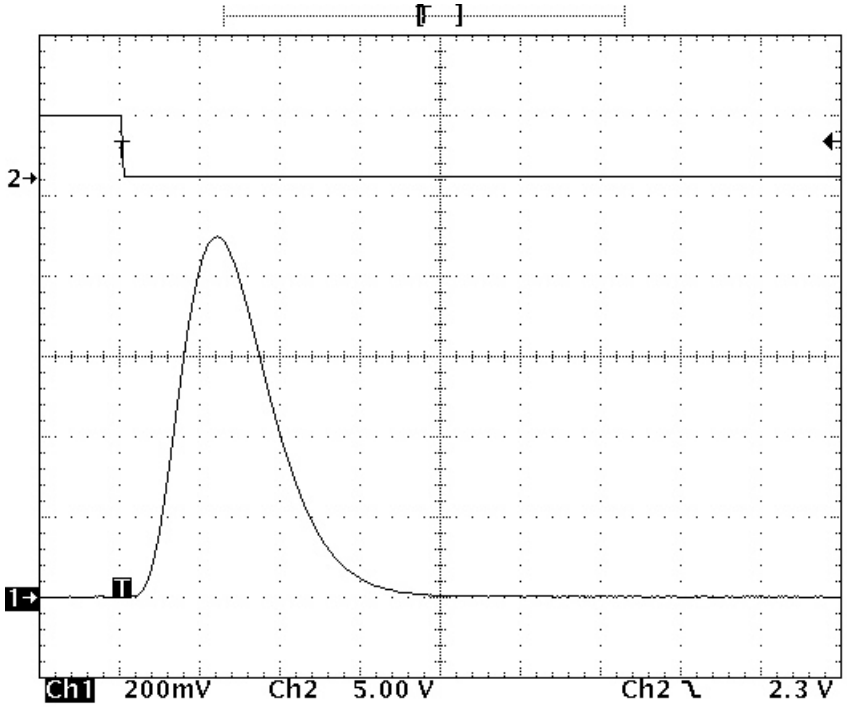
Experimental results: pramplifier



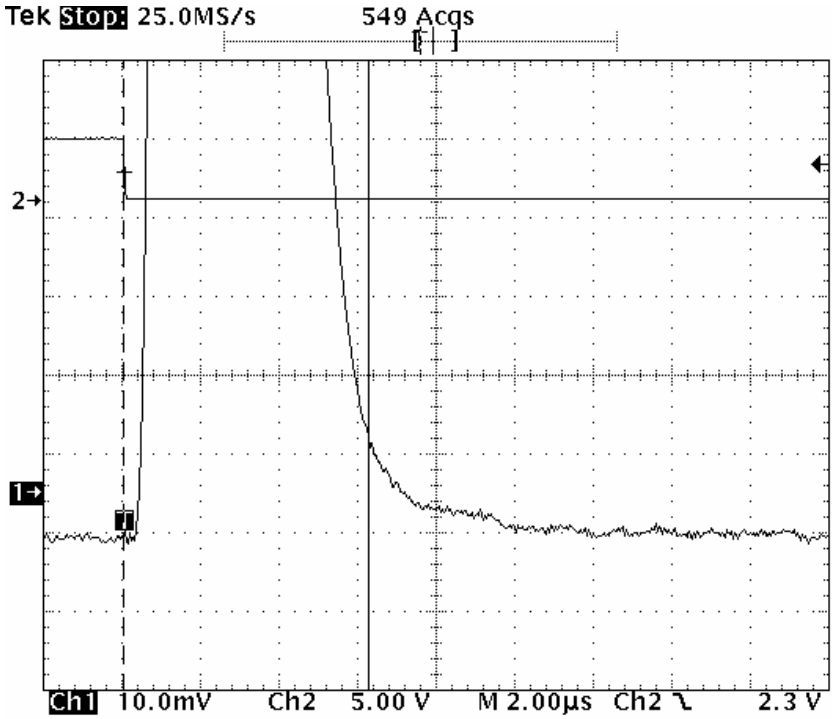




Experimental results: return to zero



Output response with τ_{Peak}=2μs

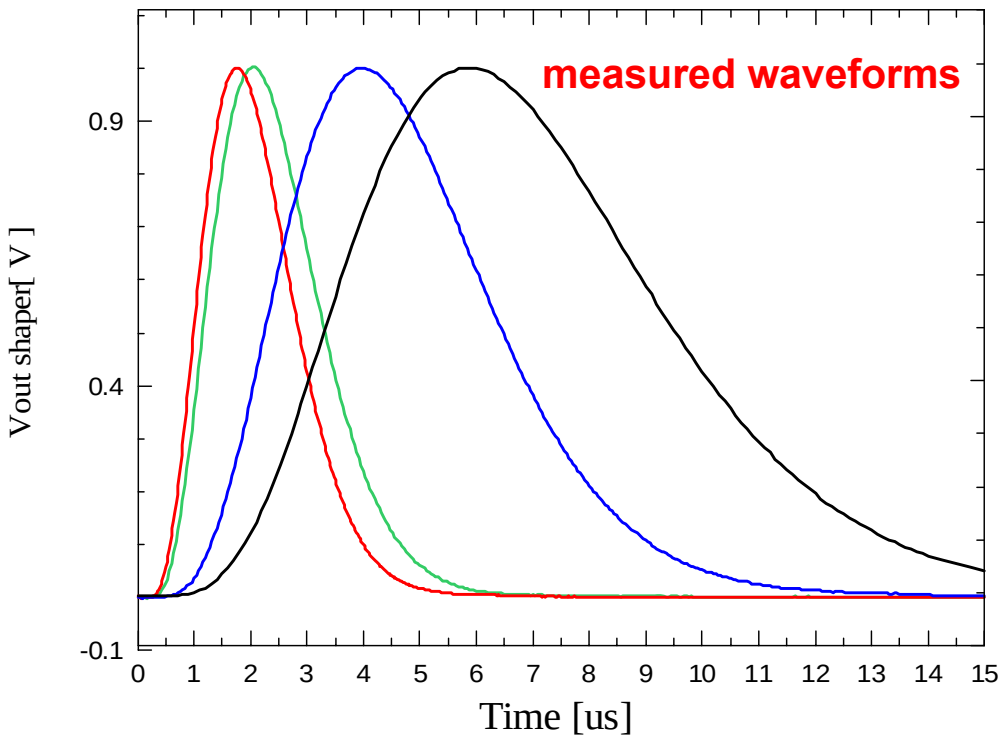


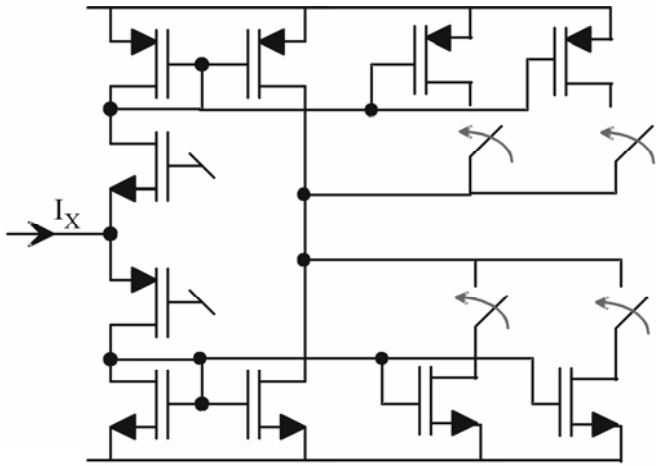
Return to zero of the waveform:

1% is reached in $3 \cdot \tau_{Peak}$

Experimental results: variable peaking times

Physical values:
R=20 Kohm
C=1.2 pF



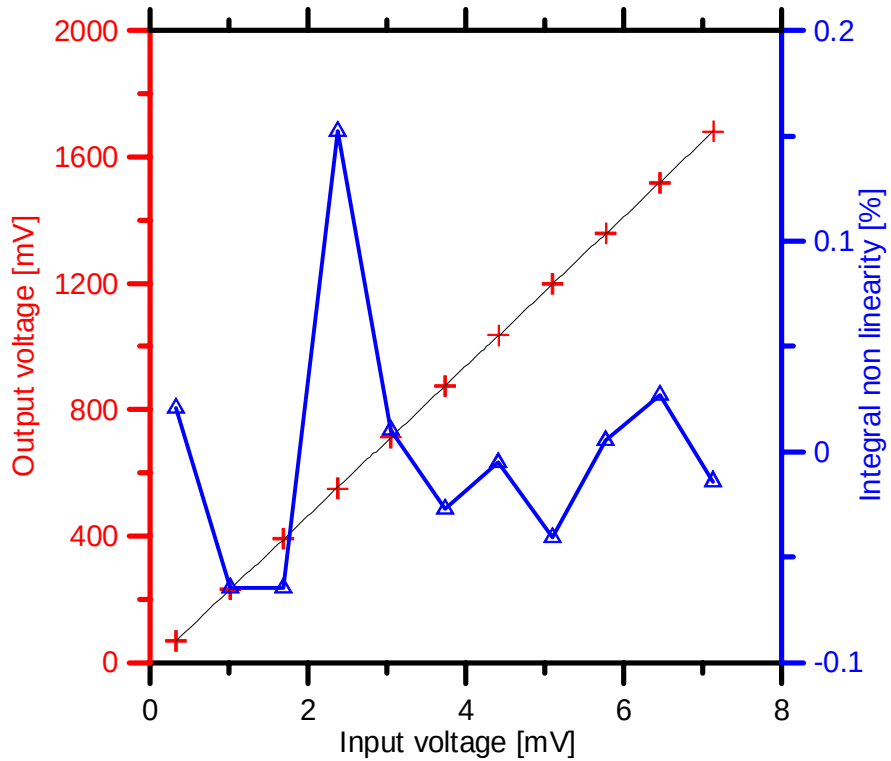


Mirror factors are changed by digital control

λ=14	τ=1.7μs
λ=17	τ=2μs
λ=33	τ=4μs
λ=50	τ=6μs

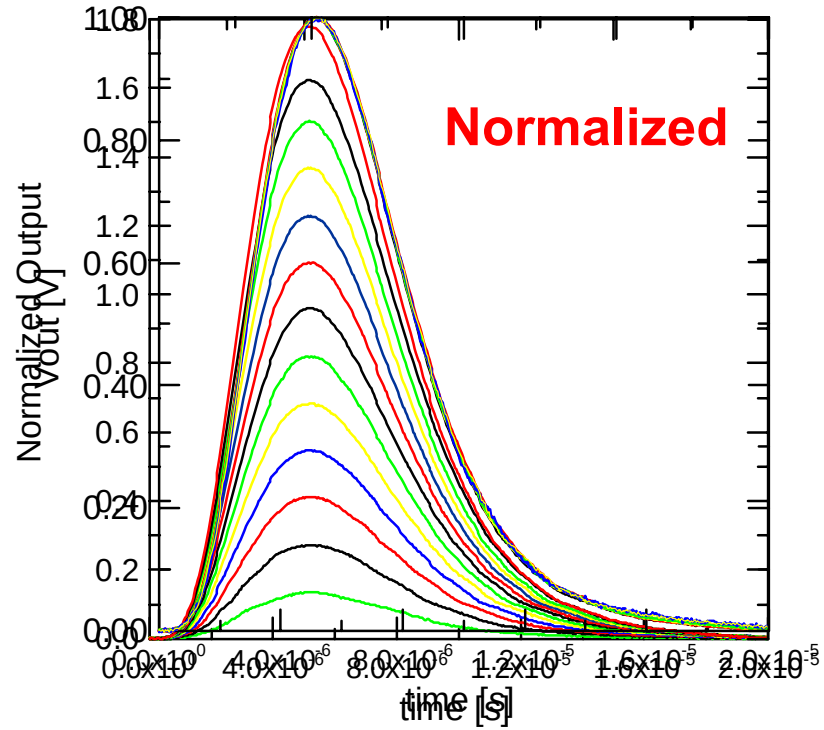
Experimental Results: Linearity

Input dynamic range: **0-8mV**
equivalent to 0-5750 el. with SDD
Output Range: **0-1.6 V**

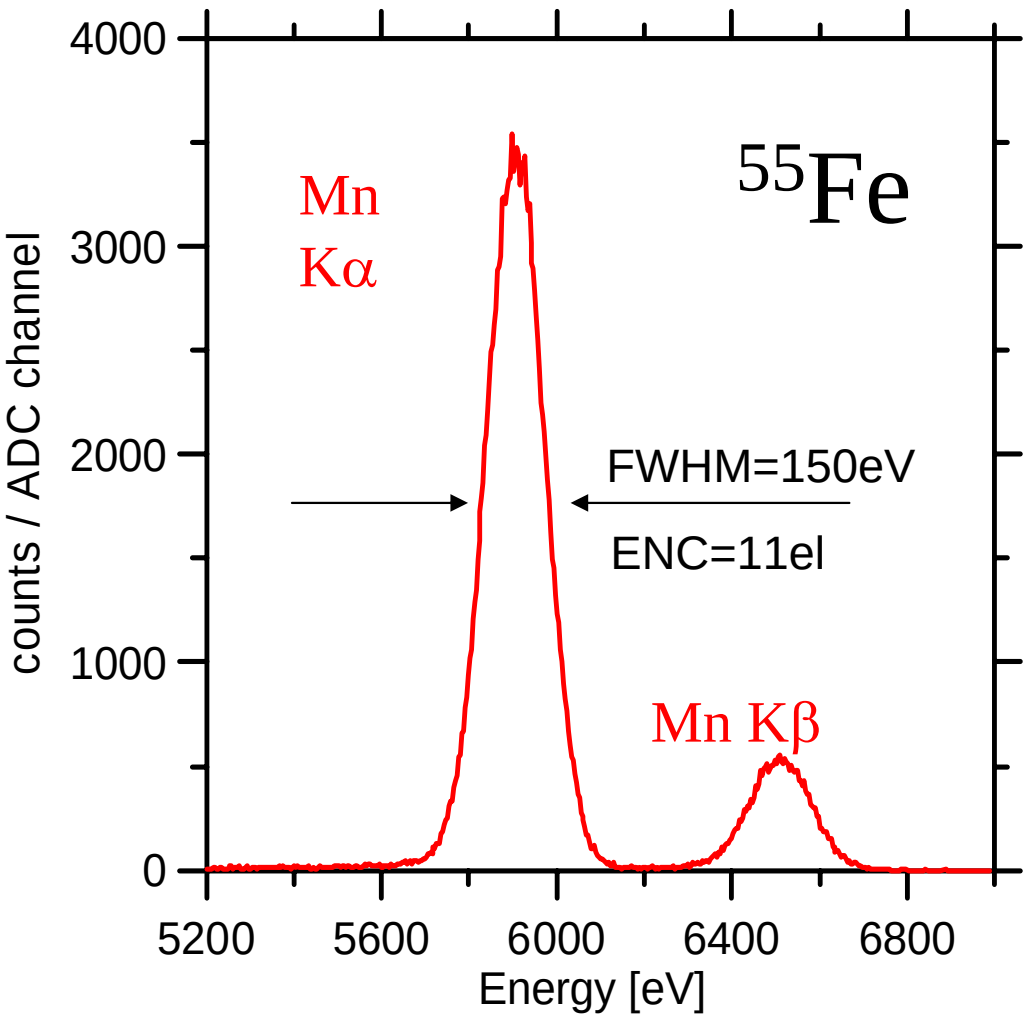


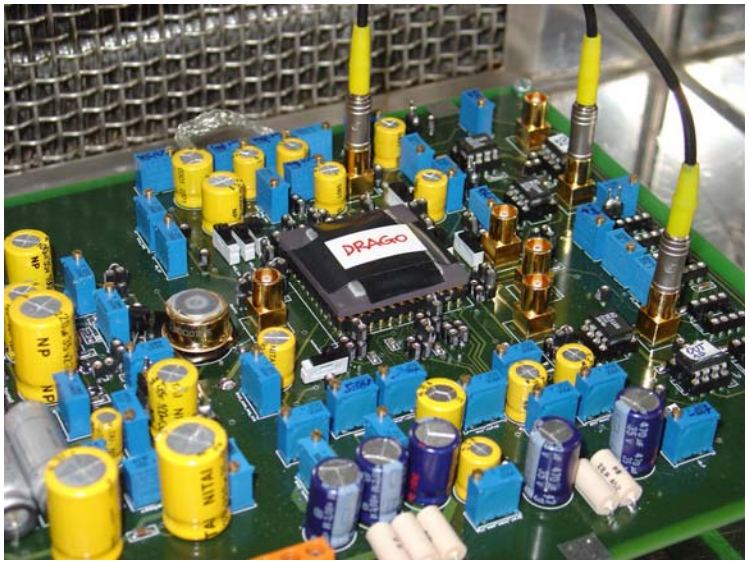
Non linearity ≈ 0.15%

shape stability vs. input signal amplitude



X-ray spectroscopy with SDD

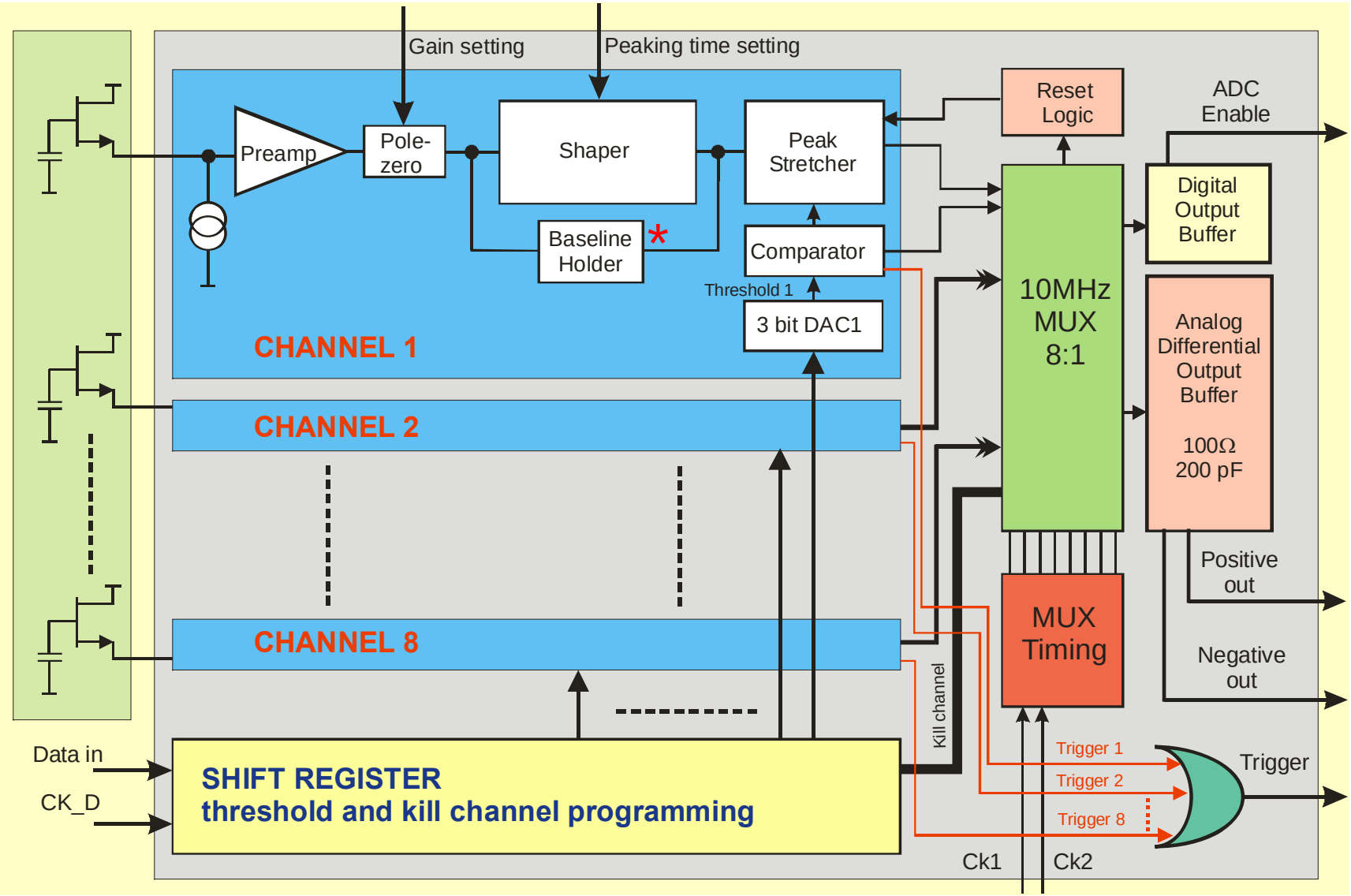




- SDD input capacitance: 115 fF
- SDD @ T=-10°
- τ_{Peak}=1.7 μs
- ENC= 11 el. r.m.s.

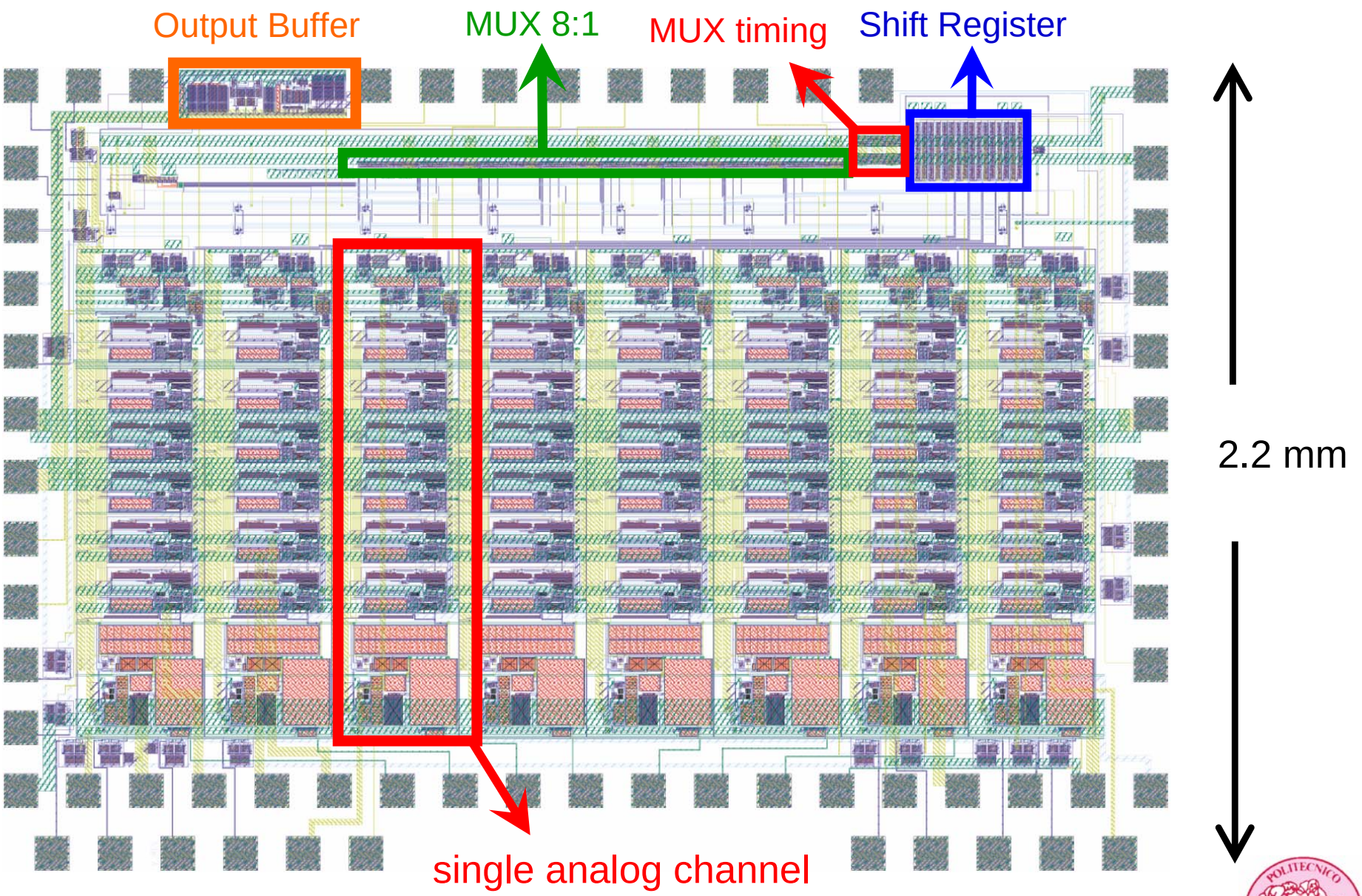
14 el. r.m.s. have been measured with τ_{Peak}=6μs adequate to CsI(Tl) scintillator

8-channel Chip: schematic

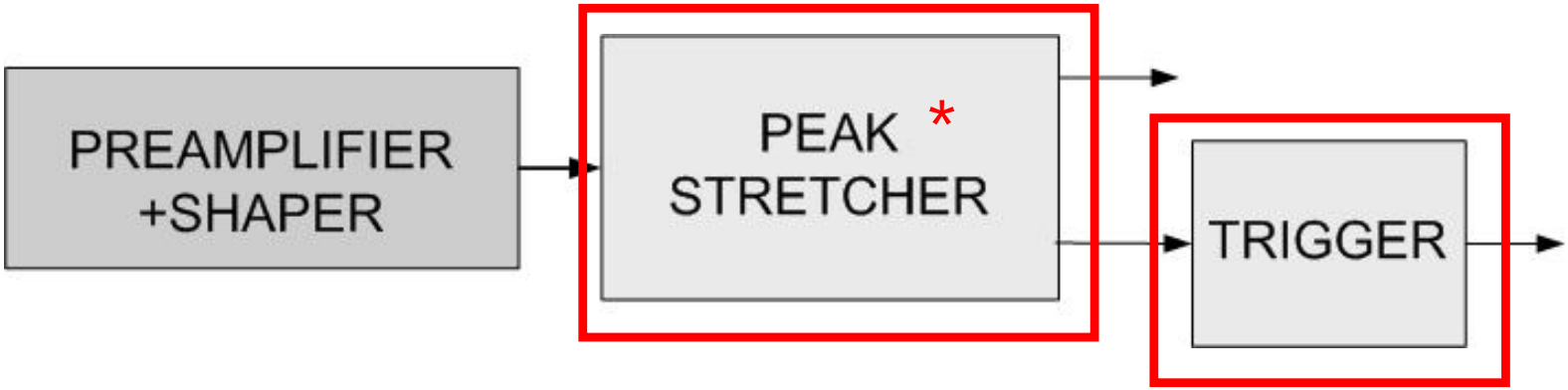


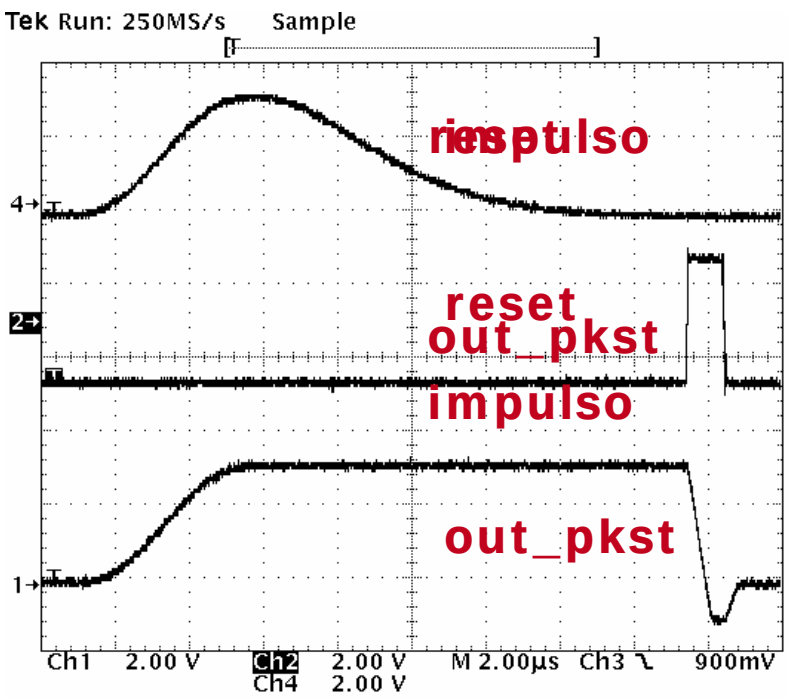
*De Geronimo, O'Connor and Grosholz, *A CMOS Baseline Holder for Readout ASICs*

8-channel Chip: layout

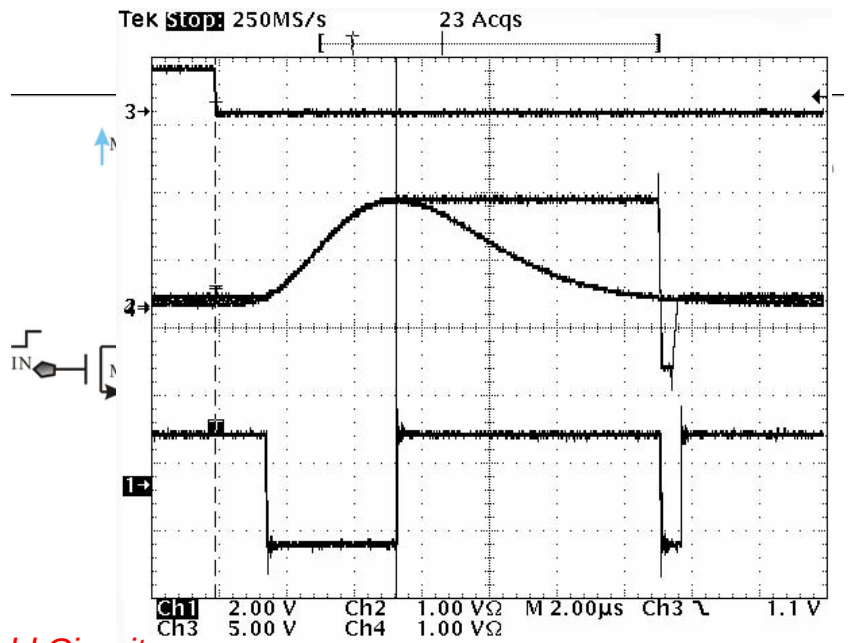


Peak stretcher



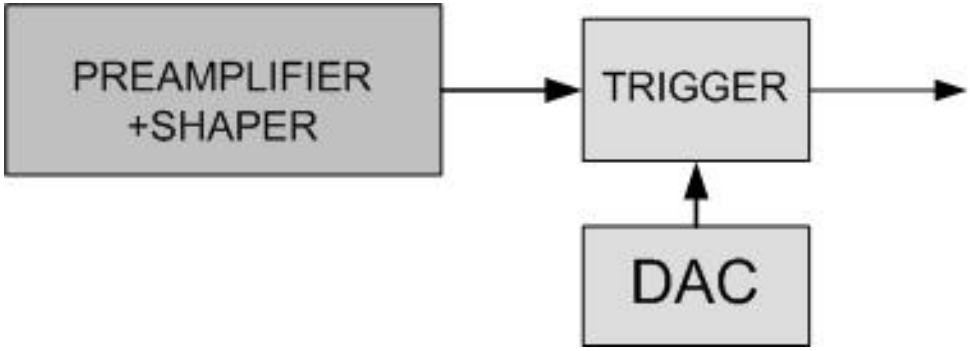


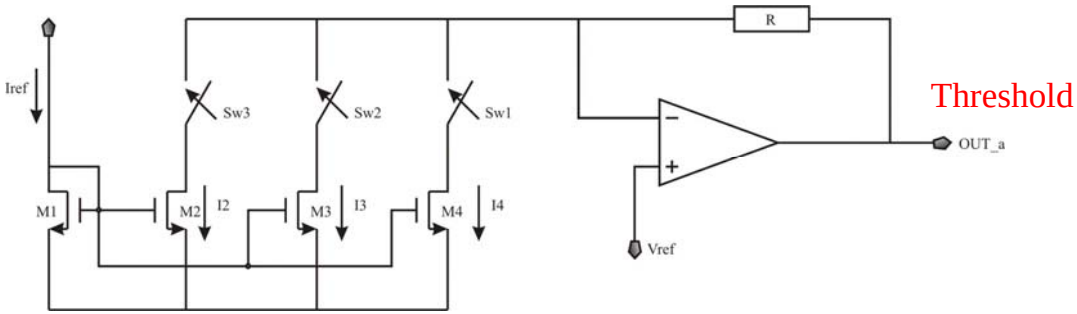
minimum detectable amplitude: 15mV

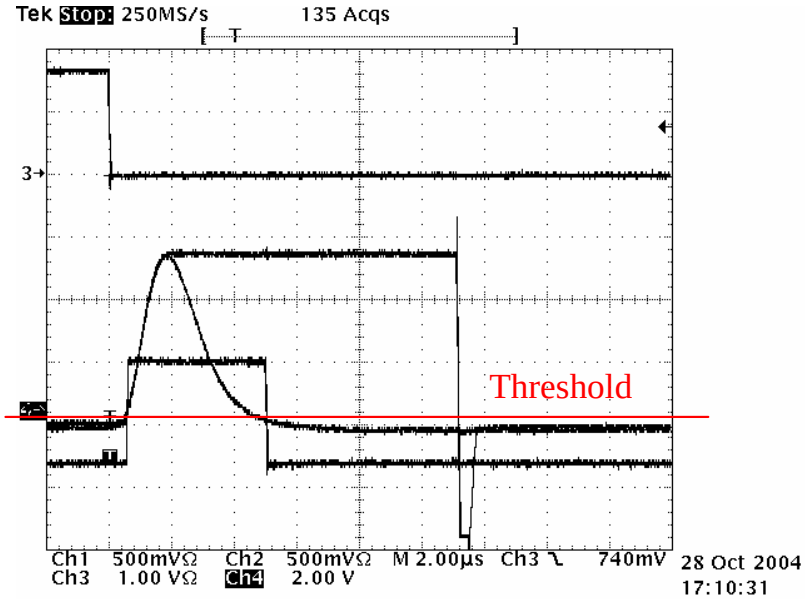


*Kruiskamp, *A CMOS Peak Detect Sample and Hold Circuit*

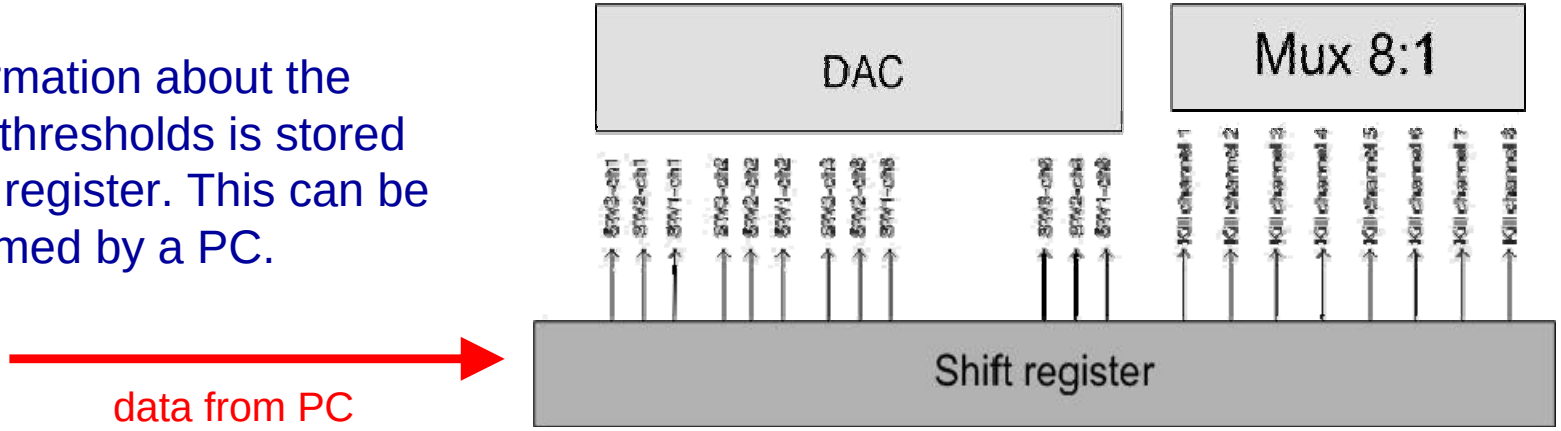
DACs and Shift Register



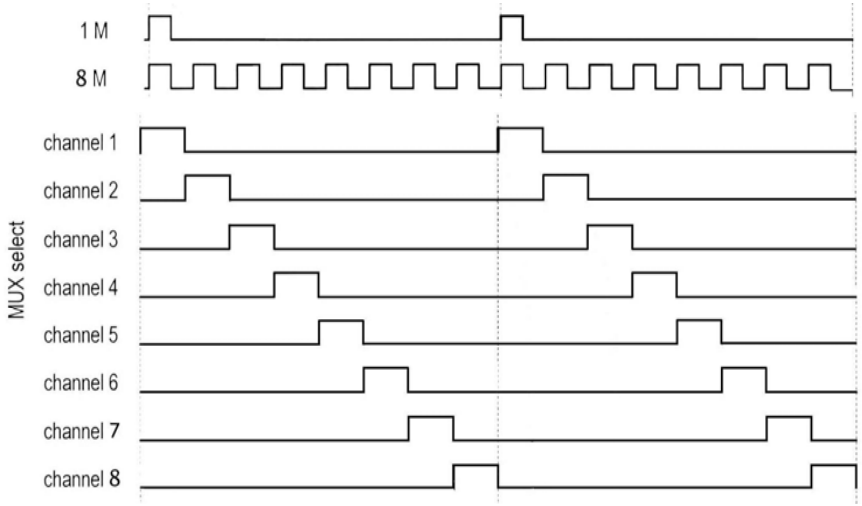


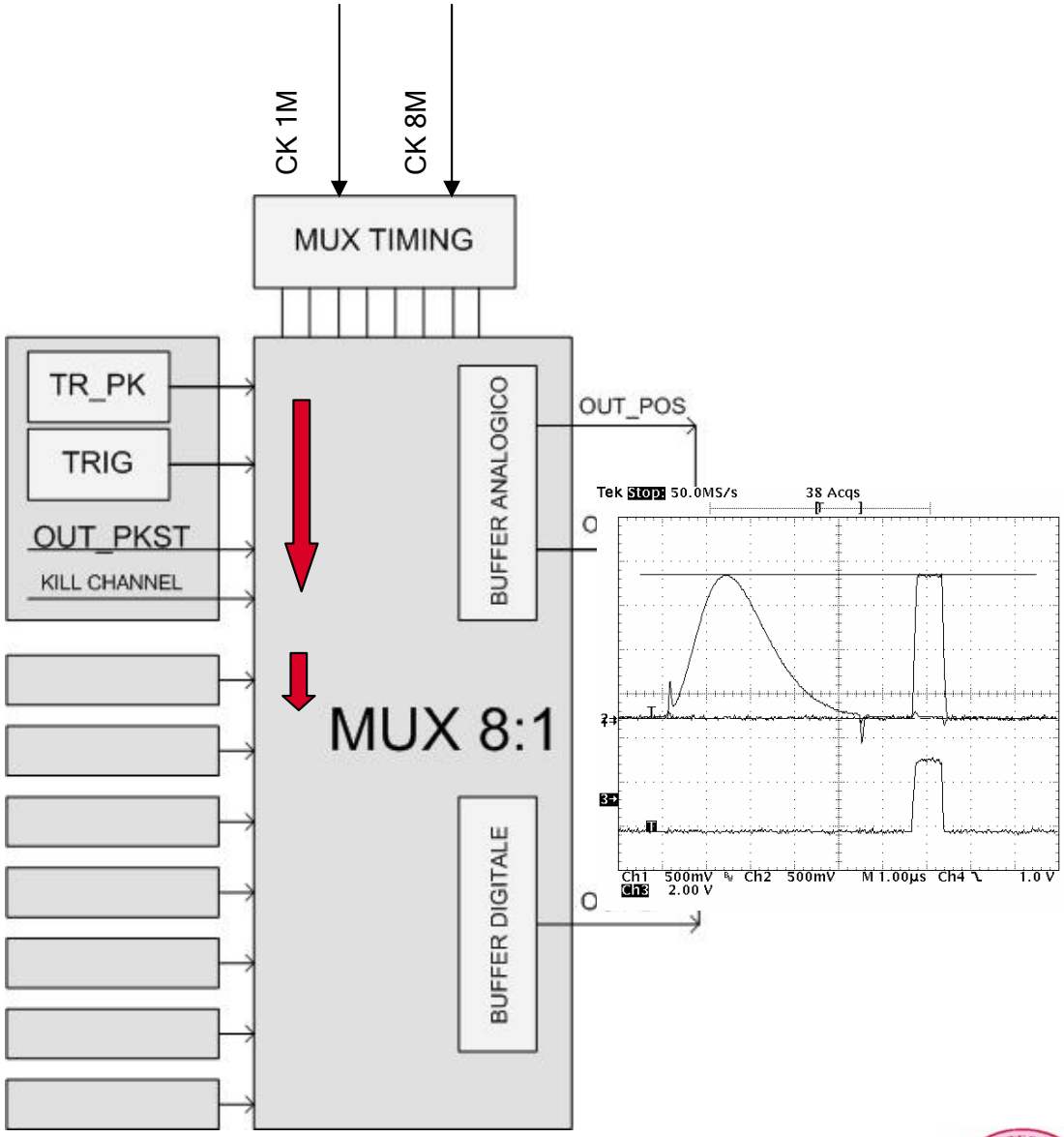


The information about the different thresholds is stored in a shift register. This can be programmed by a PC.



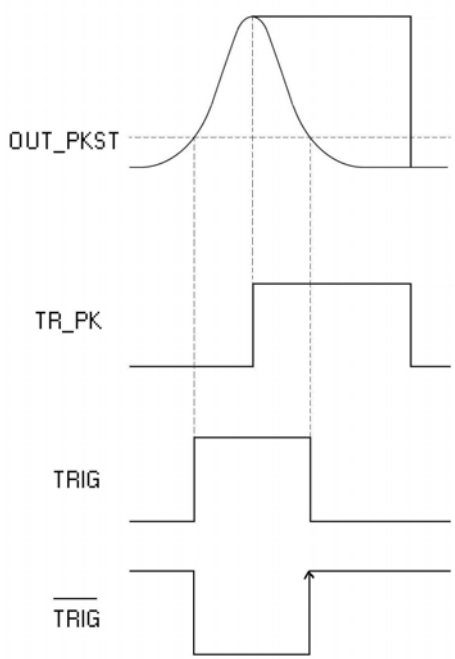
The 8:1 MUX



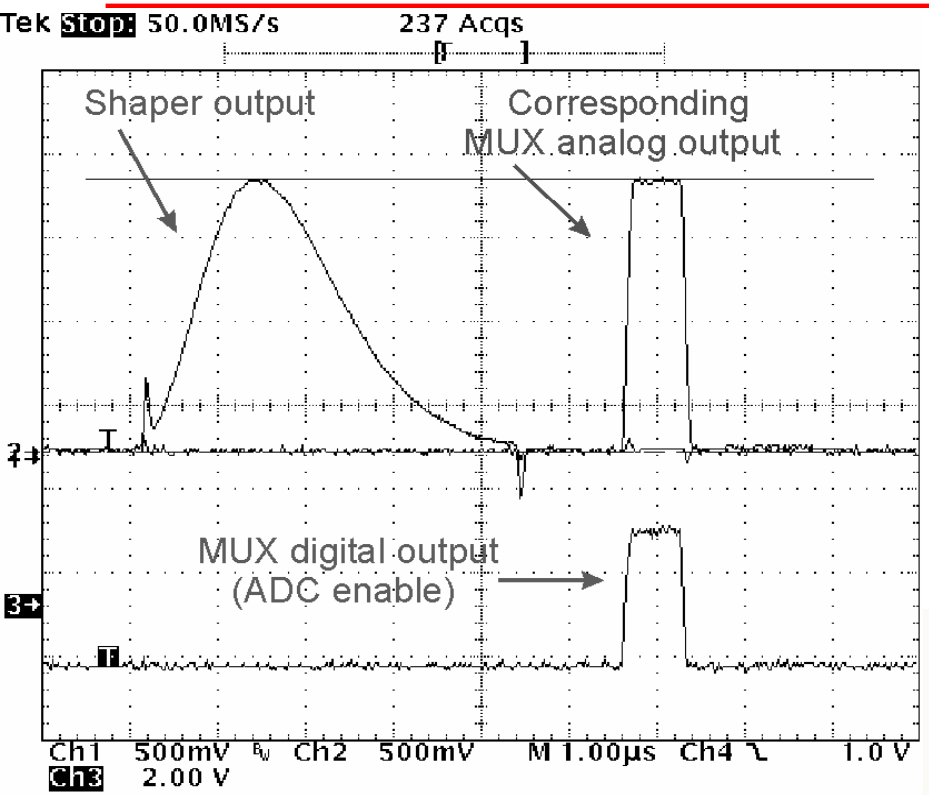


Polling st

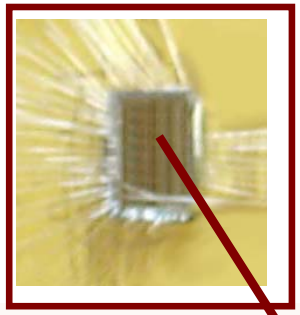
timing sig
on-chip s ks
provided

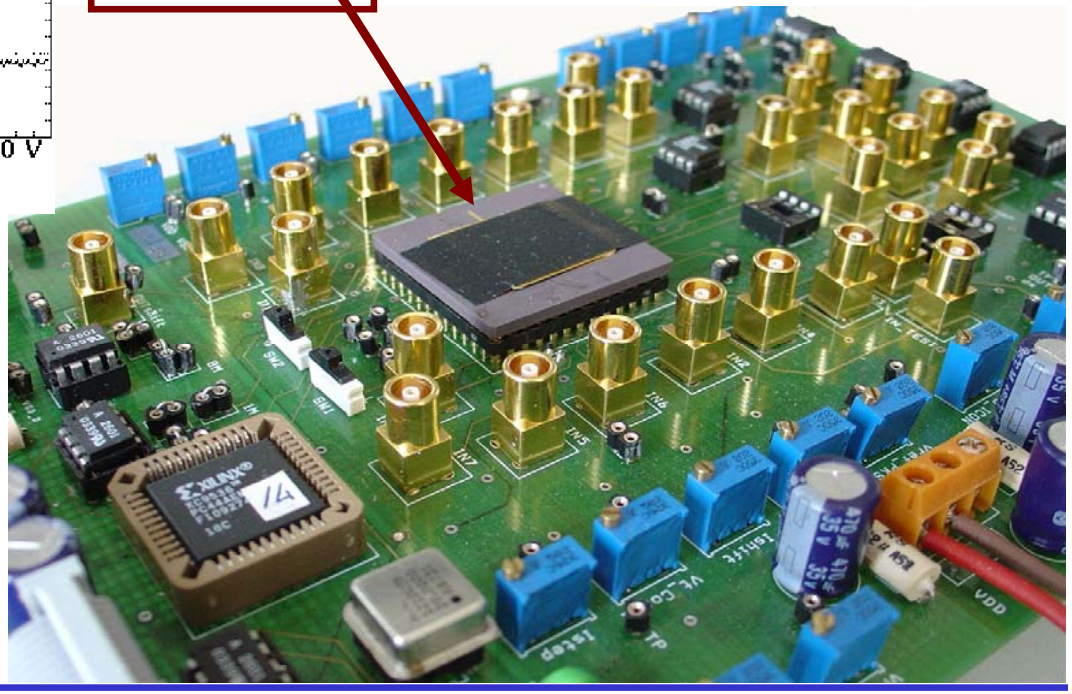


8-channel Chip: measured waveforms



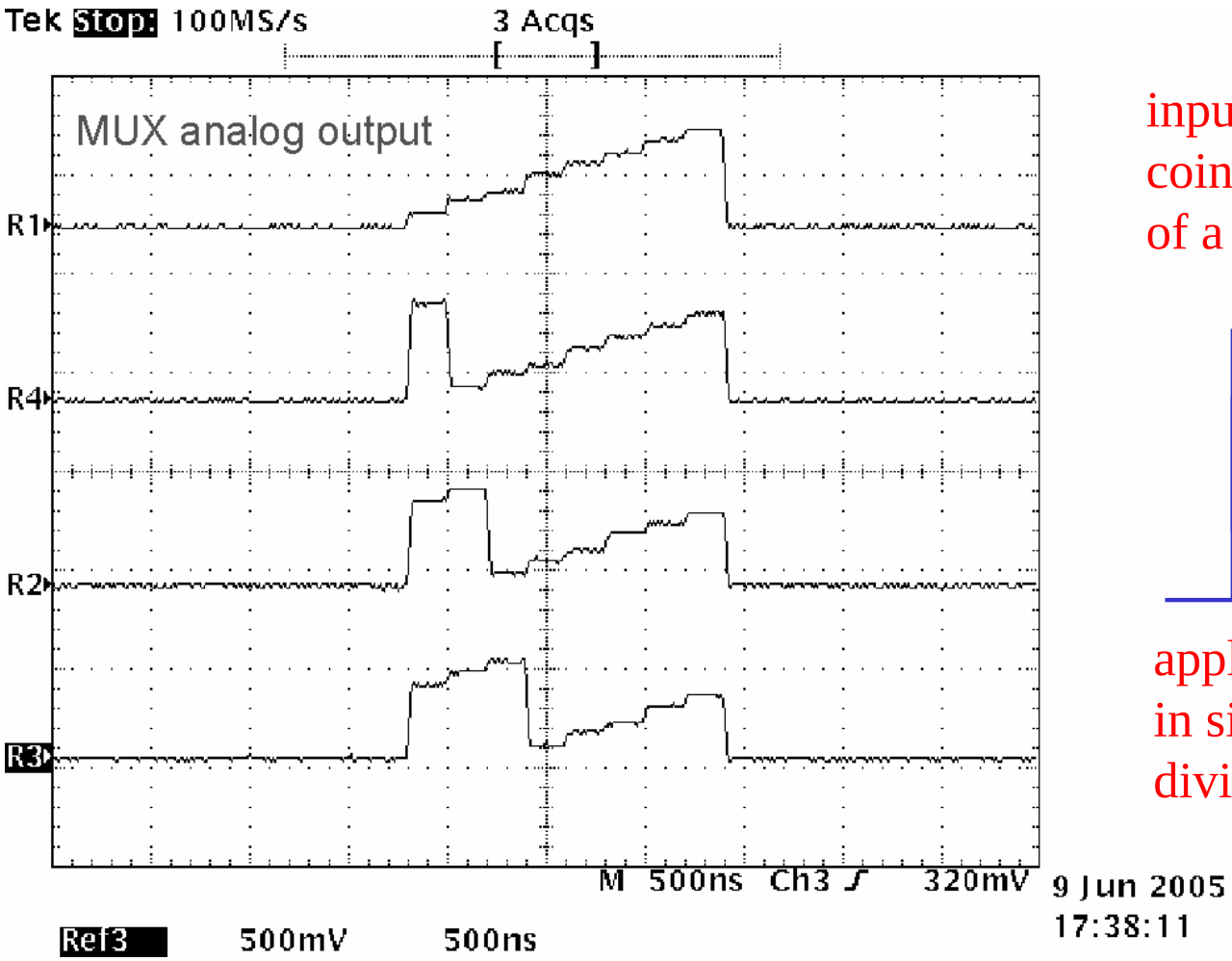
A minimum time of 800 ns has been used to read out the 8 channels



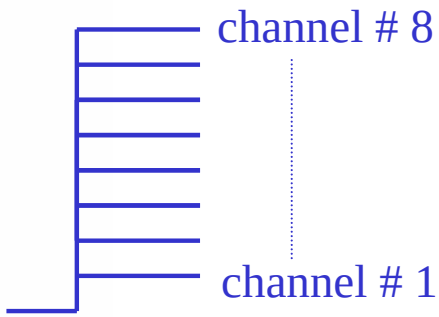


The digital output can be used as an enable signal for the external ADC

8-channel Chip: measured waveforms

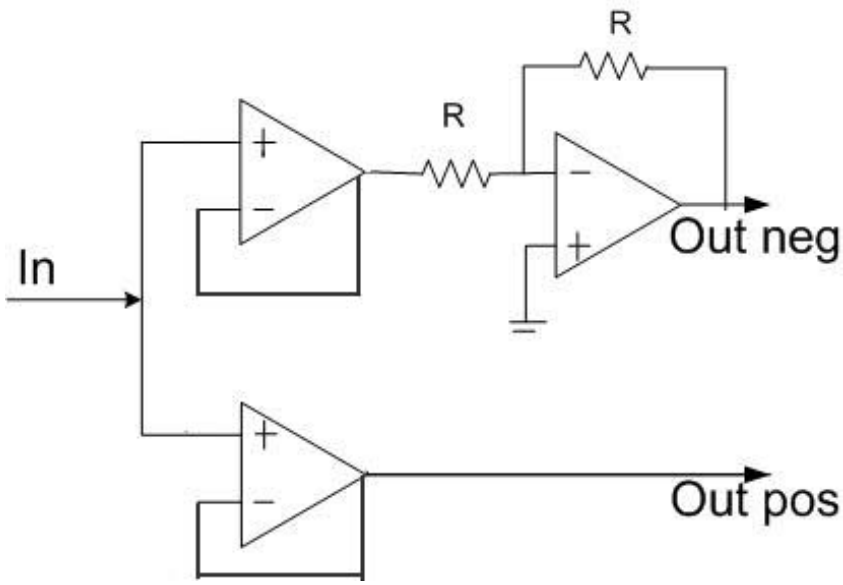


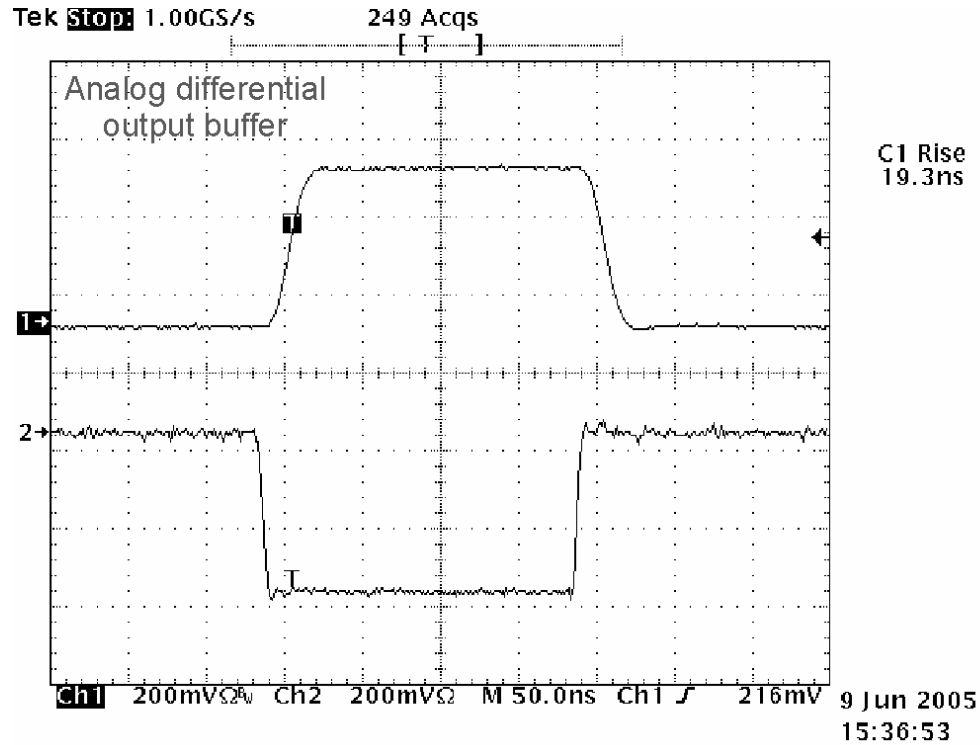
input step signals coincident on all 8 channels of a single MUX

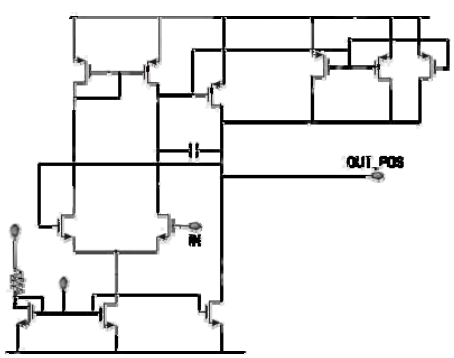


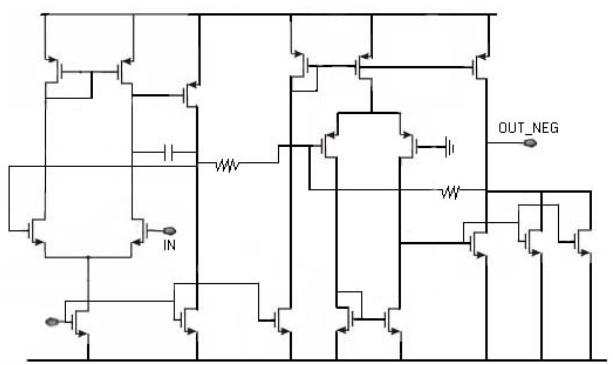
applied voltage divided in six values by a voltage divider

8-channel Chip: output Buffer





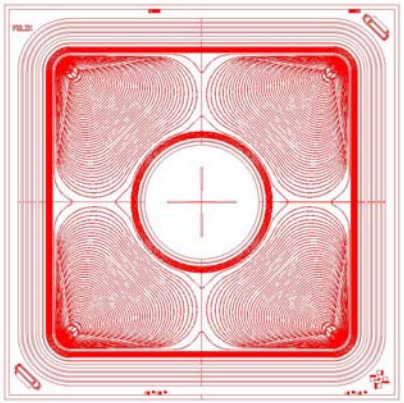


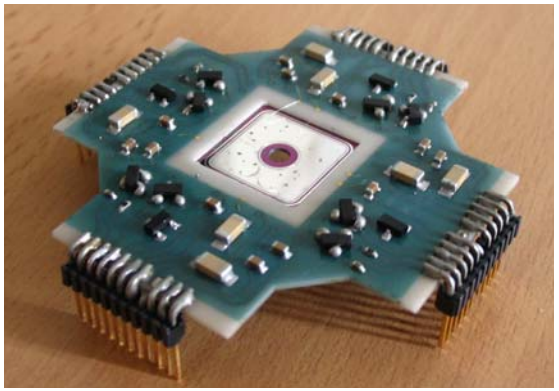


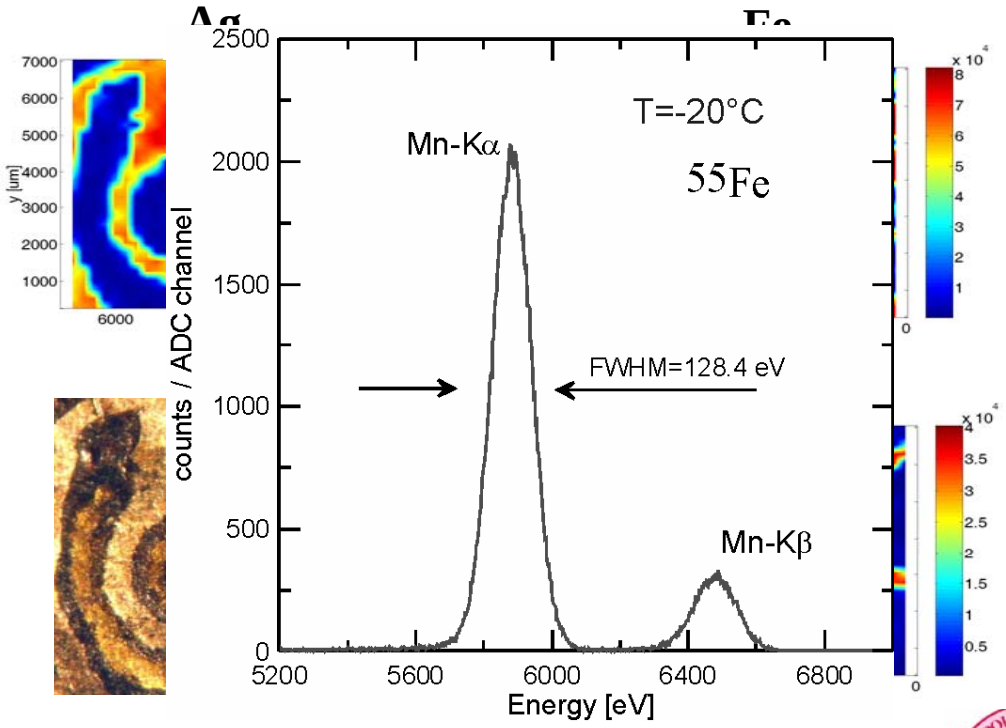
- Rising time: 20 ns
- R_L=100Ω
- C_L=100 pF

Other applications I

- SD^3 for material analisys and archeometry
  (INFN FELIX PROJECT)*
- C_D=65 fF







Lombard buckle – inlaid work (agemina)
Second quarter of VII century A.C.
Trezzo d'Adda, Italy

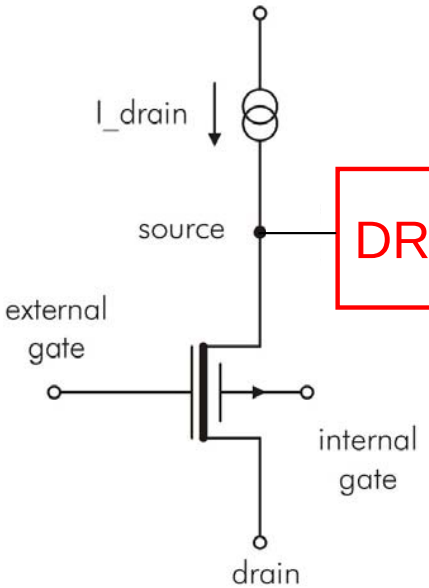
*special thanks to: S. Buzzetti, C. Guazzoni, A. Longoni,

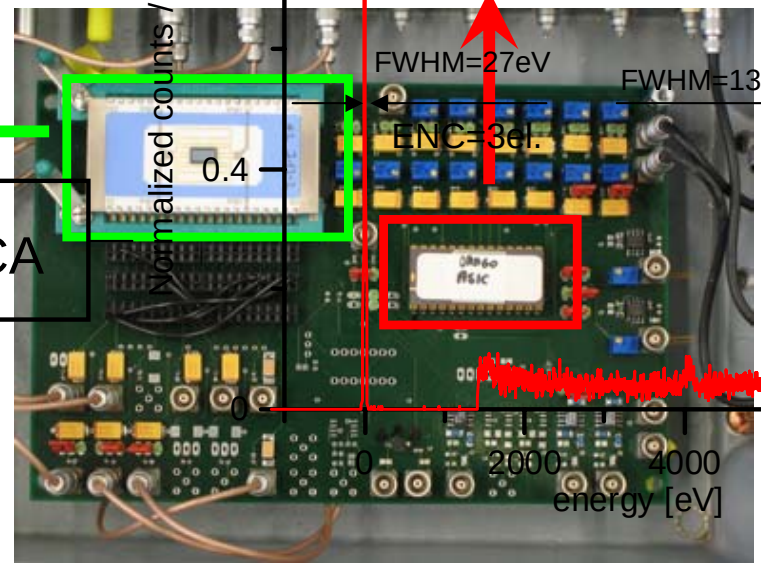
Other applications II

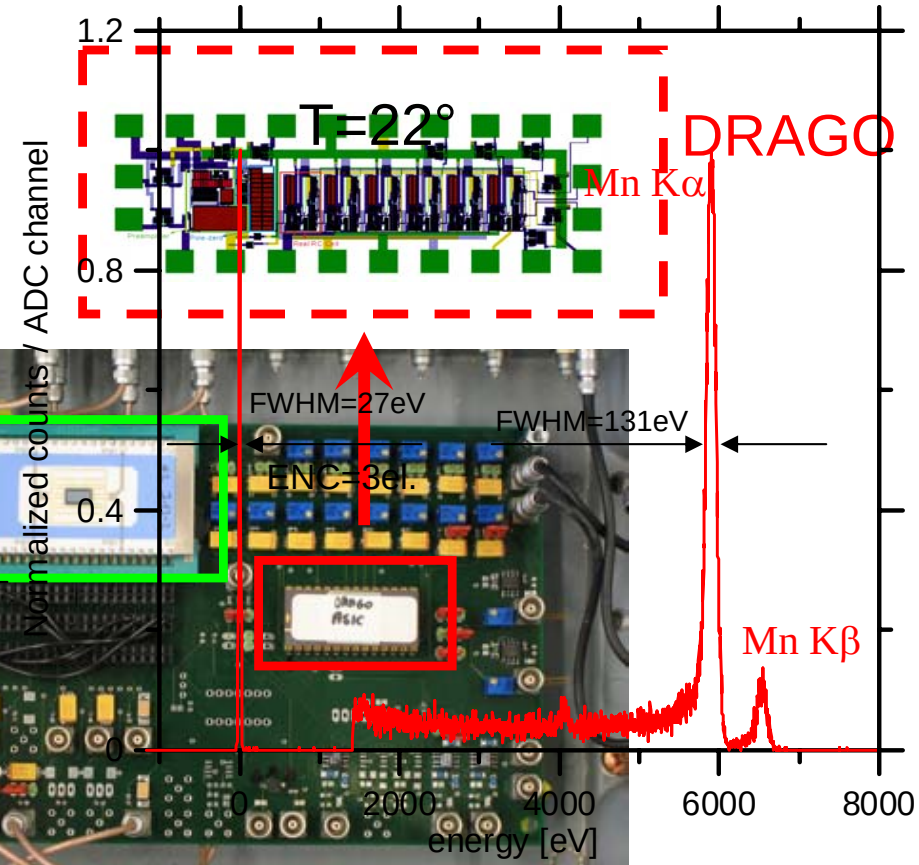
➢DePMOS Detector

(Max Planck Institut Halbleiterlabor)*

C_{eq}=35fF, I_L=10fA @ T=22°C







➢The shaping section has been used in the design of the Readout circuit for ΔE/E detector (Microelectronics Group of INFN, Catania) and for a readout circut in the SIDDHARTA project (INFN, Frascati) for the study of Kaonic atoms

*special thanks to:L.Strueder, S.Herrmann, R. Klotz

Conclusions and Perspectives

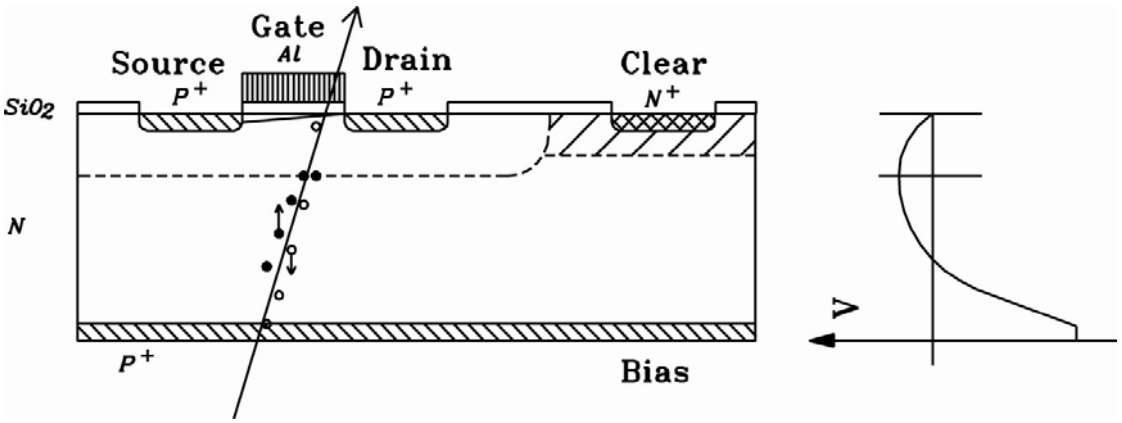
- A **complete readout chip for SDD** has been developed *(current source for the detector, preamplifier, shaper)*

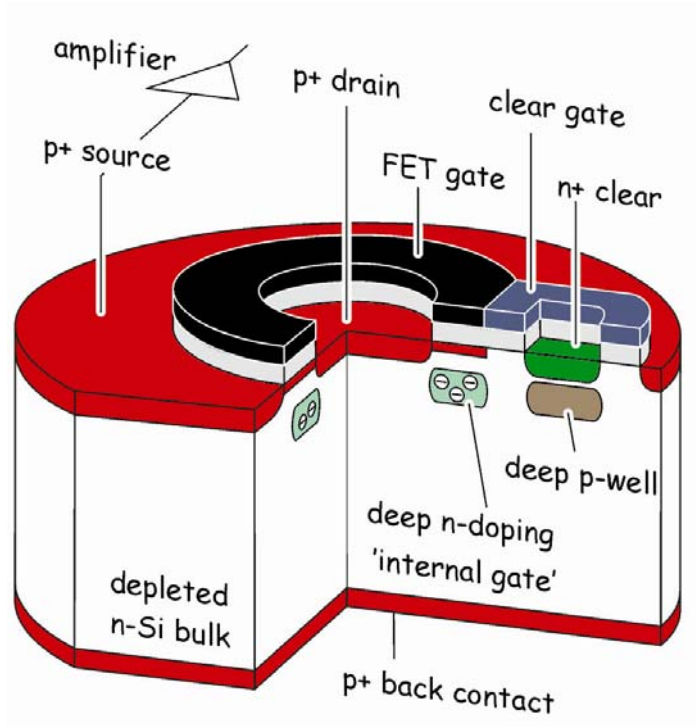
- Measurements on the single channel of the first prototype show the expected performances *(shaping functionality,* ***stability of time contants****, dynamic,* ***linearity****...)*

- Spectroscopic **performances match the requirements of DRAGO** Project *(**best measured ENC=11el**. at 1.7μs and ENC=14 el. at 6μs)* and demostrate that the chip is suitable to be used also with intrinsic very low noise detectors *(3el. have been measured with DePMOS at room temperature)*

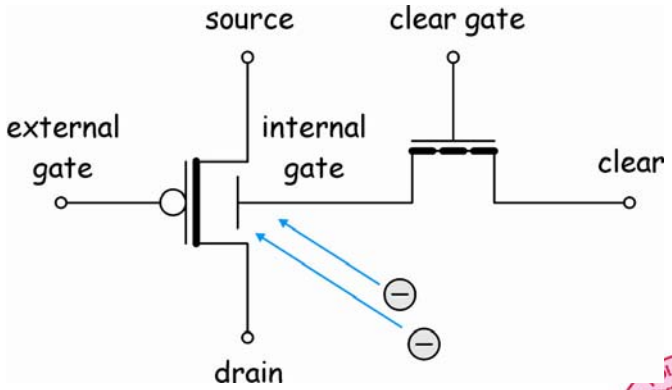
- The **8 channel version** including a peak stretcher and a BLH per channel, a 8:1 MUX and a digital memory is under test and **has shown up to now the expected performances**

The DePMOS Concept

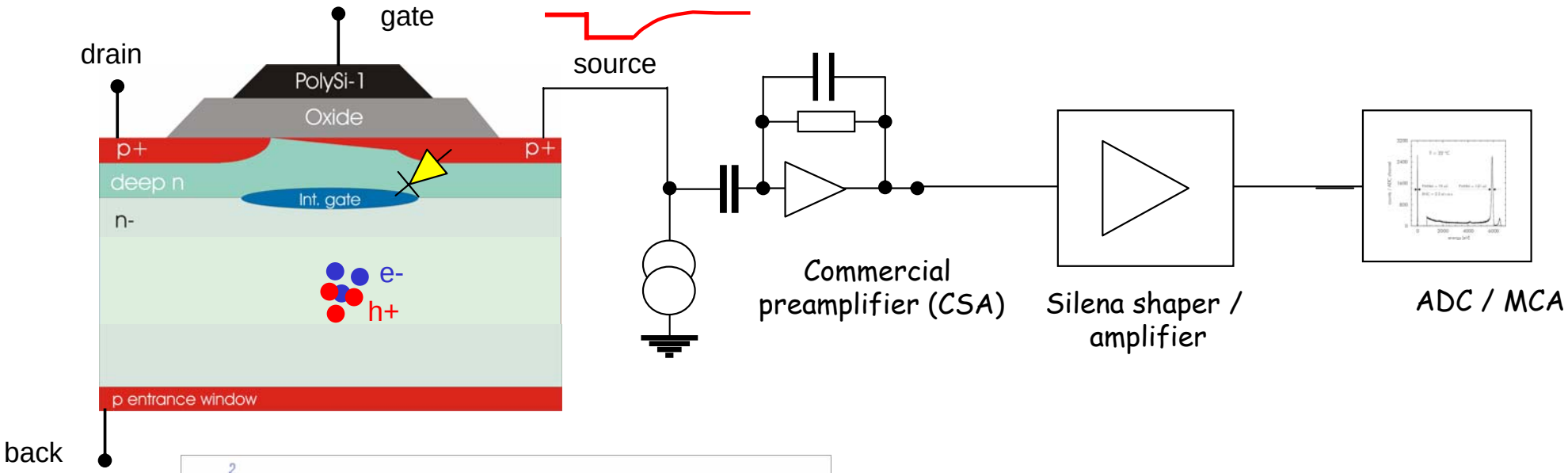


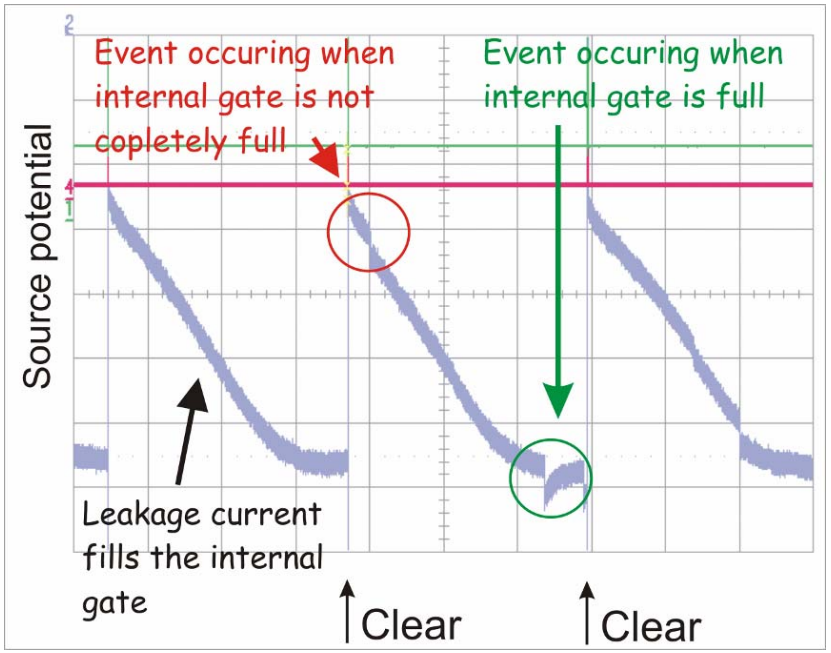


- p-channel MOSFET integrated on high-ohmic, sideward depleted n-substrate
- a potential minimum is formed by S/D potentials aided by a deep n implantation
- electrons are collected in an internal gate close to the surface
- the transistor current is modulated by charge collected in the internal gate
- the transistor can be switched on/off by an external (top) gate



Single pixel in continuous mode





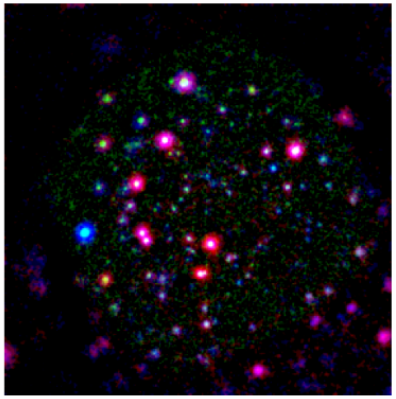
- DePMOS is always ON
- signal is read out during charge collection
- a time continuous shaping amplifier can be used
- In this mode DePMOS can be used e.g. as the readout device for Silicon Drift Detectors

XEUS project

(X-ray Evolving Universe Spectroscopy)

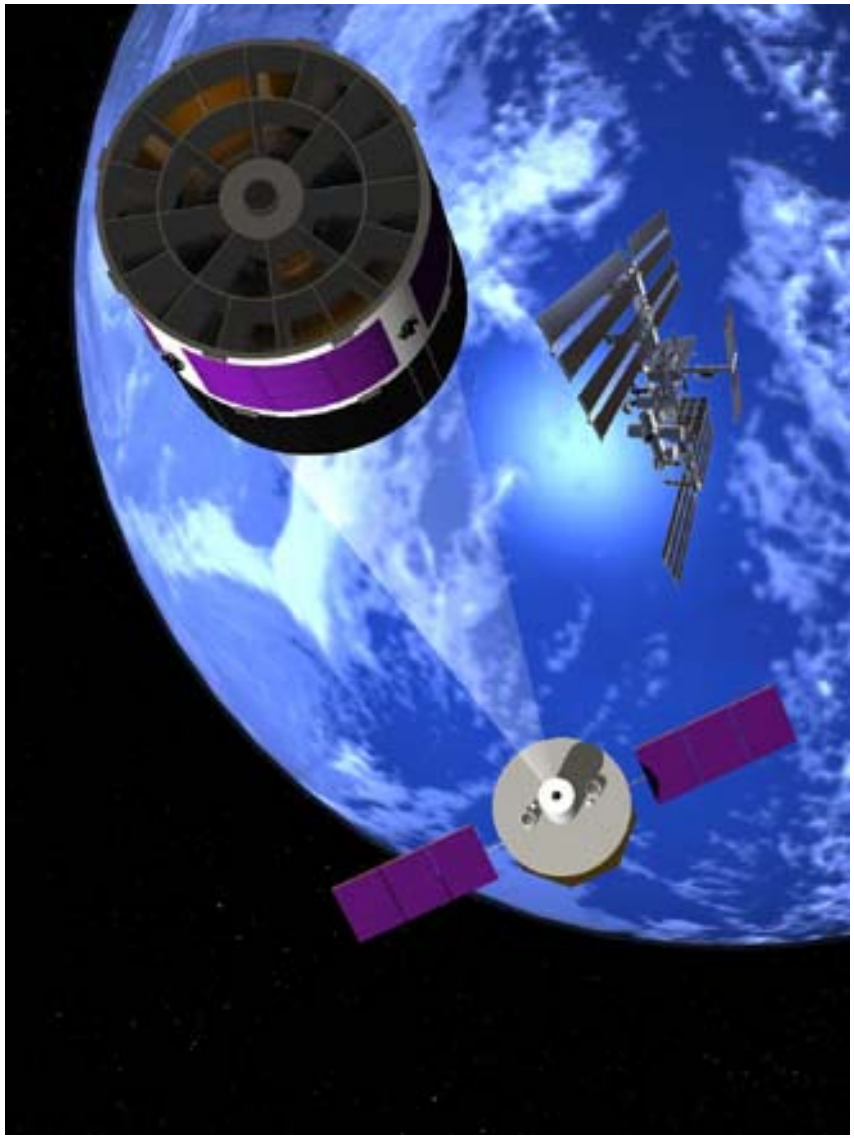
Exploring the early universe by imaging spectroscopy in the X-ray band (100 eV – 30 keV)

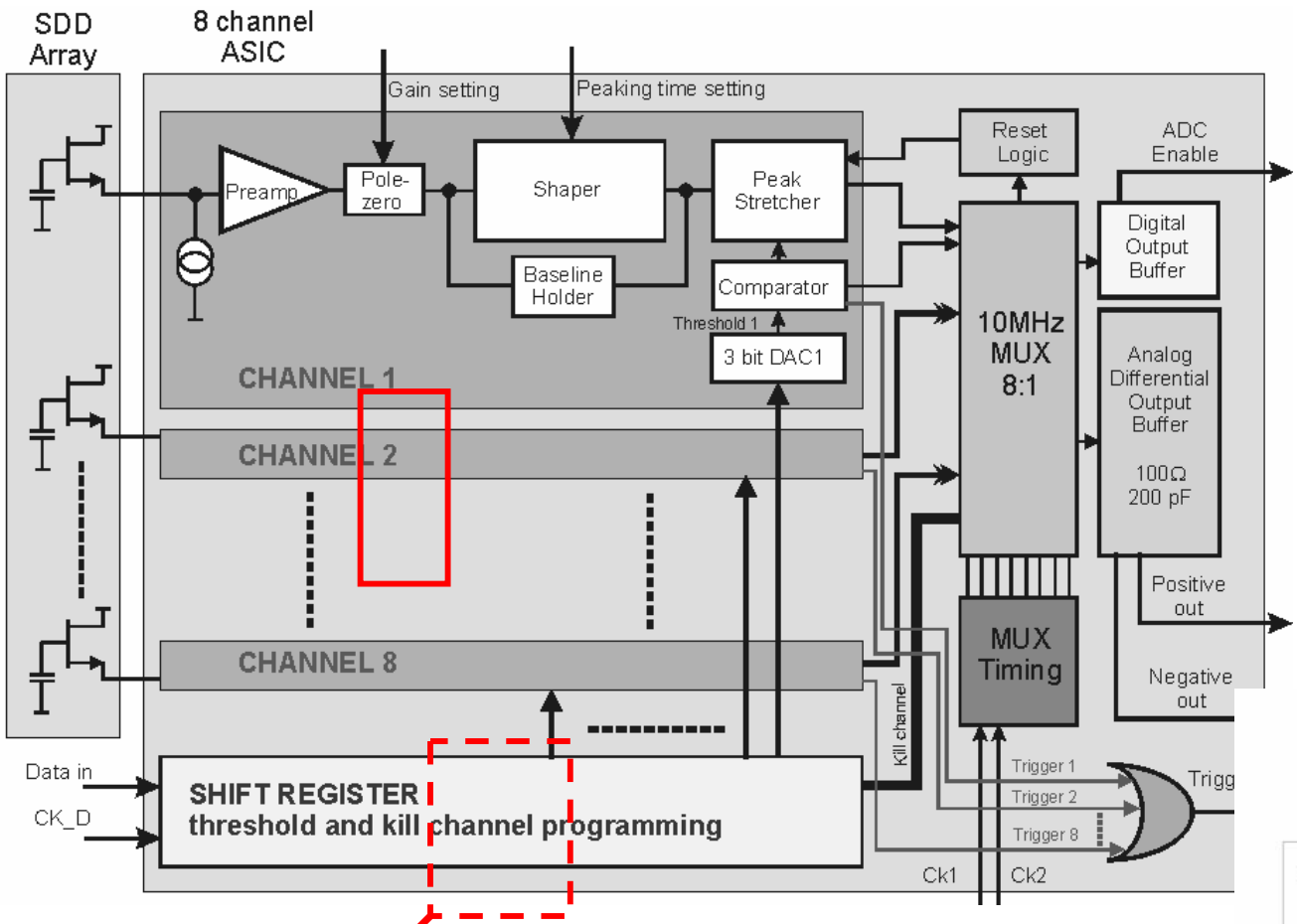
Observation of the hot Universe at high redshifts

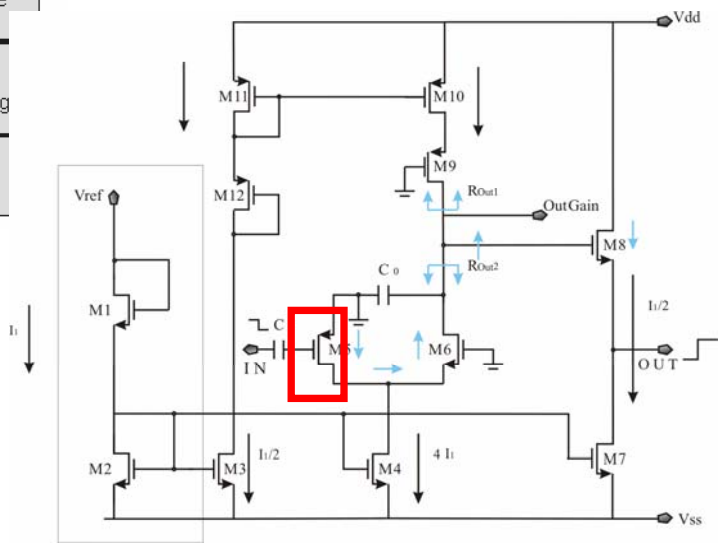


Device active area 7.68 x 7.68 cm^2
Device thickness 450 μm
Pixel size: 75 x 75 μm^2
Position resolution ca. 30 μm
Total 1024 x 1024 pixel cells

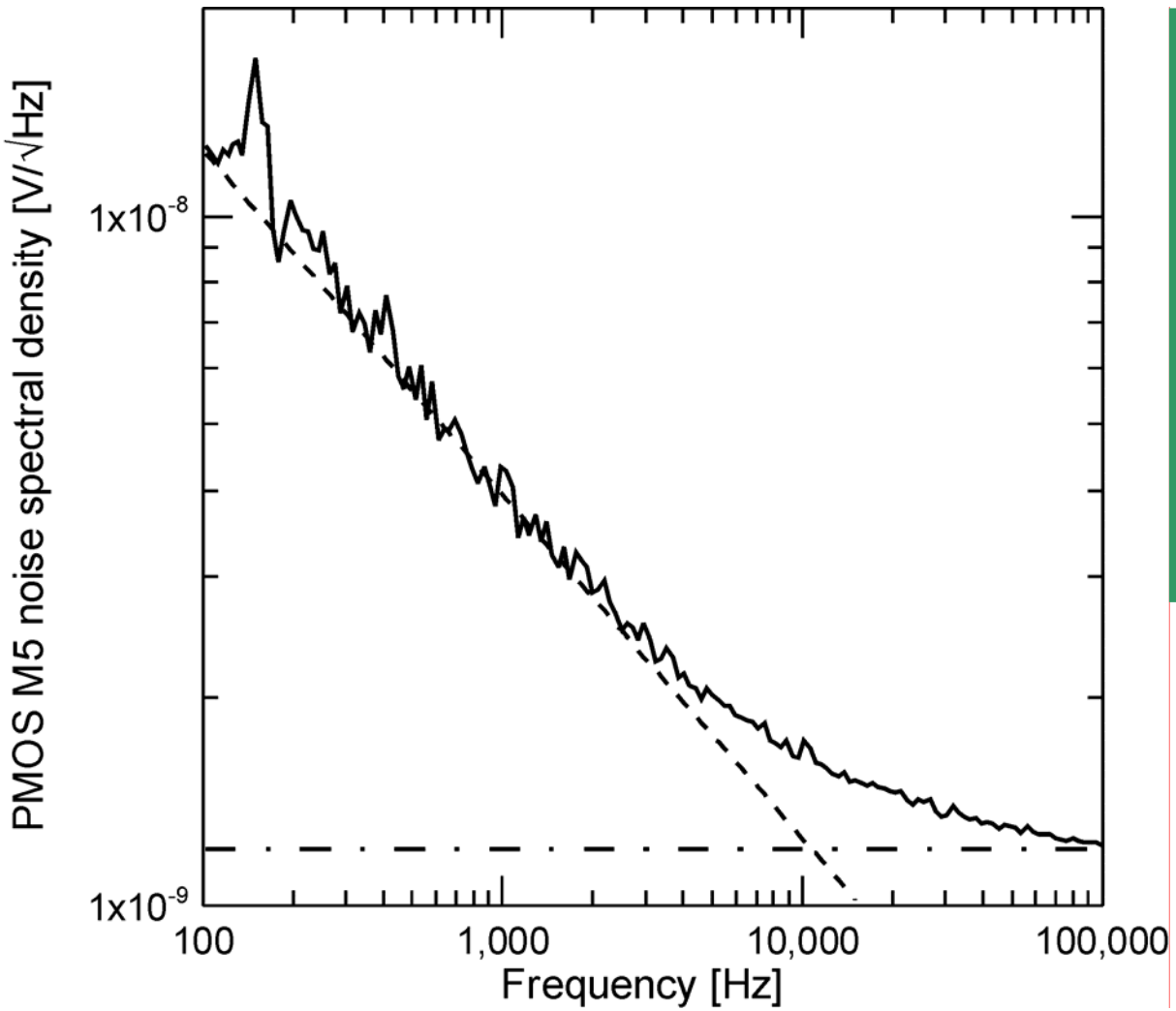
Energy resolution @ Mn-Kα 125 eV
Energy resolution @ C-Kα 50 eV
System noise 3-5 e^- ENC




SDD Array
8 channel ASIC
Gain setting
Peaking time setting
Preamp
Pole-zero
Shaper
Peak Stretcher
Baseline Holder
Comparator
Threshold 1
3 bit DAC1
CHANNEL 1
CHANNEL 2
CHANNEL 8
Reset Logic
ADC Enable
Digital Output Buffer
10MHz MUX 8:1
Analog Differential Output Buffer
100Ω
200 pF
Positive out
Negative out
MUX Timing
Kill channel
Trigger 1
Trigger 2
Trigger 8
Trigg
Ck1
Ck2
Data in
CK_D
SHIFT REGISTER
threshold and kill channel programming


Vdd
M11
M10
M9
M12
Vref
OutGain
M8
M1
M6
IN
OUT
M2
M3
M4
M7
Vss

Noise power density I



SDD Integrated JFET

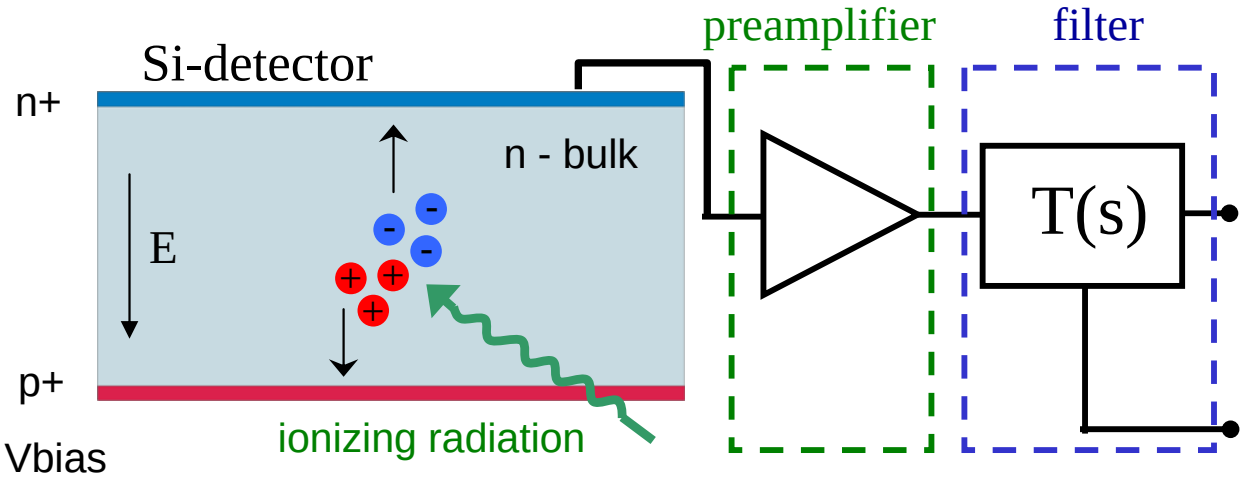
$$\overline{e^2_{D,W}} = 3.5 \cdot 10^{-17} \frac{V^2}{Hz}$$

$$\overline{e^2_{D,\frac{1}{f}}} = 5 \cdot 10^{-12} V^2$$

$$\overline{e^2_{PMOS,W}} = 1.45 \cdot 10^{-18} \frac{V^2}{Hz}$$

$$\overline{e^2_{PMOS,\frac{1}{f}}} = 1.56 \cdot 10^{-14} V^2$$

System Definition



- Design of suitable detector that minimizes C_{TOT}
- Choice of an adequate filter function
- Realization of a cicuit architecture to implement the desired filter function in a low power compact system, without adding significant physical noise contributions

System:

- silicon detector (with on chip amplification)
- front-end amplifying electronics
- integrated filtering stage

$$ENC^2 = \frac{a}{\tau} C_{TOT}^2 A_1 + 2\pi a_f C_{TOT}^2 A_2 + b\,\tau A_3$$

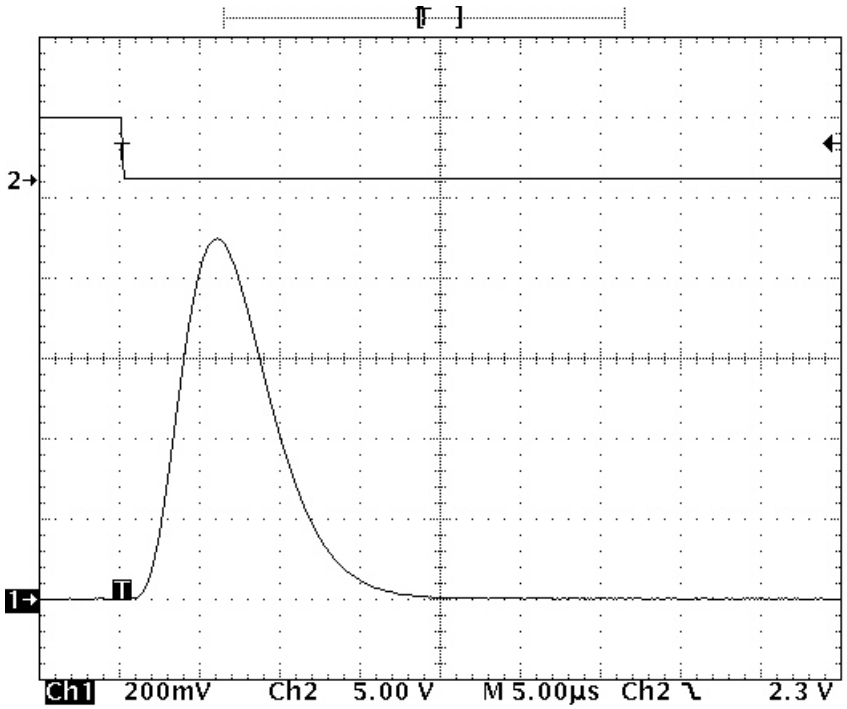
- C_{TOT} detector+front end capacitance
- a, a_f, b physical noise sources
- $A_1 A_2 A_3$ filter parameters
- τ filter shaping time

Energy resolution is limited by

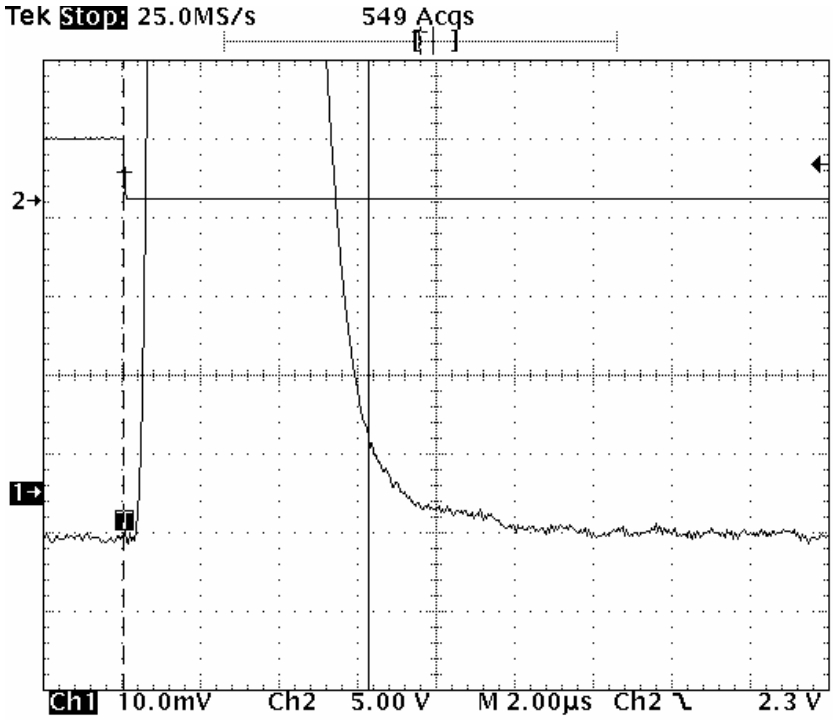
- statistical fluctuation of the electron-hole pairs generated in the detector (mainly dependent on detector material)
- measurement of the charge delivered in the detector, affected by unavodable noise sources.

$$\tau_{opt} = \sqrt{\frac{a}{b}}\sqrt{\frac{A_1}{A_3}}C_{TOT}$$

Experimental results

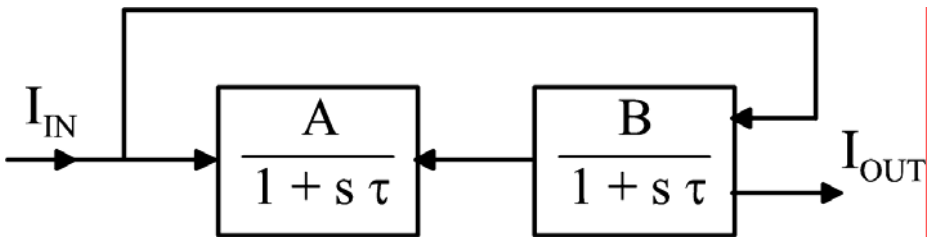


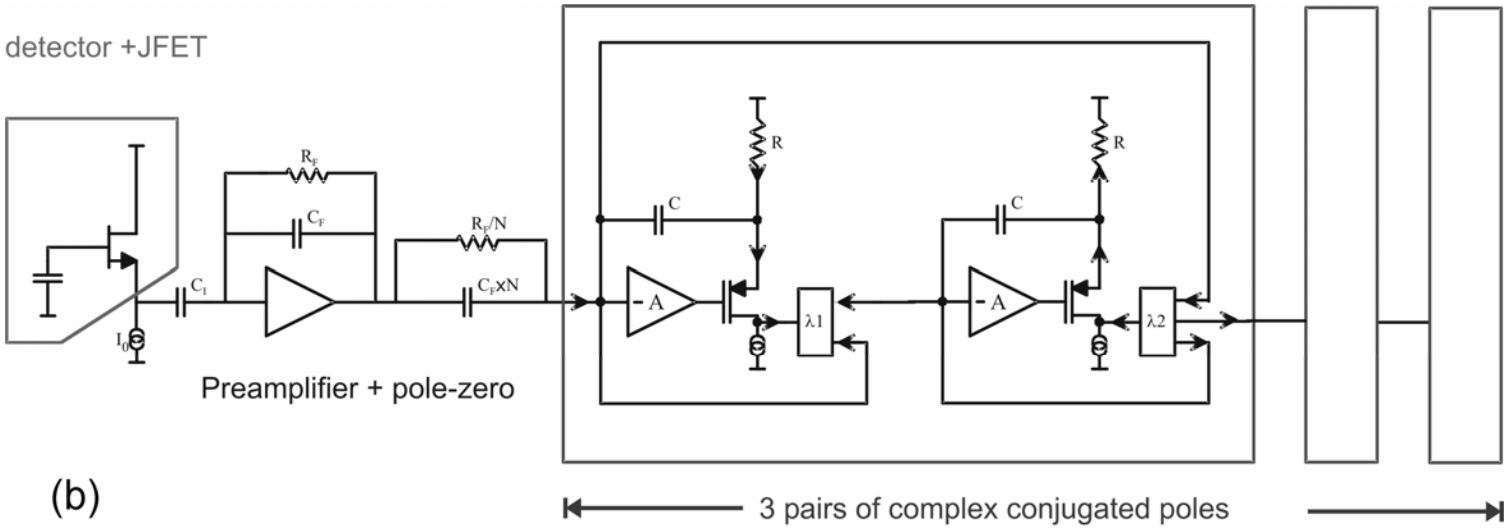
Output response with τ_{Peak}=2µs



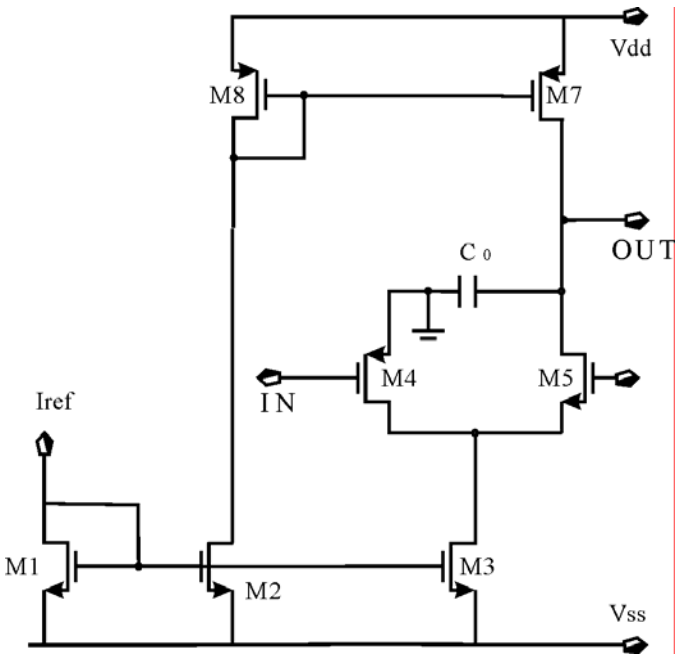
Return to zero of the waveform

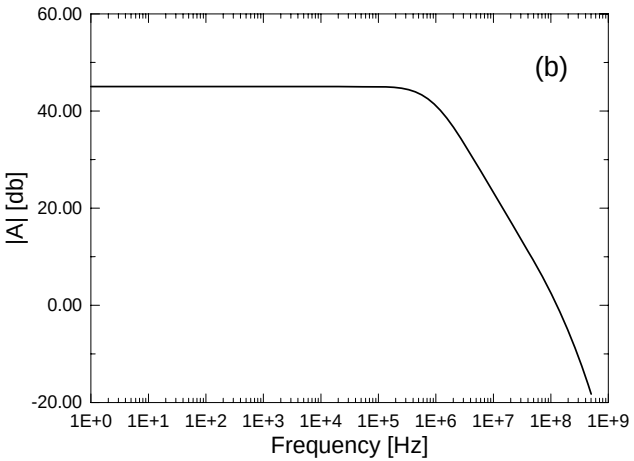
Complex-conjugates pole channel





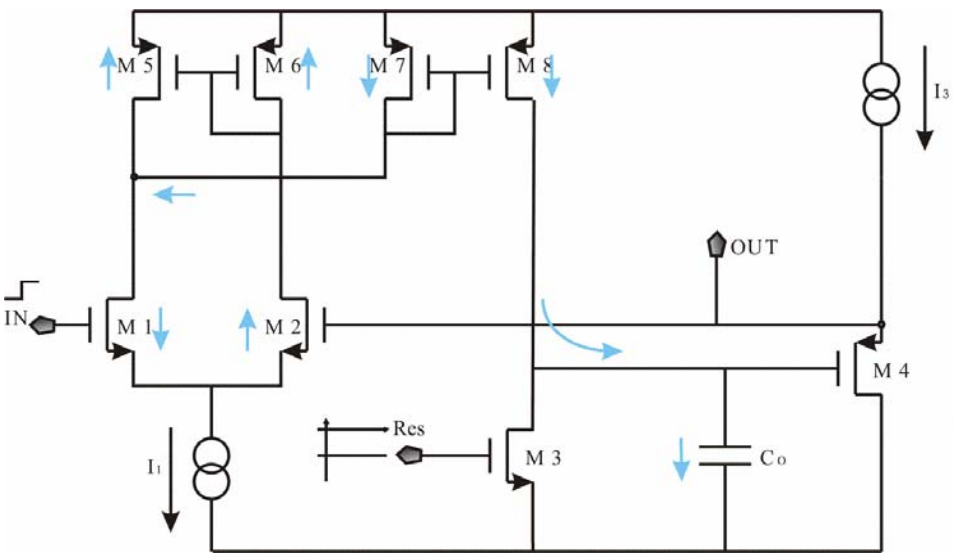
Single cell amplifier

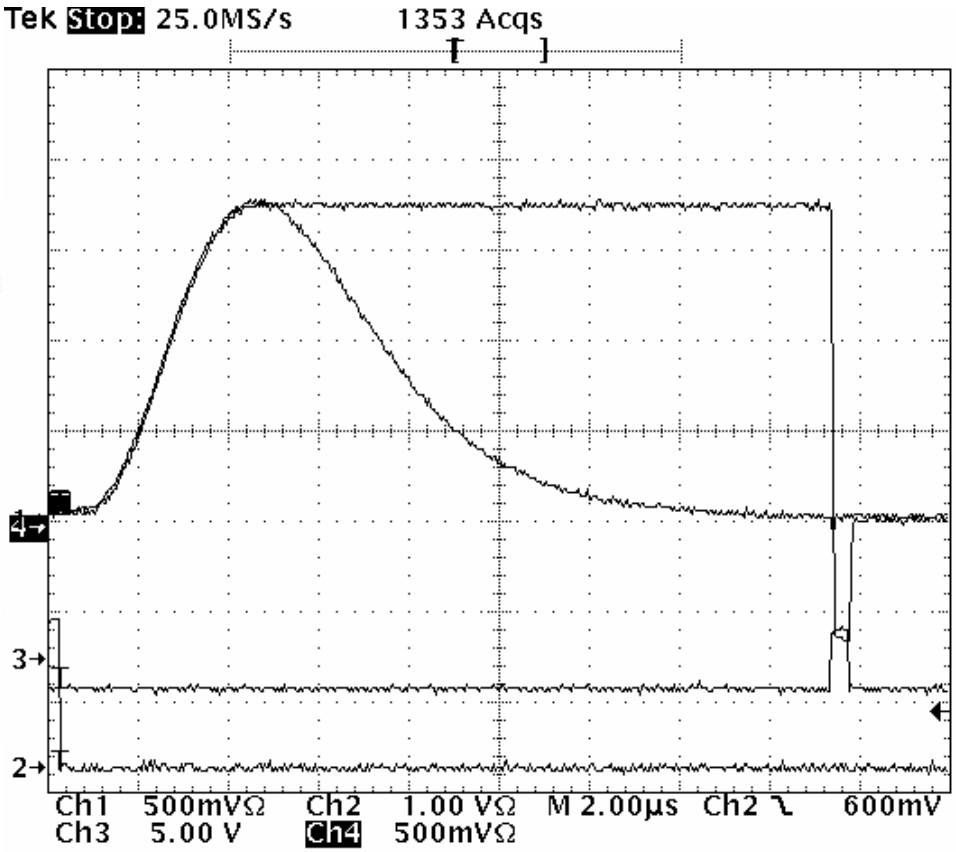




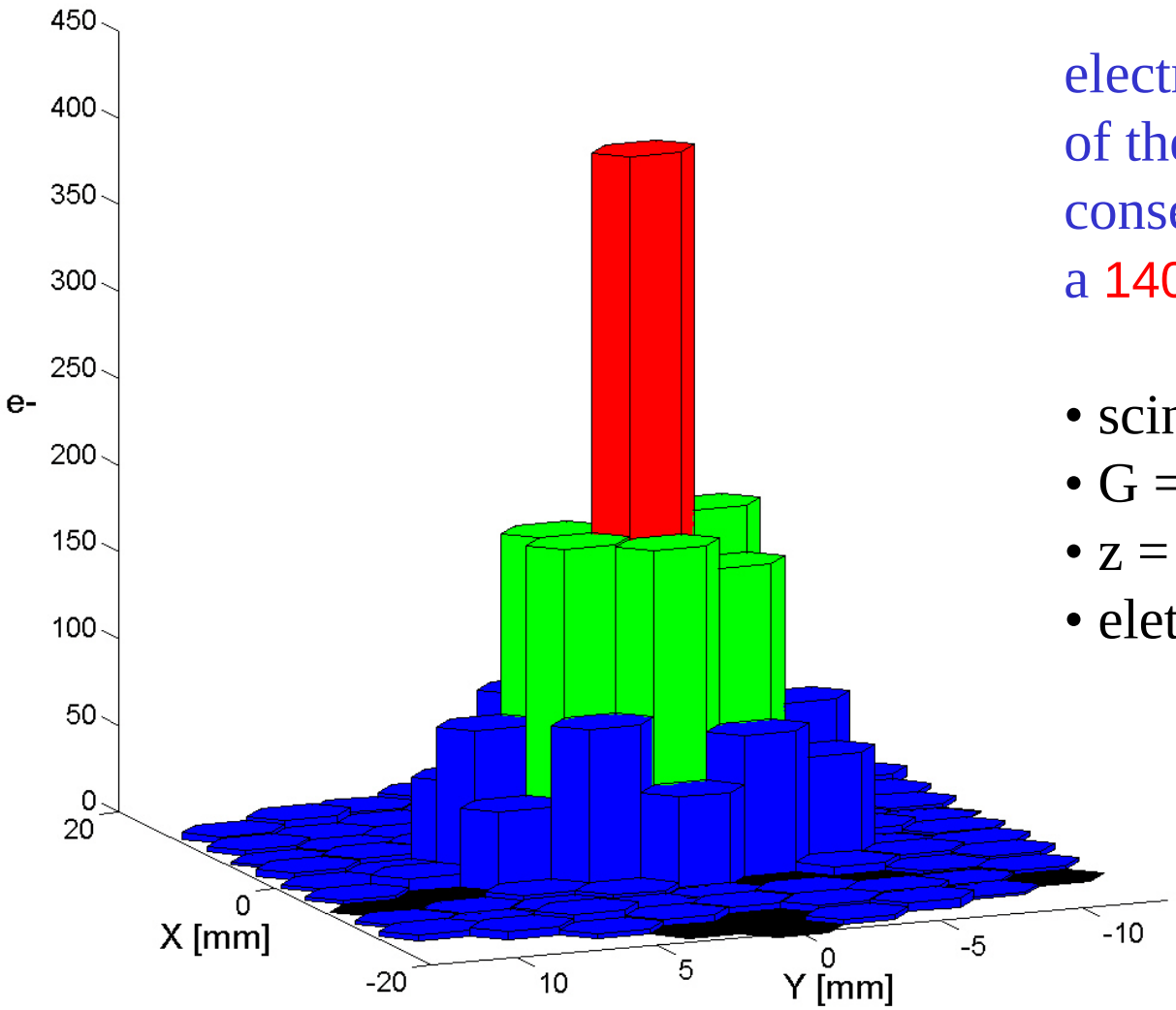
Gain=110

Peak stretcher





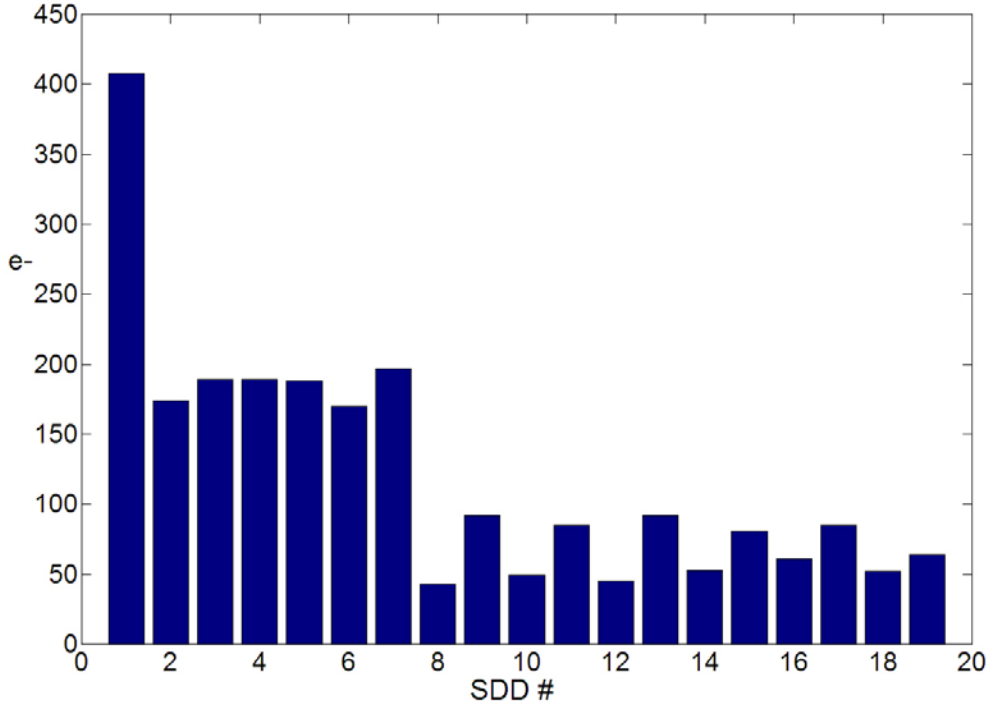
Electronic noise and spatial resolution



electrons collected by the units of the SDD matrix as a consequence of the absorption of a 140keV γ ray

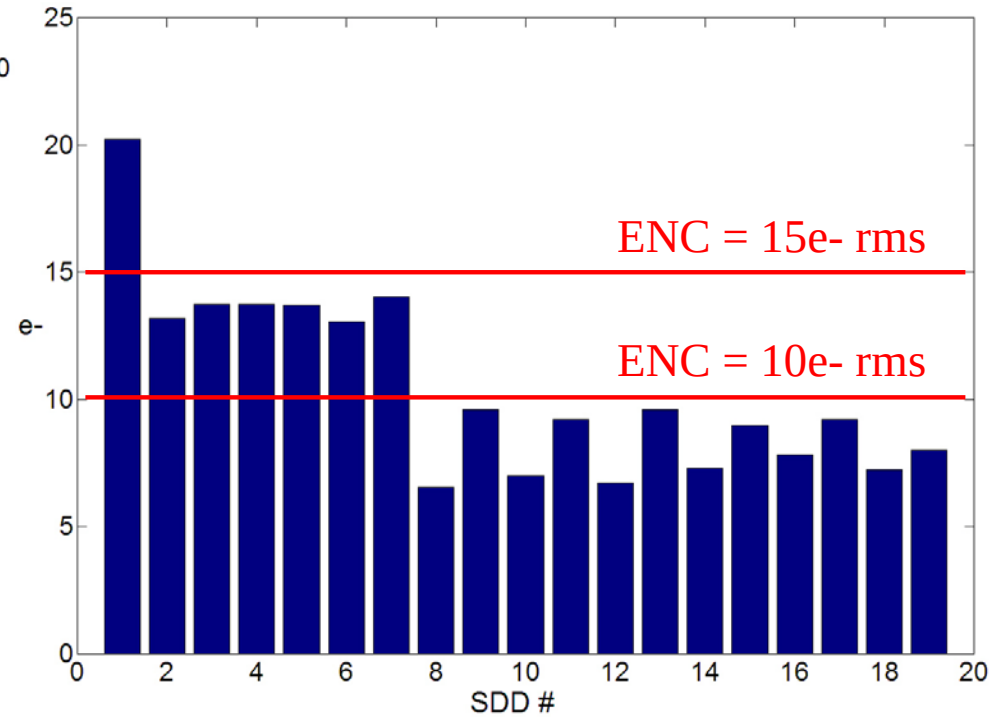
- scintillator: CsI(Tl)
- G = 15 e-/keV
- z = 5 mm
- elettronic noise not present

(Monte Carlo simulation)

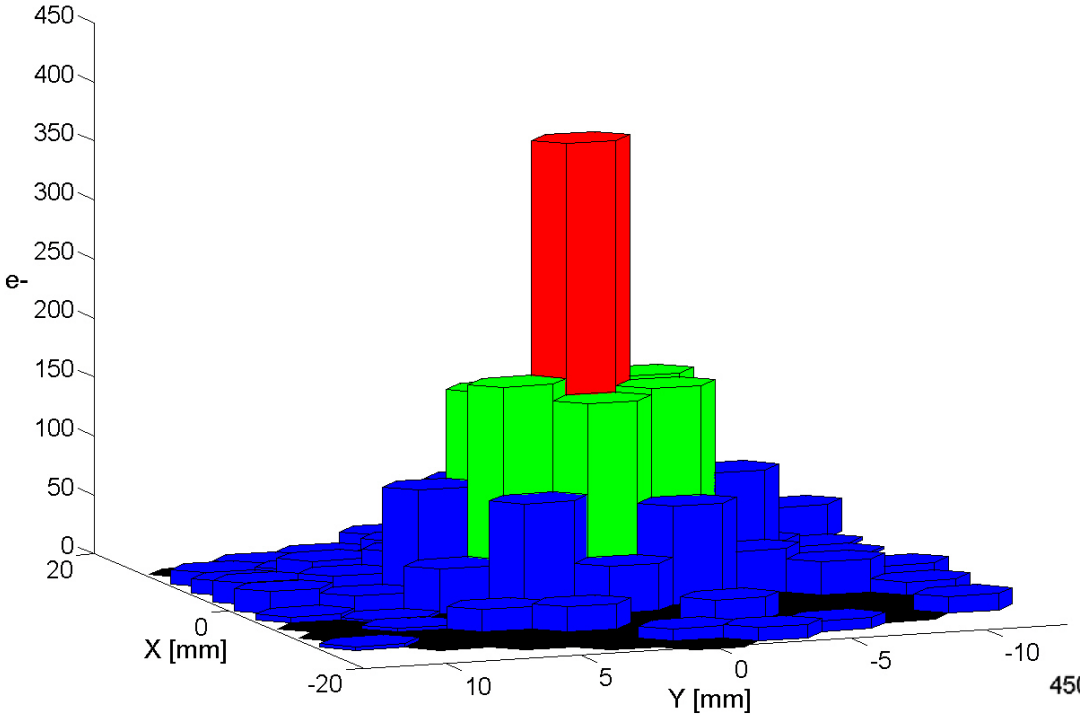


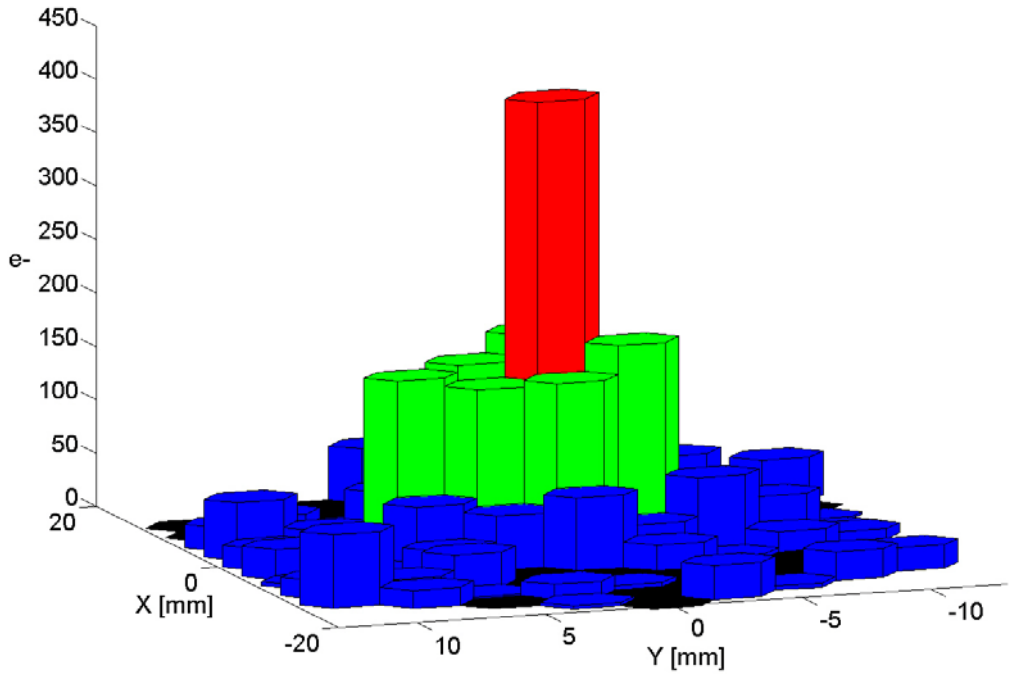
electrons collected by the 19 detectors with the highest signal

statistical fluctuation ($\sigma\, rms$) of the charge collected by the detectors, in the hypothesis of Poisson ststistics (no correlation)



$\Rightarrow$ to have an electronic noise smaller than the statistical fluctuation, ENC < 10-15 e- rms



ENC = 15 e- rms

ENC = 30 e- rms