Integrated circuits of pixel architecture in 2D i 3D technologies

Paweł Gryboś

on behalf of ASIC Design Group

Department of Measurements and Electronics
AGH University of Science and Technology. Krakow, Poland

e-mail:pawel.grybos@agh.edu.pl

http://www.kmet.agh.edu.pl/www/asics

1. Who we are?

2. Hybrid pixel detectors (examples of existing solutions)

3. PXD18k – fast single photon counting chip with energy window

4. Pixel prototypes in new technologies (90 nm, 3D)

5. Algorithms to solve problem with charge sharing

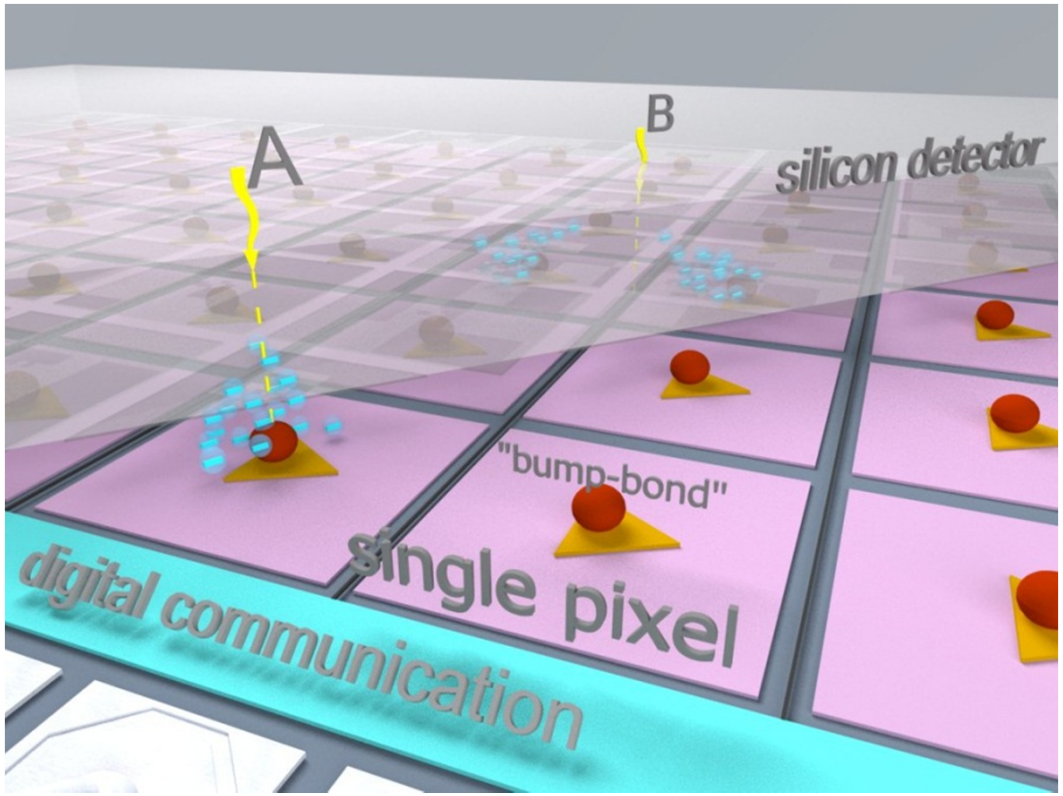
6. Other applications of pixel readout chips

AGH University of Science and Technology

- established on 20th October, 1919
- 33000 students, 500 PhD students
- 2000 researchers,
- 15 faculties (30 branches of studies, over 170 specializations)

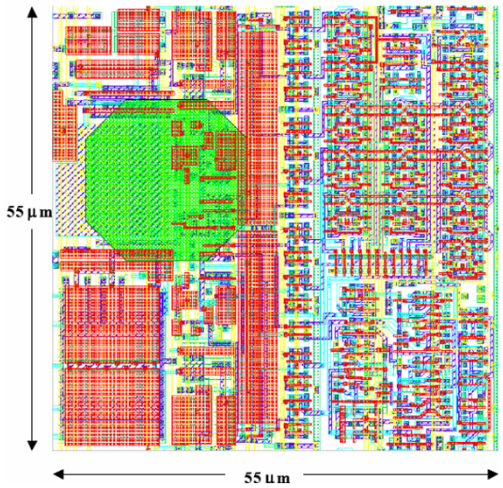
Detector readout electronics:
- Faculty of Physics ….
- Faculty of Electrical Engineering …..

Hybrid pixel detector

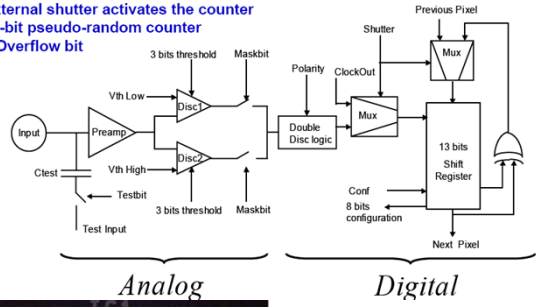


Si detector
- 3.6eV/e-h pair
- 320 um thick detector has good Q.E. fron 5 to 15 keV

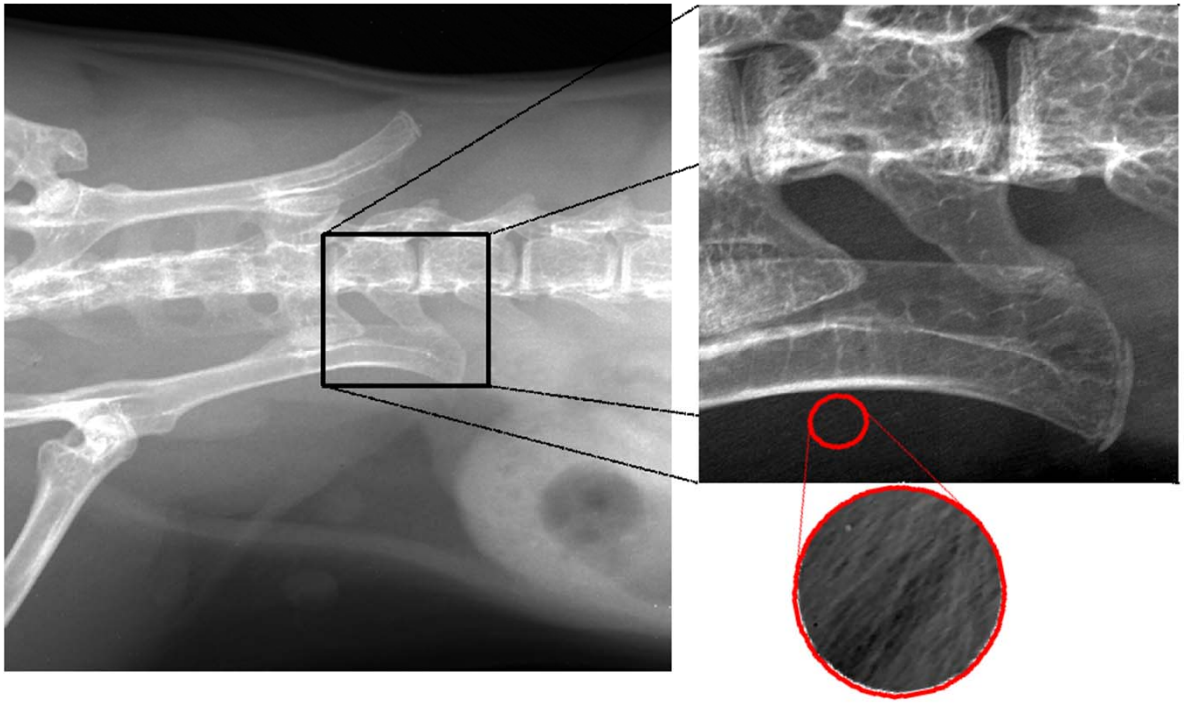
Existing solutions: MEDIPIX – CERN, CMOS 0.25 um



Charge sensitive preamplifier with individual leakage current compensation
2 discriminators with globally adjustable thresholds
3-bit local fine tuning of the threshold per discriminator
1 test and1 mask bit
External shutter activates the counter
13-bit pseudo-random counter
1 Overflow bit



256 x 256 pixels,
~1.4 × 1.6 cm^2



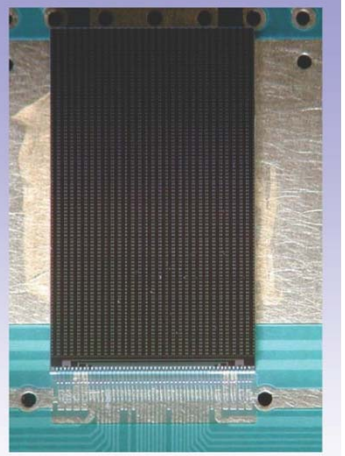
In vivo X-ray radiograph of a mouse pelvis and surrounding soft tissue structures demonstrates extremely high contrast of the corrected images taken by Medipix2 (with microfocus tungsten X-ray tube at 50 kV). Even structure of overlaying hair (circular inset) is seen through full thickness of mouse body! [NIMA]

medipix.web.cern.ch

Existing solutions: Pilatus II - PSI, CMOS 0.25 um

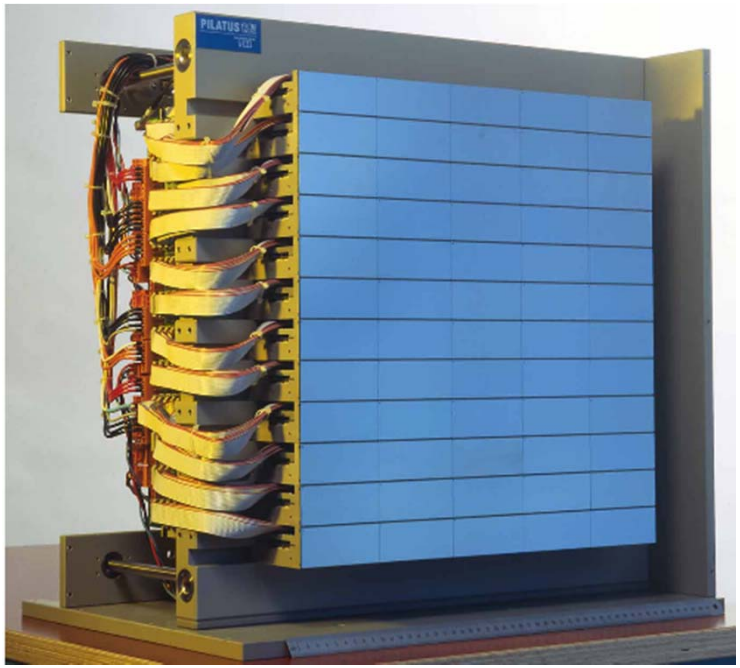
PILATUS II Chip

- Radiation hard design
- 60 x 97 pixels = 5820 pixels
- Pixel size 172 x 172 um^2
- 17.540 x 10.450 mm^2
- Count rate: 1MHz/pixel
- 20 bit counter/pixel (1'048'575 X-rays)
- 6 bit DAC for threshold adjustment
- T_{ro} = 2.6 ms (@ 66MHz)



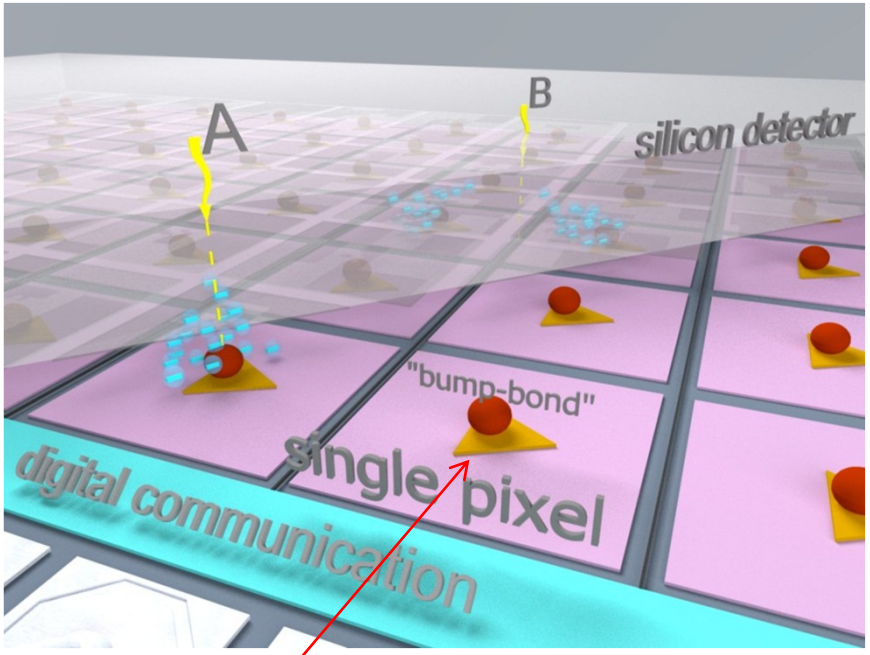
- 16 chips bump-bonded to 1 Silicon Sensor
- Active Area is 79.4 x 34.1 mm^2

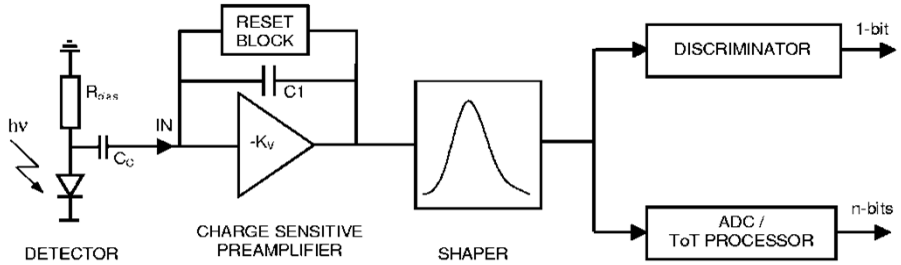
Large area detetcors: 6 M pixels



pilatus.web.psi.ch

Main limitations





1. Area (pixel ptich 55-200 um)
2. Power (< 30 uW)
3. Noise, speed
4. Matching
5. Functionality
6. Quality of bump-bonding process

PXD18k - Fast Single Photon Counting Chip with Energy Window for Hybrid Pixel Detector

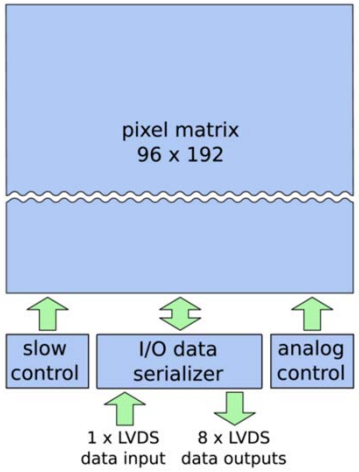
PXD18k - fast single photon counting chip with energy window for hybrid pixel detector
Szczygiel, R.; Grybos, P.; Maj, P.; Zoladz, M.
Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE ,
Page(s): 932 - 937

PXD18k - chip designed at AGH UST, CMOS 180 nm

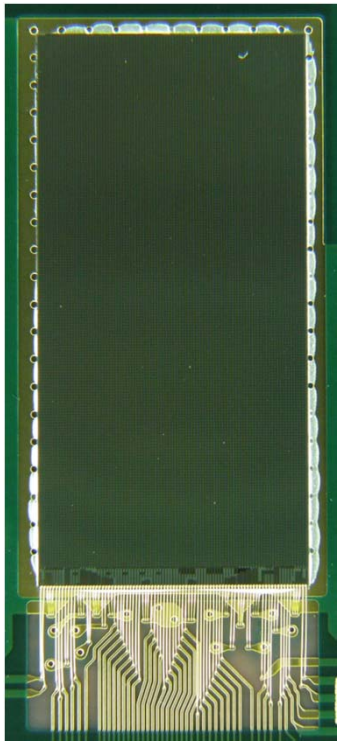
- Prototype readout chip for hybrid pixel detector
  - X-ray imaging applications:
  - 8 - 20 keV with Si detector

- Functionality:
  - single photon counting,
  - energy window,
  - continuous readout

- Critical parameters:
  - pixel size 100x100 μm^2
  - noise - matching – high count rate
  - continuous: tests for crosstalk and frame rate



Chip: PXD18k



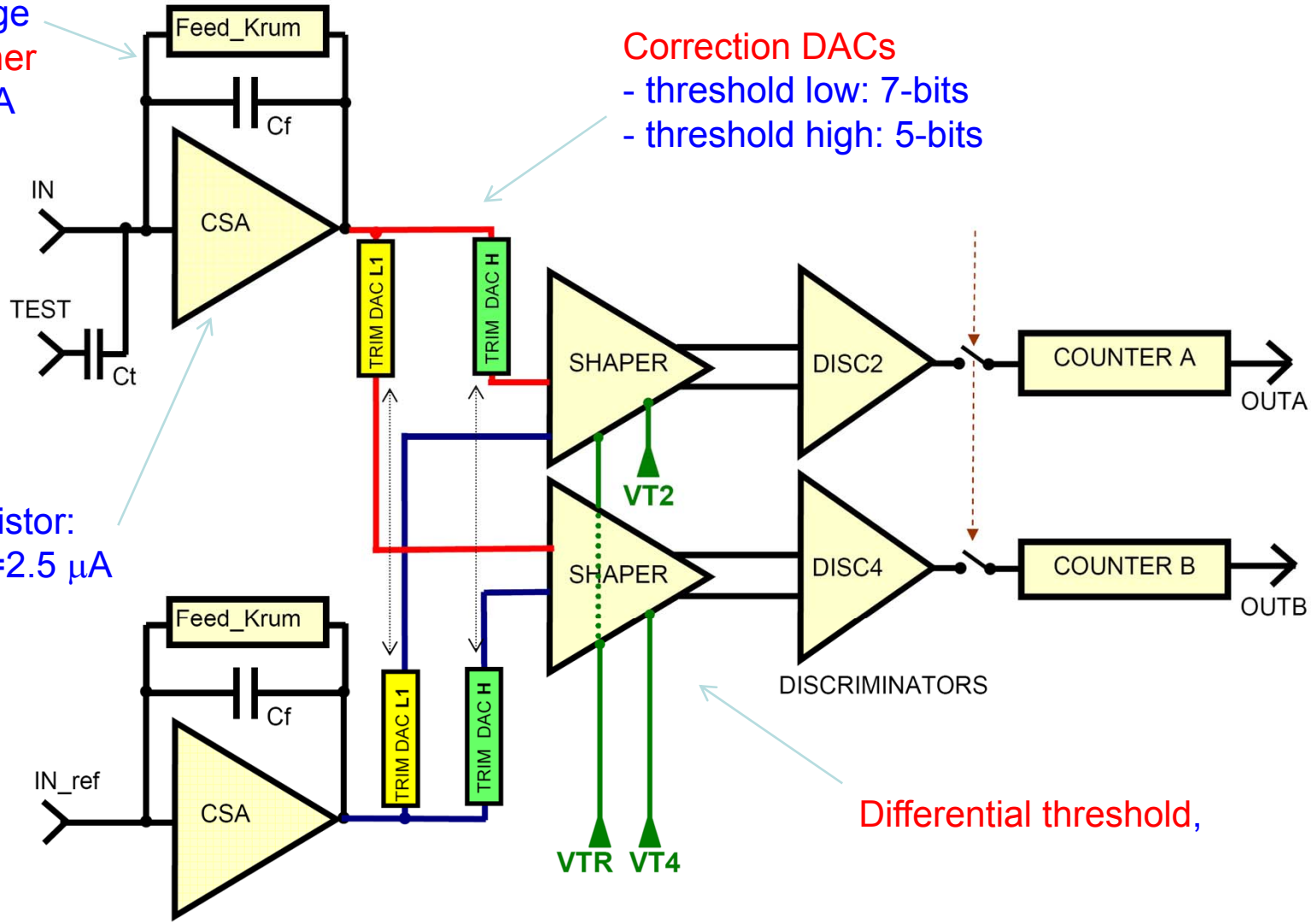
192 x 96 = 18.432 pixels (100x100 μm^2)

chip size 9.64x20 mm^2 , UMC 180 nm

Single channel architecture

Cf = 8 fF, discharge with Krummenacher circuit Ikrum=20nA

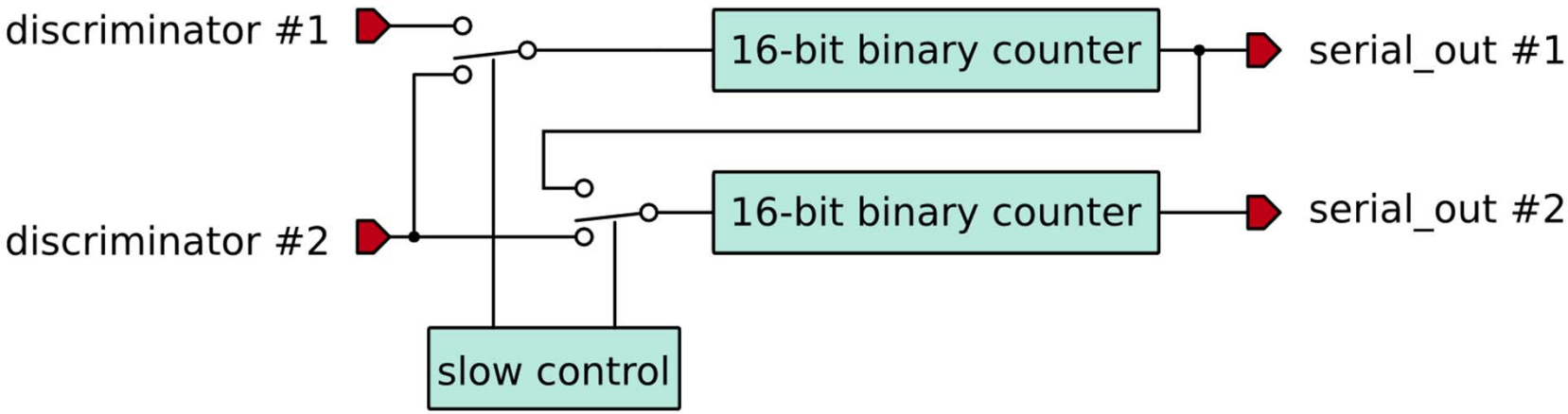
Correction DACs
- threshold low: 7-bits
- threshold high: 5-bits



Input PMOS transistor:
W/L = 30/0.18, Id=2.5 μA

Differential threshold,

Two 16-bits counters in each pixel



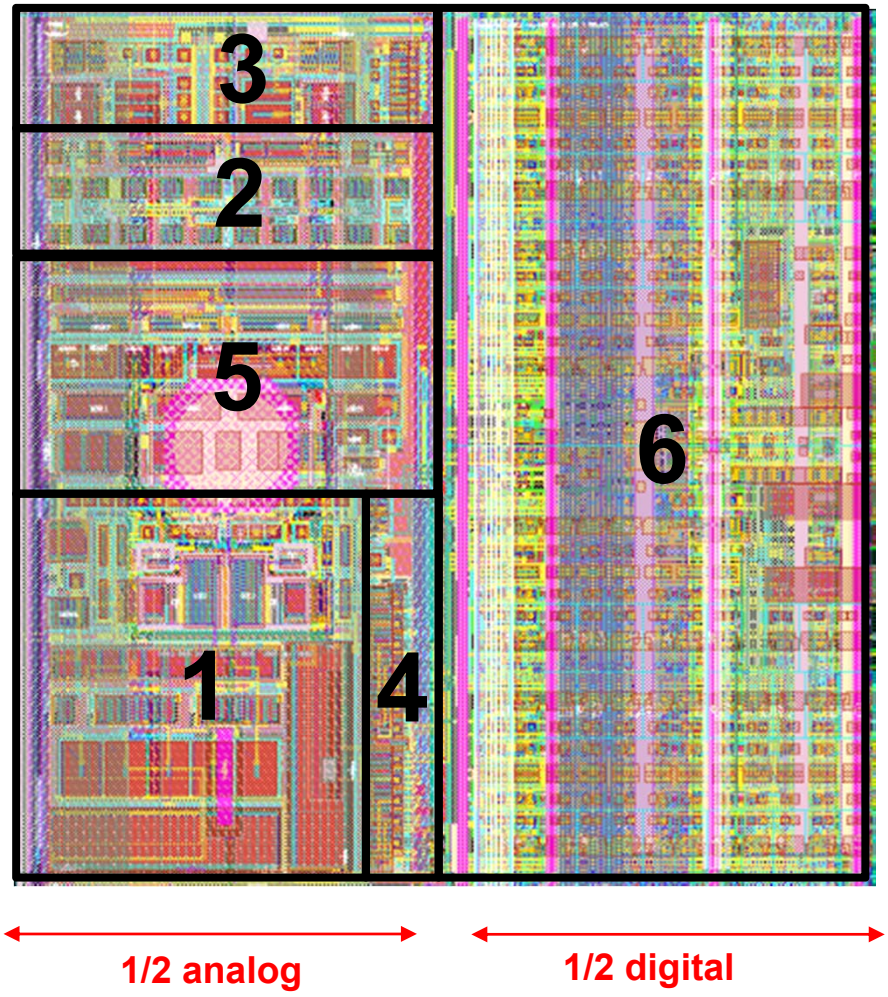
Three different modess:

STANDARD MODE WITH ENERY WINDOW:
discriminator1 ⇒ counter1 (16 bits), discriminator2 ⇒ counter2 (16 bits),

STANDARD MODE WITH SINGLE THRESOLD AND LONG COUNTER:
discriminator1 ⇒ counter12 (32- bits) or discriminator2 ⇒ counter12 (32- bits) – test, correction procedure

CONTINOUS MODE WITH SINGLE THRESOLD:
Phase 1 : discriminator1 ⇒ counter1 (M-bits), counter2(M-bits) ⇒ data readout
Phase 2: discriminator1 ⇒ counter2 (M-bits), counter1(M-bits) ⇒ data readout
Number of readout bits M can be controlled 1-16 to increase the frame rate

Layout of single pixel: 100 μm x 100 μm



Blocks in single pixel (MET4-MET6 are removed):

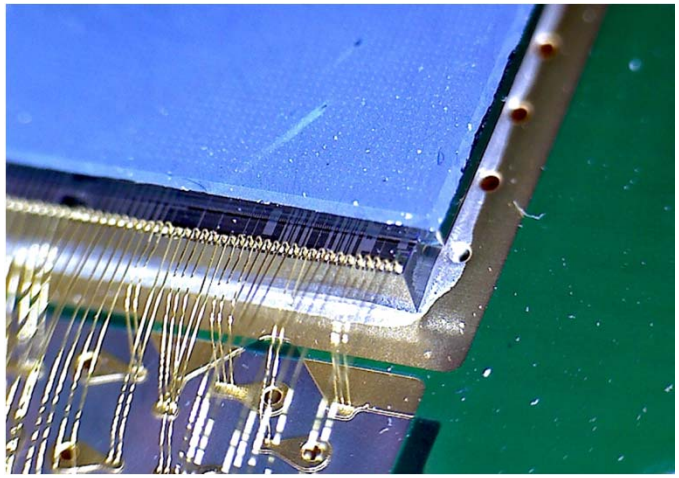
1 - CSA & CSAREF,
2 - shapers,
3 - discriminators,
4 - trim DACs & test injection,
5 - reference blocks,
6 - counters and registers

Additional layout rules:

- **ELT for NMOS**
- **Guardrings**
- **All digital blocks in deep N-well**
  Round detector bonding pad ϕ = 13 μm

Tests

power consumption, functionality



The following tests were performed for PXD18k IC:

- static and dynamic power consumption,
- functionality of the digital block,
- effective threshold spread and its correction,
- gain measurement and noise performance,
- crosstalk in continuous readout mode.
- high count rate tests,

Power supply voltage:

- analog part: 1.2 V (CSA input) and 1.8V
- digital part: 1.2V (core) and 1.8V (LVDS)

Power consumption per pixel:

23 μW/pixel (analog part)

Functionality: OK.

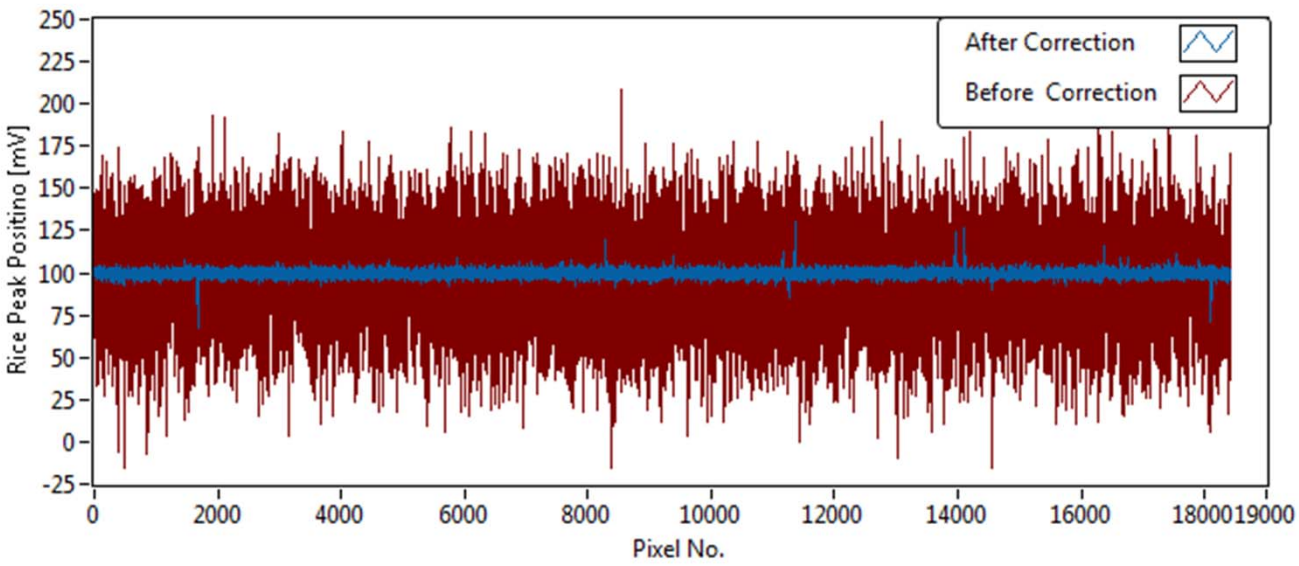
LVDS input/output;

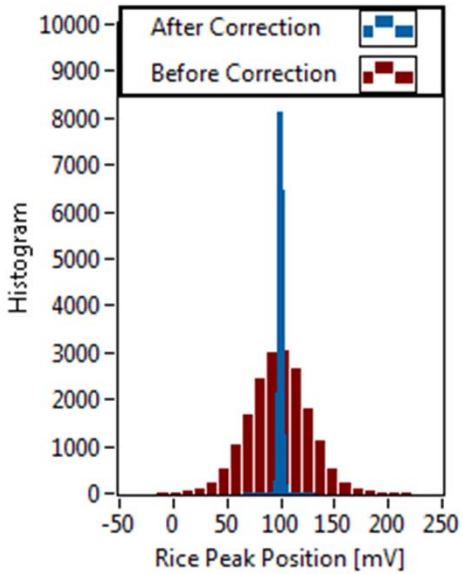
nominal frequency of 100 MHz

Photo: chip with bonded detector

DC offsets

before and after correction





Before sd = 26.9 mV

After sd = 1.79 mV

calculetd to the input 42 el. rms

Comments:

1) automatically in LabView software

2) correction time: 20 – 40 sec

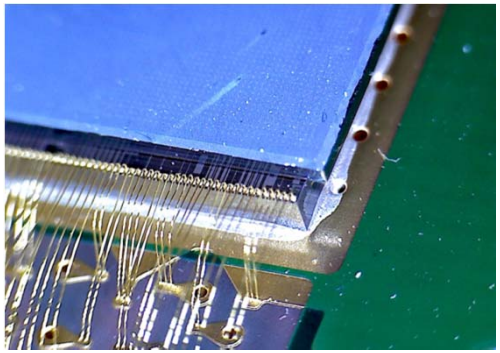
3) correction point:

a) maximum of noise hit

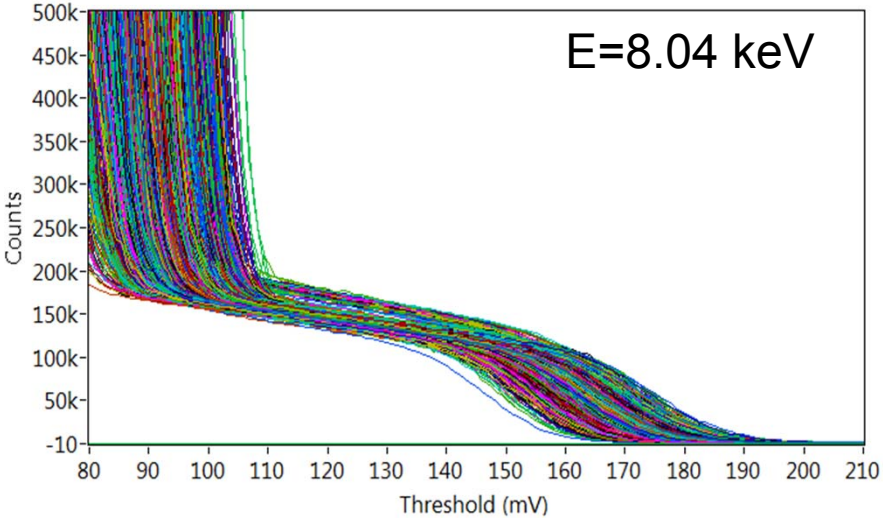
b) minimum threshold for zero noise hit

c) given X-ray energy

Noise and gain:
calculated using X-ray source



Threshold scan of **18.432 pixels**



$$f(x) = \frac{a}{2}\left(1 - \mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right)(bx + c)$$

a - average number of input pulses of given energy,
μ - threshold of the pixel for the given X-ray energy,
σ - related to the electronic noise and energy spectrum,
(*bx*+*c*) - linear term to model the charge sharing.

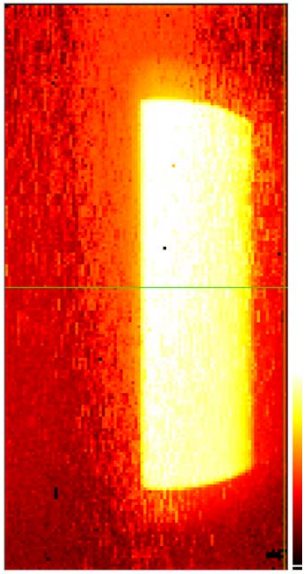
Gain:

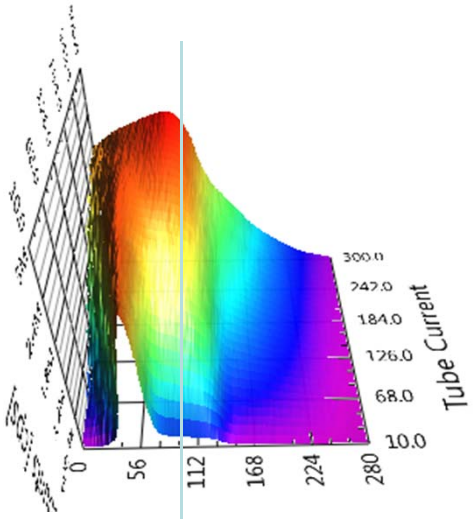
Average: 42.5 μV/el.
Sigma: 5 μV/el.

Noise:

Connected to the the detector:
Average: 168 el. rms
Sigma: 17 el. rms

Tests for high count rate performance (Cu X-ray tube)

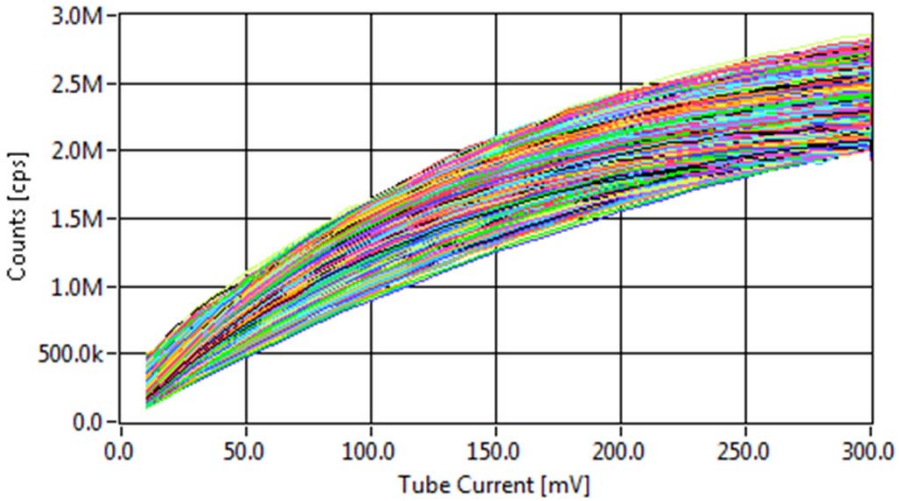


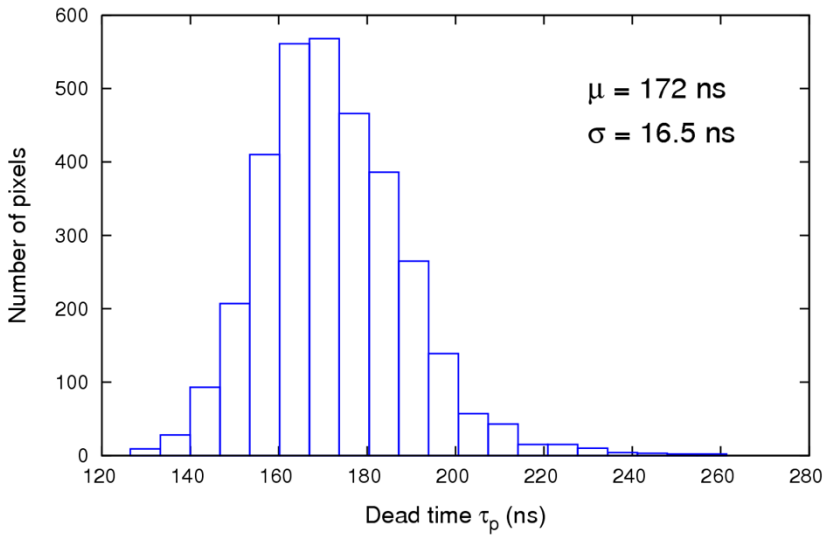


1. X-ray tube with Cu anode (8 keV) operated at 30 kV and the current was changed in the range from 10 mA up 300 mA with a step of 10 mA
2. The illuminated detector area with the input pulse rate above 5 Mcps ⇒ 3300 pixels
3. The threshold scans for nominal setting in bias current of CSA feedback: *Ikrum* = 20 nA.
4. Model of paralyzable photon counter

$$N_{reg}(f) \sim \exp(-f\tau)$$

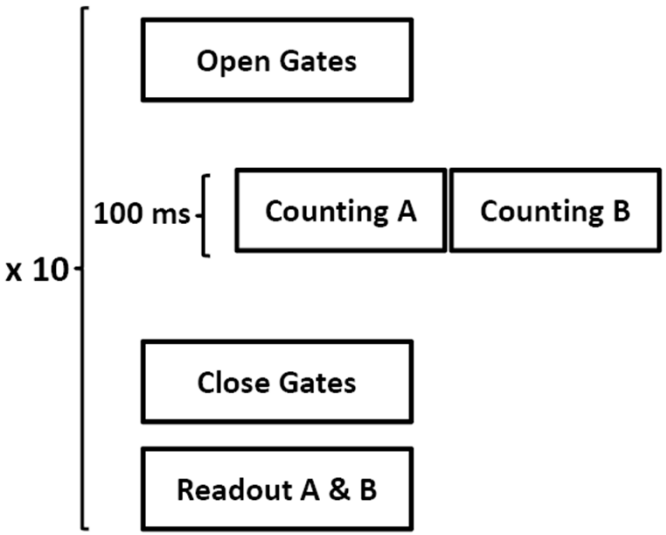
Threshold set at half of X-ray energy



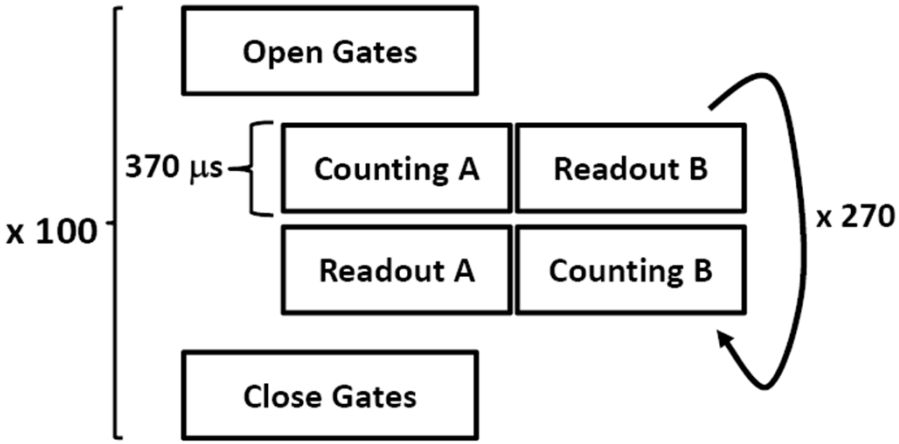


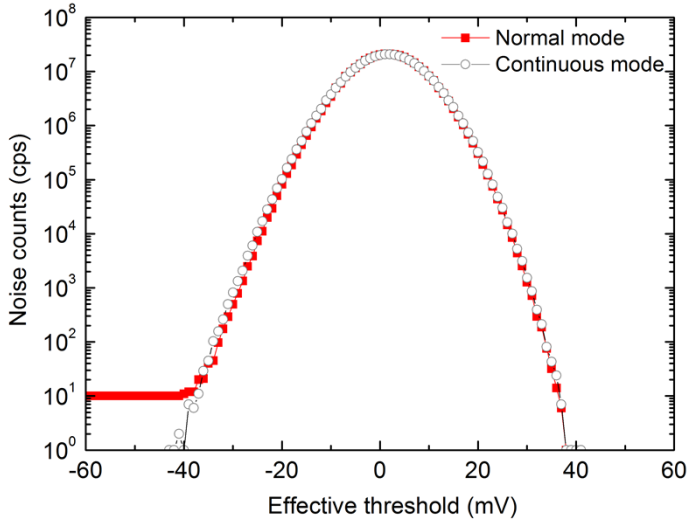
Tests for digital crosstalk in continuous mode of operation (noise counting)

Standard mode



Continuous mode





Continous mode of operation:
Zero dead time:
without noise increase

Frame rate depends on:
N-bits/pixel, and bias voltage of digital core

VddCORE = 1.2 V

N- bits	Frame rate
16	2720
13	3110
10	3620
7	4340
4	5410

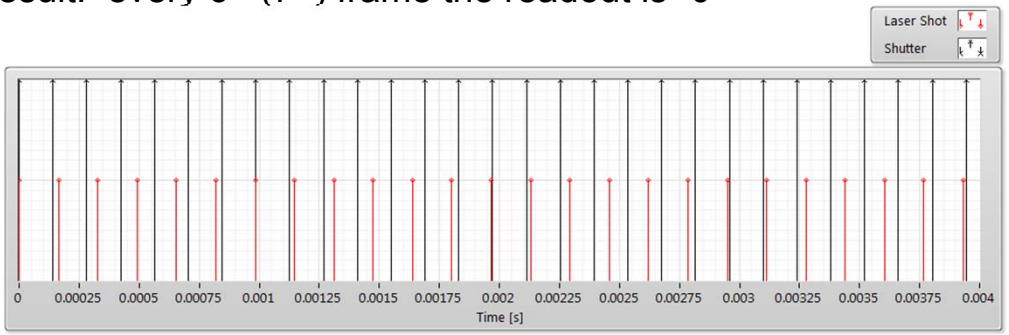
VddCORE = 1.8 V

N- bits	Frame rate
16	2720
11	3620
6	5400
4	7100

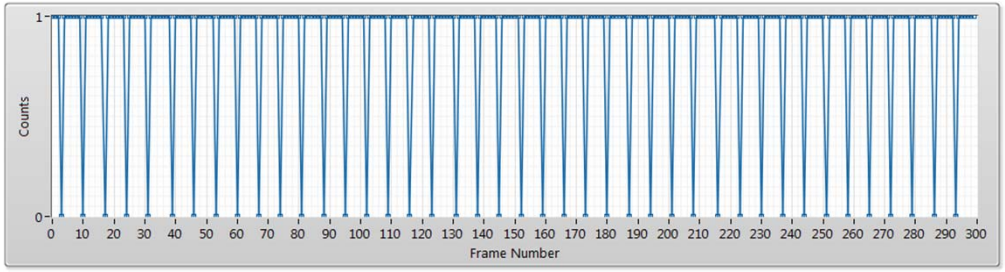
Tests with femtosecond laser

To confirm the proper operation of the circuit with high frame rate we also performed the test with a femtosecond fiber laser Calmar OPP-UTF01 (λ = 1060nm), which is equipped with a pulse picker, and allows controlling the frequency of incoming pulses.

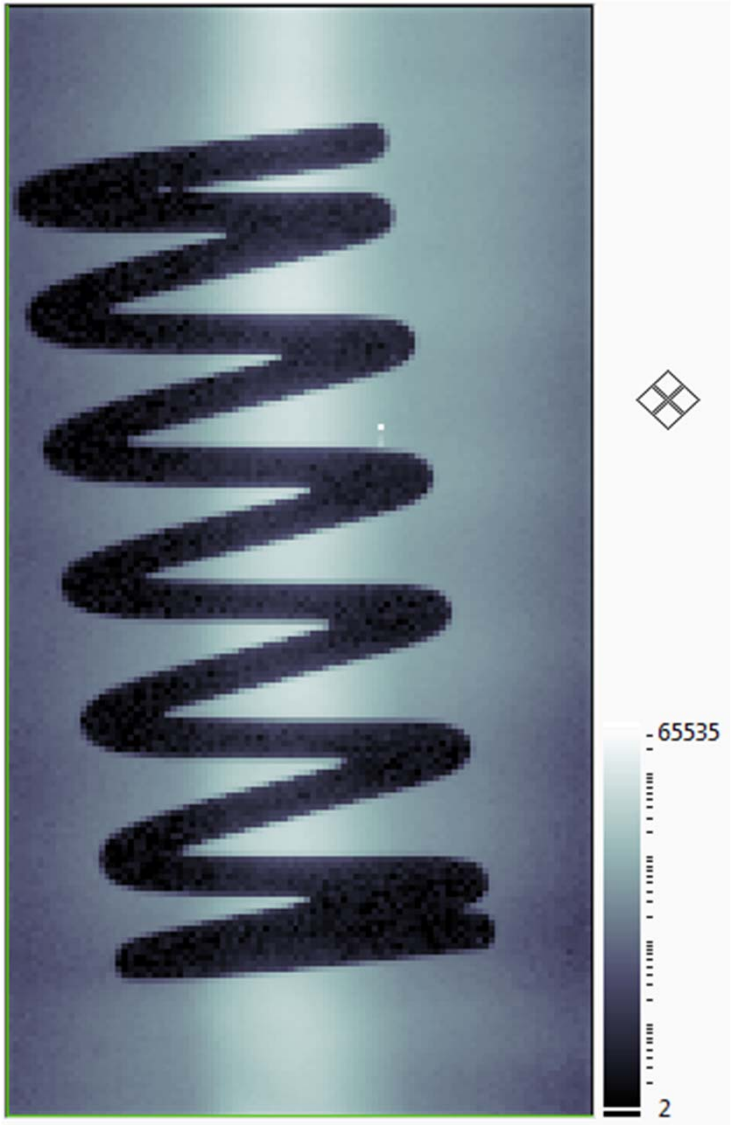
Simulations:
- laser sends pulses (pulse width 2ps with frequency of 6.103 kHz
- frame rate of PXD18k (4-bit/pixel) is 7.1 kHz
- result: every 6th (7th) frame the readout is ”0”

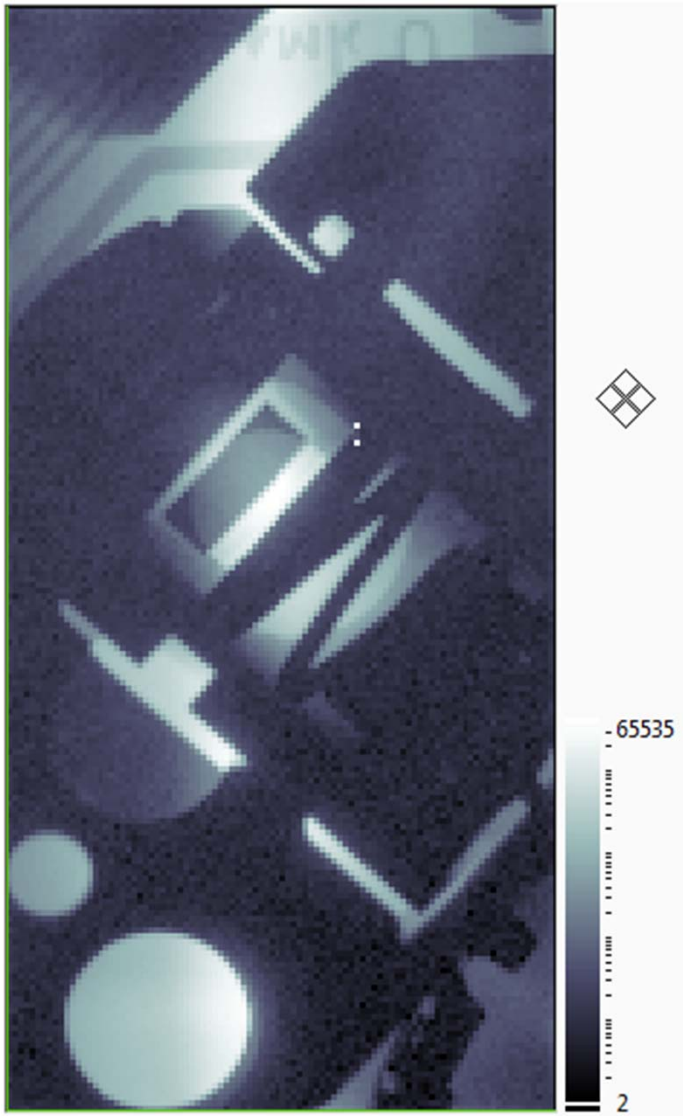


Measurements:
- result: every 6th (7th) frame the readout is ”0”



Example of X-ray image





COMPARISON OF COUNTING PIXEL CHIPS IN SUBMICRON TECHNOLOGY

Chip	Medipix II	Pilatus 2	XPAD3S	Eiger	PXD18K
Technology	250 nm	250 nm	250 nm	250 nm	180 nm
Chip area [mm^2]	16.1×14.1	17.5×10.5	17.4×10.4	19.3×20.1	9.46×20
Pixel matrix	256×256	60×97	80×120	256×256	192×96
Pixel size[μm^2]	55×55	172×172	130×130	75×75	100×100
Power per pixel [μW]	8*	10	40	8.8	23
Noise [e^- rms]	141	123	127	180	168
Offset spread after correction [e^- rms]	100	10	57	20	42
Count rate per area [photons/mm^2s]	33×10^6	101×10^6	59×10^6	–	350×10^6
Double threshold	Yes	No	No***	No	Yes
Counters per pixel	1 ×15 bit	1 × 20 bit	1 × 12 bit	1 × 12 bit	2 × 16 bit
Continuous readout	No	No	Yes	Yes	Yes

* only analog part

** count rate in both cases is about a few Mcps/pixel,

***version XPAD3C has double threshold.

Pixel prototypes in new technologies
(90 nm, 3D)

Deep submicron technologies

For example CMOS 90 nm – since 2009 avialable via EUROPRACTICE

Deep submicron technologies offer very good density of transistors in digital blocks and good digital functionality, however the question is still open concerning the analog blocks and their critical parameters. Without prototyping it is difficult to answer if there are significant benefits from using these technologies and what new possibilities they present for readout electronics used in hybrid semiconductor detectors. **Our task was to design a prototype integrated circuit of pixel architecture in deep submicron technology (90 nm CMOS) for the mentioned applications and measure its critical analog parameters like noise, matching and digital crosstalk.**

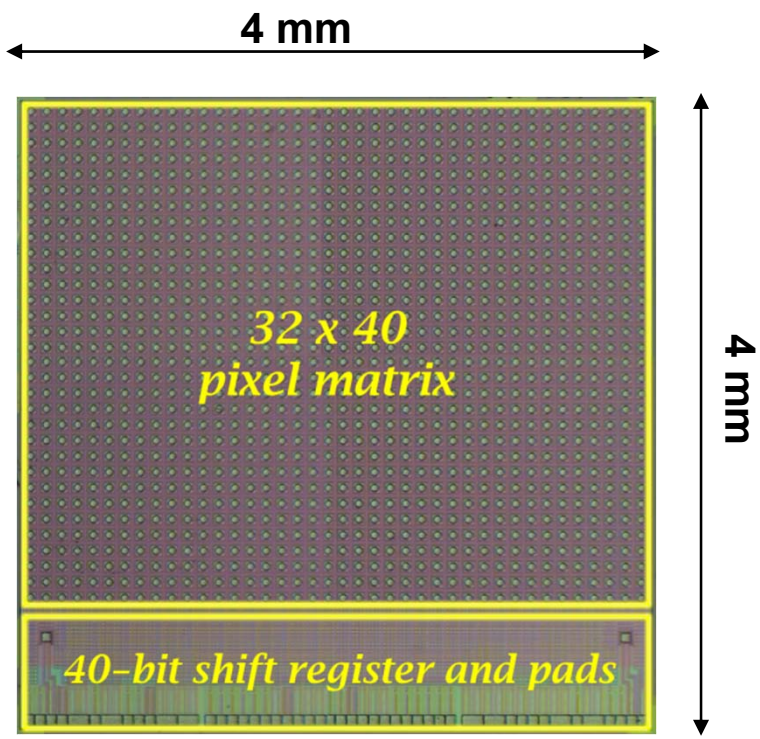
Architecture of prototype chip – TSMC 90 nm

- Prototype readout chip for hybrid pixel detector (X-ray imaging applications: 8 keV)

- Functionality:
  - single photon counting,
  - energy window,
  - continuous readout

- Critical parameters:
  - pixel size 100x100 um^2,
  - noise - matching – high count rate

- Submicron technology (CMOS 90 nm):
  - the first prototype PX90 – 2009
  - the second prototype **FPDR90 – 2010/2011**

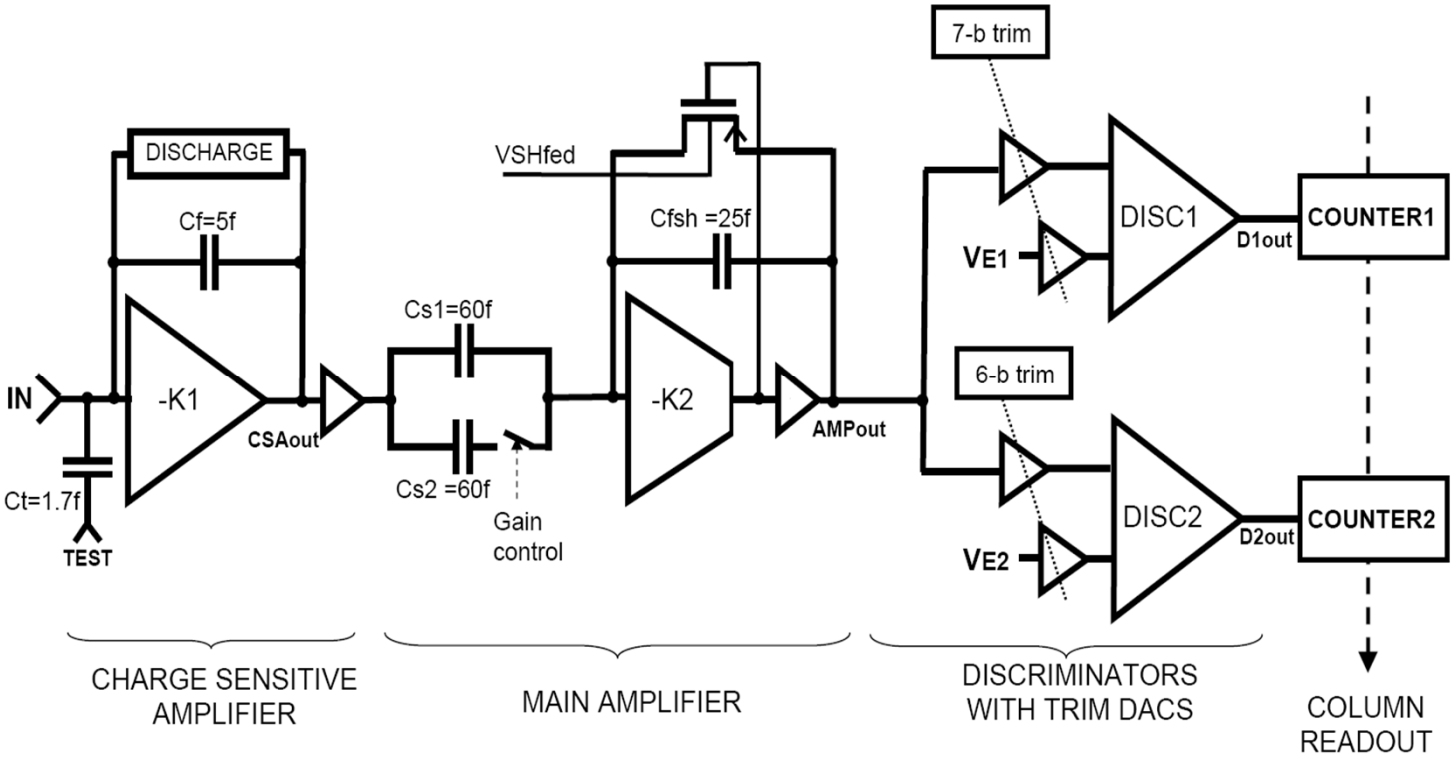


Chip photo

1280 pixels (100x100 um^2)

FPDR90—A Low Noise, Fast Pixel Readout Chip in 90 nm CMOS Technology
Szczygiel, R.; Grybos, P.; Maj, P.
Nuclear Science, IEEE Transactions on
Volume: 58 , Issue: 3 , Part: 3 , 2011 , Page(s): 1361 - 1369

Single channel architecture



Comments:

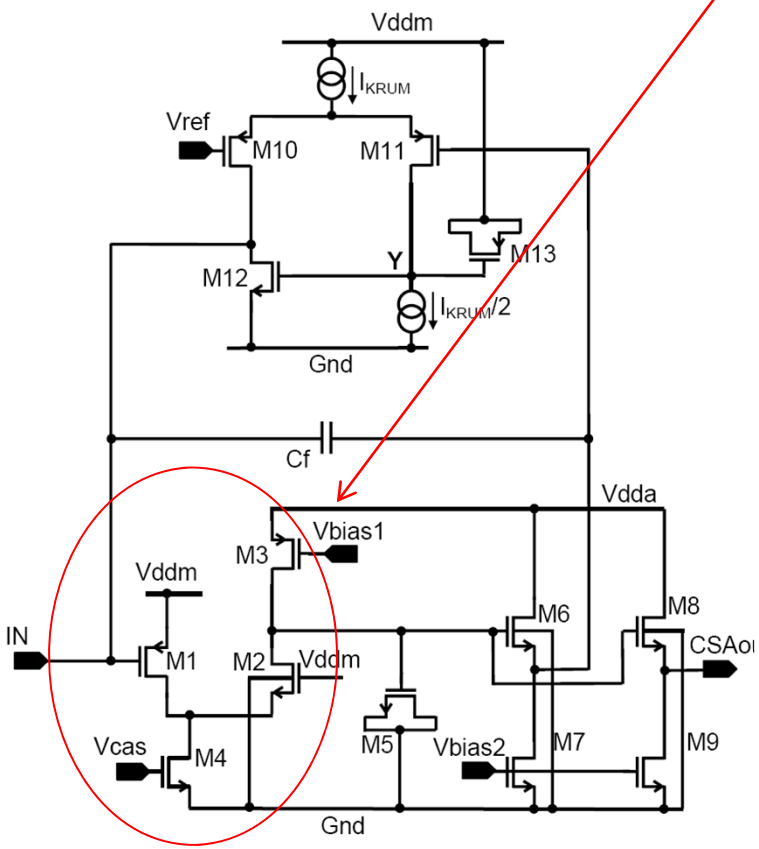
- **single ended CSA and main amplifier (AC coupling)**
- **noise minimization in CSA**
- **main amplifier with feedback bias**
- **offset correction**

Charge sensitive amplifier

Vddm =0.8V
Vdda=1.2V

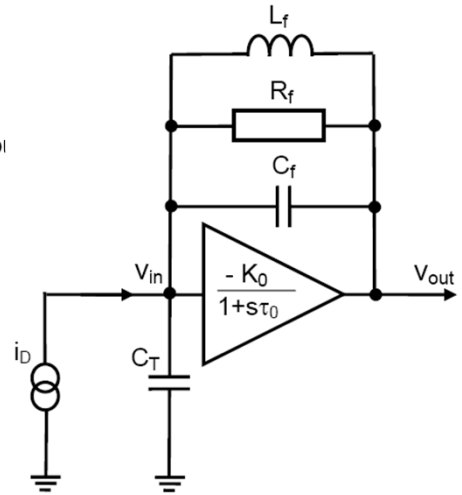
Noise performance .

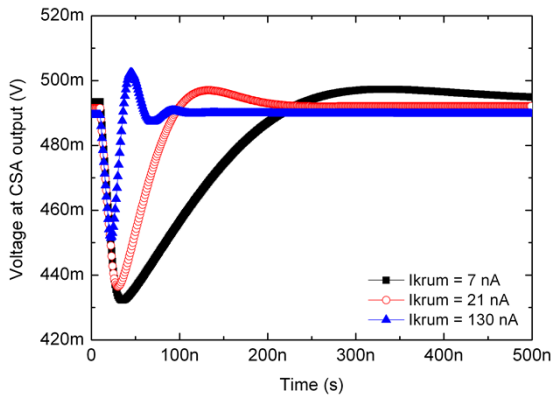
$$\frac{\overline{dv_{core}^2}}{df} \approx \frac{\overline{dv_1^2}}{df} + \frac{\left(g_{ds1}+g_{ds4}\right)^2}{g_{m1}^2}\frac{\overline{dv_2^2}}{df} + \frac{g_{m3}^2}{g_{m1}^2}\frac{\overline{dv_3^2}}{df} + \frac{g_{m4}^2}{g_{m1}^2}\frac{\overline{dv_4^2}}{df}$$



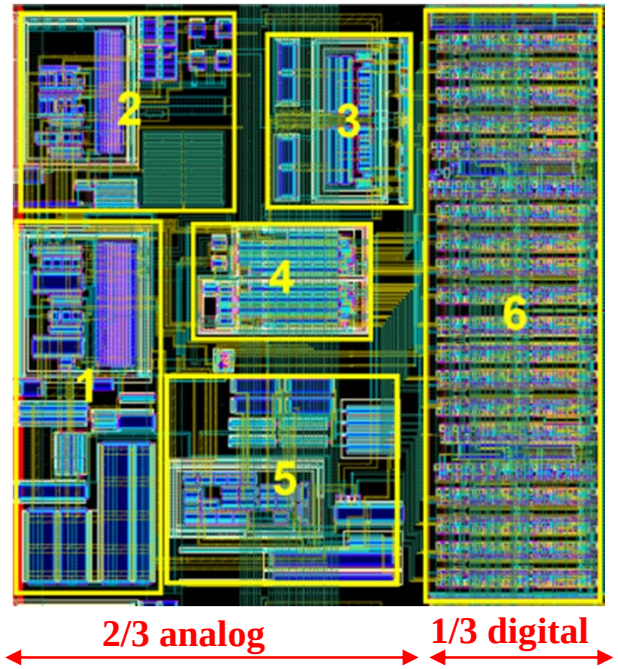
OPERATING POINT OF SELECTED TRANSISTORS IN CSA

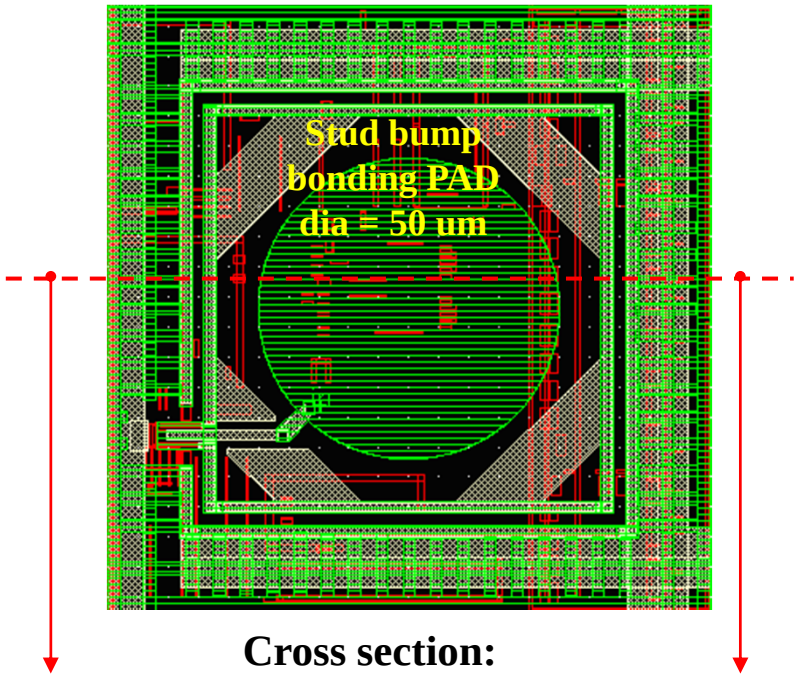
Device	W/L [μm/μm]	I_{DS} [μA]	g_m [μA /V]	g_{ds} [μA /V]	I_F
M1	20/0.2	5.06	124	3.73	0.273
M2	5/0.2	1.07	27.3	0.87	0.076
M3	2/3	1.07	11.1	0.19	8.67
M4	1.44/20	6.13	6.7	10.2	151



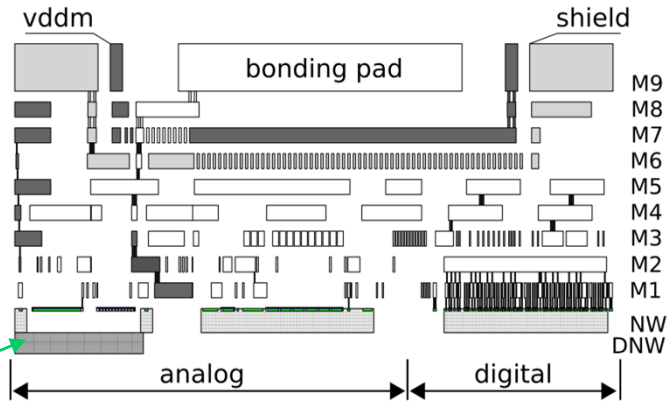


Layout of single pixel





Cross section:



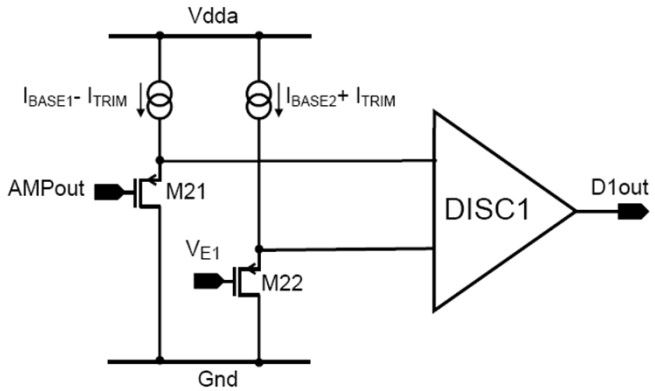
Blocks in single pixel
(MET4-MET9 are removed):

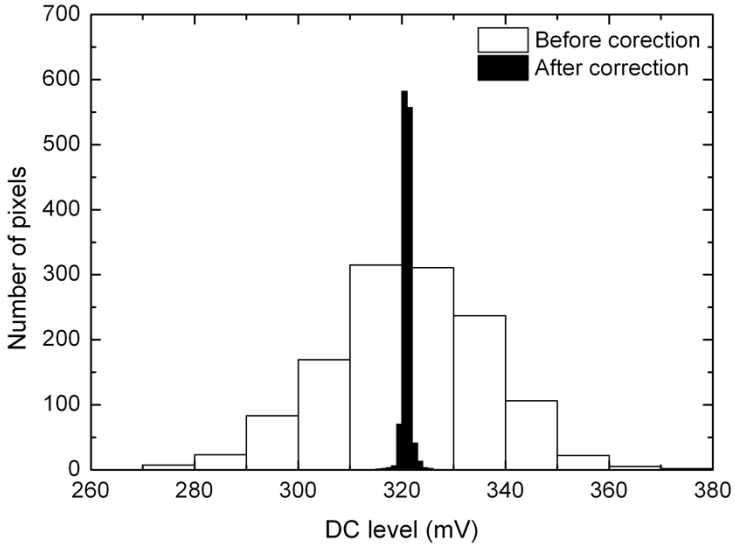
1 - CSA ,
2 – main amplifier,
3 - discriminators,
4 - trim DACs,
5 - reference blocks,
6 - counters and registers

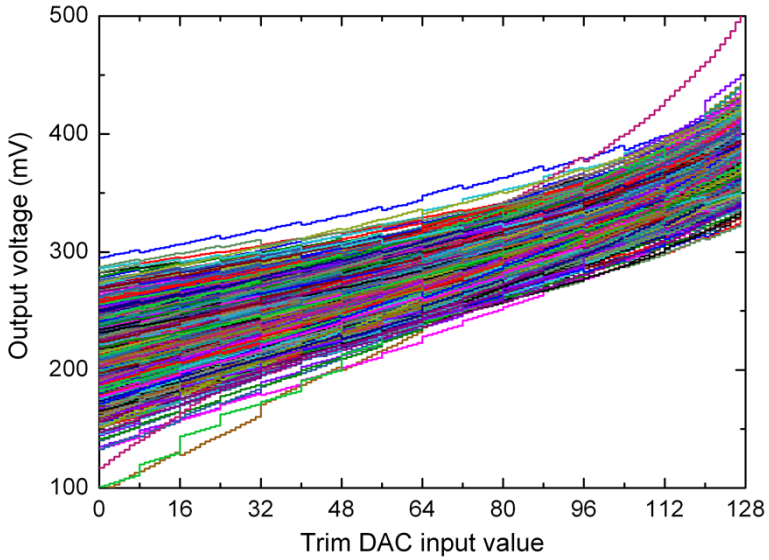
Input pad capacitance ~80 fF

NMOS transistors in Deep N-WELL

Trim DACs – offset correction



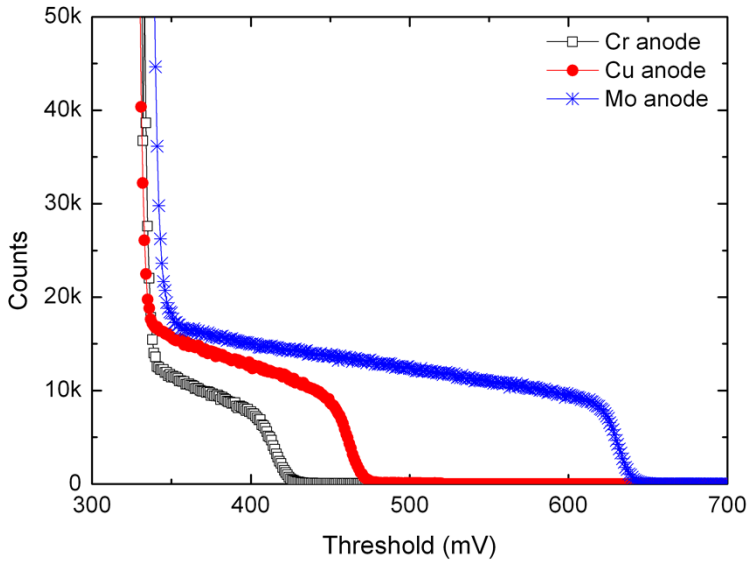


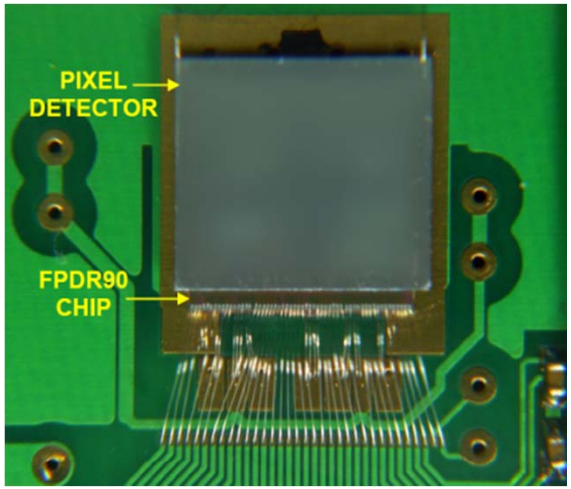


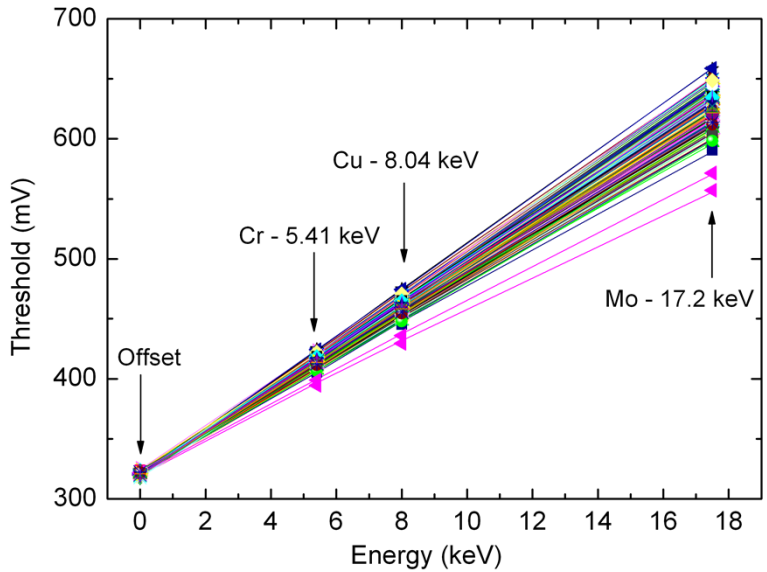
Results:
- before correction: sd = 15 mV
- 7-bit trim: sd = 0.76 mV (12 el. rms)
- 6-bit trim: sd = 1.19 mV

Comments:
- changing trim DAC value does not change power consumption of PUC,
- range of trim DAC is controlled by external resistors

Measurement with X-ray tube







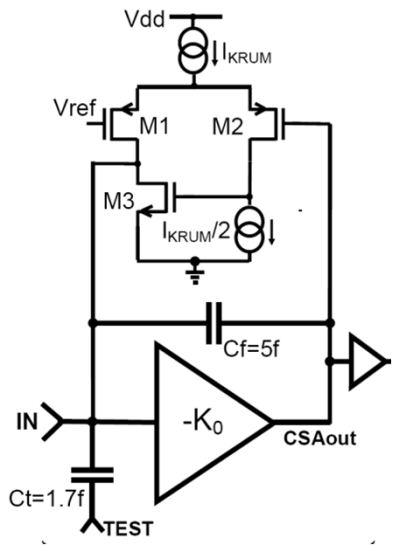
GAIN:

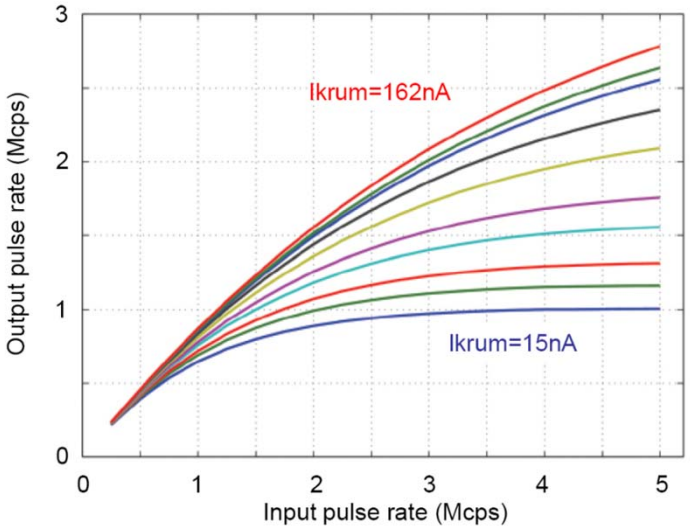
- **high gain mode: 64 uV/el (sd = 2 uV/el)**
- **high gain mode: 32 uV/el (sd = 1.2 uV/el)**

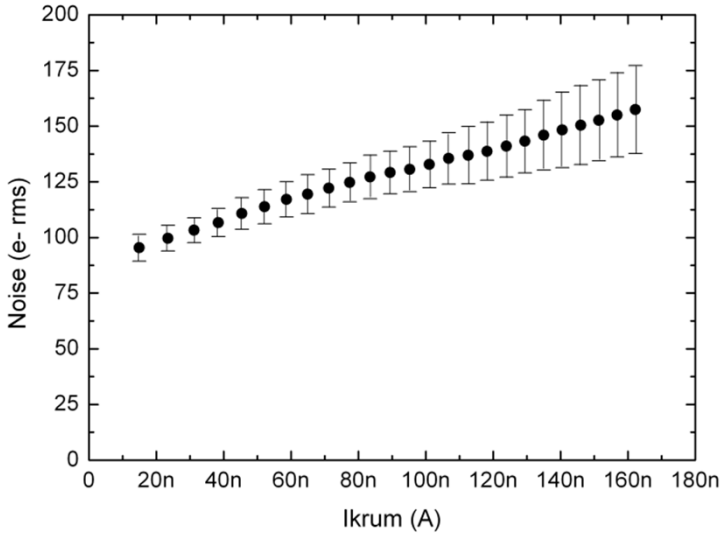
NOISE (high/low gain)

- **pixel connected to the detector: 106/107 el rms.**
- **pixel not connected to the detector: 91/95 el rms.**

Tests for high count rate performance (Cu X-ray tube)





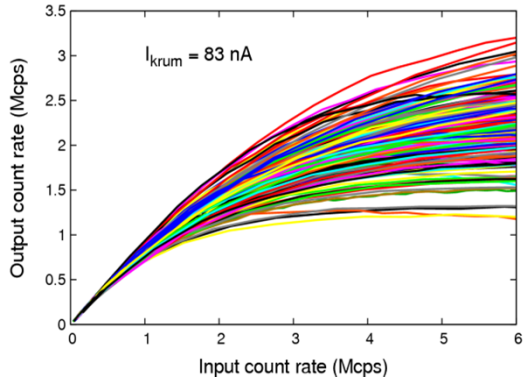


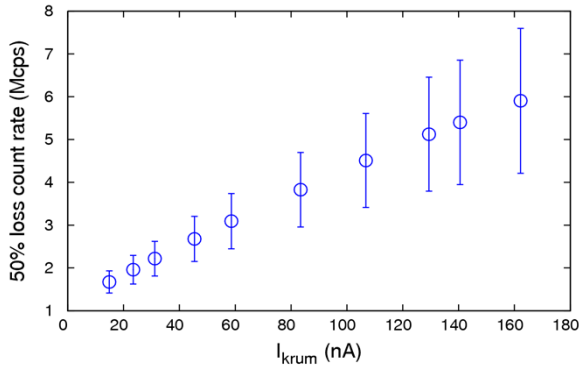
With stud-bonded detector

Low Ikrum=15nA (gain/ENC)

32.2 μV/e– /95 e– rms

Spread of count rate

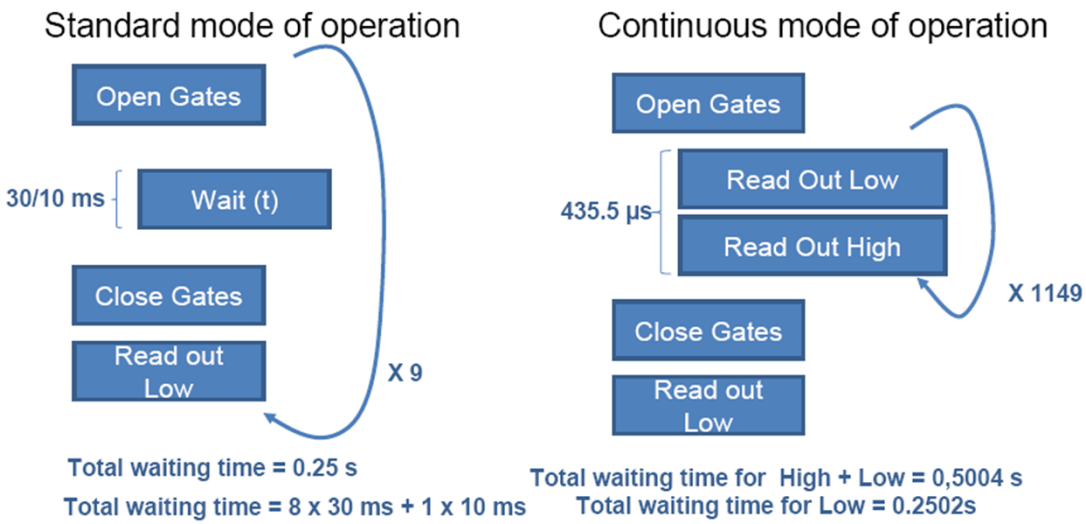


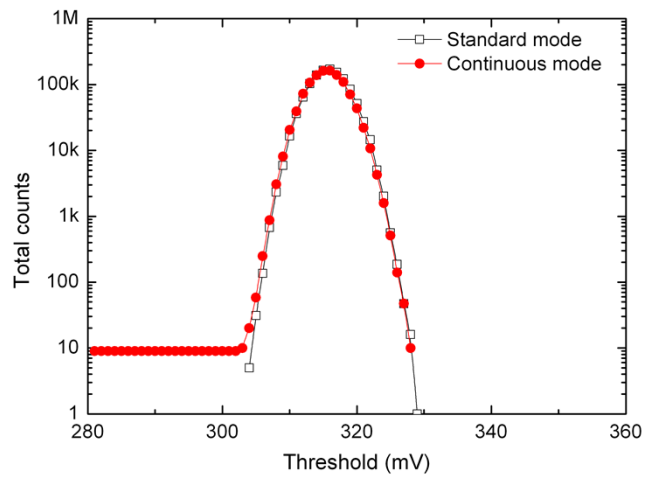


High Ikrum= 162nA (gain/ENC)

7.5 μV/e– /157 e– rms

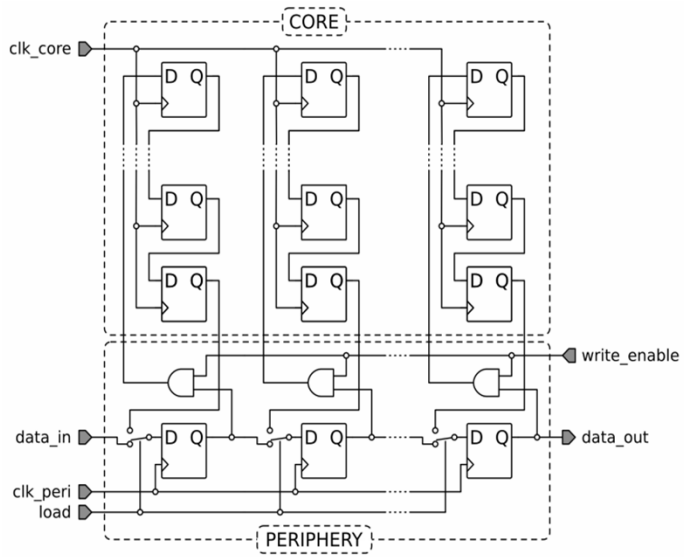
Continuous mode of operation

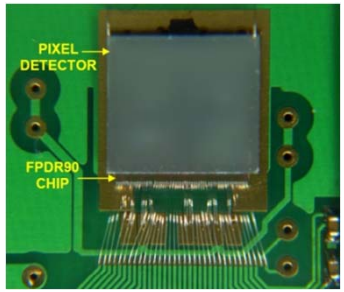


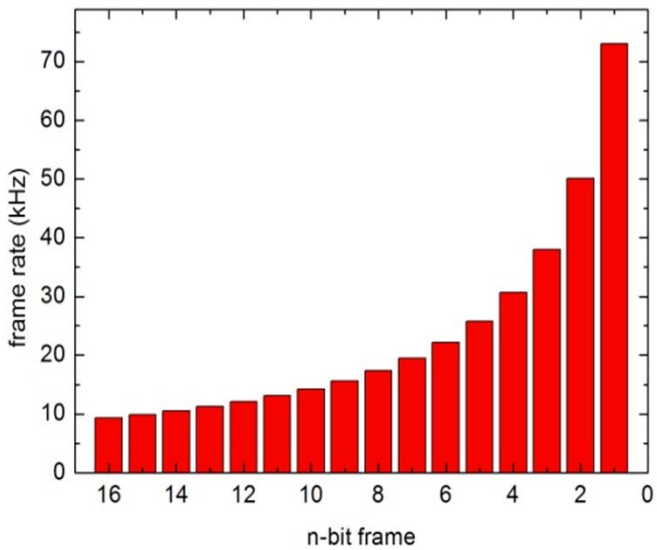


Digital part of the chip

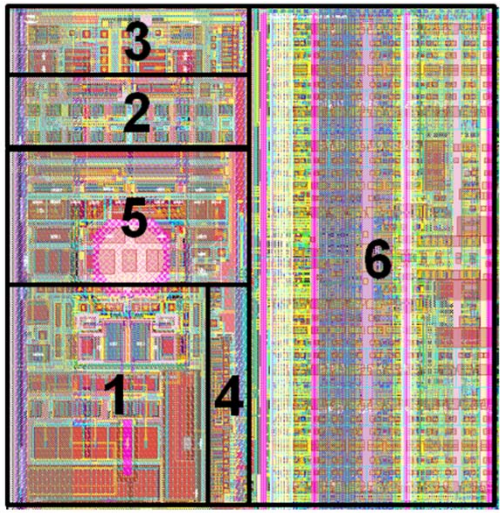
The prototype has only one data output (200 MHz)



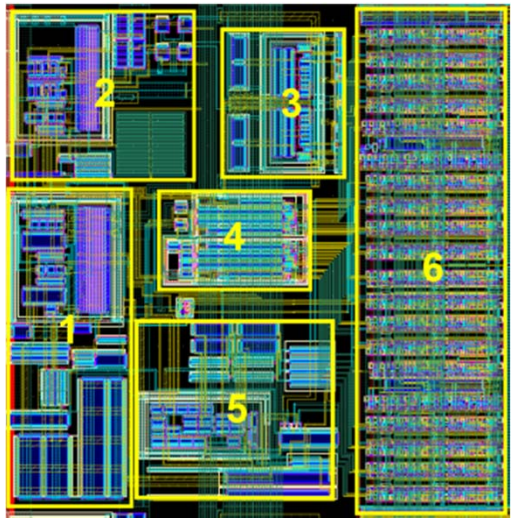




Conclusions from 90 nm prototype (pixel 100 x 100um^2)



UMC 180nm



TSMC 90nm

1. Analog parameters

Noise = 106 el. rms
Offset spread = 12 el. rms
Dead time = 117 ns
Max count rate > 5Mcps/pixel

2. Digital parameters

Density – 2x better compare to 180 nm

3. Technology characterisation

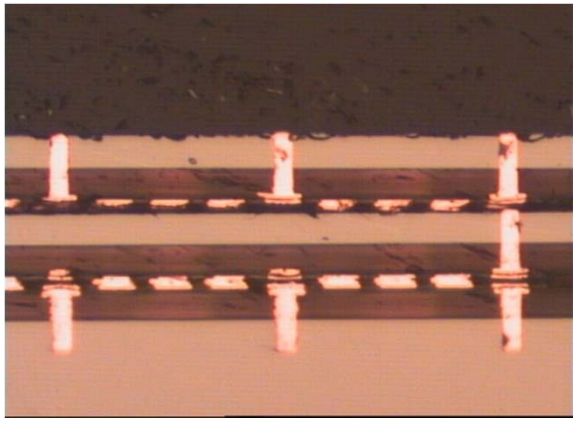
TSMC 90 nm – one of the best as we have ever used,
Deep N-well consumes a lot of extra area

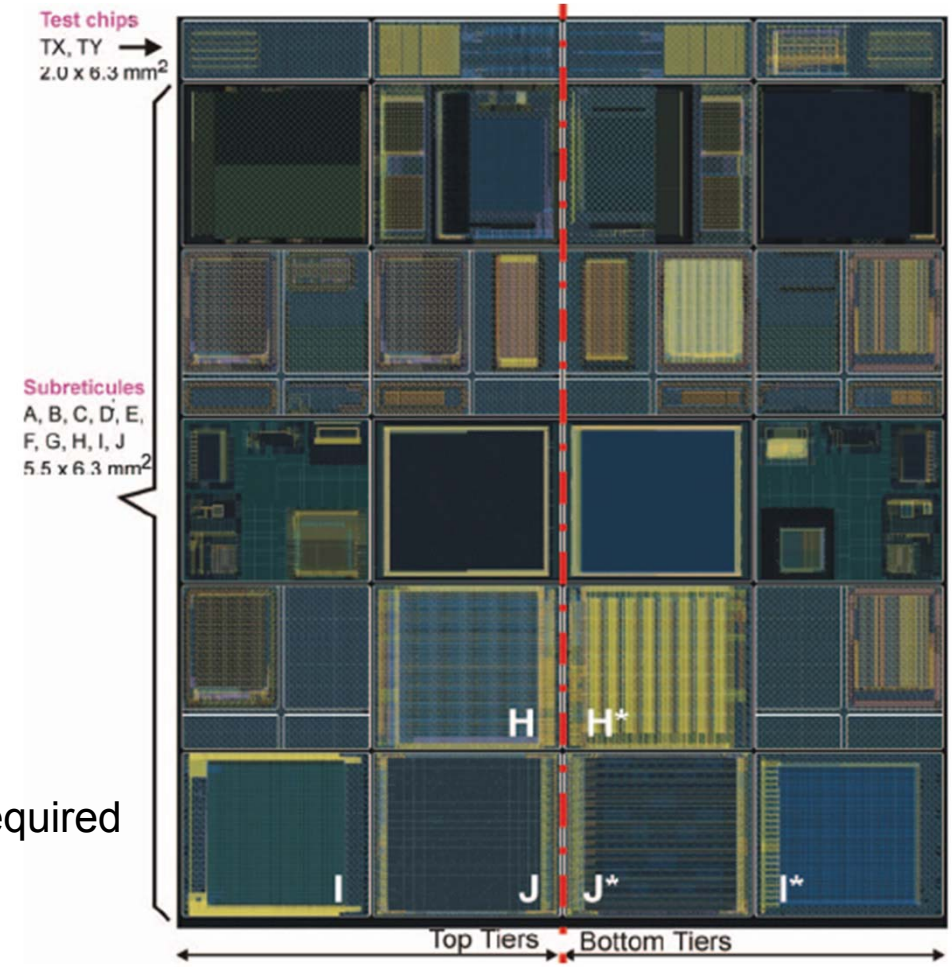
4. Main problem

Cost of enginnering run

MPW in 3D technology organized by FNAL

(17 member groups: France, Italy, Germany, Poland, Canada, USA)





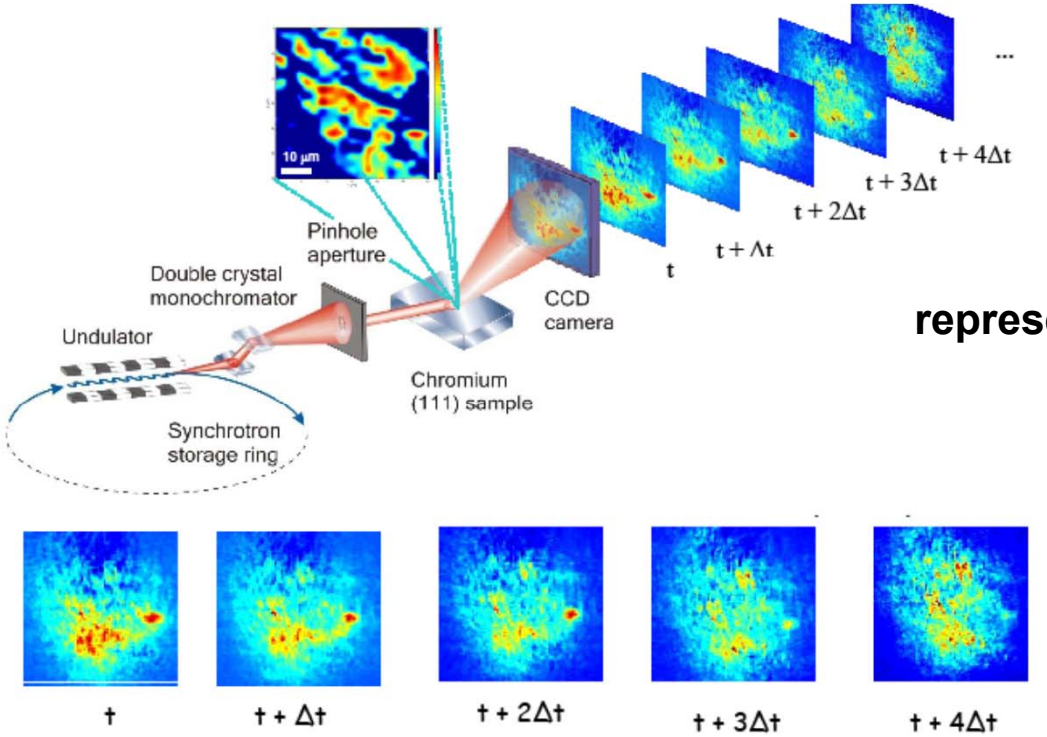
Tezzaron Semiconductor, USA

2 layers face to face: CMOS 130 nm
TSV 1.3 μm in diameter,
6 μm deep and 3.8 μm minimum spacing is required

VIPIC IC - 3D Pixel Chip

FNAL, USA
AGH UST, Poland
BNL, USA

Application: X-ray Photon Correlation Spectroscopy



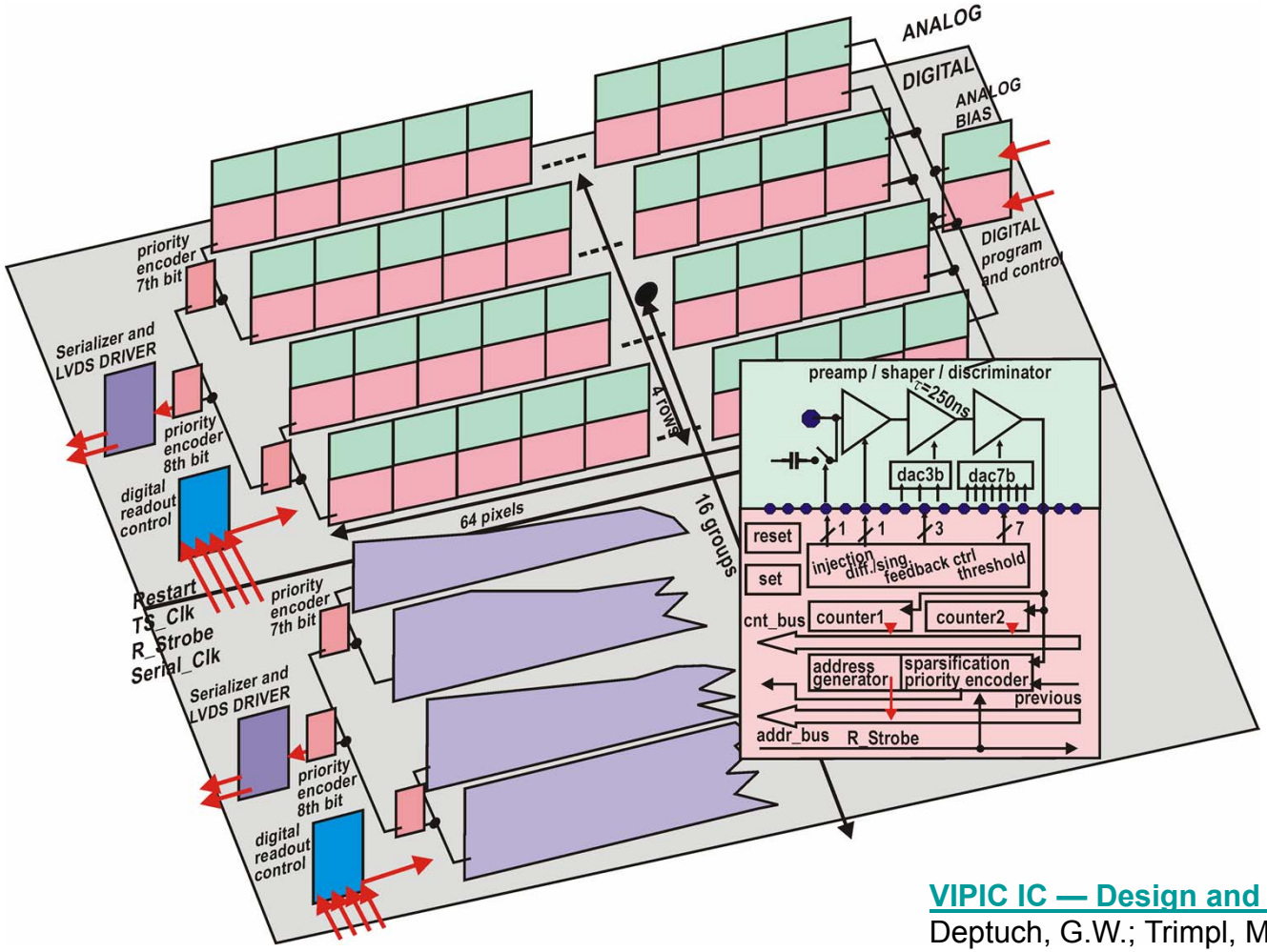
O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

final results are not actual images but mathematical representation of autocorrelation series computed per spatial position

the speckle pattern changes

Architecture of VIPIC

VIPIC = Vertically integrated Photon Imaging Chip



- 160 ns / hit pixel in sparsified mode
- 50×10^3 frame/s in imaging mode (5 bit counting)

VIPIC IC — Design and test aspects of the 3D pixel chip
Deptuch, G.W.; Trimpl, M.; Yarema, R.; Siddons, D.P.; Carini, G.; Grybos, P.; Szczygiel, R.; Kachel, M.; Kmon, P.; Maj, P.
Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE, 2010 , Page(s): 1540 - 1543

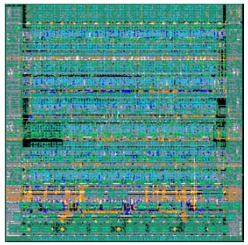
VIPIC chip in collaboration with Fermilab, USA:
2 layers CHRT 130 nm – MPW in 3D consortium

VIPIC chip: 5.1 x 5.1 mm²

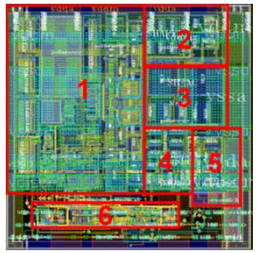
Pixel: 80 x 80 um²

Number of pixels: 64 x 64

Continuous readout

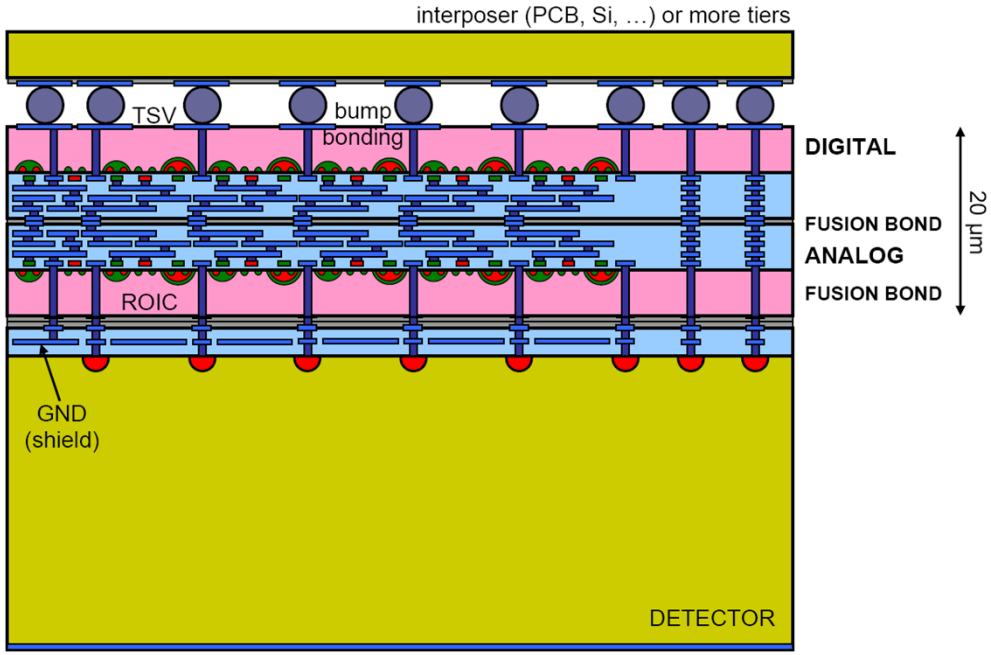


FNAL



AGH

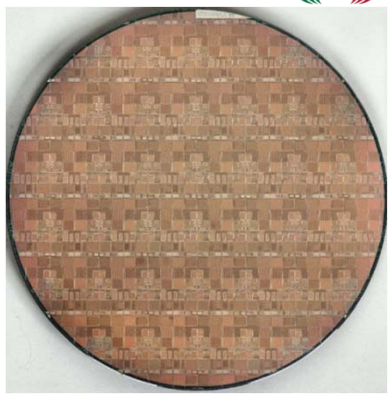
BNL

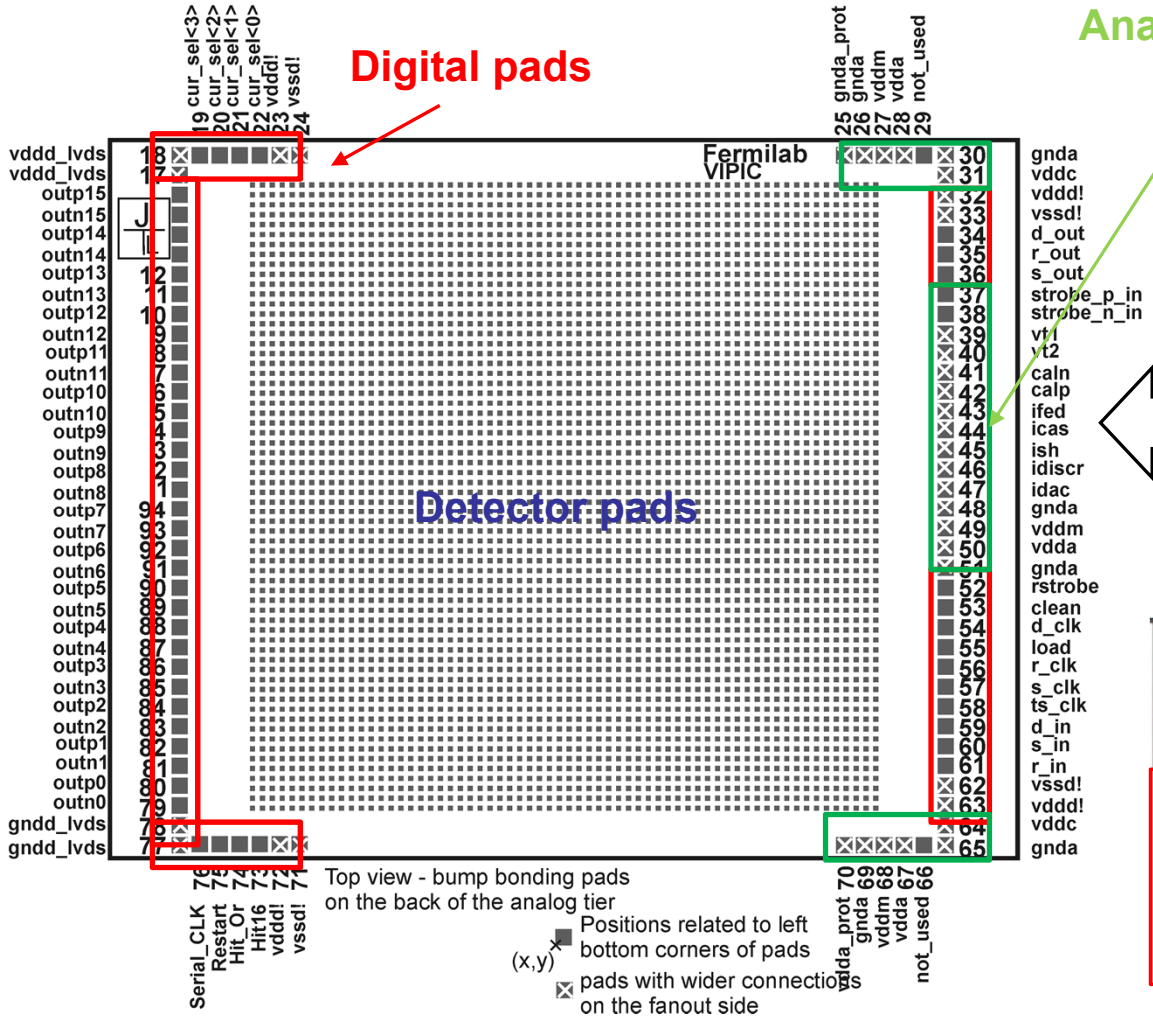


The project aims to build a 4-side buttable pixel detector tile. The detector will be fabricated using the whole available area of a wafer and the chips will be tailed on the detector wafer by fusion bonding.

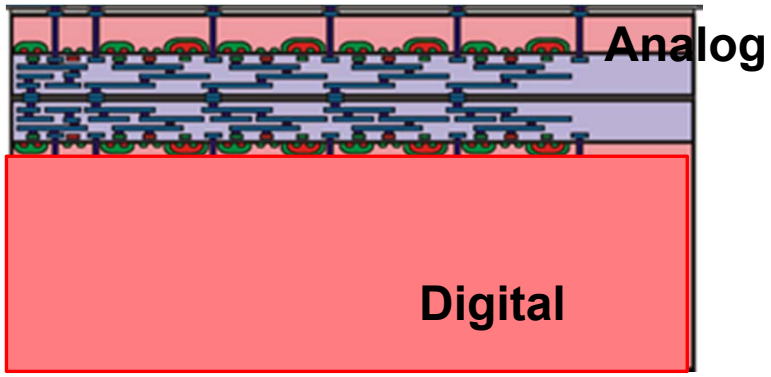
VIPIC IC - Tests of the 3D Pixel Chip

AGH UST - FNAL

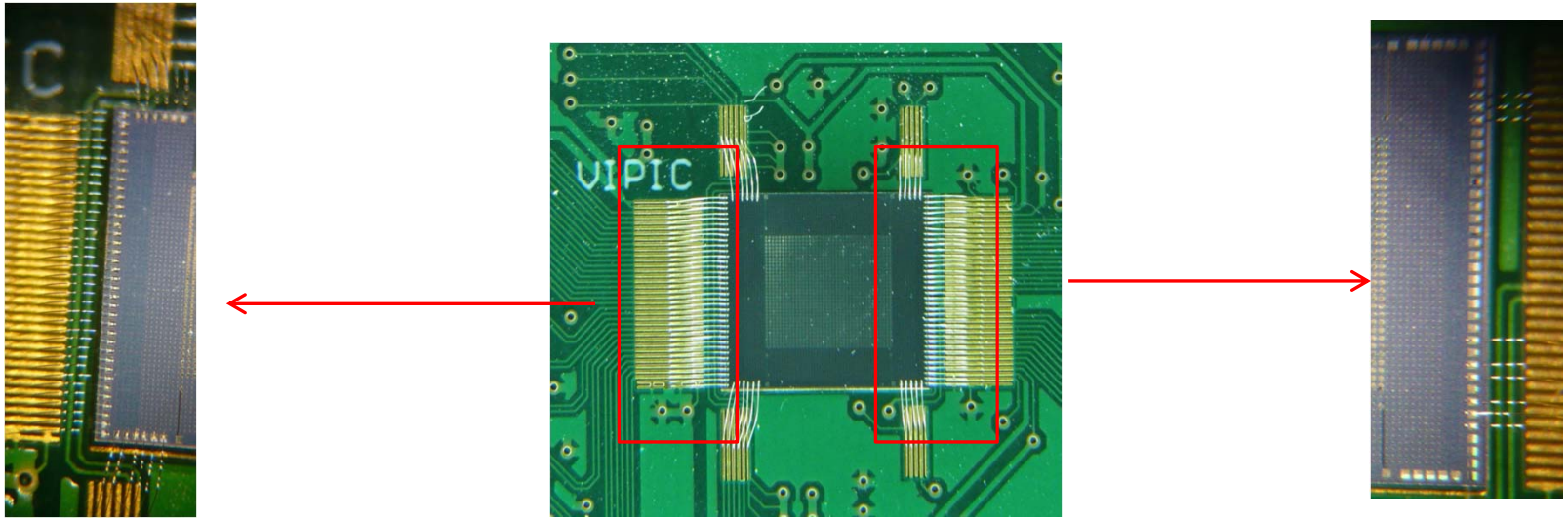




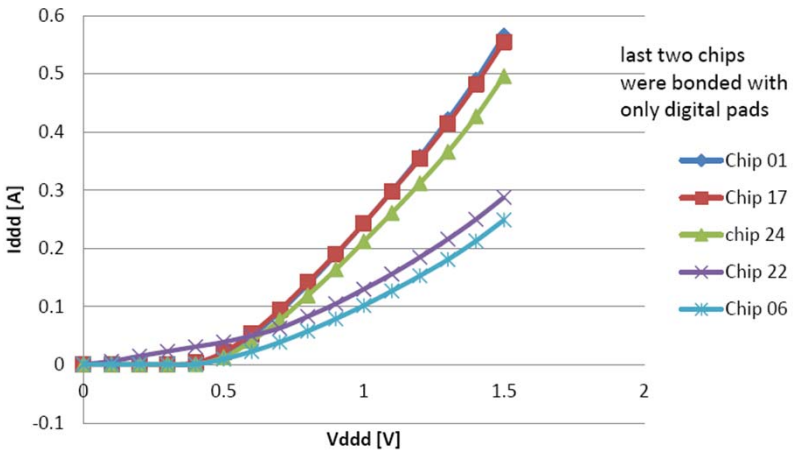
Top view of bonding pads



11 chips => 5 chips were bonded



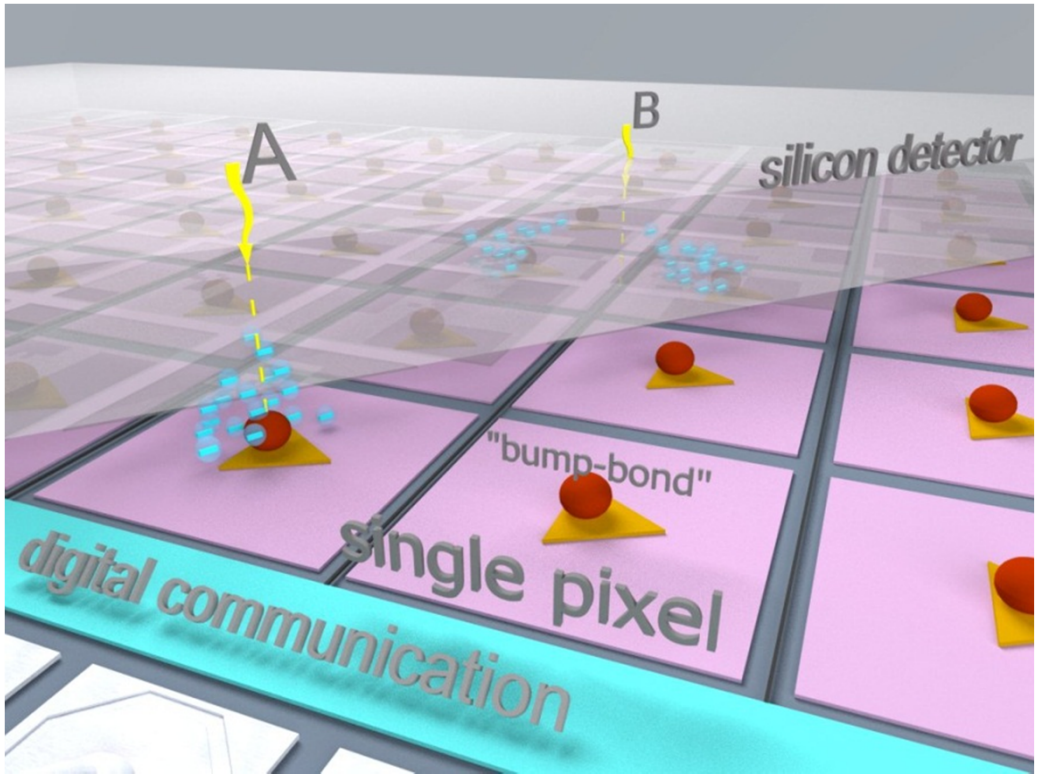
3 chips = all 96 pads were bonded



Submitted to production – May 2009
1st chips – 2011,
2nd –next week

Algorithms to solve the problem with charge sharing

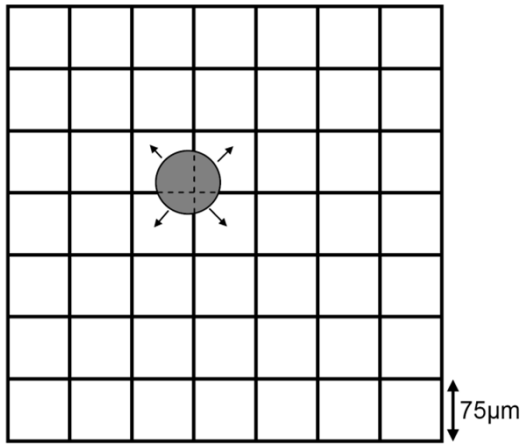
Charge division effect

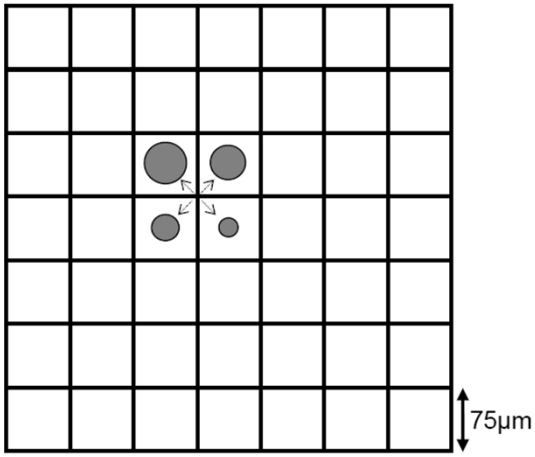


A charge sharing effect is the main limitation of hybrid pixel detectors for using them in spectroscopic applications, noting that this observation applies to both time and amplitude/energy spectroscopy.

The first solution of this problem was proposed by a group from CERN and it was implemented in the Medipix III chip. However, due to pixel-to-pixel threshold dispersions and some imperfections of the simplified algorithm, the hit allocation was not functioning properly [NIMA 636, 2011].

Charge division effect





Our task:

1) **perform proper hit position identification** = hit is assigned to the pixel with a largest deposition

2) use the information from summing (interpixel) nodes for **spectroscopy measurement**,

3) question: if it is possible to **increase a position resolution** in counting systems using a relatively simple algorithm?

Three steps:

- Proper algorithm
- Simulation taking into account hardware limitation (noise and mismatch)
- Possible hardware implementation (architecture, limited silicon area)

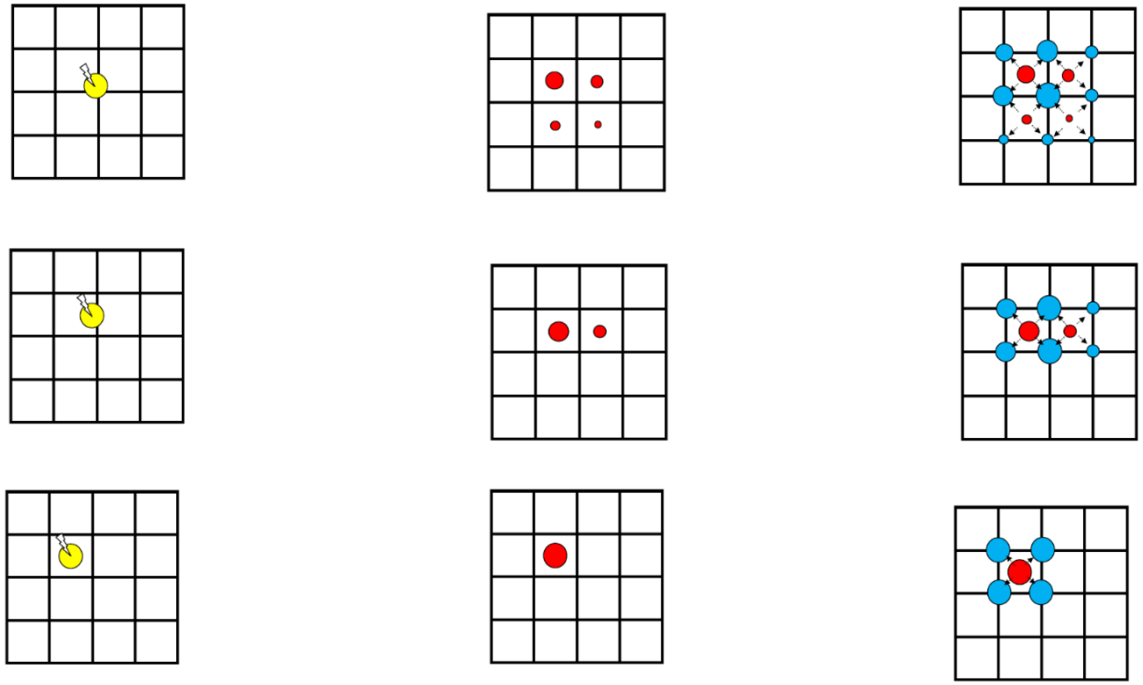
Algorithms: information from two points: single pixel & summing node

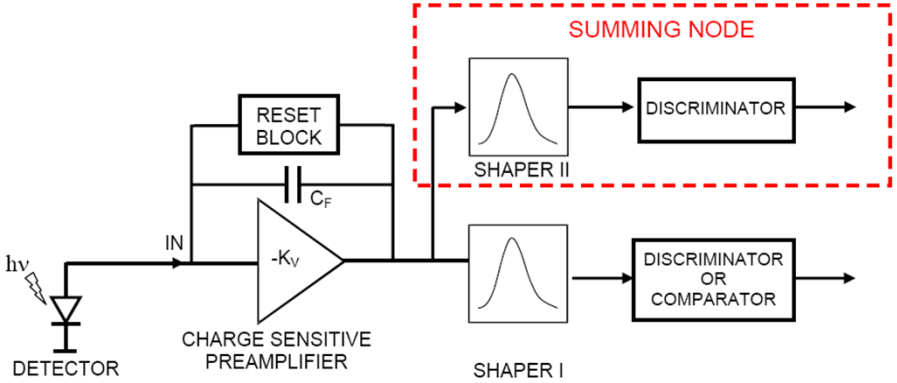
hit | single pixel | & summing node

between 4 pixels

between 2 pixels

in 1 pixel



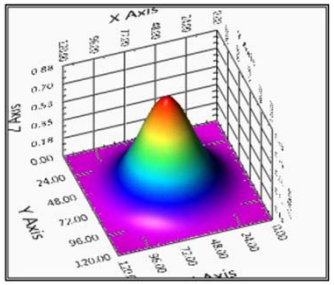


Simulation assumptions

Simulation parameters:

Silicon detector: 300 um thick, 75 um pitch, charge cloud has spread of σ=10 um

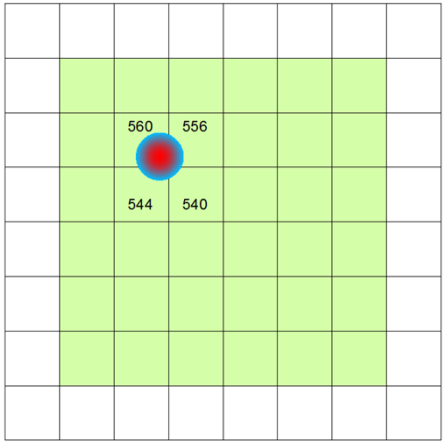
Array of 8 x 8 pixels, simulation resolution 0.5 um



White noise (without shaper filtering):
0, 75, 100, 125, 150 e^- rms

Offset spread: 0, 20, 40, 80 e^- rms

Gain spread: 5 % at 1 sigma level



X-ray energy range :
6 keV (1650e^-), 8 keV (2200e^-), 12 keV (3300e^-)

For each set of parameters we simulate 10.000 photon hits

Important assumptions:

Noise : in pixel = σ_{rms} , in summing node = $2\sigma_{rms}$

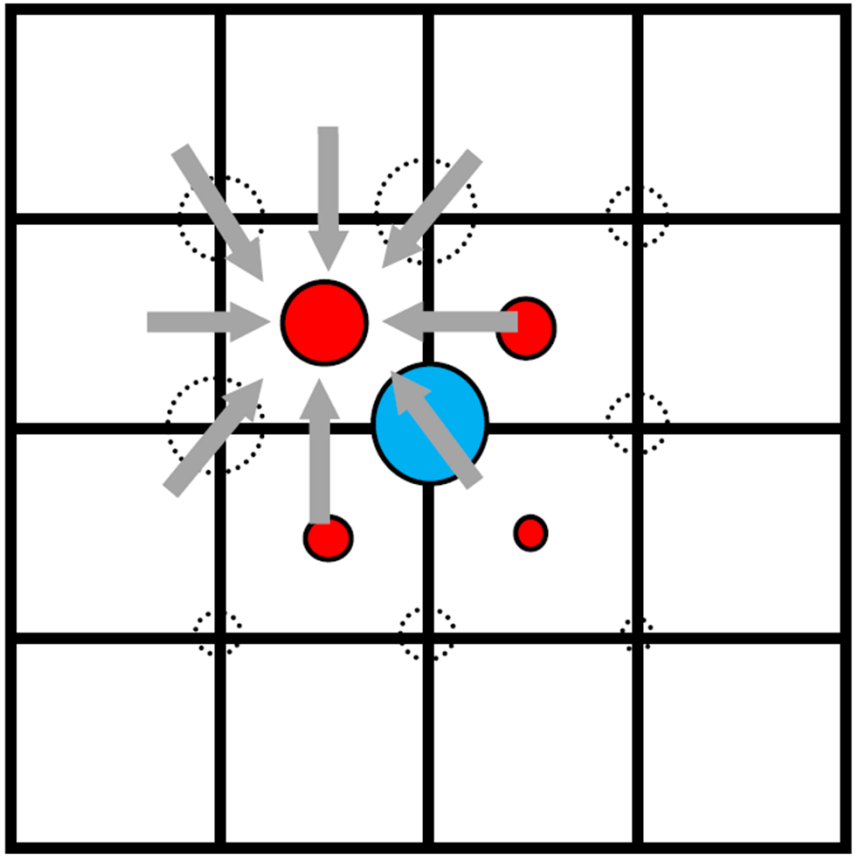
Offsets: in pixel and summing node are independent (**AC coupling is used**)

The first tested algorithm: C8P1
(AGH – FNAL)

Hit position identification (C8P1)
1) pulse at **summing node is above a threshold**

2) **comparision** of pulse amplitude in a single pixel with its 8 neighbours

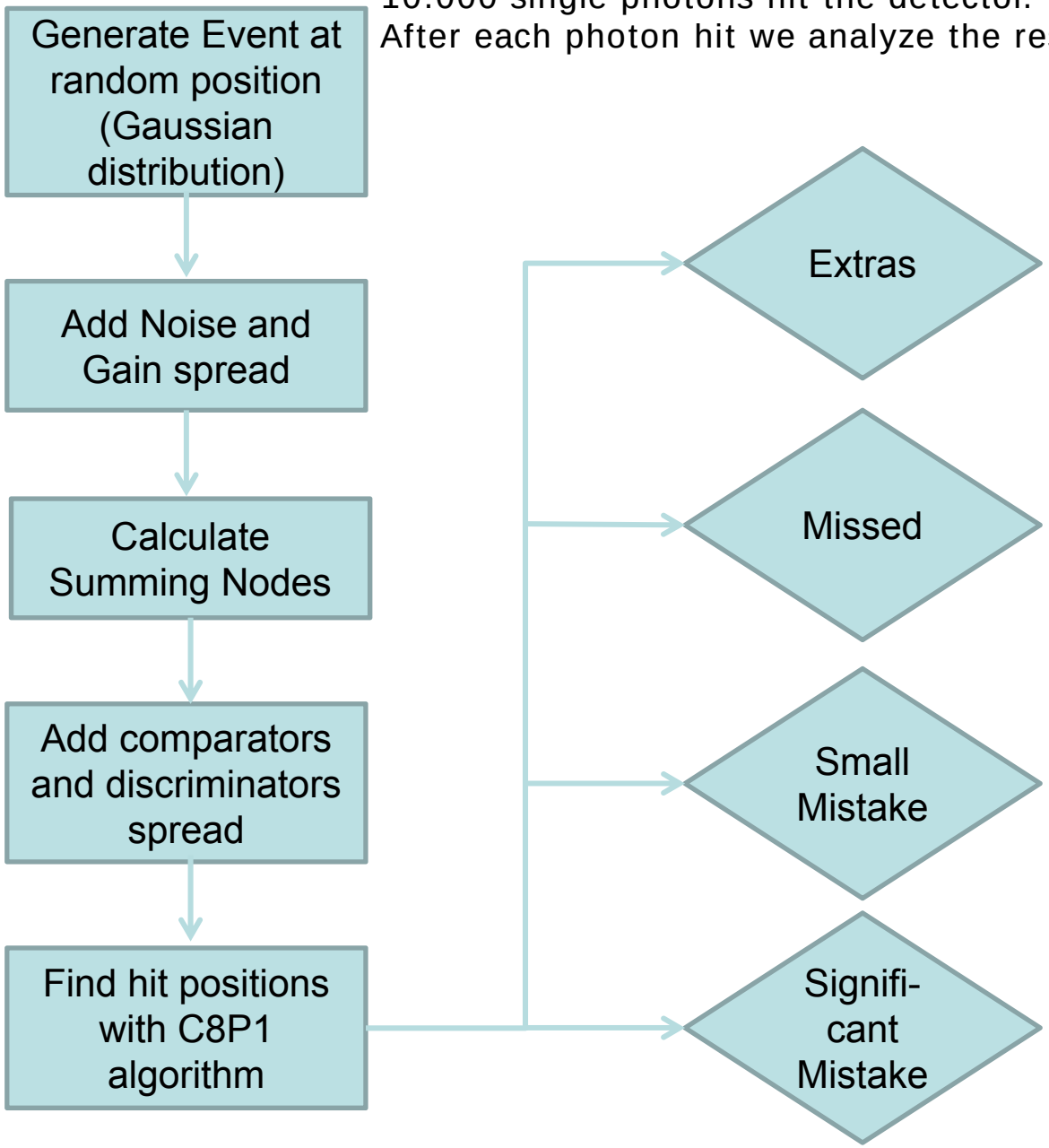
Selected pixel: all 8 comparators point out this pixel and one of its summing node is above the threshold

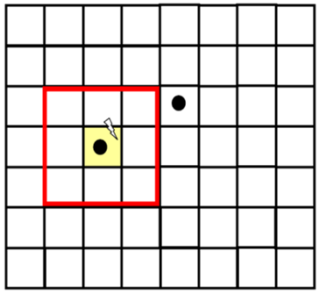


*** Analysis of Full Charge Reconstruction Algorithms for X-Ray Pixelated Detectors**
A. Baumbaugh, et. al **poster NSS 2011, Valencia, Spain**

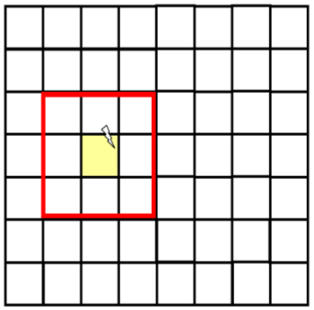
Simplified flowchart of the C8P1 algorithm

10.000 single photons hit the detector.
After each photon hit we analyze the response of pixel matrix:

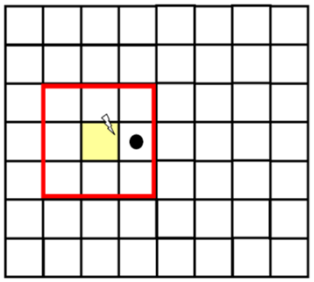




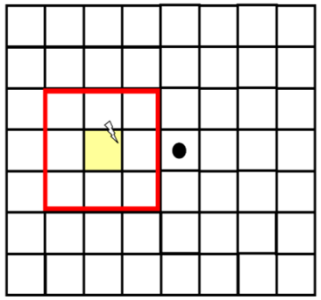
Extra hit – if in a single event more than one hit is found ("number of found hits – 1" is added to extra



Missed hit – if in a single event no hit is found (missed is incremented)

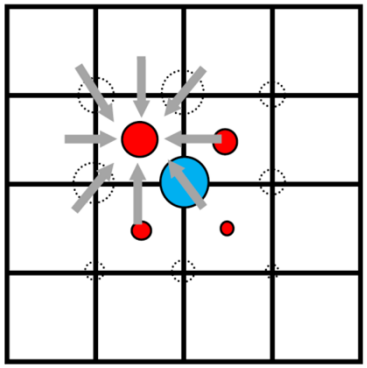


Small mistake – hit is found in a neighbour pixel

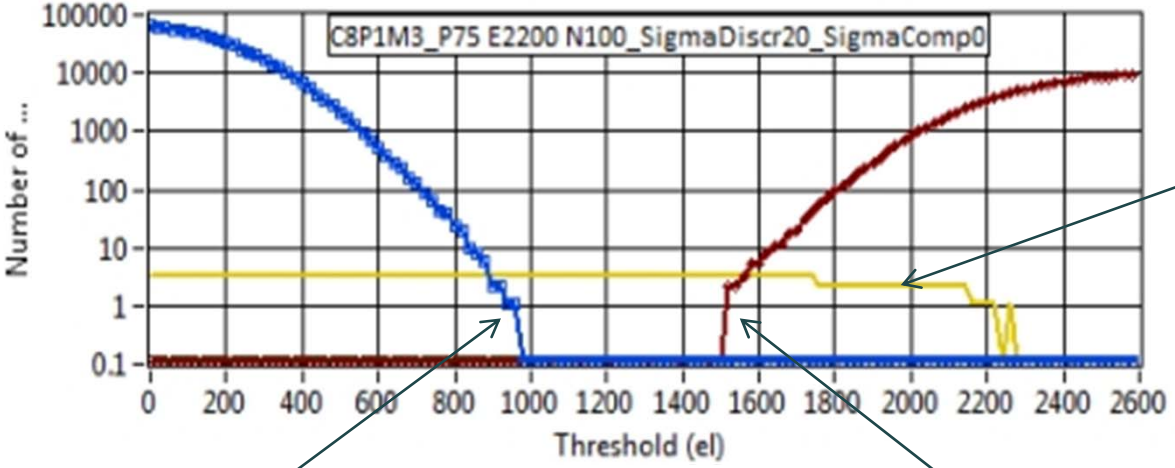


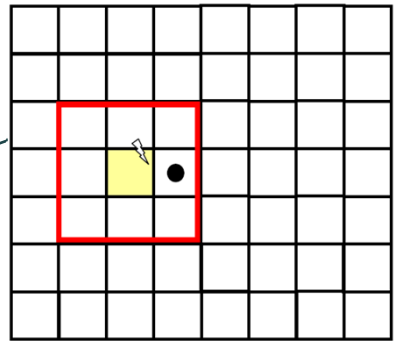
Significant mistake – hit is found but in a distance more than pixel pitch from its proper location

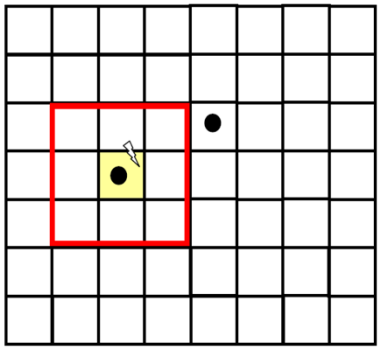
What is the proper settings of summing node threshold in C8P1 algorithm?



Qin=2200e-, ENC=100e-, Std_gain=5%, Std_discr = 20e-, Std_comp =0

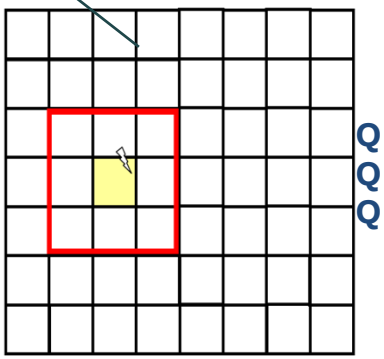






ENC=0e- → THex =0
ENC=50e- → THex =460e-
ENC=75e- → THex =780e-
ENC=100e- →THex =940e-
ENC=125e- →THex =1160e-
ENC=150e- →THex =1440e-
(Std_discr=0)

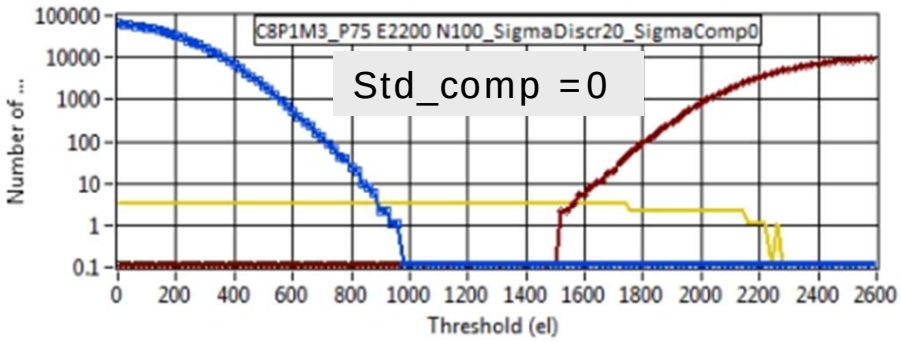
Depends on ENC & Std_discr

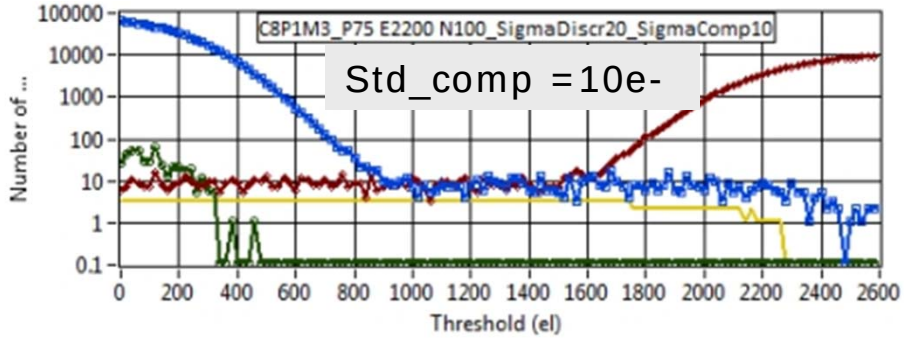


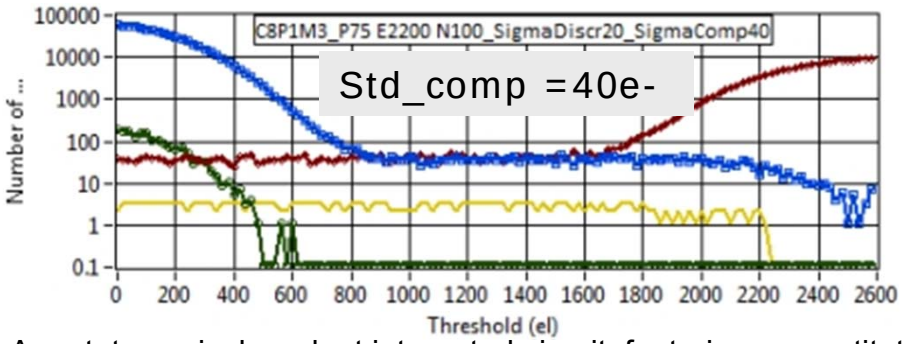
Qin=1650e- → THm =980e-
Qin=2200e- → THm =1520e-
Qin=3300e- → THm =2480e-

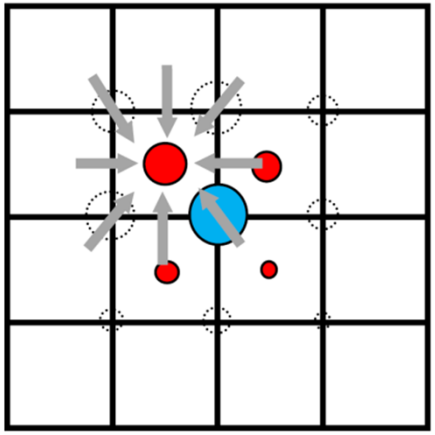
Depends on Qin

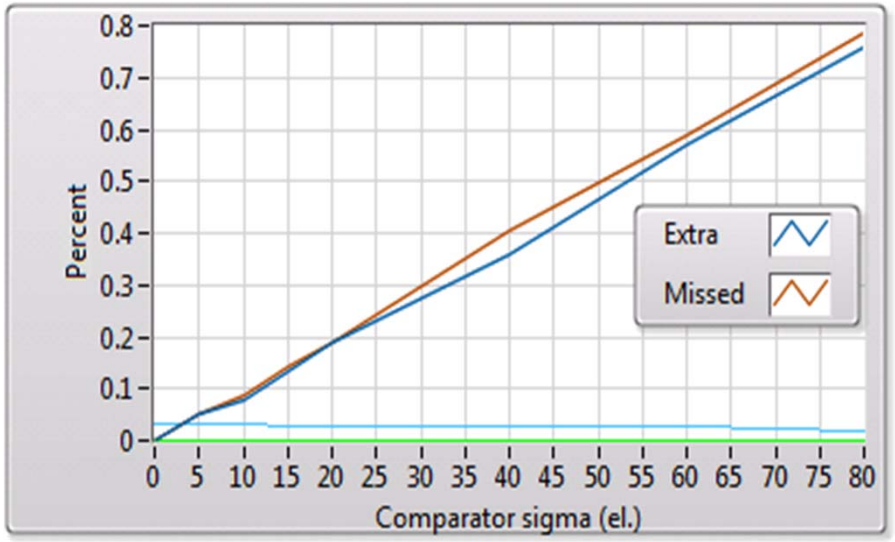
Influence of comparator offsets











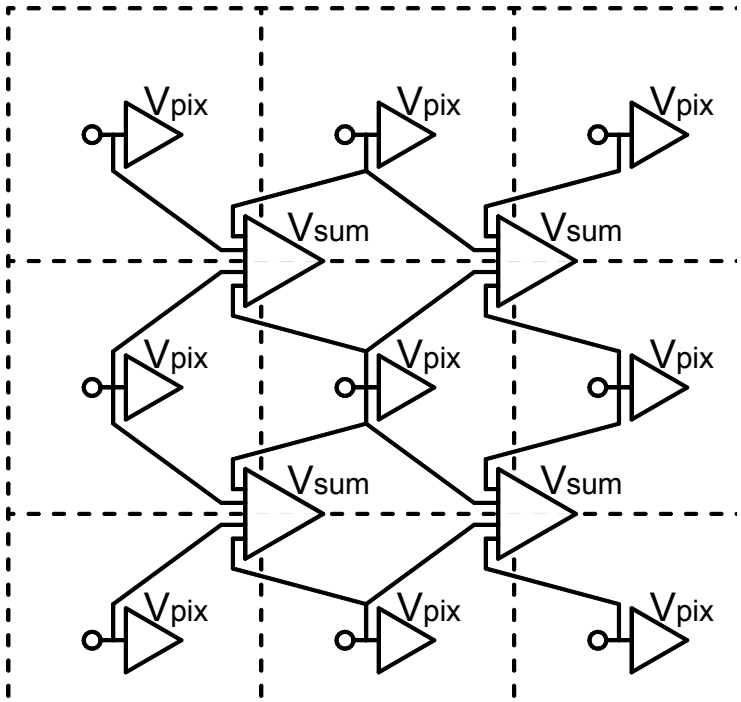
A prototype pixel readout integrated circuit, featuring reconstitution of full signals from charge shares collected by neighboring channels, was designed in a 130 nm CMOS process. The chip contains an array of 32×32 pixels; each pixel is 100×100 mm^2. The prototype is a test platform for the algorithm before its final implementation in a three-dimensionally integrated circuit.

Oral presentation during NSS2012: **A Prototype Pixel Readout Integrated Circuit with Reconstitution of Full Signals for X-ray Photon Science. G. Deptuch**, **P. Gryboś, J. Hoff, P. Maj, R. Szczygieł, M. Trimpl**

The second tested algorithm: Pattern Recognition (AGH-FNAL)

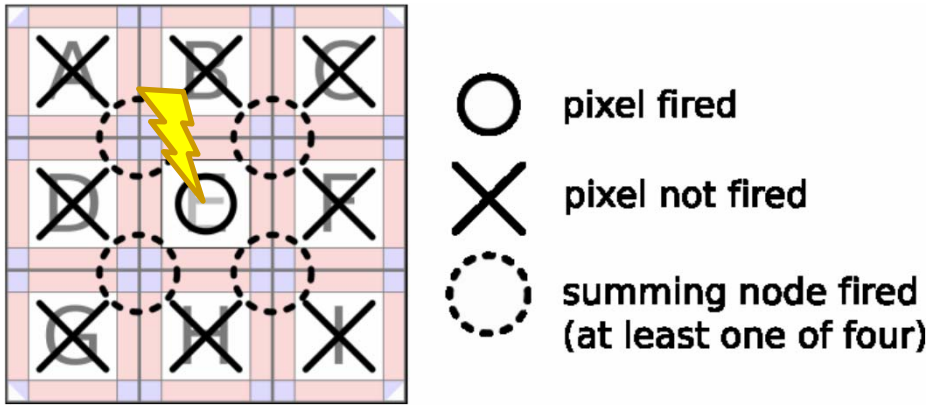
Assumptions:

1. each pixel corner has a summing discriminator with a configurable threshold V_{sum},
2. each pixel contains a single discriminator with a configurable threshold level V_{pix},



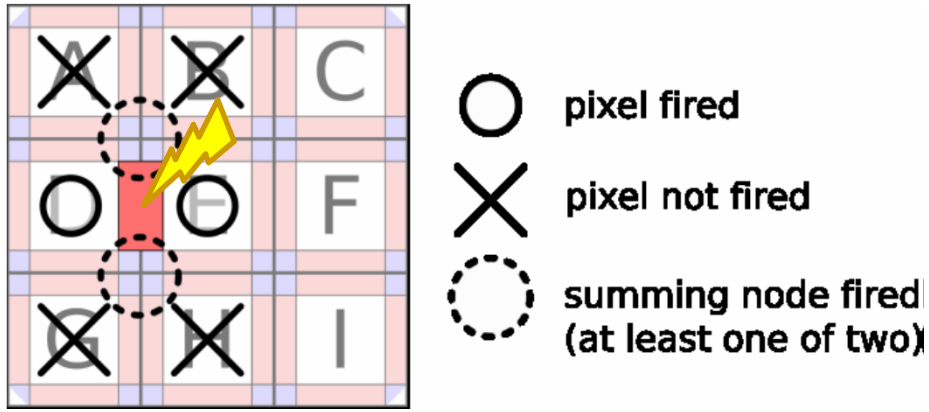
Possible cases I

in 1 pixel



$$H_E = E\,\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{F}\,\overline{G}\,\overline{H}\,\overline{I}\,(S_{ABDE} + S_{BCEF} + S_{DEGH} + S_{EFHI})$$

between 2 pixels

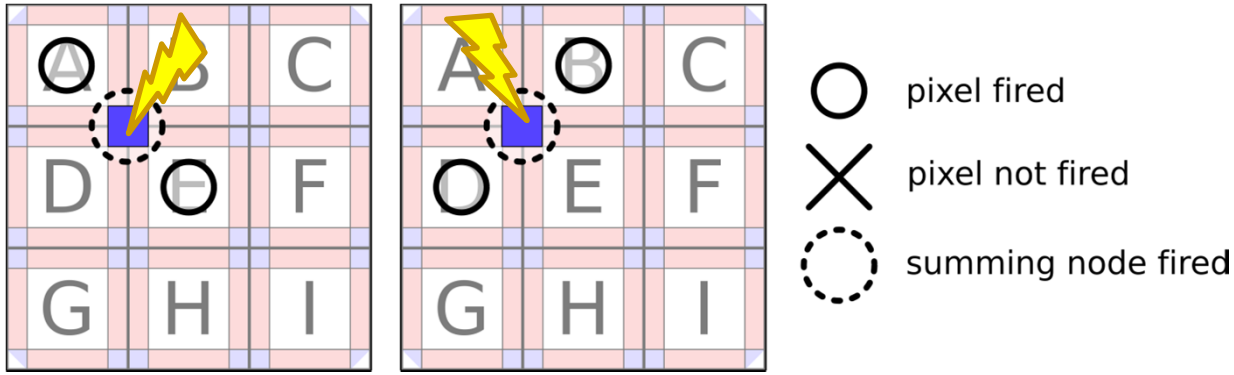


$$H_{DE} = D\,E\,\overline{A}\,\overline{B}\,\overline{G}\,\overline{H}\,(S_{ABDE} + S_{DEGH})$$

(a vertical case is simillar)

Possible cases II

Between 4 pixels



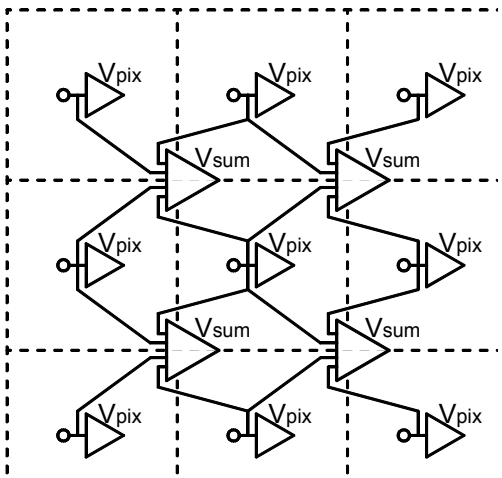
$$H_{ABCD} = \left((A\ B) + (D\ E)\right) S_{ABDE}$$

Error definiton

10.000 single photon hits the detector. After each photon hit we analyze the response of pixel matrix:

Efficiency – percent of a good pixel identification,

for example efficiency = 99,8%
For 10.000 photon hits we find:
- in 9980 (or more) cases proper pixel identification,
- in max. 20 cases we have errors (missing, extra, not proper position)

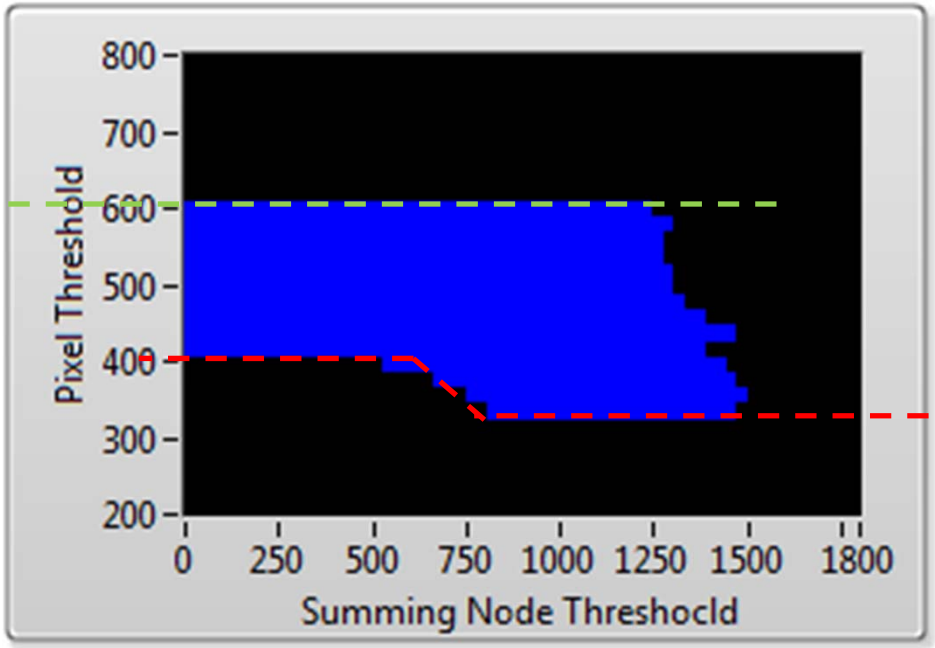


What is the proper settings of summing node threshold and pixel threshold?

What is the proper settings of summing node threshold and pixel threshold?

Efficiency = 99.8%, Qin=2200e-, ENC=100e-, Std_gain=5%, Std_sum_discr = 0, Std_pix_discr =0

The upper limit of pixel threshold is close to Qin/4 and does not depend on summing node threshold

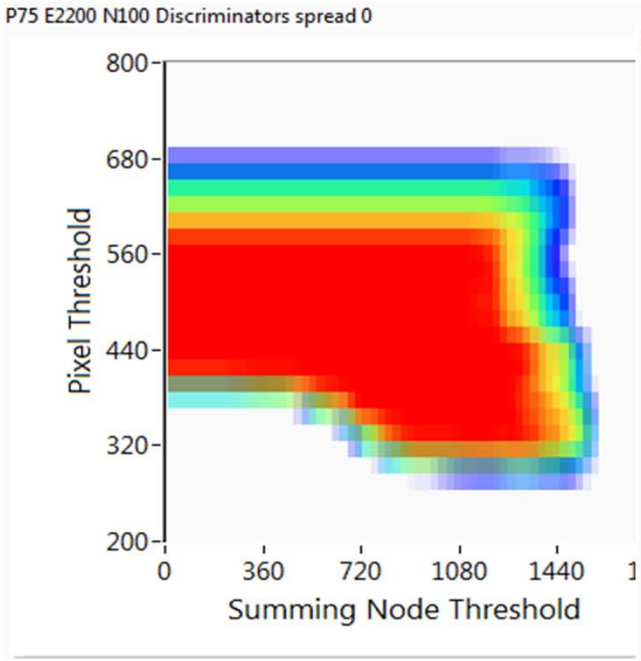


The bottom limit of pixel threshold comes from the noise.

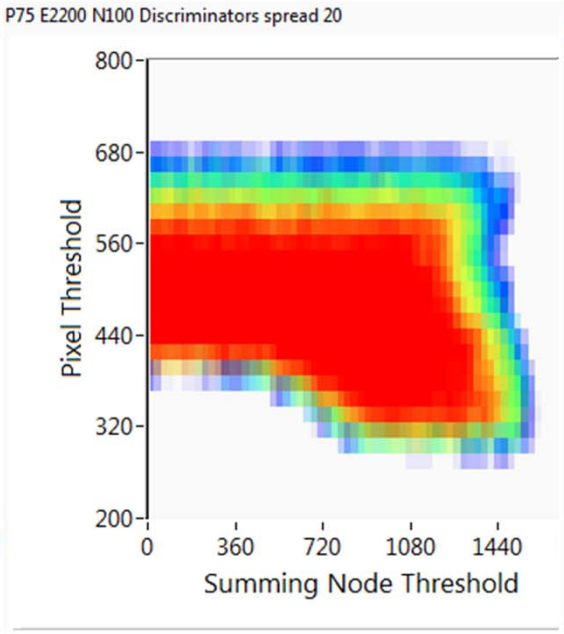
Setting a low value of pixel is possible only for high values of the summing node threshold.

Different cases: discriminator spread

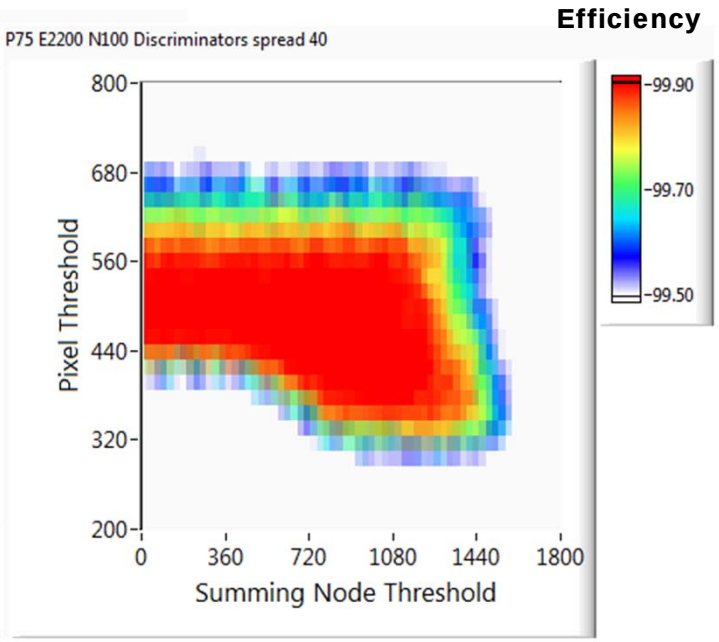
Std_discr=0e-



Std_discr=20e-



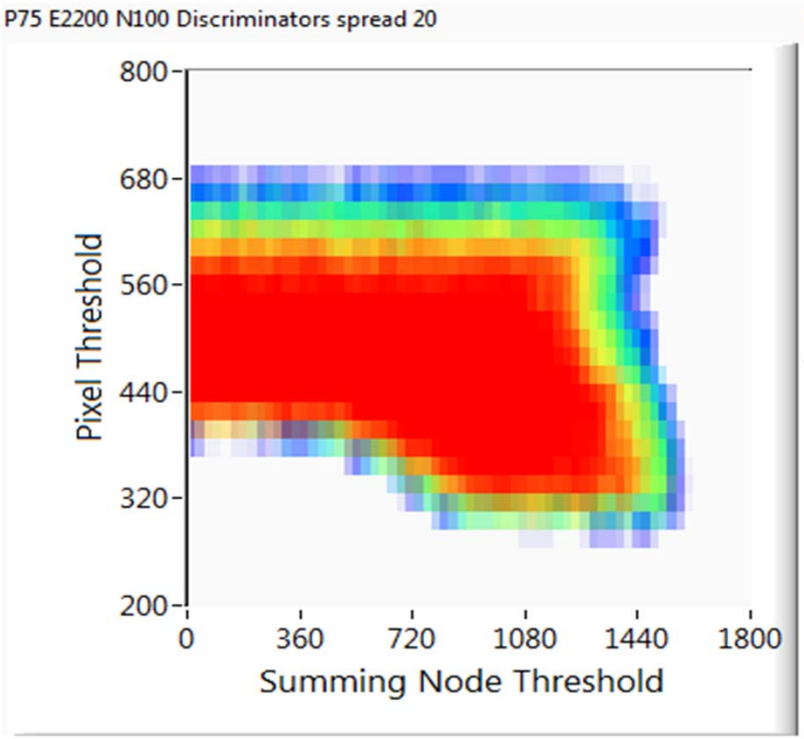
Std_discr=40e-



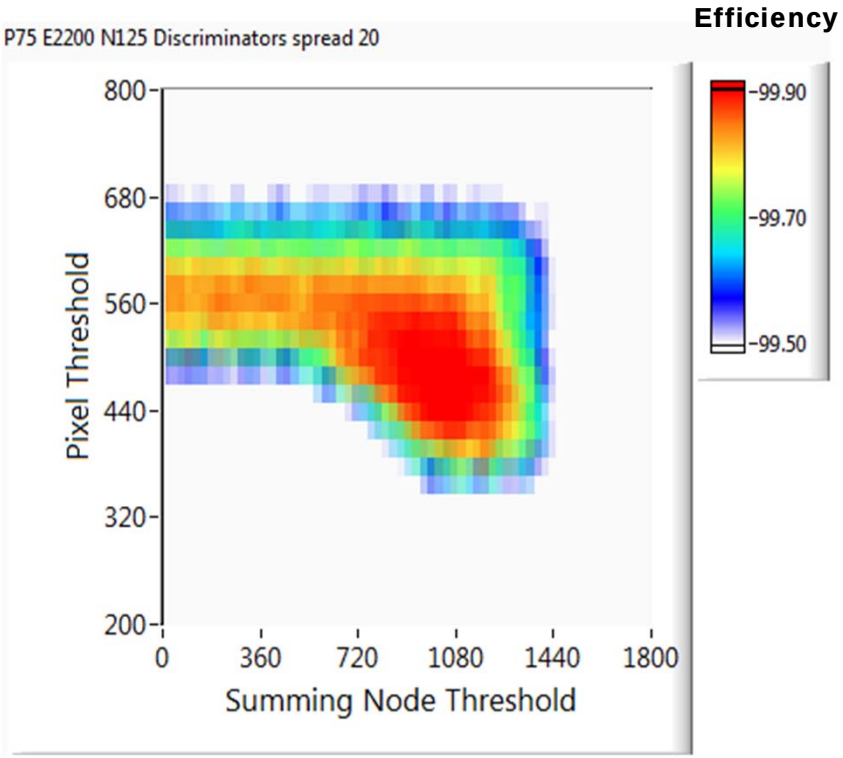
Qin=2200e-, ENC=100e-, Std_gain=5%

Different cases:
noise

ENC=100e-



ENC=125e-

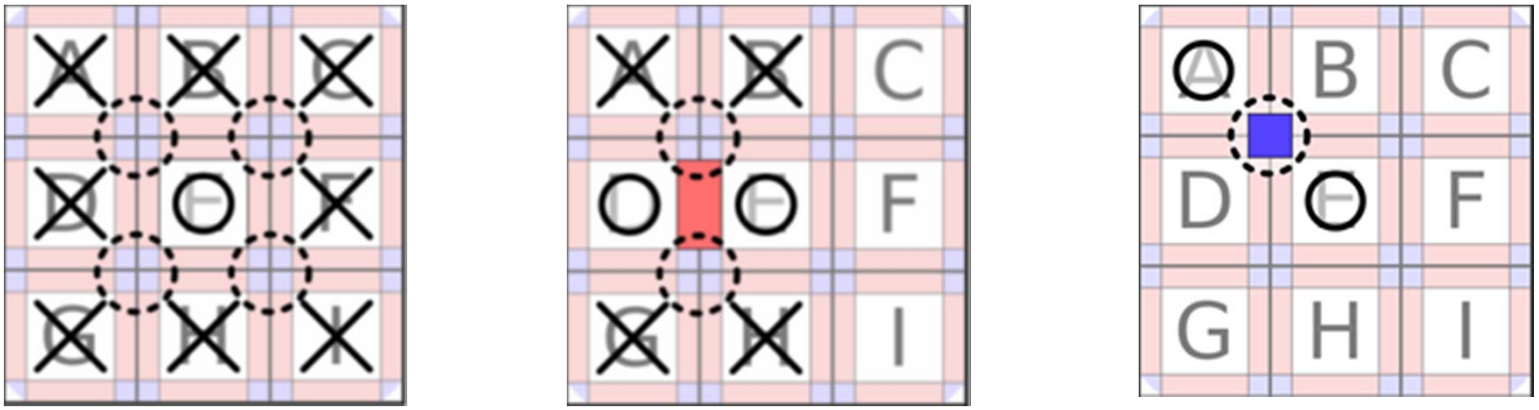


Qin=2200e-, Std_gain=5%, Std_discr=20e-

Additional features

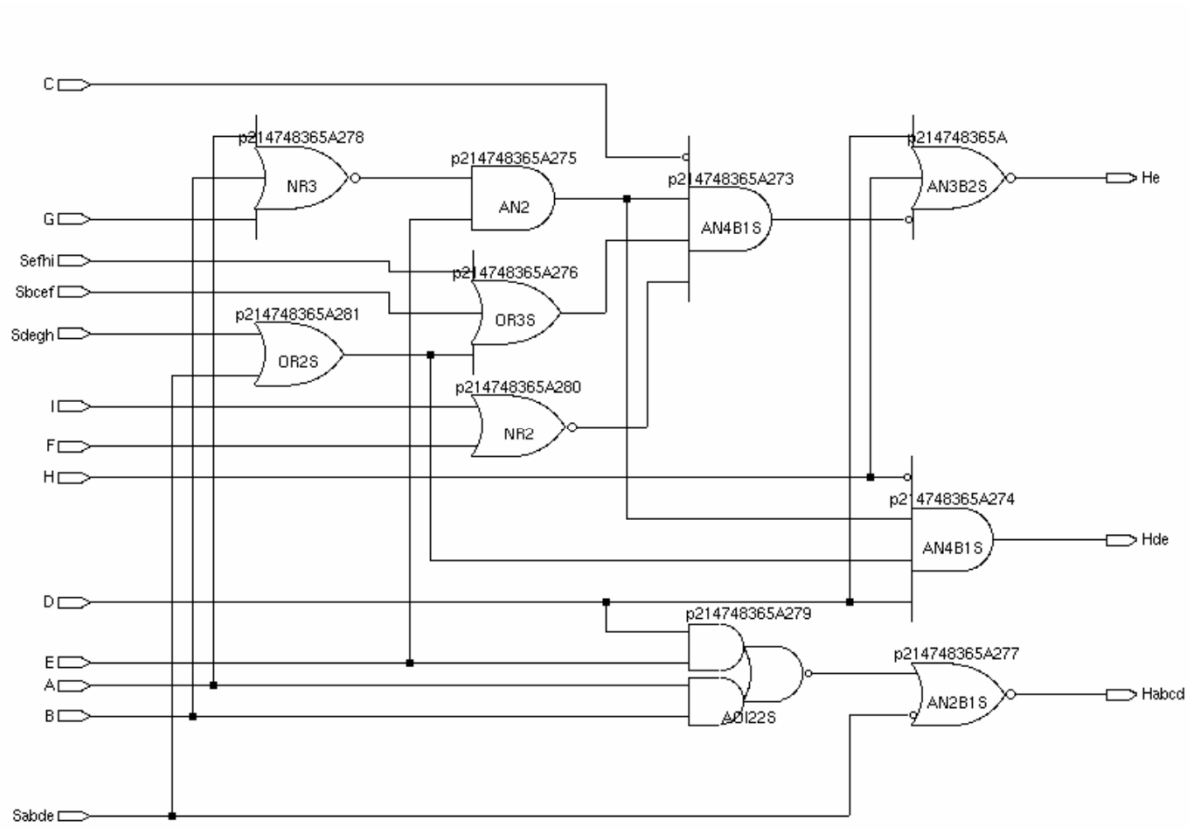
1. by proper allocation of the hit to the given pixel, we are able to obtain the information of photon energy which is given by pulse amplitude at the input of summing discriminator,

2. the position resolution in single photon counting system can be increased; areas, where the charge is shared between pixels, can be supplied with additional counters – **question: how useful this property can be?**



Counter and logic for Pattern Recognition Algorithm

Logic (90 nm) estimated area is only 10 µm x 15 µm



Ripple counters (90 nm):
8–bit: area 15 µm x 25 µm
4–bit : area 8 µm x 25 µm

Conclusions – algorithms for charge sharing effects

1. Two algorthms were checked by simulations
- C8P1
- Pattern Recognition

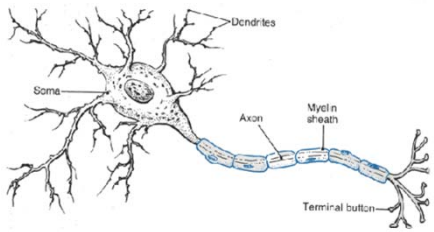
Both of them are working properly: Qin=2200 e-, ENC=100e-, std_gain=5%, std_discr=40 e- rms

2. Pattern Recognition seems to be easily used for energy binning and increasing position resolution in counting systems, however C8P1 aloorithm seems to be more roboust to small signal/noise ratio and signal/offset ratio.

Other application of pixel readout chips

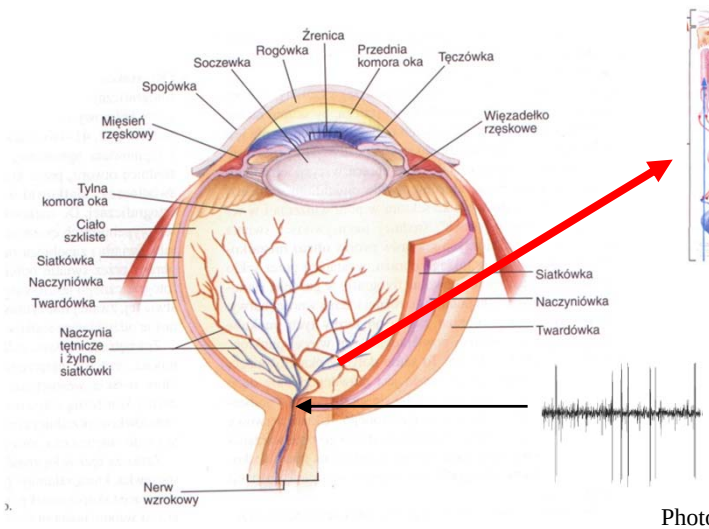
Neural systems

SINGLE NEURON



To understand the mechanisms of information processing in the correlated activity of different cells simultaneous detection of signals from many neuronal cells is necessary

RETINA



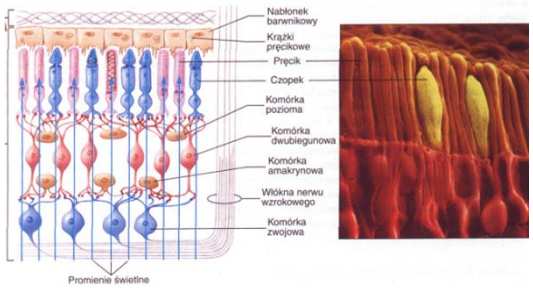
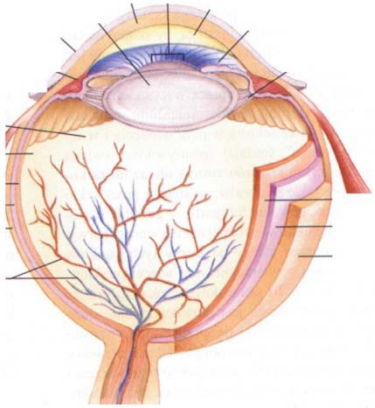


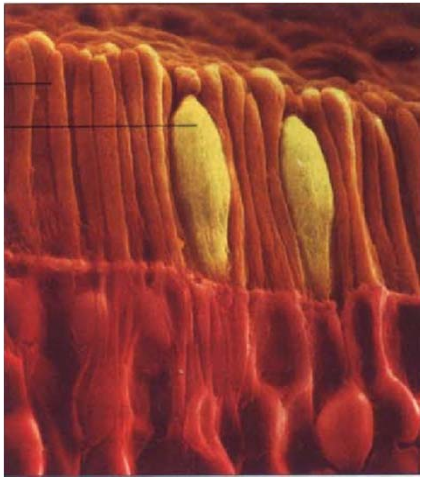
Photo: Biologia, PWN

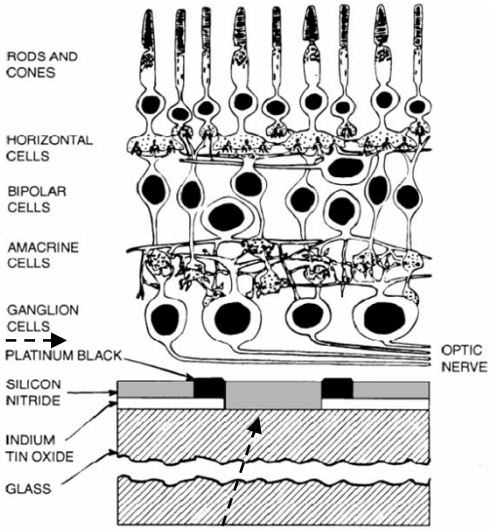
Cones: 6.5 x 10^6 (colours)
Rods: 125 x 10^6 (move, shape)
Optical nerve: 1 x 10^6 fibers

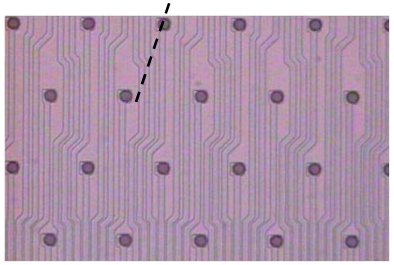
Example of application:
RETINAL READOUT SYSTEM

Four group of people from:
UC - Santa Cruz: data acquisition system & analysis
AGH UST - Krakow: IC design and testing
Univ. Glasgow – UK: microelectrode fabrication
Salk Institute - San Diego: neurobiology

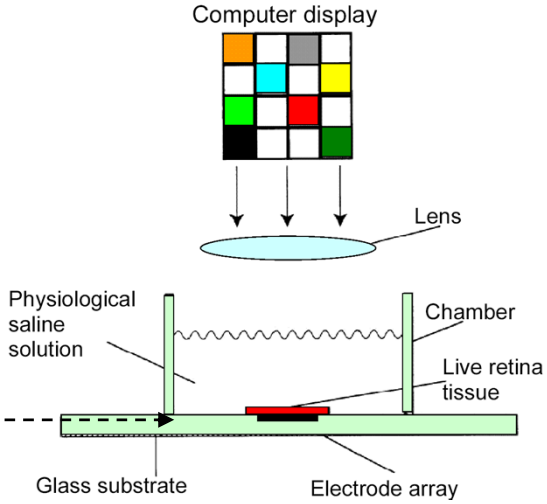








512-electrode array 32x16:
spacing = 60 um diameter = 5 um



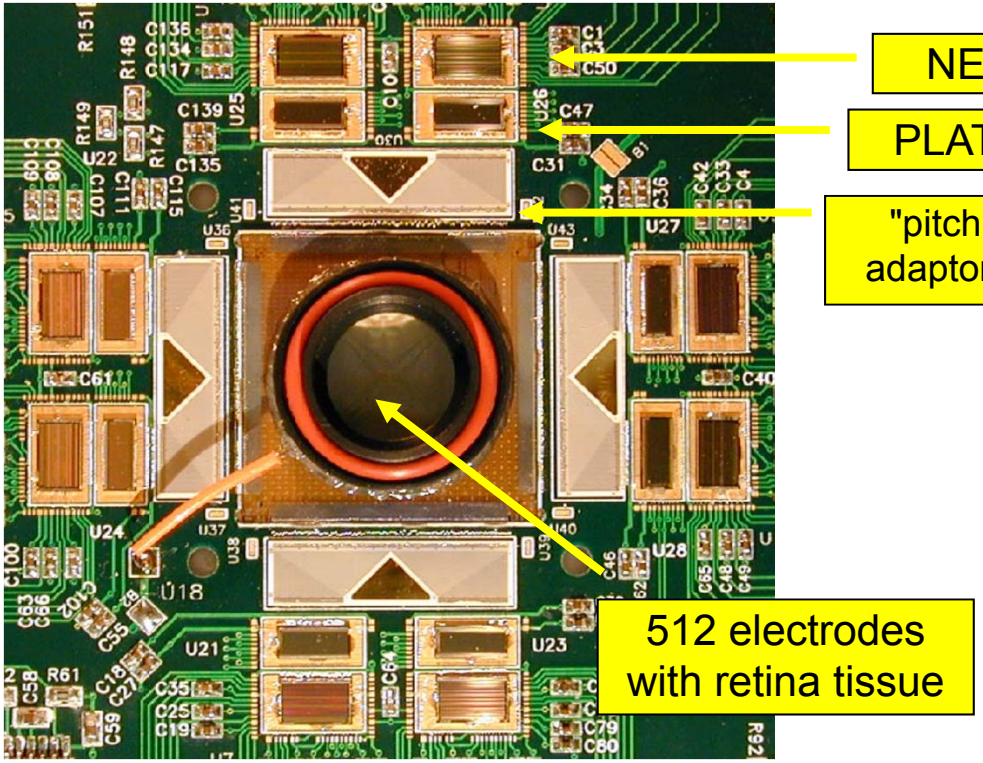
A movie is focused on the retina tissue

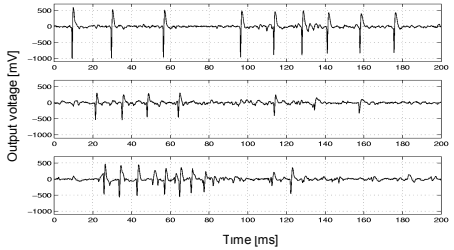
⇓

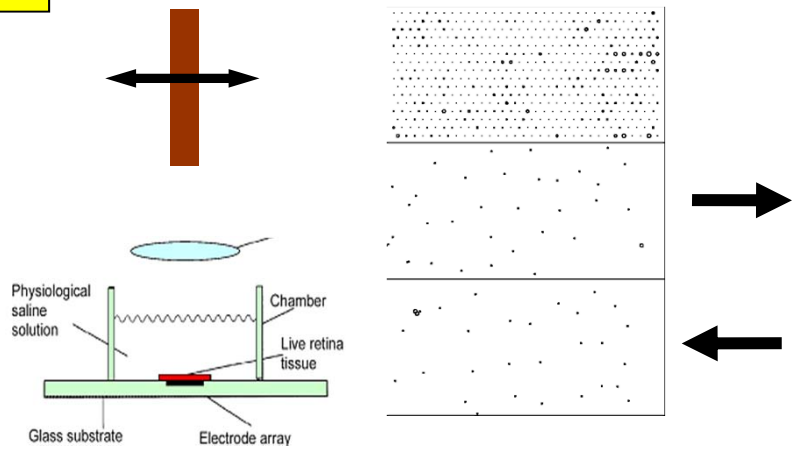
The patterns of electrical activity generated by hundreds of retinal output neurons are recorded

System of 512 readout channels for retina

To understand how the retina processes and encodes dynamic visual image





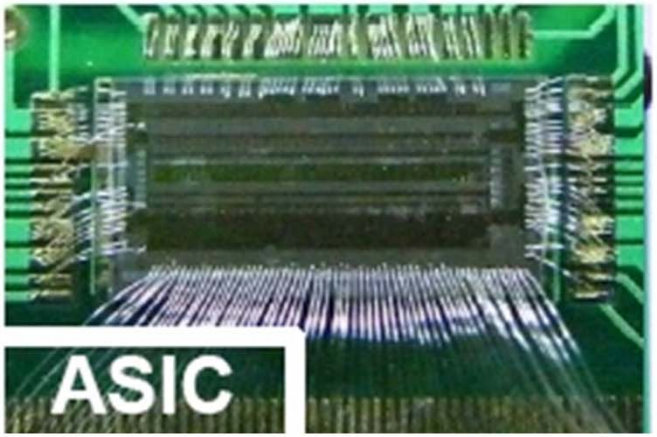


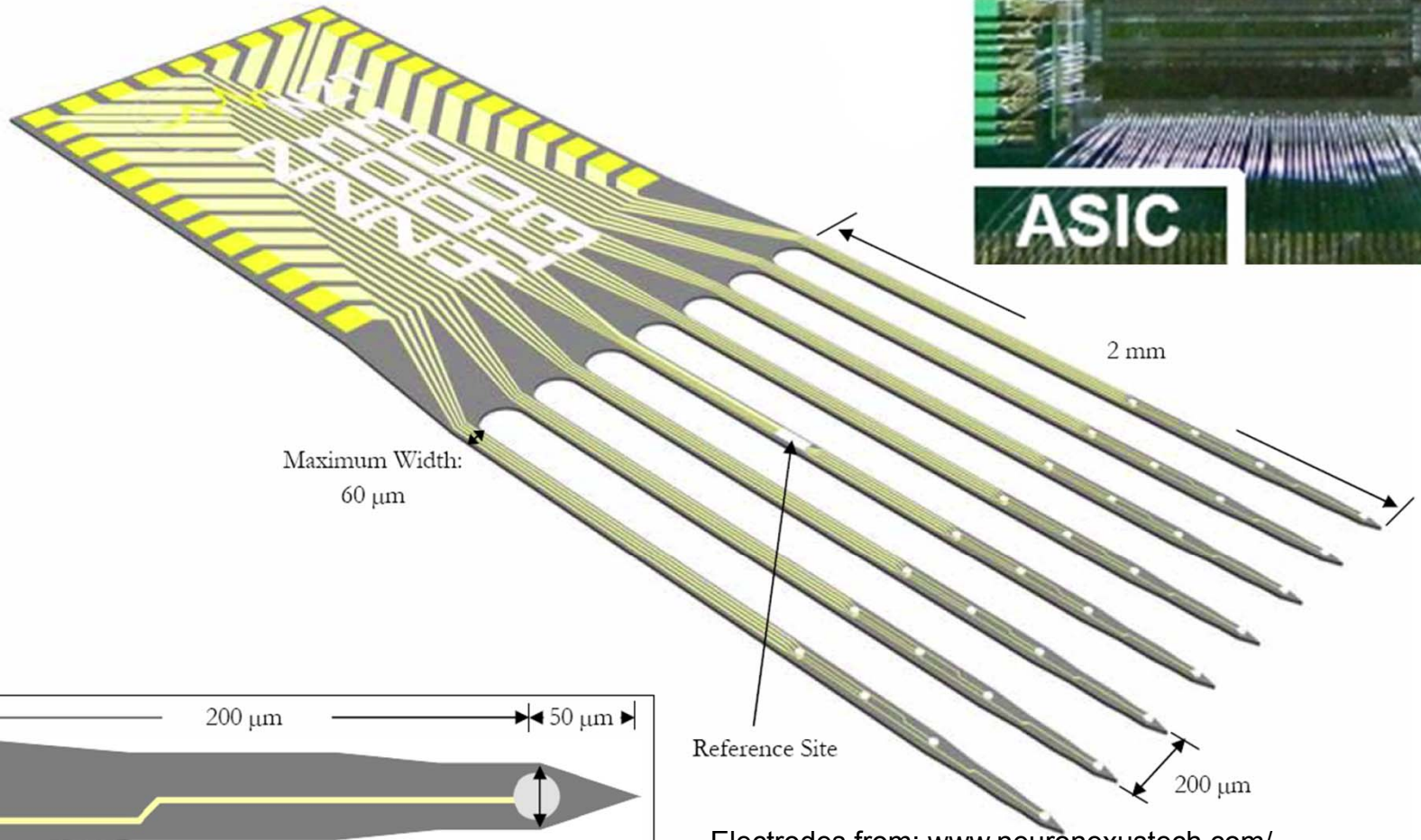
More about above system in ref:

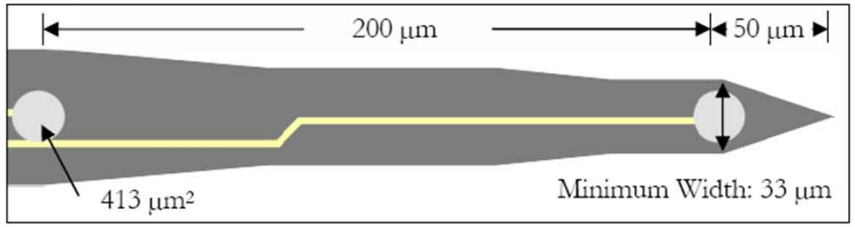
Litke AM, Bezayiff N, Chichilnisky EJ, Cunningham W, Dabrowski W, Grillo AA, Grivich M, Grybos P, Hottowy P, Kachiguine S, Kalmar RS, Mathieson K, Petrusca D, Rahman M, Sher A.
What does the eye tell the brain?: Development of a system for the large-scale recording of retinal output activity.
IEEE Transactions on Nuclear Science, vol.51, no.4, Aug. 2004, pp.1434-40.

Readout ASIC design details - P. Gryboś: "Low Noise Multichannel Integrated Circuits in CMOS Technology for Physics and Biology Applications", Monografie 117, AGH Uczelniane Wydawnictwa Naukowo-Dydaktyczne AGH, Kraków, 2002.

Signals from the brain:
ASIC for vivo neurobiology experiments + electrodes

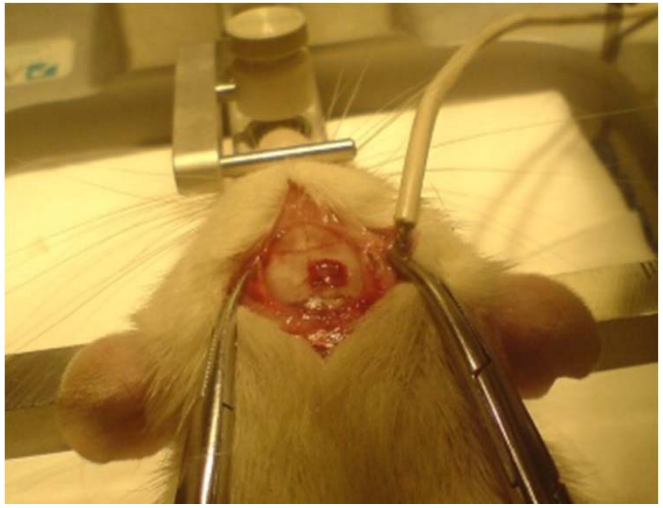


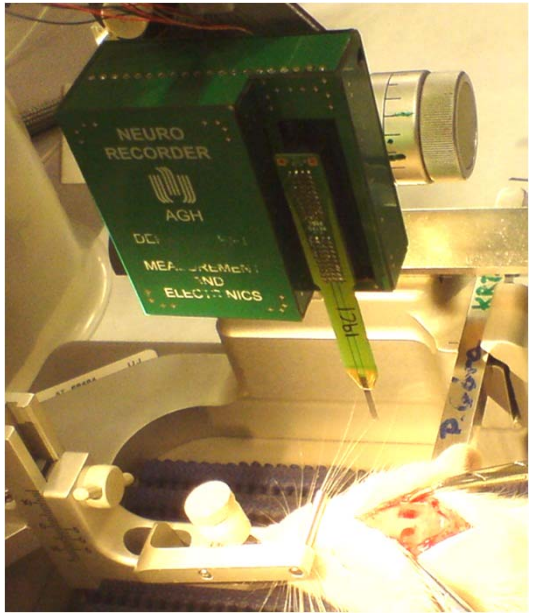


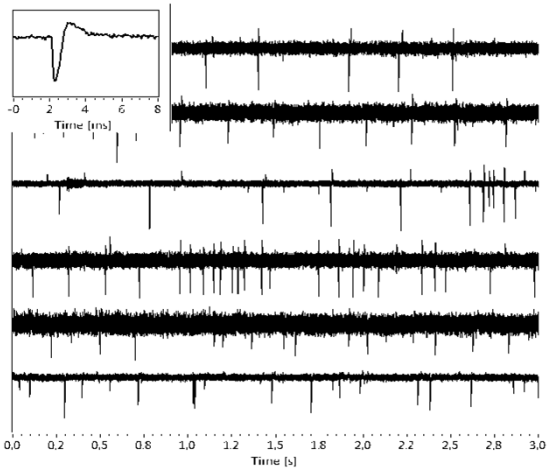


Electrodes from: www.neuronexustech.com/

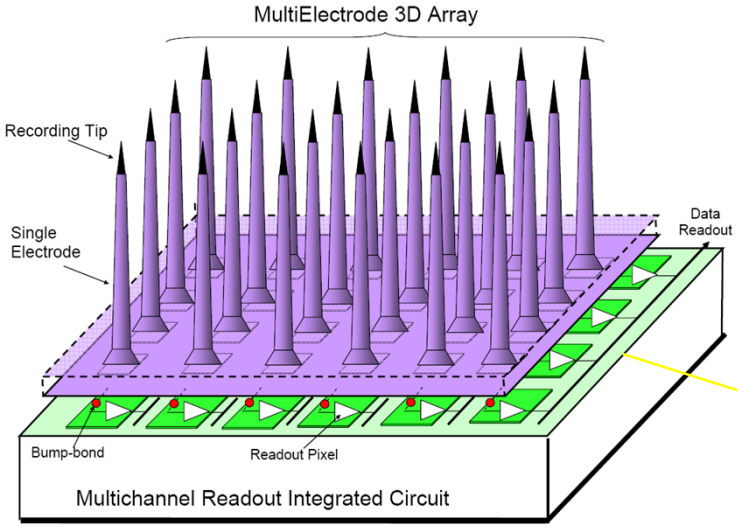
Neurobiological tests
cooperation with Jagiellonian University

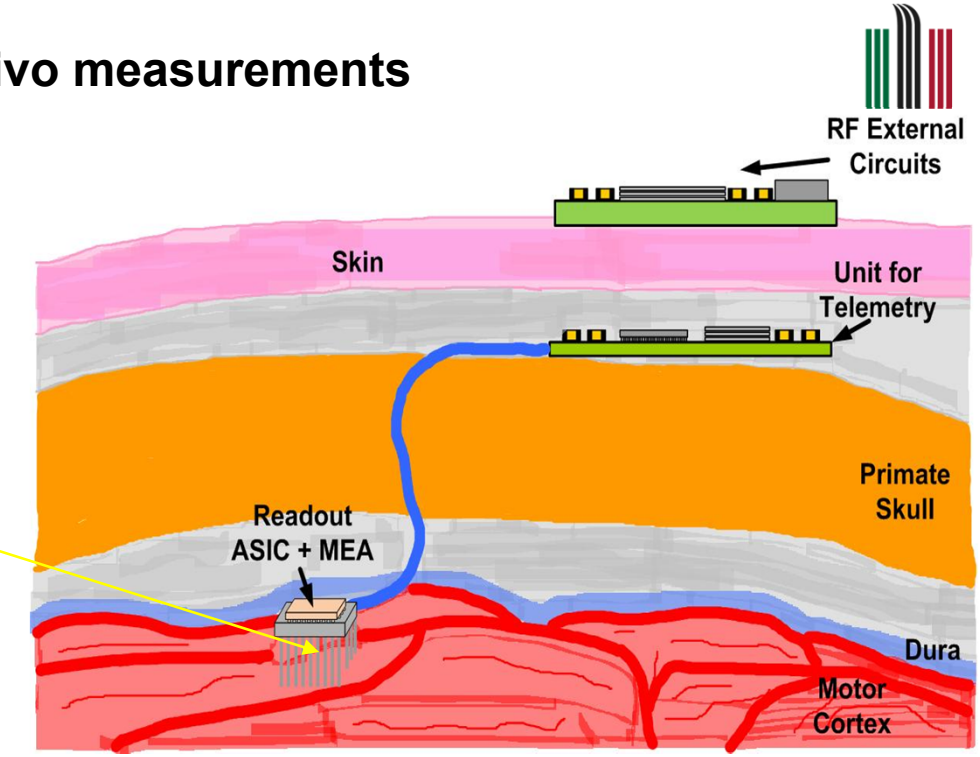






Plans – ideal system for in vivo measurements





IDEA FOR UNIQUE EXPERIMENT ⟺ **WITH ASIC IS POSSIBLE**

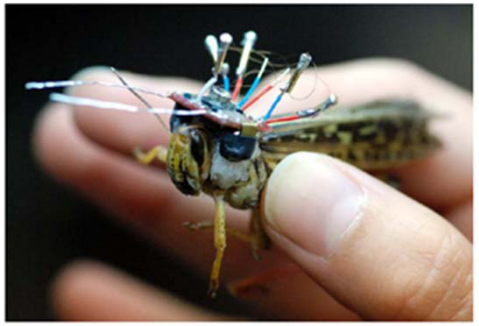
Other groups:

Reach and grasp by people with tetraplegia using a neurally controlled robotic arm

Leigh R. Hochberg[1,2,3,4], Daniel Bacher[2*], Beata Jarosiewicz[1,5*], Nicolas Y. Masse[5*], John D. Simeral[1,2,3*], Joern Vogel[6*], Sami Haddadin[6], Jie Liu[1,2], Sydney S. Cash[3,4], Patrick van der Smagt[6] & John P. Donoghue[1,2,5]

A Wireless Neural/EMG Telemetry System for Freely Moving Insects

Reid R. Harrison, Ryan J. Kier, University of Utah, Salt Lake City, UT 84112, harrison@ece.utah.edu
Anthony Leonardo, Janelia Farm Research Campus, Howard Hughes Medical Institute, Ashburn, VA 20147
Haleh Fotowat, Raymond Chan, Fabrizio Gabbiani, Baylor College of Medicine, Houston, TX 77030



ASIC design group
Department of Measurement and Electronics, AGH UST

Acknowledgments: This work was supported by the Ministry of Science and Higher Education, Poland. We would like to thank Cadence Academic Network for helpful discussion.

Working at the AGH-UST:

- a lof of lectures
- access to good students