PHENIX Muon Tracker Electronics in Year-1

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• Phenix Experiment
• Muon Tracking System Design Specs
• Analog and Digital Design
• Results from RHIC Run-II
Physics - QGP?

\[ J/\psi(c\bar{c}) \rightarrow \mu^+\mu^- \]

\[ M_{J/\psi} = 3.1 \text{GeV} \]
PHENIX Experiment

• Central Arms
  – Tracking, EMCal, PID
  – $|\eta| < 0.35$

• Muon Arms
  – Tracking+MuID
  – $1.2 < |\eta| < 2.4$
  – $\Delta\phi = 2\pi$
Muon Tracking Chamber

0.5 cm Cathode Strip Chamber
STRUCTURE OF A STATION

Cathode strips
1 cm pitch

Anode wire direction

momentum kick

Internal alignment <25 microns

Cross Section of Station 1

98 mm

6 cathode planes

Cathode plane
Anode plane

Gap 1, 0°

Gap 2, +11.25°

Gap 3, -11.25°

98 mm
Muon FEE Design Specs

- **Low Noise**
  - 100 µm resolution
  - 1 cm cathode strip readout
  - input cap 10-150pF

- **High Speed**
  - sample new data on every beam crossing
  - 4 samples per pulse
  - hold 5 events
  - 25kHz LVL-1 [40uS]

- **Serial Control and Monitor**
  - FPGA, AMUADC, CPA
  - Temp, Voltage, Current

- **Performance**
  - 11 bits dynamic range[0-2047]
  - typical charge 80fC (0.4-800fC)
  - gain: 3.5mV/fC
  - noise requirement 1% or 0.8fC
  - pulse shape
    - rise time 0.7uS
    - decay time 10uS
  - optical link to outside world
  - reasonable power-up defaults;
  - calibration control

Good J/Psi mass resolution
Muon FEE

- Low noise high speed FEM

resolution: $100 \mu m = x \cdot 1 cm \Rightarrow x = 1\%$

noise: $Q' = 80 \, fC \cdot 1\% = 0.8 \, fC$

Thermal noise:

$$\frac{1}{2} \frac{Q_{thermal}^2}{C_{det}} = \frac{1}{2}kT \Rightarrow Q_{thermal} = 0.65 \, fC$$

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Diagram:

- CPA
- x64 AMU
- 10 MHz Beam Clock
- ADC
- GL-1
- 11-bit, 200MHz
- Data
Cathodes Read-Out Card (CROC)

**Design Requirements**
- 64 Channel Readout per CROC
- Less than 3125 electrons (RMS) noise for 10-150 pF of detector capacitance (including 24” cable)
- Less than 1% crosstalk between any channels on the board
- Gain: 3.5mV/fC
- Digital/Analog isolation

**Main Components**
- AMU-ADC
- CPA

![Image of CROC card with digital and analog signals]
Muon FEE - CROC

- **CPA (Charge Pre-Amp)**
  - low noise (<3000 e’s)
  - 8-channel preamp/shaper
  - 34-bit serial control
    - pedestals
    - pulse shape

- **AMU-ADC**
  - 32 channels
  - 64-cell AMU
  - serial control
    - V_ref, I_ref
    - 9-12 bits ADC conversion
  - 200MHz clock
Controller Card (CNTL)

- **Design Requirements**
  - Control AMU/ADC data collection, conversion and read-out
  - Provide connection to 2 CROC boards
  - Provide connection to the outside world
  - Support the T&FC and DCM interface
  - Provide data relay from remote controller board to DCM
  - Support ARCnet connectivity to serial configuration bus

- **FPGA - the brain**
  - developed by Jack
  - work in progress
MUON TRACKER
CNTL FPGA

FPGA

TFC
DCM

AMU ADC DATA
AMU ADC CONTROL AND DATA ADDRESS
AMU ADC READ WRITE ADDRESS

AUXPORT
ARCNET
Muon FEE

- FPGA - current code
  - store every beam crossing
  - 4-sample per pulse
  - readout time 53uS
  - hold 4 events
Muon Tracking FEE Overview

- LVDC Power Supplies
- LVDC distribution cards
- GTM
- Glink2Clink
- ARCNet
- Signal from Counting House
- Counting House
- CRA manifold
- Nitrogen manifold (Under Platform)
- CRA manifold
- H₂O manifold (Under Platform)
- Counting House
- Clink2Glink
- Patch Panel (platform)
- DCM (counting house)
- Slow Controls Monitors
- VME Crate (platform)
- HV Plane
- Pulser (platform)
- Chambers
- Gas system interface (platform)
Supporting Muon Tracking Electronics

G/Clink cards

Calibration
Grounding Configuration

- HVSG
- Chamber
- HV
- Earth Ground
- LV Supply
- ARCNet
- F&FC/DCM

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Shield tied to ANLG-gnd
Analog cable
Shield tied to frm-gnd
differential
differential
FEE Overview

- Inside Magnet/no access
- Limited Space
- Power constrain
- Many Channels
  - 168+192 FEMs
  - over 40,000 channels
PHENIX South Muon Tracker
Interface to PHENIX DAQ

- Data readout and DAQ system

Diagram showing the flow of data from the Interaction region to the Countingroom, including components such as Trigger, GL1, Clock, LI, Bay, GTM, RHIC clocks, SEB, ATP, and online monitoring. The diagram also indicates that ~350,000 channels are handled.

Notations:
- Missing components: ARCNET Serial Interface to FEMs, High and Low Voltage Control and associated control systems, Alarm system.

Facilities:
- RHIC Computing Facility
  - User End
  - Linux Farm (~600 CPUs)
  - Tape storage 1.2PB
  - 20MB/s, 250TB/yr
Detector Commissioning

- Electronics
- HV
- Noise Reduction
- Timing in Detector

Channels

Cathode Strip Charge

RMS

Good Timing

Low noise rms ~ 2 ADCs

chamber resolution ~100um

Octant Test Resolution (cm)
Muon Tracker Calibration System

MuTr Calibration System - M. Leitch, P. McGaughey
Calibration

ADC distribution from real data
Most probable ~ 200 ADC cnts
Chamber Alignment Monitoring

A good tracking resolution:
- low electronics noise
- stable gain
- geometry and alignment
Optical Alignment System

Cameras on station-3 chambers
Data QA: calib. & online monitor

- 4 Samples’ relative timing
  - (1,6,7,8) beam-crossings
- DAQ Zero-Suppression (<5%)
  - (peak - pedestal) > 3*rms
- Stable Pedestals and Gains
  - daily calibration

Pedestals from calibration data
Dimuon Mass

Red: unlike-sign pair
Blue: like-sign pair

$J/\psi (c\bar{c}) \rightarrow \mu^+ \mu^-$
$M_{J/\psi} = 3.1 GeV$

Significant enhancement of unlike-sign pair in the $J/\psi$ mass region
- Peak (3123 ± 56 MeV/c²) is consistent with $J/\psi$ mass
- Mass width (230 ± 40 MeV/c²) is consistent with expectation -> further improvement is expected
Current Status and Issues

• Worked as expected in Run-2
  – no major problems
  – luminosity was low

• G/Clink loss and readout problem
  – very sensitive to external disturbance --> replaced all bad cables
    • “dead” FEMs, ~5% --> loss acceptance
  – can’t re-lock on the fly -->DAQ hung

• For higher luminosity (Run-4, 5, ...)
  – conversion time 53 uS is too long [40]
  – need to hold 5 events
  – new FPGA work in progress
ACTIVE MUON TRACKER CHANNELS

Visualization of active regions of three tracking stations. Dead regions are due to problems with HV and front end modules during 2001-2 run. Majority of problems corrected for next run.
First collision events were observed on 07/18/2001

- Successfully installed and commissioned muon detector in the PHENIX
- More work to improve FPGA code to handle:
  - 5 events buffer (4)
  - 40uS conversion (53)
Conversion Time and Baseline Shift - AMUADC

- Problem is eliminated by adding 4 uS delay between conversion and data transfer (add 12+uS).
- Possible remedial actions
  - tune delay to minimize
  - use only three samples
  - relax requirement for five events
Disabled HV & FEMs

- **HV**
  - Station-1,2,3
  - 1825V:1850:1850
  - 72/304=23.7% disabled

- **FEMs (total 168)**
  - Sta-1: 4/40
  - Sta-2: 2/64
  - Sta-3: 2/64
  - were disabled
  - (loss ~15% acceptance)
DIMUON CANDIDATE

Dimuon candidate from p+p collision (rotated for clarity with beam line running vertically)

3 stations of Muon Tracker

Interaction point

2 muon candidates penetrate muon identifier panels