Microelectronic group: Integrated electronic Overview


LAL Orsay
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• A strong team of 9 ASIC designers…
  ✓ A team with critical mass
  ✓ Expertise in low noise, low power, high level of integration
  ✓ 2 designers/ project
  ✓ 2 projects/designer
  ✓ Regular design meetings

• …Within an electronics department
  ✓ Support for tests, measurements, PCBs…

• 4-5 large productions/year

• A strong on-going R&D
  ✓ Building blocks SiGe 0.35µm
Orsay micro-electronics team

• microelectronic group is designing integrated front-end electronic for particle physics

• This talk will introduce a bunch of Front-end ASICs designed by LAL microelectronic group

• Turn to Silicon Germanium 0.35 µm technology

• Readout for MaPMT and ILC calorimeters
MAROC has been designed to read out 64-anode MA-PMT from HAMAMATSU.

The first application is the ATLAS luminometer.

Other applications:

- medical imaging (project with ISS Roma)
- neutrino experiments (PMM2)
- SIPM read-out

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Experiments and applications

- **Main one**: ATLAS Luminometer (absolute measurement of the luminosity)
- **Roman Pots**:
  - 0.5mm² scintillating fibers
  - 1 RP = 10*64 fibers in U + 10*64 fibers in V
- **Multi Anode PM Tubes**
  - 64ch Hamamatsu H7546
  - HV = 800-950 V
  - Gain 3.10⁵-10⁶
  - Maximal signal: 4-6 photoelectrons
  - 1-3 non uniformity
- **200 readout chips needed** (to be produced in 2008)
• Technology: AMS SiGe 0.35µm
• Package: CQFP240
• Power consumption: 350mW
  ✓ 5mW/ch
• Area=16mm²
• Submitted March 2006
• Received July 2006

MAROC block diagram

- Hold signal 1
- Photomultiplier
- 64 channels
- Photons
- Variable Gain Preamp.
- Variable Slow Shaper 50-100 ns
- Bipolar Fast Shaper
- Gain correction 64*6bits
- 3 discri thresholds (3*12 bits)
- 64 inputs
- Or 64 SiPM

- Hold signal 2
- S&H 1
- S&H 2
- MUX
- 64 Wilkinson 12 bit ADC
- 80 MHz encoder
- EN_serializer
- Cmd_LUCID
- LUCID
- LUCID
- 3 DACs 12 bits
- SUM of 7 fibres
- 64 trigger outputs
- Multiplexed Analog charge output
- Multiplexed Digital charge output
- 9 Sums
• Variable gain preamplifier (6 bits)
• Super common base inputs:
  ✓ Low impedance (50-100 W) tunable
  ✓ Low bias current (20mA)
• Slow shaper
• 2 Track & Hold (baseline and max)
• Analog and digital multiplexed charge output

Thresholds are set thanks to 10 bits DACs

Possibility to have 3 encoded trigger outputs
MAROC - Specifications

- Variable gain preamplifier 0-4 to correct PM non uniformity
- 100% trigger efficiency at 1/3 p.e (= 50fC)
- $Q_{\text{max}} = 5pC (=30 \text{ p.e})$
- Noise = 2fC
- Linearity ~ 2%
- Cross talk : 1%

- Characterisation tests performed in lab
- Dedicated test board driven by a PC through a USB connection
- Labview software
Threshold - DAC Linearity

- Three DACs made of two parts
  - Thermometer:
    - 4 bits DAC
    - coarse tuning
    - ~200 mV/bit
  - Mirror:
    - 6 bits DAC
    - fine tuning
    - ~3 mV/bit
- Dynamic range ~2V
- Linearity: +/- 1%
Pedestals

• Uniform slow and fast shaper pedestal
  ✓ Dispersion < 0.1 %

• Very nice stability
  ✓ Variation < 0.1%
S-curves vs injected charge

- Input charge ($Q_{inj}$) scan with fixed threshold
  - Trigger efficiency 100% around 50 fC ($1/3p.e \approx 50$ fC with $10^6$) as requested
  - Nice spread of 50% trigger efficiency point: 2.85 fC rms
  - Unipolar Fast Shaper 5 fC peak to peak

Channel dispersion without any correction
S-curves linearity vs threshold

- Study of threshold effect on S-curves vs Qinj
- Linearity better than ±1%
- Linear for different gains
S-curves vs threshold

- Threshold scan with fixed injected charge
- Linearity vs injected charge is ~1%
Trigger output crosstalk

- Central channel fed with signal up to 10pC triggers at 50fC
- Neighboring channels do not trigger before 1.5-2.5pC
  ⇒ Cross talk ~2-3%

- Cross talk sensitive to the gain
  - It comes from the entry (preamplifier or test board)

- Cross talk signal appears for an input signal >10pe for a threshold~50fC
Slow Shaper – Charge Output

- Waveforms taken for different preamplifier gains with fixed input charge: Qinj=100fC
  - Gain: ~150mV/pC
  - Linearity vs gain:±1%

- Cross talk on the slow shaper path is <1%
Charge output linearity

- Measurements performed with the external ADC of the test board
- The pedestal (measured with the first T&H) was suppressed
- Linearity of ±2% approximately
Conclusions - what next?

• Second version of MAROC has showed nice performances
• It will be used during beam tests this winter
  ✓ Full Roman Pot prototype
  ✓ New generation of the PMF (PhotoMultiplier Front-end)
Asic production for CALICE calorimeter: HARDROC, SKIROC, SPIROC
(CAlorimeter for the LInear Collider Experiment)

- **Detectors:** ✓ **ECAL:** electromagnetic calorimeter:  
  → Front PCB  
  → Front end ASIC  
  → Calibration

- **HCAL:** Hadronic Calorimeter:  
  → AHCAL: Analogue  
  → DHCAL: Digital

- **Requirements for electronics**
  ✓ Large dynamic range (15 bits)
  ✓ Auto-trigger on ½ MIP
  ✓ On chip zero suppress
  ✓ Front-end embedded in detector
  ✓ **Ultra-low power:** (≈ 100µW/ch)
  ✓ 10⁸ channels
  ✓ Compactness
HARDROC has been designed to read out the CALICE RPC DHCAL technical prototype.

RPC: Resistive Plate Chamber

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HARDROC main features

- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output @ 1 or 5MHz
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format: $128 \times (2\text{bit} \times 64\text{ch} + 24\text{bit(BCID)} + 8\text{bit(Header)}) = 20\text{kbits}$
- BASICALLY: MAROC with internal RAM and time counting
HARDROC1: TESTBOARD with a packaged chip
HARDROC1: TESTBOARD with Chip On Board
Slow Shaper and Bipolar Fast Shaper waveforms (scope measurements)

- BFS: 100fC => 350mV, tp=15ns, ie 3.5mV/fC
- SS: 10 pC => 535mV, tp=150 ns
### Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs/outputs</td>
<td>64 inputs, 1 serial output</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>50-70Ω</td>
</tr>
<tr>
<td>Gain Adjustment</td>
<td>0 to 4, 6bits, accuracy 6%</td>
</tr>
<tr>
<td>Bipolar Fast Shaper</td>
<td>$\approx 3.5 \text{ mV/fC, } \text{tp}=15\text{ns}$</td>
</tr>
<tr>
<td>10 bit-DAC</td>
<td>2.5 mV/fC, INL=0.2%</td>
</tr>
<tr>
<td>Trigger sensitivity</td>
<td>Down to 10fC</td>
</tr>
<tr>
<td>Slow Shaper (analog readout)</td>
<td>$\approx 50 \text{ mV/pC, } 5\text{fC to } 15\text{pC, } \text{tp= 50ns to 150ns}$</td>
</tr>
<tr>
<td>Analog Xtk</td>
<td>2%</td>
</tr>
<tr>
<td>Analog Readout speed</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Memory depth</td>
<td>128 (20kbits)</td>
</tr>
<tr>
<td>Digital readout speed</td>
<td>5MHz or more</td>
</tr>
<tr>
<td>Power dissipation (not pulsed)</td>
<td>100 mW (64 channels)</td>
</tr>
</tbody>
</table>
Auto trigger with 10fC:
Q_inj = 10fC in Ch7
DAC0 and DAC1 = 255 (~5fC)
SKIROC -> Silicon Kalorimeter Integrated Read Out Chip

- W-SI electromagnetic calorimeter
- 36 channels

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Main features

• Designed for 5*5 mm² pads
• 36 channels (instead of 72 to reduce cost of prototype)
• Auto-trigger
  ✓ MIP/noise ratio on trigger channel : 16
• 2 gains / 12 bit ADC → 2000 MIP
  ✓ MIP/noise ratio : 11
• Power pulsing
  ✓ Programmable stage by stage
• Calibration injection capacitance
• Embedded bandgap for references
• Embedded DAC for trig threshold
• Compatible with physic proto DAQ
  ✓ Serial analogue output
  ✓ External “force trigger”
• Probe bus for debug

• 24 bits Bunch Crossing ID
• SRAM with data formatting
• Output & control with daisy-chain

Digital on FPGA for debug
One channel description

- **Preamp**
  - Gain: 10
  - Time Constant: 200 ns

- **Slow Shaper**
  - Gain: 1
  - Time Constant: 200 ns

- **Analog Memory**
  - Depth: 5

- **Amplifier**
  - Gain: 5

- **Fast Shaper**
  - Gain: 100
  - Time Constant: 100 ns

- **Hold**

- **10-bit DAC**
  - Common to the 36 Channels

- **3-bit Threshold Adjustment**

- **12-bit ADC**

- **Gain Selection**

- **Charge Measurement**

- **Trigger**

- **Input**
  - 20 MΩ
  - 1 MΩ
  - 0->6 pF

- **Calibration Input**
  - 3 pF
The technologic prototype

- A tungsten-carbon fiber structure
- Detector slabs, hosting silicon wafer and front-end electronic slid in the structure
The ASU (Active Sensor Unit)

- Each detector slab is composed of several Active Sensor Unit (ASU) stitched together.

- An ASU is a ultra-thin PCB hosting Si Wafers on one side and VFE electronic on the other.

To ensure such a high integration, the VFE ASIC:
- Run autonomously
- Don’t need external component
  - No bias resistor
  - No decoupling capacitance
  - No matching component

VFE ASIC bonded in a PCB
SPIROC: Silicon Photomultiplier Integrated Read Out Chip

SPIROC has been designed to read out the CALICE AHCAL technical prototype.

Equip 10,000 channels demonstrator in 2009

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• 36-channel readout chip
• Self triggered
• Energy measurement:
  ✓ 2 gains / 12 bit ADC 1 pe → 2000 pe
  ✓ Variable shaping time from 50ns to 100ns
  ✓ pe/noise ratio : 11
• Time measurement:
  ✓ 1 TDC (12 bits) step~100 ps – accuracy ~1ns
  ✓ pe/noise ratio on trigger channel : 24
  ✓ Fast shaper : ~15ns
  ✓ Auto-Trigger on ½ pe
• Internal input 8-bit DAC (0-5V) for SiPM gain adjustment

Technology: AMS SiGe 0.35μm technology
Surface: 32mm² (4.2mm × 7.2mm)
Power supply: 5V/3.5V
Consumption: 25μW per channel (in power pulsing mode)
Package: CQFP240

It is a System on chip device, including control and communication features
Simulation obtained with SiPM gain $= 10^6$ \(-1\) pe $= 160$ fC

High gain Preamplifier response

Low gain Preamplifier response

Fast shaper

Tp$=15$ns

Noise/pe ratio $= 25$

120mV/pe

High gain Slow shaper

Tp$=50$ns

Noise/pe ratio $= 11$

10mV/pe

Low gain Slow shaper

Tp$=50$ns

Noise/pe ratio $= 3$

1mV/pe

Simulation obtained with SiPM gain $= 10^6$ \(-1\) pe $= 160$ fC

High gain Preamplifier response

Low gain Preamplifier response

Fast shaper

Tp$=15$ns

Noise/pe ratio $= 25$

120mV/pe

High gain Slow shaper

Tp$=50$ns

Noise/pe ratio $= 11$

10mV/pe

Low gain Slow shaper

Tp$=50$ns

Noise/pe ratio $= 3$

1mV/pe
Several large dynamic range ASICs have been developed for CALICE physics prototypes

- ECAL W-Si calorimeter: FLC_PHY3 = 10^4 channels in beam, dynamic range 0.1-600 MIPS
- AHCAL Tile-SiPM calorimeter: FLC_SiPM = 10^3 channels installed, beam in summer 06
- DHCAL GEM/RPC

3 major second generation ASICs for technological prototypes were submitted

- HARdROC submitted for DHCAL RPCs: Ongoing measurements
- SKIROC submitted for ECAL Si-W: Ongoing measurements
- SPIROC for AHCAL SiPM
ASPI: Analog Signal Processing IC – CMOS 0.35um

- 8 (16) channels for 2800 channels read out
- 2 solutions in the first ASIC prototype: ‘Double Correlated Sampling’
  ‘Clamp & Sample’

1st prototype: July 25th, 2007

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IN2P3 Electronics Contribution

• Requirements

✓ 5nV/Hz maximum noise density [5 to 6 e- read noise (10nV/Hz) for the whole CCD chain]
✓ Operation @ 250kHz to 500kHz
✓ 0.01% maximum crosstalk at 500kHz
✓ 100.000e- full well capacity
✓ less than 20 to 25mW/channel power dissipation
✓ 0.5% or better linearity [defined over 0 to 100.000 e- full well]
✓ differential output OV +/- 2.5V
✓ Output Load ~ 25pF // 1kΩ
✓ Power Supply : +/- 2.5V with respect to references = ground.
✓ ASiC is driven by a MOS with an equivalent output resistance around 5kΩ to 10 kΩ.
✓ To avoid excessive number of penetrations, the circuit has to operate inside this cryostat at a temperature of ~173K.
• Technology 0.35µm SiGe:
  ✓ Low noise
  ✓ More fast
  ✓ Low consumption

• The versatility of our chips – using programmable parameters (gain, peaking time, thresholds) make them suitable for many applications

• More digital part integrated in chip

• 4 new complex multi channel chips were made in short term

• Electronic to read out MA-PMT, SiPM or APDs, RPC...
• Collaboration in the CALICE project
  (CAlorimeter for the LInear Collider Experiment)

• Other experiments and collaborations:
  ✓ ATLAS luminometer
  ✓ PMM2: neutrino
  ✓ Medical imaging: ISS at Roma
  ✓ Double chooze (neutrino): Nevis Columbia
  ✓ LSST: Brookaven and LPNHE (Jussieu)
  ✓ So one….