Performance of Programmable Logic Devices (PLDs) in read-out of high speed detectors

Jack Fried
INSTRUMENTATION DIVISION

- PLD
- Muon Tracker PLD
What Is a PLD
PLD Building Blocks
Logic Block
# Device Features

## Table 1. FLEX 10K Device Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPF10K10</th>
<th>EPF10K20</th>
<th>EPF10K30</th>
<th>EPF10K40</th>
<th>EPF10K50</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (logic and RAM) (1)</td>
<td>10,000</td>
<td>20,000</td>
<td>30,000</td>
<td>40,000</td>
<td>50,000</td>
</tr>
<tr>
<td>Maximum system gates</td>
<td>31,000</td>
<td>63,000</td>
<td>69,000</td>
<td>93,000</td>
<td>116,000</td>
</tr>
<tr>
<td>Logic elements (LEs)</td>
<td>576</td>
<td>1,152</td>
<td>1,728</td>
<td>2,304</td>
<td>2,880</td>
</tr>
<tr>
<td>Logic array blocks (LABs)</td>
<td>72</td>
<td>144</td>
<td>216</td>
<td>288</td>
<td>360</td>
</tr>
<tr>
<td>Embedded array blocks (EABs)</td>
<td>3</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>6,144</td>
<td>12,288</td>
<td>12,288</td>
<td>16,384</td>
<td>20,480</td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>150</td>
<td>189</td>
<td>246</td>
<td>189</td>
<td>310</td>
</tr>
</tbody>
</table>

## Table 1. APEX II Device Features

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum gates</td>
<td>1,900,000</td>
<td>2,750,000</td>
<td>3,000,000</td>
<td>5,250,000</td>
</tr>
<tr>
<td>Typical gates</td>
<td>600,000</td>
<td>900,000</td>
<td>1,500,000</td>
<td>3,000,000</td>
</tr>
<tr>
<td>LEs</td>
<td>16,640</td>
<td>24,320</td>
<td>38,400</td>
<td>67,200</td>
</tr>
<tr>
<td>RAM ESBs</td>
<td>104</td>
<td>152</td>
<td>160</td>
<td>280</td>
</tr>
<tr>
<td>Maximum RAM bits</td>
<td>425,984</td>
<td>622,592</td>
<td>655,360</td>
<td>1,146,880</td>
</tr>
<tr>
<td>True-LVDS channels</td>
<td>36 (1)</td>
<td>36 (1)</td>
<td>36 (1)</td>
<td>36 (1)</td>
</tr>
<tr>
<td>Flexible-LVDS™ channels (2)</td>
<td>56</td>
<td>56</td>
<td>88</td>
<td>88</td>
</tr>
<tr>
<td>True-LVDS PLLs (3)</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>General-purpose PLL outputs (4)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>492</td>
<td>612</td>
<td>735</td>
<td>1,060</td>
</tr>
</tbody>
</table>
PLD Features
(cont)

The Altera® APEX™ embedded programmable logic device (PLD) family, meets the system-level design challenge by offering complete system integration on a single device. (Click on the features above for more information.)
Plug In Manager

Available Megafuntions:

Which megafuntion would you like to customize?

Which type of output file do you want to create?
- AHDL
- VHDL
- Verilog HDL

What name do you want for the output file?

Note: To compile a project successfully in the MegaWizard software, your design files must be in the project directory of a user library that you specify with the User Libraries command (Options menu).

Your current user library directories are:

Which optional output control signals do you want?

- full
- empty
- used[] (number of words in the FIFO)
- almost full
- almost empty
- synchronous clear (flush FIFO)

Do you want to add a common clock for reading and writing the FIFO?
- Yes, synchronize both reading and writing to 'clock'.
- No, do not use 'clock'.

How wide should the FIFO be?
- 8 bits
- 256 words

How deep should the FIFO be?
- 8 bits
- 256 words

Do you want the FIFO to clear its output flags?
- Yes, add logic to achieve this.

Do you want the FIFO to clear its output flags?
## Mega Functions

<table>
<thead>
<tr>
<th>Megafunction Name</th>
<th>Vendor</th>
<th>PDF</th>
<th>Free Evaluation</th>
<th>Certifications</th>
<th>Device Families Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>10/100 Ethernet MAC</strong></td>
<td>Altera Corporation</td>
<td></td>
<td>Try OpenCore</td>
<td>SDPC Builder Ready, I-Tested</td>
<td>APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, HardCopy</td>
</tr>
<tr>
<td><strong>8b:10b Encoder/Decoder version 1.1.0</strong></td>
<td>Altera Corporation</td>
<td></td>
<td>Try OpenCore</td>
<td></td>
<td>APEX, FLEX 10KE, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Mercury, HardCopy</td>
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<tr>
<td><strong>ARM922T</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>ARM-based Excalibur</td>
</tr>
<tr>
<td><strong>ATM Cell Processor Compiler</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>Atlantic Compliant</td>
<td>APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon DMA</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon Interface to User Logic</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon On-Chip RAM</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon On-Chip ROM</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon PIO</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
<tr>
<td><strong>Avalon SDRAM Controller</strong></td>
<td>Altera Corporation</td>
<td></td>
<td></td>
<td>SDPC Builder Ready</td>
<td>FLEX 10KE, APEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy</td>
</tr>
</tbody>
</table>
Design Verification

• Simulation
• Built in real time
  Logic analyzer
PLD Design Flow
PHENIX Muon Tracker
Cathodes Read-Out Card (CROC)

- **Design Requirements**
  - 64 Channel Readout per CROC
  - Less than 3125 electrons (RMS) noise for 10-150 pF of detector capacitance (including 24” cable)
  - Less than 1% crosstalk between any channels on the board
  - gain: 3.5mV/ fC
  - Digital/ Analog isolation

- **Main Components**
  - AMU-ADC
  - CPA

Digital/Analog isolation
Controller Card (CNTL)

- **Design Requirements**
  - Control AMU/ADC data collection, conversion and read-out
  - Provide connection to 2 CROC boards
  - Provide connection to the outside world
  - Support the T&FC and DCM interface
  - Provide data relay from remote controller board to DCM
  - Support ARCnet connectivity to serial configuration bus

- **FPGA - the brain**
  - developed by Jack
  - work in progress
Requirements for Muon tracker PLD

- Trigger rate 25Khz
- 4 samples per pulse
- Sample new data on every beam crossing
- Holds 5 events
- 100ns between triggers (burst rate)
- Control digital part of AMUADC -RD -WR
- Send data to DCM
- Allow for Master and slave modes
Muon Tracker

PLD Programming Difficulties

- Board already designed
  - PLD already chosen (FLEX 10K 50E)
  - Pins allocated
  - PLD to small
- Overlapping events
- AMUADC noise problems
- AMUADC requires special RD WR sequence
ALTERA
10K50

Table 1. FLEX 10KE Device Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPF10K30E</th>
<th>EPF10K50E</th>
<th>EPF10K50S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (f)</td>
<td>20,000</td>
<td>50,000</td>
<td></td>
</tr>
<tr>
<td>Maximum system gates</td>
<td>119,000</td>
<td>189,000</td>
<td></td>
</tr>
<tr>
<td>Logic elements (LEs)</td>
<td>1,726</td>
<td>2,930</td>
<td></td>
</tr>
<tr>
<td>EABs</td>
<td>0</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>24,576</td>
<td>40,990</td>
<td></td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>220</td>
<td>264</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5. FLEX 10KE EAB Memory Configurations

Figure 6. Examples of Combining FLEX 10KE EABs
Memory Requirements

- 4 samples per event
- Need to be able to store 5 events
- Each sample is 11 bits
- 32 channels per AMUADC
  - 4 AMUADC PER CNTL 128 channels

28160 BITS TOTAL
Memory Implementation

- Used 9 EABs
- Only 1 EAB left for PLD algorithm
- Lost 8704 bits
AMUADC cell

Writing & Reading

SINGLE EVENT

STORES ANALOG VALUE EVERY BEAM CLOCK

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | …… | 60 | 61 | 62 | 63 | 64 |

SAMPLES 10 11 12 15

40 beam clocks back

TRIGGER LVL1

AFTER CELLS SELECTED THEY ARE REMOVED TILL CONVERTED AND STORED THEN THEY ARE PUT BACK
Overlapping Events

Overlapping Event

Stores analog value every beam clock.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | …… | 60 | 61 | 62 | 63 | 64 |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

After cells selected they are removed till converted and stored then they are put back.

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
<th>17</th>
<th>18</th>
<th>19</th>
<th>20</th>
<th>……</th>
<th>60</th>
<th>61</th>
<th>62</th>
<th>63</th>
<th>64</th>
</tr>
</thead>
</table>

Samples 14 15 17 19

4 clock later

Samples 10 11 13 15

40 beam clocks back

Trigger LVL1
MUON TRACKER
PLD

FPGA

TFC

DCM

AMU ADC DATA

AMU ADC CONTROL AND DATA ADDRESS

AMU ADC READ WRITE ADDRESS

AUXPORT

ARCNET
MUON TRACKER
PLD
If conversion list fifo empty signal is false (not empty) than there is data that needs to be converted.

After reset load shift reg with a 0-64 counter.

EVENT LIST IN CORRECT ORDER TO DATA READ OUT MANAGER

Data available signal

Conversion list

IN ORDER OF CONVERSION

MUX 43 to 1  6 bit

MUX 43 to 1  6 bit

MUX 43 to 1  6 bit

MUX 43 to 1  6 bit

COUNT to 4 counter.

Start on level 1 and sav = high when counting.
AMU ADC Controller

- AMU ADC Controller
- COUNTER
- CONTROL
- LOGIC
- FSC
- DATA AVAILABLE
- CLK
- NEXT LOGICAL MEMORY LOCATION (9..5)
- MEMORY LOCATION COUNTER
- 4 x clk
- COUNTER
- LOGIC
- start
- stop
- AZ
- ICS
- AMP_RST
- DB_RST
- COMPRST
- LOAD
- CLK_EN
- R_EN
- AMU READ ADDRESS AND MEMORY WRITE ADDRESS (4..0)
- CLK
- clk
Read Out Manager
part 1

From Cell Manager
Cell Events list
in correct order

SAV
CLK

counter
0-19

5bits

DECODE
5 to 20

CELL EVENT LIST

0

event 1\textsuperscript{x} sample 1

1

event 1\textsuperscript{x} sample 2

2

event 1\textsuperscript{x} sample 3

3

event 1\textsuperscript{x} sample 4

4

event 2\textsuperscript{y} sample 1

18

event 5\textsuperscript{x} sample 3

19

event 5\textsuperscript{x} sample 4

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}

6 bit
\text{dflip}
Read Out Manager
part 2

Cell Event list location 1
Cell just converted

Cell Event list location 2
Cell just converted

Cell Event list location 3
Cell just converted

Cell Event list location 4
Cell just converted

Cell Event list location 19
Cell just converted

mem add = logical memory address where the cell just converted is located

mem add (4..0)

clk

DFLIP

&

LOGIC

compare

1

mem add (4..0)

clk

DFLIP

&

LOGIC

compare

1

mem add (4..0)

clk

DFLIP

&

LOGIC

compare

1

mem add (4..0)

clk

DFLIP

&

LOGIC

compare

1

mem add (4..0)

clk

MUX 20 to 1

5 bit

mem rd add [9..5]

COUNTER

0 to 19

NEXT SAMPLE

clk

sel
Read Out Manager
Part 3

DATA STORAGE

DUAL PORT RAM
512kX44
6 - 512x8
EABs

DUAL PORT RAM
128kX44
3 - 256x16
EABs

SIMPLIFIED MEMORY
BLOCK DIAGRAM

LOGICAL MEMORY
BREAK UP

20 POSSIBLE LOCATION TO STORE SAMPLES TO COVER 5 EVENTS 4 SAMPLES WITH UNIQUE CELLS
### Compilation Result

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total dedicated input pins used:</td>
<td>3/6</td>
<td>50%</td>
</tr>
<tr>
<td>Total I/O pins used:</td>
<td>166/283</td>
<td>50%</td>
</tr>
<tr>
<td>Total logic cells used:</td>
<td>2403/2880</td>
<td>83%</td>
</tr>
<tr>
<td>Total embedded cells used:</td>
<td>94/160</td>
<td>58%</td>
</tr>
<tr>
<td>Total EABs used:</td>
<td>10/10</td>
<td>100%</td>
</tr>
<tr>
<td>Average fan-in:</td>
<td>2.16/4</td>
<td>54%</td>
</tr>
<tr>
<td>Total fan-in:</td>
<td>4238/11520</td>
<td>36%</td>
</tr>
</tbody>
</table>

#### **Device Summary**

```markdown
<table>
<thead>
<tr>
<th>Chip/Device</th>
<th>Pins</th>
<th>PIns</th>
<th>Bidir</th>
<th>Memory</th>
<th>Memory</th>
<th>LcS</th>
<th>Lcs</th>
<th>Utilized</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTRL Pld EPF10K300I240-2</td>
<td>8L</td>
<td>68</td>
<td>20</td>
<td>28352</td>
<td>60%</td>
<td>2403</td>
<td>83%</td>
<td></td>
</tr>
<tr>
<td>User Pins:</td>
<td>8L</td>
<td>68</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

***** Project compilation was successful *****

** Total input pins required: 61 **
** Total input I/O cell registers required: 20 **
** Total output pins required: 68 **
** Total output I/O cell registers required: 5 **
** Total buried I/O cell registers required: 0 **
** Total bidiirectional pins required: 20 **
** Total reserved pins required: 0 **
** Total logic cells required: 2403 **
** Total flipflops required: 1141 **
** Total packed registers required: 0 **
** Total logic cells in carry chains: 142 **
** Total number of carry chains: 22 **
** Total number of carry chains of length 1-8: 19 **
** Total number of carry chains of length 9-16: 3 **
** Total logic cells in cascade chains: 532 **
** Total number of cascade chains: 265 **
** Total single-pin Clock Enables required: 0 **
** Total single-pin Output Enables required: 0 **
** Logic cells inserted for fitting: 27 **

Synthesized logic cells: 159/2880 | 5%
Current code
Muon FEE

- PLD - current code
  - store every beam crossing
  - 4-sample per pulse
  - readout time 53uS
  - hold 4 events

![Graph showing time and voltage readings with peaks at specific times.](image)