The First 3D Multi-project Wafer Run for HEP and Brookhaven's Contributions

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Fermilab
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Introduction/Background

- In late 2008 a large number of international laboratories and universities with interest in High Energy Physics formed a consortium for the development of 3D integrated circuits. The first joint effort was to organize a 3D multi-project run utilizing wafers from the Chartered 0.13 um CMOS process and 3D assembly by Tezzaron. This talk will present an overview of that multi-project wafer run.

Consortium Formed for 3D Design

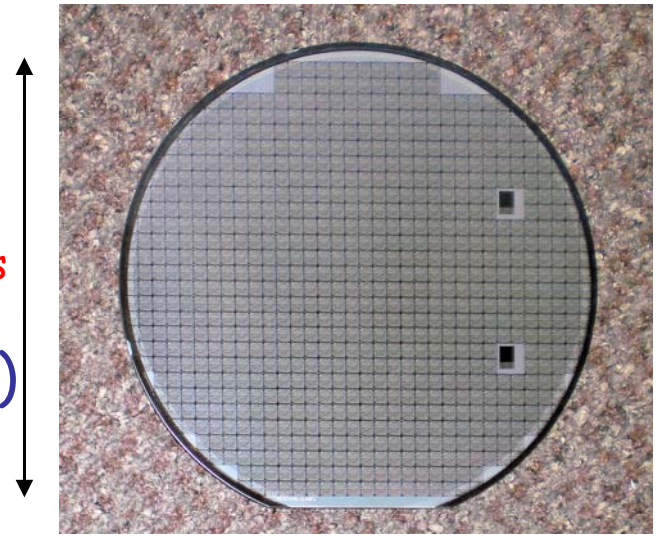
- Consortium presently comprised of 15 members from 5 countries
  - University at Bergamo
  - University at Pavia
  - University at Perugia
  - INFN Bologna
  - INFN at Pisa
  - INFN at Rome
  - CPPM, Marseilles
  - IPHC, Strasbourg
  - IRFU Saclay
  - LAL, Orsay
  - LPNHE, Paris
  - CMP, Grenoble
  - University of Bonn
  - AGH University of Science &Technology, Poland
  - Fermilab, Batavia
- Others contributing to first MPW
  - BNL, Brookhaven
  - LBNL, Berkeley

Consortium

- To join
  - LOI to Fermilab asking to participate in MPW run
  - NDA with Tezzaron
  - No cost (only cost is for MPW space)
- Members receive from Tezzaron
  - Cadence PDK for Chartered 0.13 um
  - Calibre DRC/LVS/PEX(XRC) deck for Chartered 0.13 um CMOS with correct process options
  - Calibre DRC deck for Tezzaron 3D design rules
    - Cu-cu bond interface
    - Via formation
  - Information for fabrication of 2D and 3D I/O pads
  - ARM Artisan library (separate NDA)
    - Full-layout views
  - Also available but not used (separate cost for each)
    - MicroMagic 3DMax (alternative to Virtuoso)
    - Magma (working on 3D LVS)
- Benefits
  - Sharing of design blocks
    - Bergamo/Pavia ← → Strasbourg
    - LBNL ← →FNAL ← → CPPM
    - FNAL ← → Strasbourg
    - Standardized bond interface, scribe line templates, alignment targets
  - Sharing of special software/libraries
    - Fill program by CMP
    - Assura DRC/LVS/RCX deck by FNAL
    - Mixed signal library with separate substrate and ground connections by FNAL
  - Design reviews
    - First check of each design done by FNAL
  - Cost reduction through MPW sharing
  - Sharing of results – to come soon ☺
- Webpage
  - http://3dic.fnal.gov

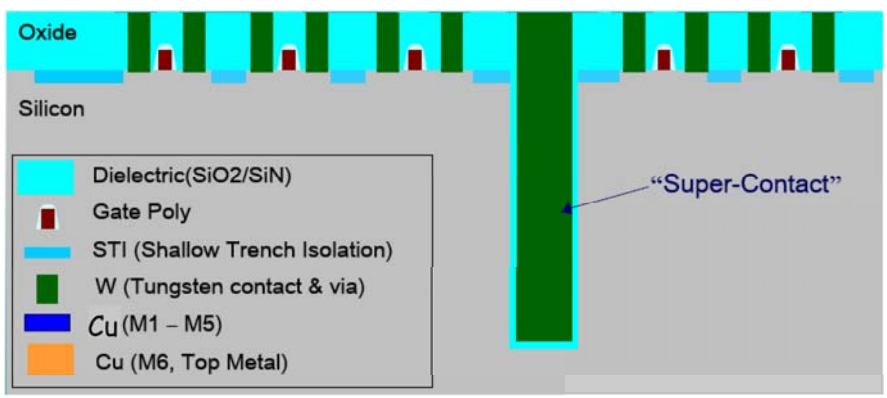
Chartered 0.13 um Process

- 8 inch wafers
- Large reticule ~ 26 mm x 31 mm
- Options chosen
  - Deep N-well
  - MiM capacitors – 1 fF/um^2 (single mask)
  - Single poly
  - 6 levels of metal (8 available) + RDL
  - A variety of transistor families are available (Nominal, Low voltage, High performance, Low power)
    - Low power option chosen
      - Standard Vt
      - Low Vt
      - Zero Vt (native NMOS)
    - I/O transistors – 3.3 V
  - High resistance poly resistors
  - Embedded through silicon vias (via first processing)

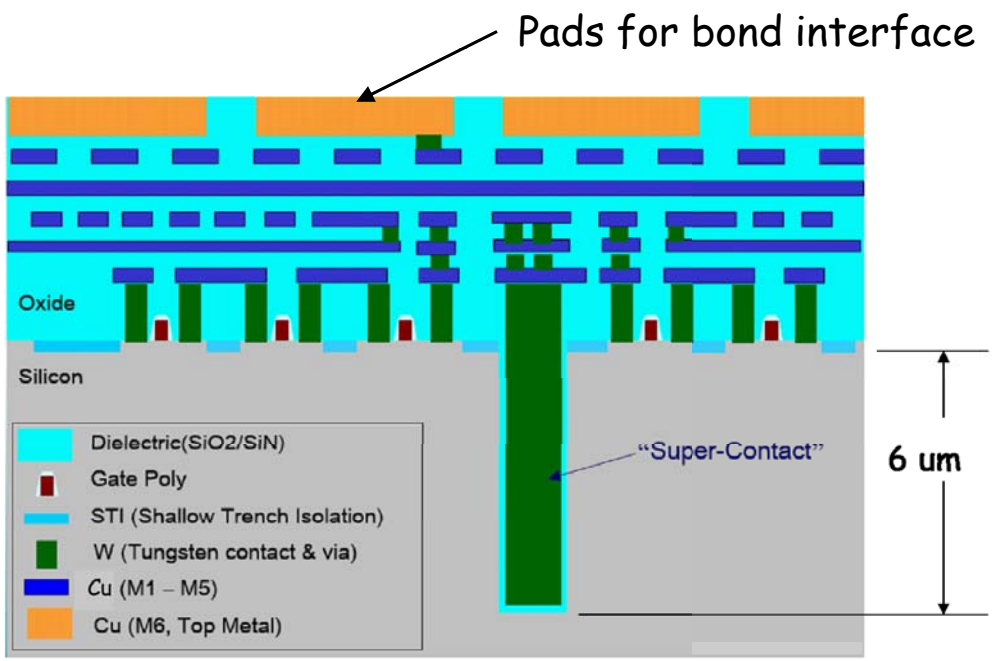


Through Silicon Via Formation

- Via first approach – tungsten through silicon vias are fabricated as a part of the foundry process
  - Fabricate transistors (FEOL)
  - Form via (6 microns deep)
  - Passivate vias
  - Fill vias and connect to transistors at same time



- Complete BEOL processing
  - Add 6 metal layers
  - 6th metal layer is used as a bond interface for Cu-Cu thermo compression.

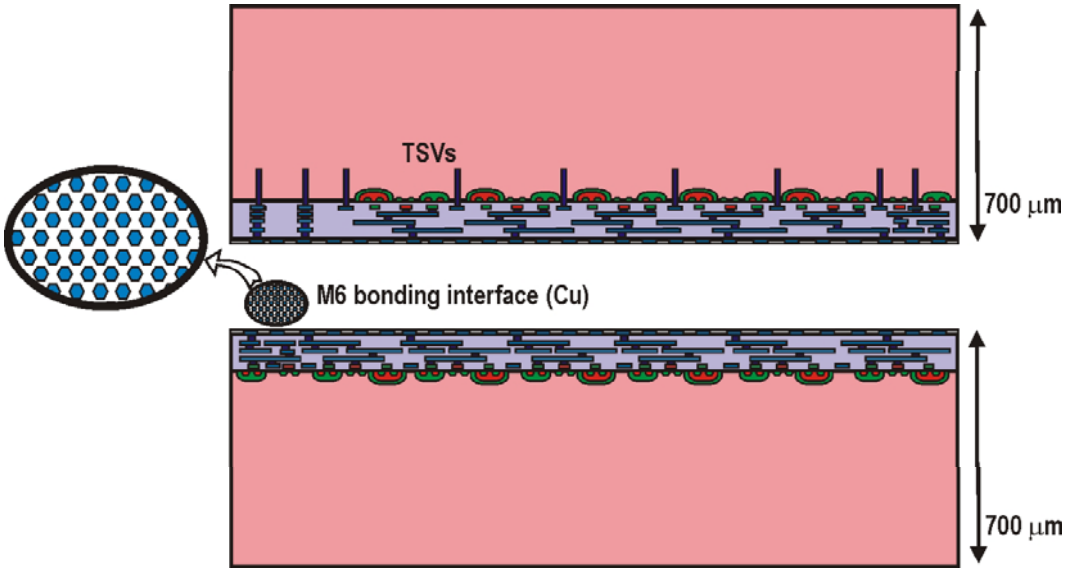


Bond Interface

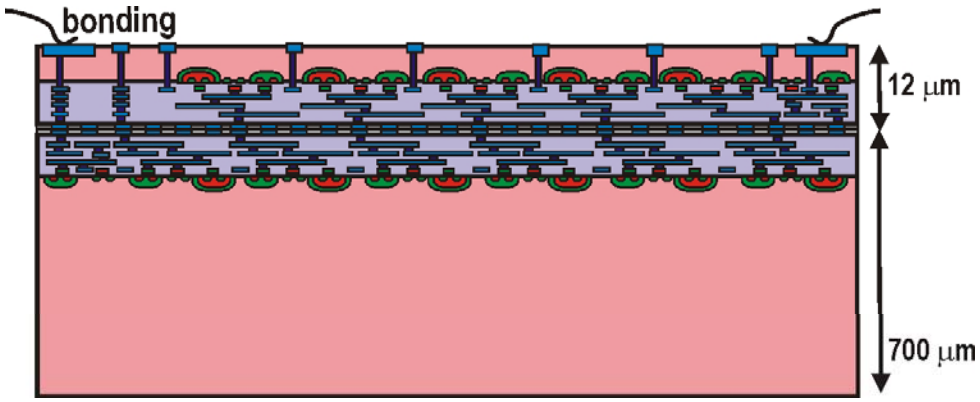
- The bond interface is critical for good yield.
  - Makes electrical and mechanical connections from one wafer to the other wafer.
  - Bond interface must be strong enough to withstand subsequent thinning process.
  - There must be very uniform M6 density across all designs and streets in the MPW run reticule.
  - Standard bond interface provided for all designers.
- Mass of bond interface is insignificant
  - M6 is ~ .8 microns thick, coverage ~ 35%
  - Two M6 layers with 35% coverage gives 1.6 um of Cu resulting in Xo=0.0056%

After Wafer Fabrication 3D Assembly is Completed

- Cu-Cu bond
  - Wafers are aligned to better than 1 micron
  - Thermo compression bond is formed between wafers

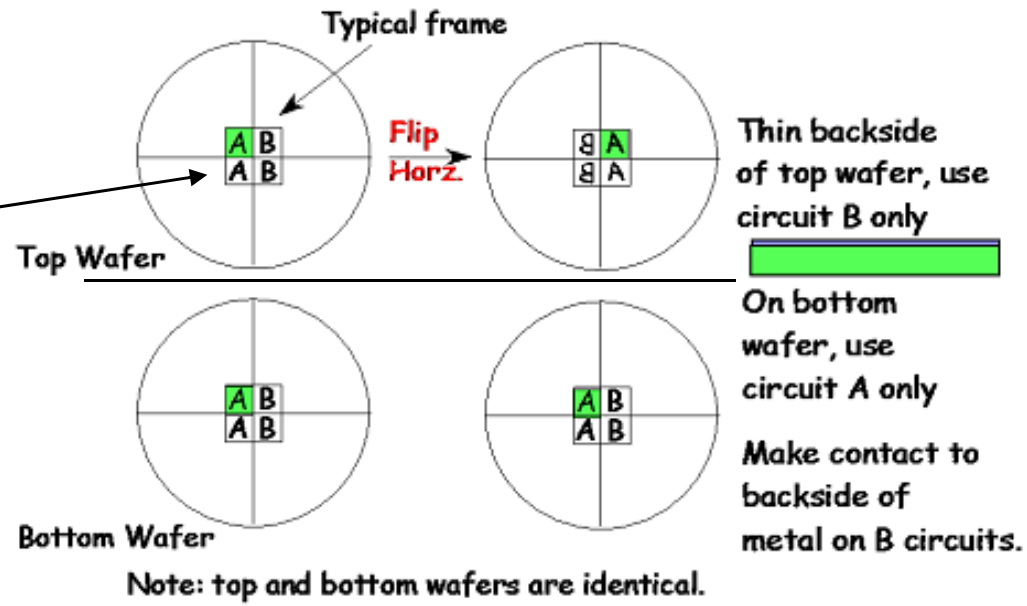


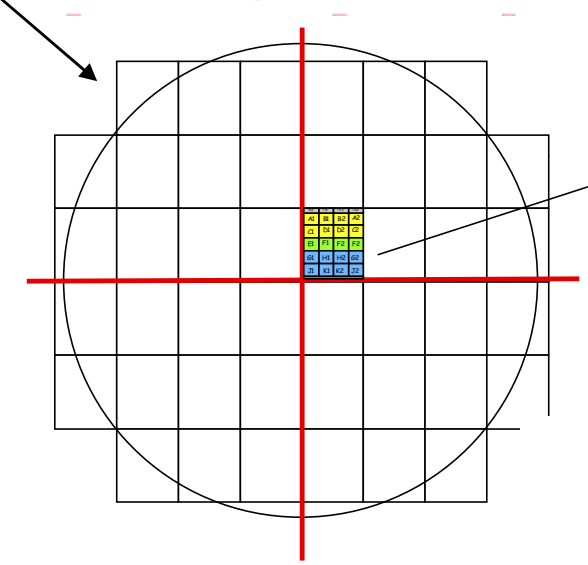
- Thinning and pad formation
  - One wafer thinned to 12 microns to expose TSVs
  - Metal pads added for wire or bump bonding



Frame for First MPW Run

- 3D chip has two tiers
- One set of masks used for both top and bottom tiers to reduce mask cost.
  - Identical wafers bonded face to face by Tezzaron.
  - Backside metallization by Tezzaron.
- Frame divided into 12 subreticules among consortium members
- More than 25 two-tier designs (circuits and test devices)
  - CMS strips, ATLAS pixels
  - ILC pixels
  - B factory pixels
  - X-ray imaging
  - Test circuits
    - Radiation
    - Cryogenic operation
    - Via and bonding reliability
    - SEU tolerance





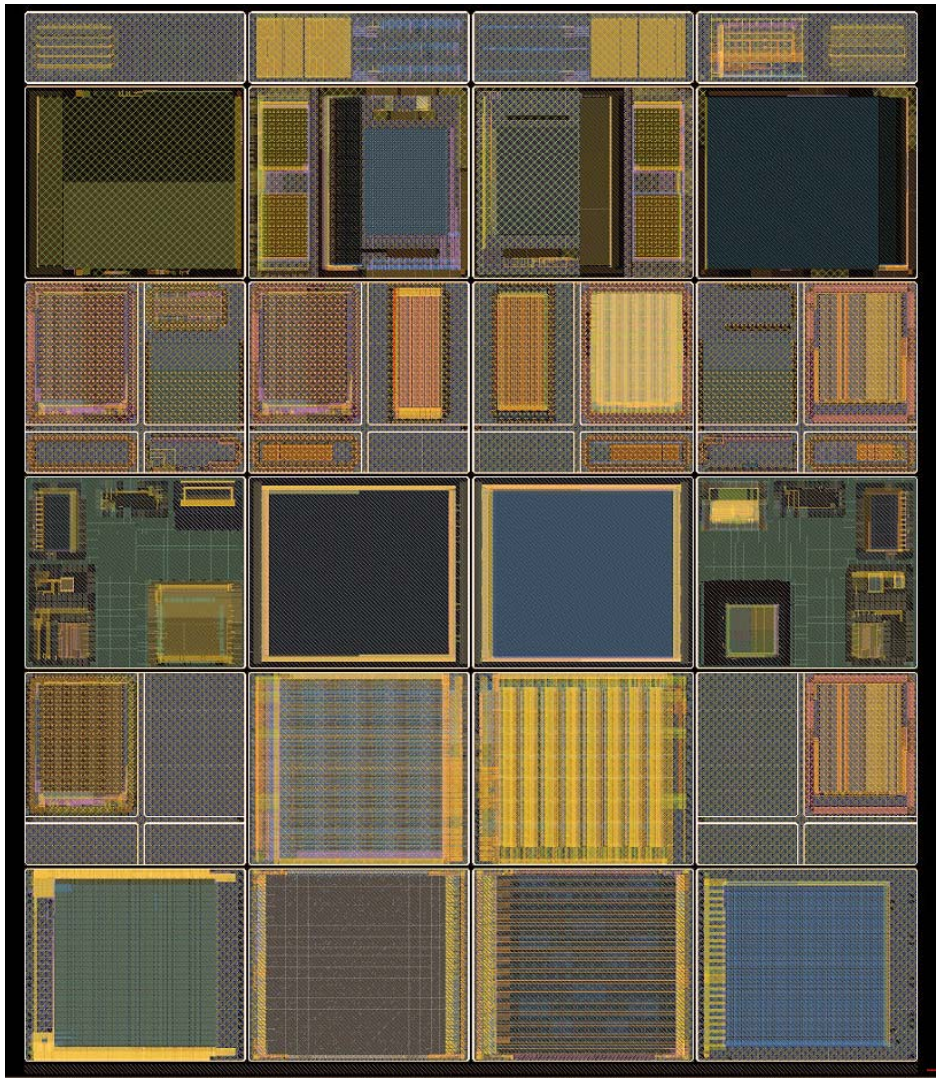
Wafer Map

TXL	TYL	TYR	TXR
AL	BL	BR	AR
CL	DL	DR	CR
EL	FL	FR	ER
GL	HL	HR	GR
IL	JL	JR	IR

MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

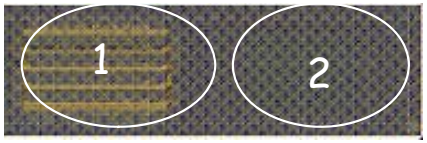
Subreticules:
A, B, C, D, E, F, G, H, I, J
5.5 x 6.3 mm



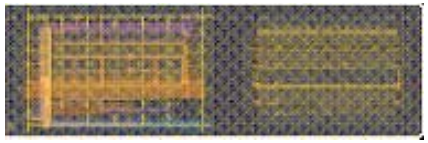
Notice Symmetry about vertical center line

← Top tiers → ← Bottom Tiers →

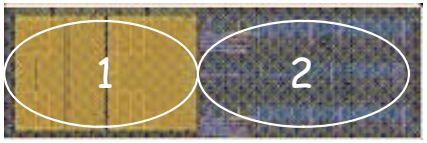
Test Chips TX & TY



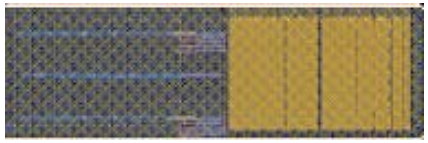
TX Left



TX Right



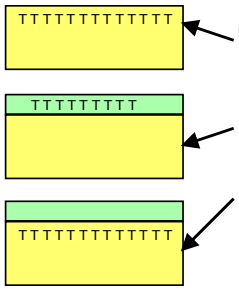
TY Left



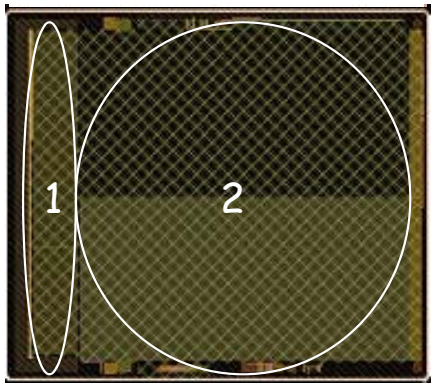
TY Right

- **Subreticule TX**
  - Test transistors for noise, radiation, and cryo measurements
    - 1) NMOS and PMOS transistor array with nominal Vt, low Vt, thick gate oxide I/O, 0 Vt, and 0 Vt thick gate oxide. Measured devices are thinned. (PAVIA)
    - 2) NMOS and PMOS transistor array with different numbers of fingers/transistor for measurements at cryo temperatures. Devices can be measured on thick or thin substrate. (FNAL)
  - 2) Test circuits for VIP2b in subreticule I – (FNAL)
    - Double correlated sampler
    - Single channel FE
    - Front ends with different W/L input transistors
    - Stand alone discriminator

- **Subreticule TY** – (FNAL)
  - 1) Two long daisy chains of bond interconnects to measure interconnect yield.
    - Two different daisy chains having different bond interface patterns
    - Each daisy chain has 140000 bond interconnects with multiple taps
  - 2) Test transistors based on a standard set of devices (~46) used by CERN to characterize different processes.
    - Devices can be measured under different conditions
      - on standard wafers (2D wafers).
      - on thin substrate bonded to a thick second wafer
      - on thick substrate bonded to a thinned second wafer.

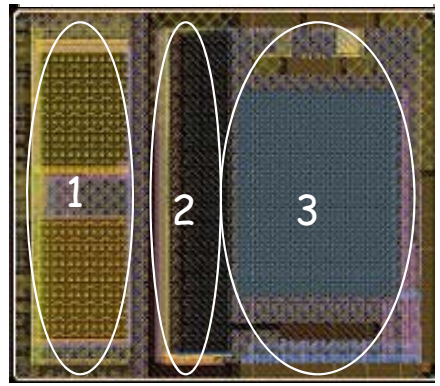


Subreticules A & B Highlights

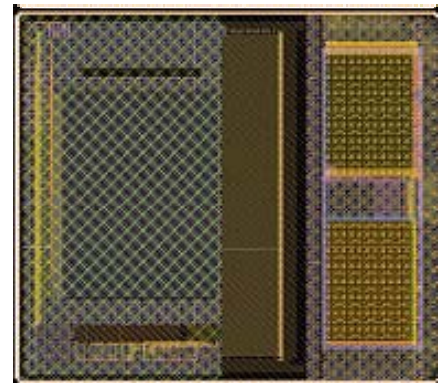


A Left

A Right



B Left

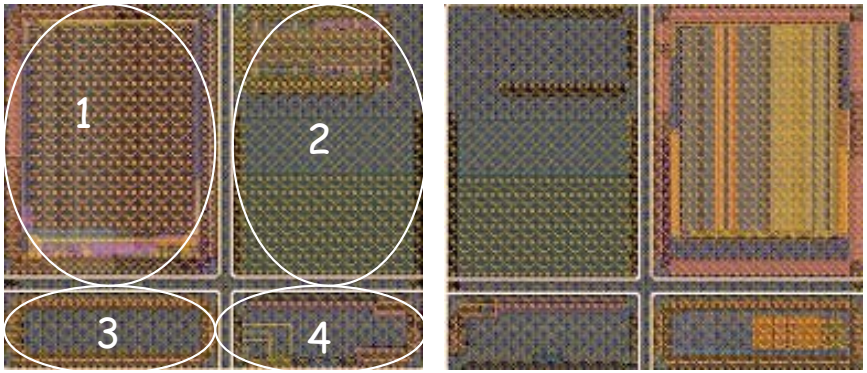


B Right

- Subreticule A – Two subcircuits, intended to be bonded to sensors from XFAB (0.35 um with high Res EPI). An amplifier may be integrated in each sensor pixel
  - 1) ILC application (Strasbourg, Saclay)
    - Rolling shutter, low power tracker, 34 X 240 array, 20 um pitch pixels
    - Amp, Disc. & latch on analog tier, 1 bit memory& readout on digital tier
      - R.O. time=integration time (80 ns/row)
  - 2) ILC and bio-medical applications (Strasbourg, Bergamo, Pavia)
    - Self triggering pixel tracker, 245 x 245 array, 20 um pitch with fast X-Y projection readout
    - 2 sub arrays with different types of feedback caps in amplifier
    - ASD on analog tier, readout on digital tier

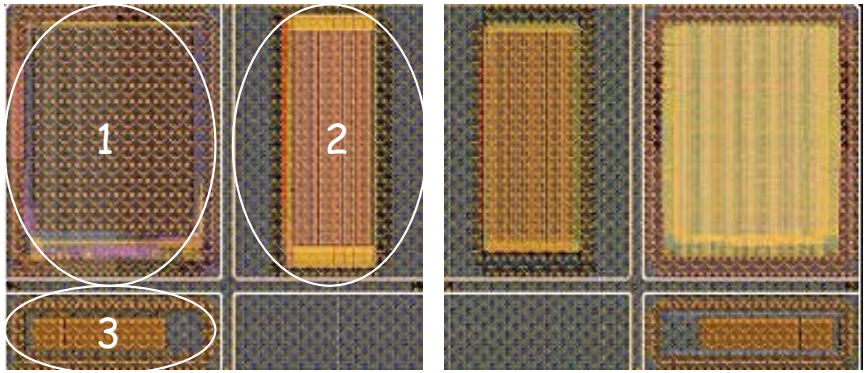
- Subreticule B – Three subcircuits
  - 1) 2 separate memory cores (CMP)
    - one standard design and one with built-in SEL hardness circuitry
  - 2) MAPS for ILC (Saclay, Strasbourg)
    - 42x240 array, 20 um pixel MAPS operating in rolling shutter mode,
      - 80 ns/row
    - Sensor, amp, Disc & latch (NMOS only) on analog tier. 1 bit memory & readout on digital tier
  - 3) MAPS for ILC (Strasbourg)
    - 128 x192 array, 12x24 um pixel MAPS with 5 bit time stamp, 2nd hit marker, full serial readout
      - Future goal: to use separate sensor tier and to reduce the pixel size to 12x12 um.

Subreticules C & D



Left Right

- **Subreticule C** – 4 subreticules
  - 1) ATLAS 2D pixel design based on earlier design in IBM 0.13 um (FEI4)* (CPPM/Bonn)
    - Left (analog) side - 14 col, 60 rows, 50x166 um pixels with simple readout
    - Mating right side comprised of counter and "noisy" cells to study coupling to the left tier with different shielding ideas.
  - 2) SEU resistant register and TSV/bond interface daisy chain to measure TSV as well as bond yield. (CPPM)
  - 3) Test structures to evaluate transistor performance with TSVs in close proximity (CPPM)
  - 4) Test structures to test robustness of circuits under wire bond pads (CPPM)

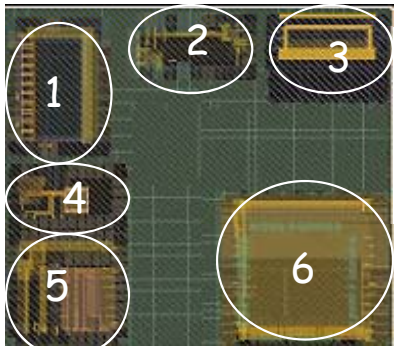


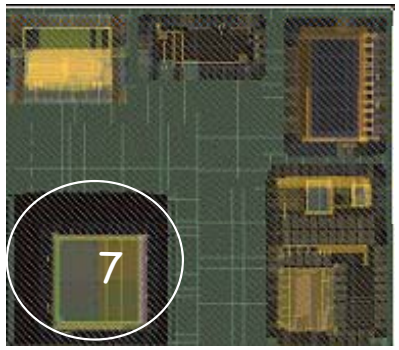
Left Right

- **Subreticule D** – 3 subreticlues
  - 1) ATLAS 3D pixel design foreseen for ATLAS upgrade* (CPPM/Bonn)
    - Left (analog) side - 14 col, 60 rows, 50x166 um pixels (same as subreticule C)
    - Mating right side contains special features such as time stamp, time over threshold, and 4 pixel grouping.
  - 2) Small pixel array for SLHC* (LAL)
    - 24 x 64 array of 50 um pixels
    - ASD, threshold adjustment DAC/pixel, 24 DFF register/pixel
  - 3) TSV capacitance test circuits (CPPM)

*Note: C1, D1, D2 are to be hybridized to sensors provided by Hans-Gunther Moser, MPI

Subreticules E & F

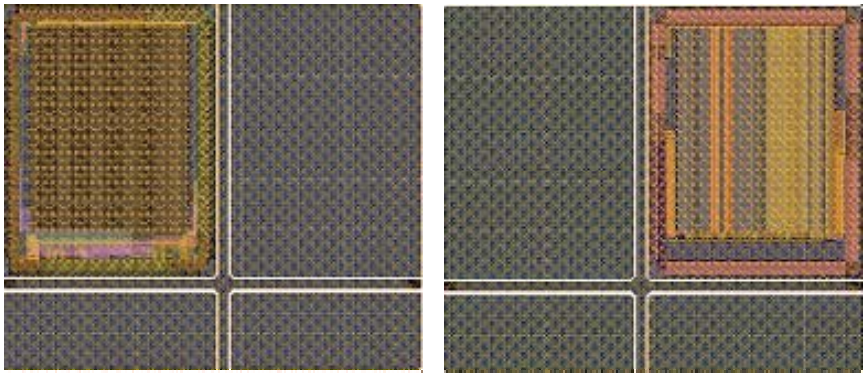




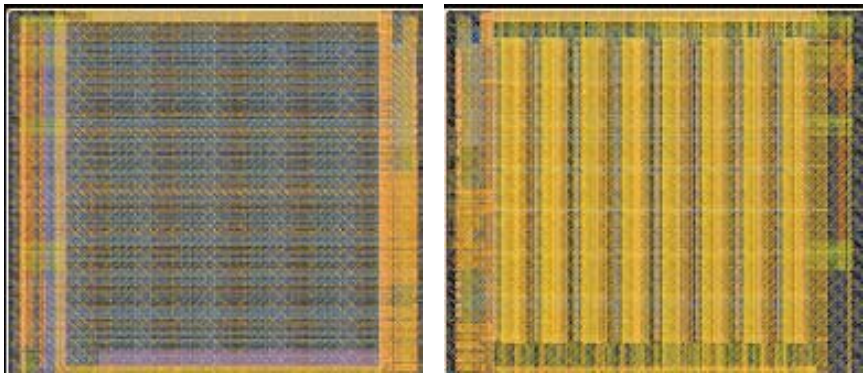
- **Subreticule E** – 7 sub-circuit areas
  - 1) 3D MAPS with 32 x 64 array of 25 um pixels with DCS, 3T FE, discriminator, auto-zeroing. All control logic in digital tier. (Roma)
  - 2) 3D MAPS test structures - Two 3 x 3 40um pitch arrays. One with shaperless preamplifiers. Other is designed with ELT input devices. (Pavia/Bergamo/Pisa)
  - 3) 3D MAPS test structure with 8 x 32 array of 40 um pixels, DNW sensors, data push architecture (Pavia/Bergamo/Pisa/Bologna)
  - 4) Two test structures for the subreticule F DNW MAPS device (Pavia/Bergamo)
    - 16 x 16 array of 20 um pixels with inter-train sparsified readout
    - 8 x 8 array of 20 um pixels with selectable analog readout of each pixel
  - 5) Two 3D test structures
    - 3 x 3 array of 20 um pixels and 4 single channels for DNW MAPS (Pavia/Bergamo)
    - 3D RAPS structures including single ended I/O buffer, two single addressable 3T pixels with small and large area detecting diodes.
      - 5x 5 and 16 x 16 pixel matrices, each one featuring small and large detecting diodes (Perugia)
  - 6) 2D version of 3D MAPS device in subreticule F, 64 x64 array of 28 um pixels (Pavia/Bergamo)
  - 7) 2D sub-matrices with 10 and 20 um pixels to test signal to noise performance of MAPS in the Chartered process (Roma)

- **Subreticule F** – Pavia, Bergamo
  - 3D MAPS device with 256 x 240 array of 20 um pixels with DNW sensors and sparsification for ILC
  - The device may be tested with both a full thickness sensor substrate or with sensor thinned to 6 microns.

Subreticules G & H

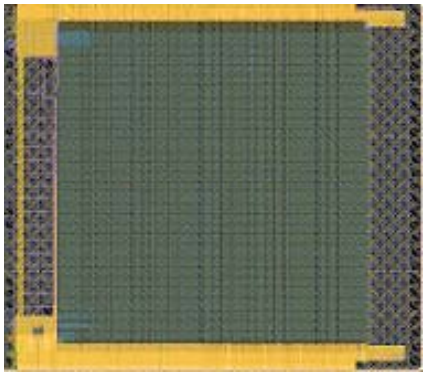
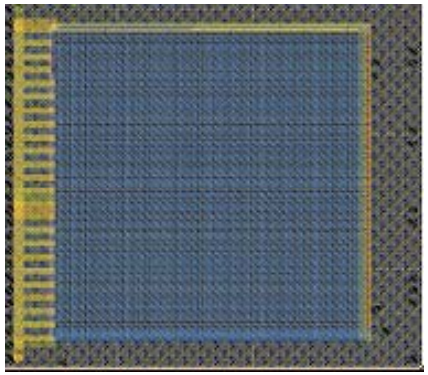


- **Subreticule G** – Orsay/LBNL
  - ATLAS 2D pixel design based on earlier design in IBM 0.13 um (FEI4)
    - Left (analog) side - 14 col, 60 rows, 50x166 um pixels with simple readout
    - Analog tier designed for opposite polarity input from circuits in subreticules C and D.
  - Mating right side comprised of counter and "noisy" cells to study coupling to the left tier with different shielding ideas.

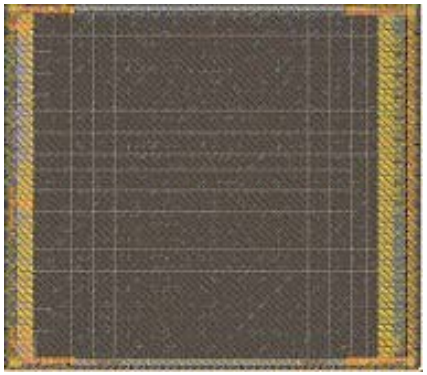
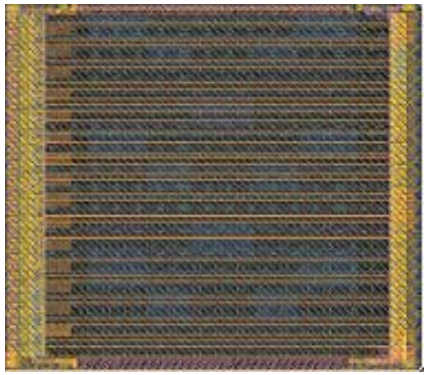


- **Subreticule H** – FNAL/CPPM/LBNL – 3D chip (VICTR) used as a demonstrator for implementation of PT cut algorithm for tracker trigger in SCMS
  - Processes signals from 2 closely spaced parallel silicon strip sensor planes (phi and Z planes).
  - Top tier looks for hits from long phi strips and bottom tier looks for coincidence between phi strips and shorter Z strips connected to bottom tier.
  - Designed for 80 micron pitch sensors
  - Serial readout of all top and bottom strips along with coincidence information
  - Downloadable hit patterns
  - Fast OR outputs
  - Circuit to be thinned to 24 microns and connections made to both the top and bottom of the chip.

Subreticules I & J

- **Subreticule I** – FNAL – 3D demonstrator chip (VIP2b) for ILC vertex detector with separate bonded sensor
  - Adapted from earlier MIT LL designs in SOI technology
  - 192 x 192 array of 24 micron pixels
  - 8 bit digital time stamp
  - Data sparsification
  - DCS analog signal information output
  - Separate test input for every pixel cell
  - Serial output bus

- **Subreticule J** – FNAL/AGH-UST/BNL – 3D demonstrator chip (VIPIC) for X-ray Photon Correlation Spectroscopy to be bonded to a separate sensor.

Fermilab, USA

Grzegorz Deptuch, Marcel Trimpl, Raymond Yarema

BNL, USA
Peter Siddons, Gabriela Carini

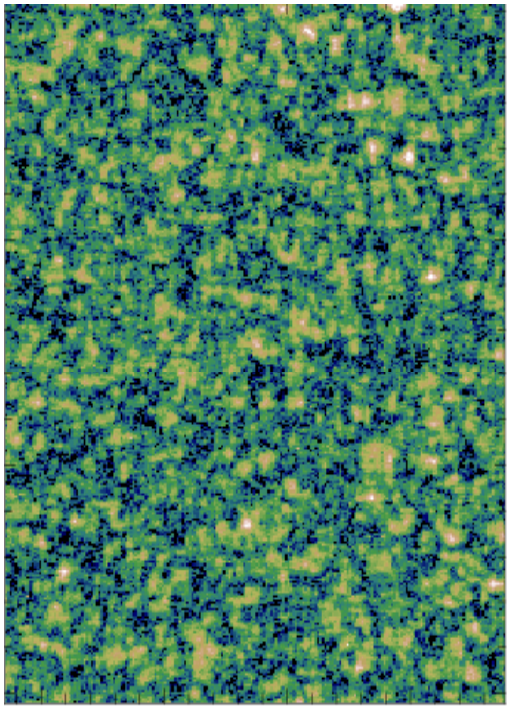
AGH UST, POLAND

Pawel Grybos, Robert Szczygiel,
PhD students: Maciej Kachel, Piotr Kmon

Choice of targetted application

Suggestion from Peter Siddons, BNL

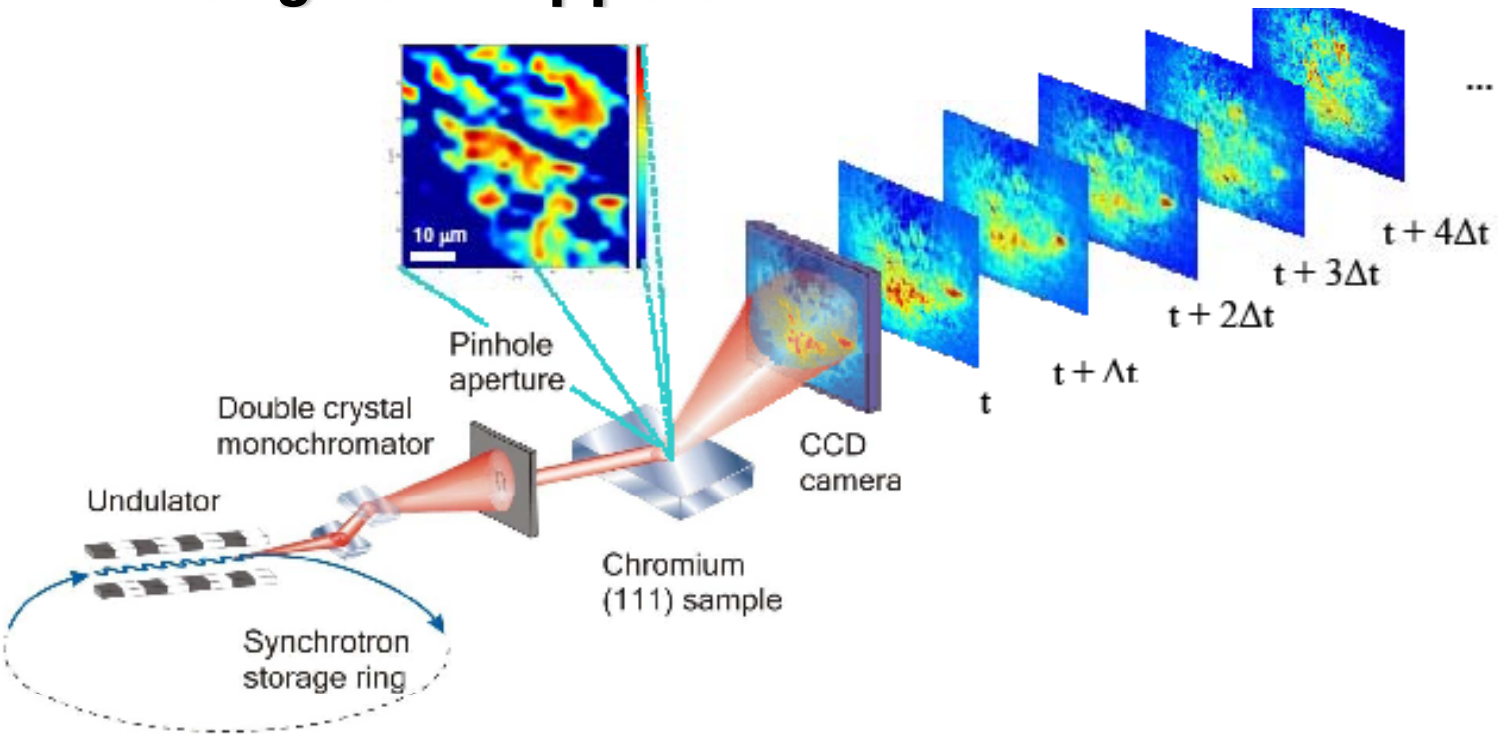
- XPCS is a novel technique that studies the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems (e.g. gels, colloids, liquid crystals, bio-materials, membranes, metals, oxides, magnets, etc.)
- XPCS is based on the generation of a speckle pattern by the scattering of coherent X-rays from a material where spatial nonhomogeneities are present.
- If the state of disorder of the system changes with time, the speckle pattern will change. Thus by studying the time dependence of the scattered intensity, one can study the dynamics of the materials both in or out of thermodynamic equilibrium (e.g. diffusion constants, magnetic domain relaxation times, phase transformations)
- Advantages
  - Observe smaller features sizes
  - Can be used to observe charge, spin, chemical and atomic structure behavior.
  - Works with non-transparent materials

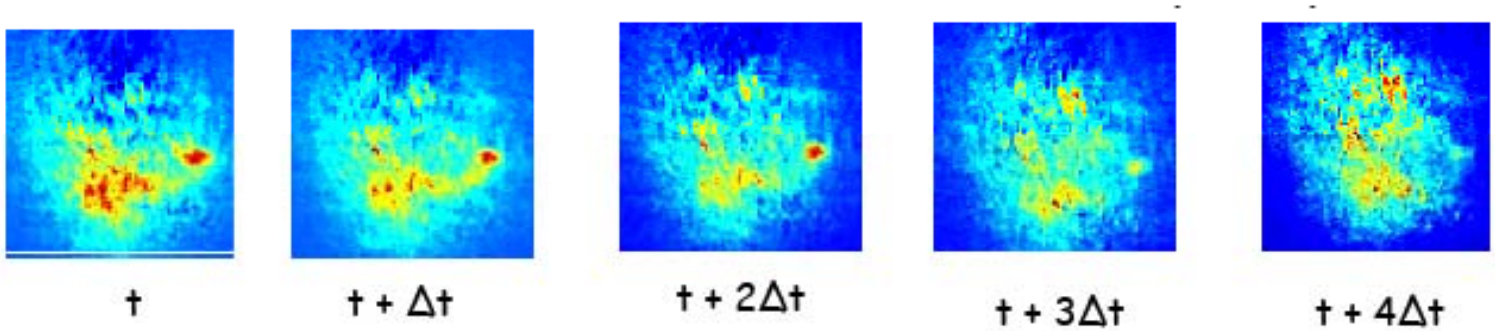


Speckle pattern

XPCS – X-ray Photon Correlation Spectroscopy

Choice of targetted application

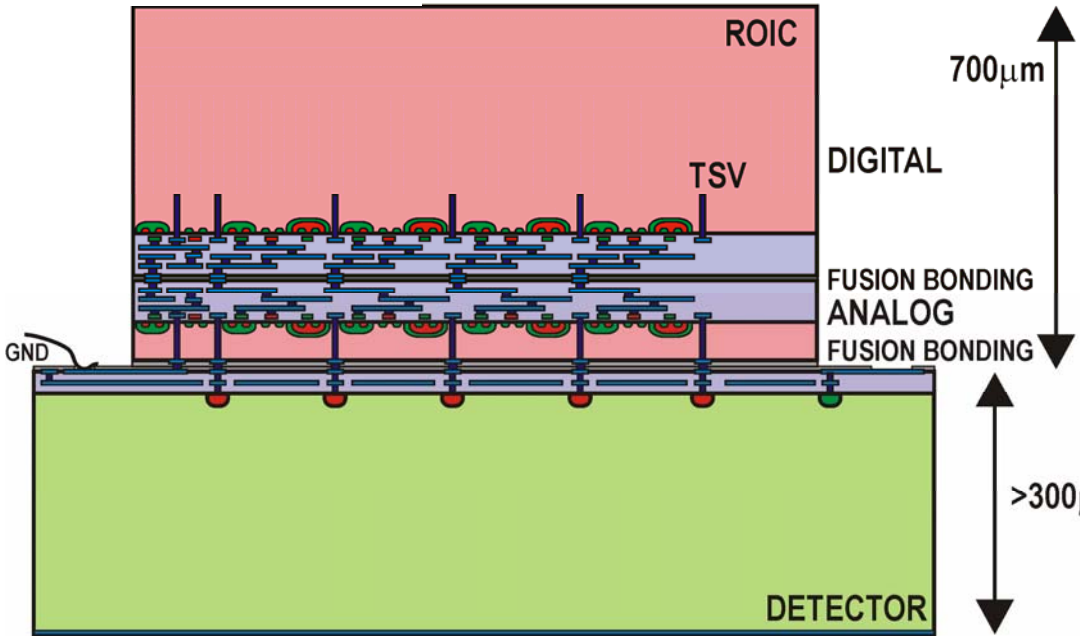




O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

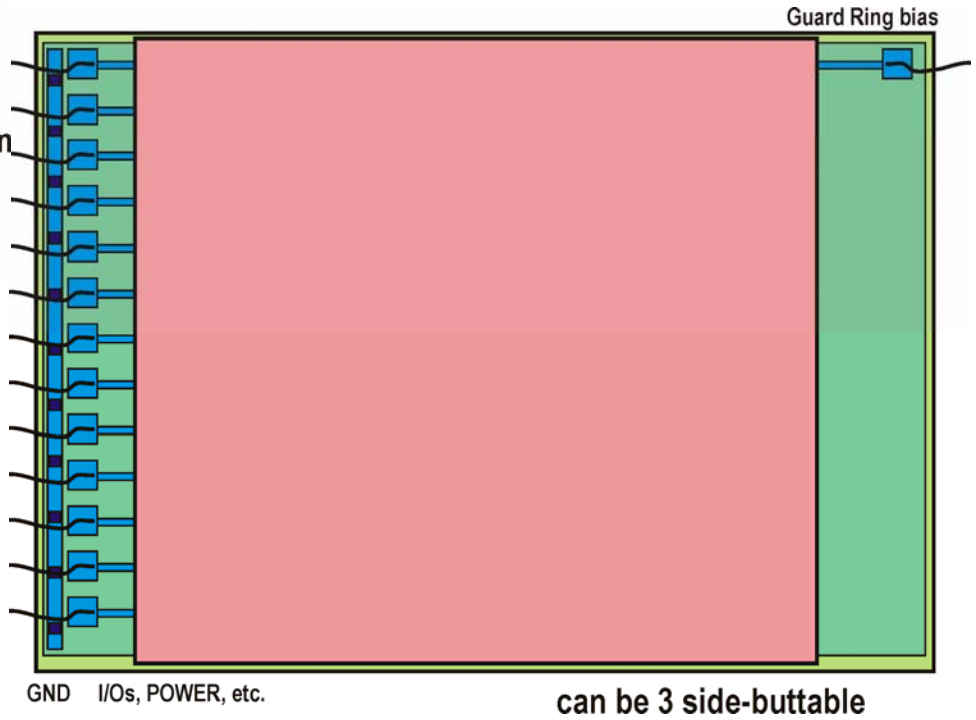
We are less interested by images, to be said, but by mathematical representation of autocorrelation series computed per spatial position

3D-IC and detector technology



- **OPTION 1**

– LESS AGGRESSIVE MOUNTING



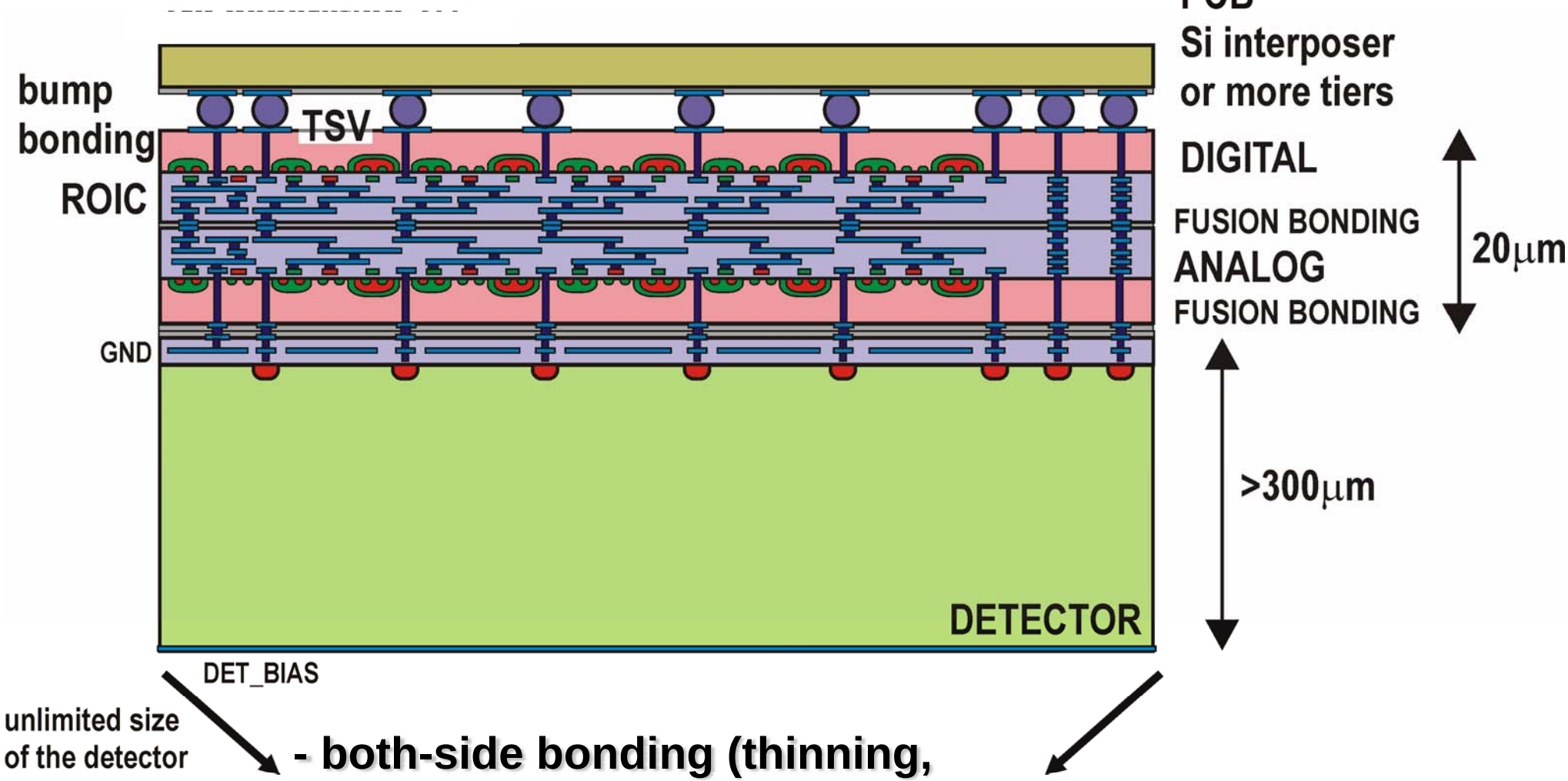
- **Access to signals, power supplies and biases, etc. :**

- fanout/routing on the detector, pads created on the detector, wire bonding to the pads on the sensor to mount in the system

3D-IC and detector technology

- **OPTION 2**

– MORE AGGRESSIVE MOUNTING for 4-side buttable sensor arrays and improved power distribution



- both-side bonding (thinning, exposing TSV, deposition of bonding pads)

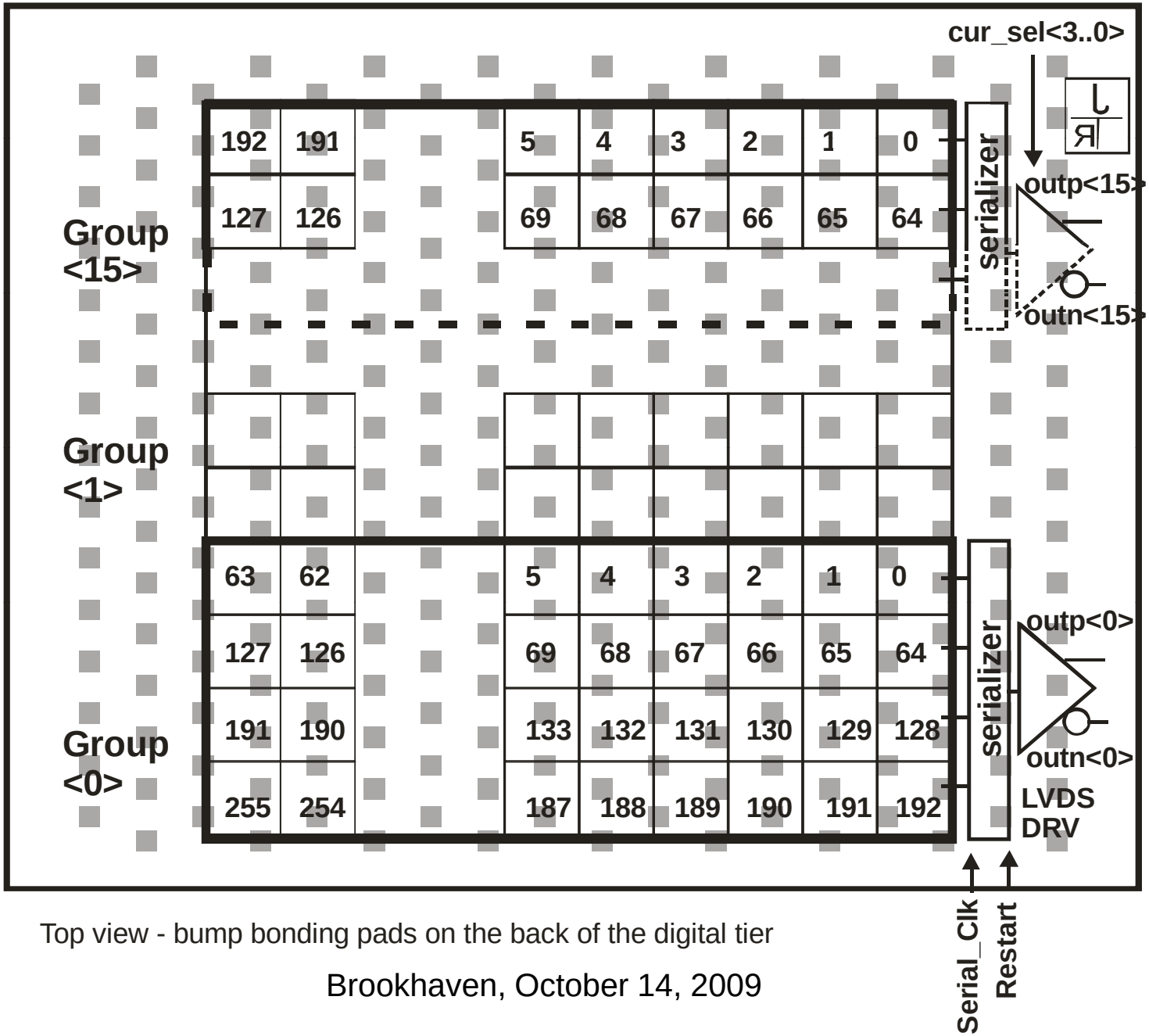
3D-IC and detector technology

- **the following statement can be formulated:**

The significance of the 3D-IC technology for development of new solid state radiation detectors is in implementation of through silicon vias to reach opposite side of the wafer for pad formation and establishing techniques, like: aggressive, high precision thinning and bonding. This leads to 4-side buttable device, while integration of more transistors/μm^2 is of secondary importance.

3D demonstrator chip (VIPIC) for X-ray Photon Correlation Spectroscopy

User-view architecture of VIPIC

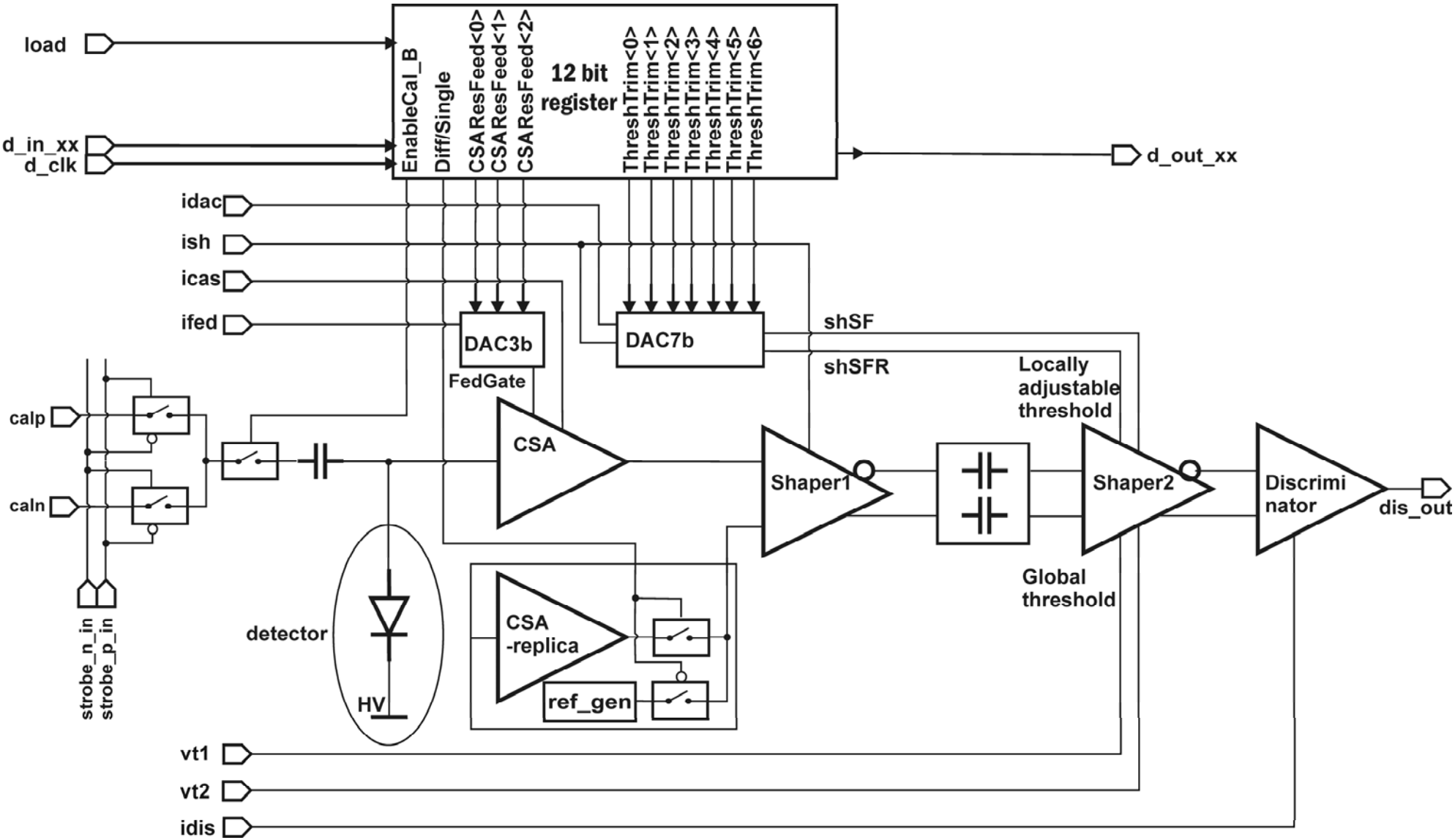


Top view - bump bonding pads on the back of the digital tier

Specification and features of VIPIC

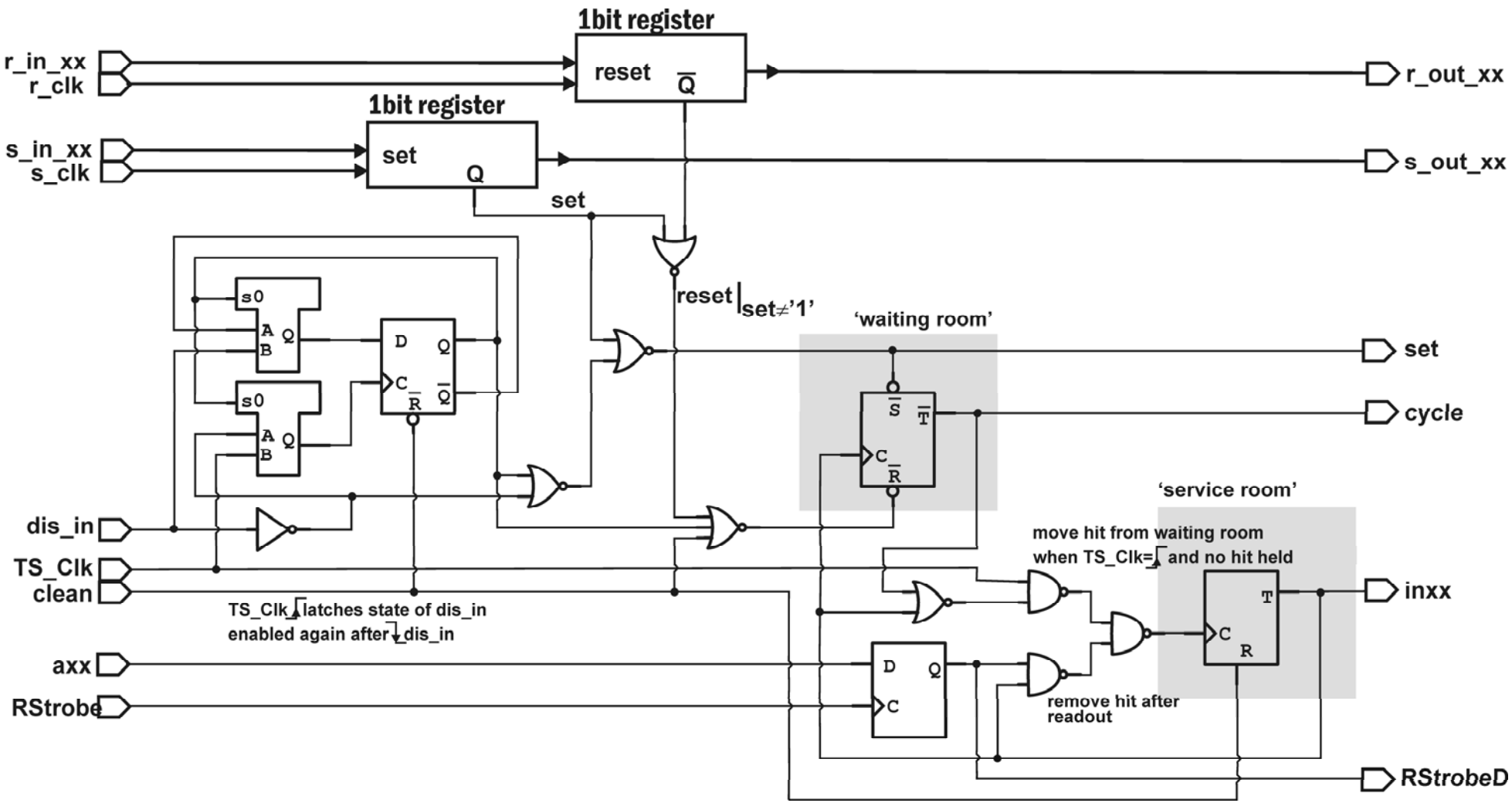
Summary of main features of the VIPIC chip	
feature	**comments**
X-ray detection (8 keV) with Si pixel detector	XCS application
64 × 64 pixels, pixel unit cell (PUC) area: 80 μm × 80 μm	5120 × 5120 mm^2
technology two-tier 3D-IC Chartered 130 nm (6 metal layers)	3D-IC by Tezzaron
separate analog and digital tiers (280 transistors, 1400 transistors/ pixel)	
chip area 6.3 mm × 5.5 mm (6.3 mm × 5.6 mm)	larger dicing for DBI
single threshold for discriminator, trim DAC/pixel for offset corrections	3bits CSA feedback, 7bits discriminator threshold
permanent set and permanent disable bit per pixel	
test charge injection circuitry, single ended or differential configuration of the front-end selection, power consumption 25 μW/analog pixel	Cinj=1.7 fF
noise ENC < 150 e^-	
peaking time < 250 ns	
gain 115 mV / 8 keV	Cfeed=8fF
calibration test block at the CSA input	
Readout modes: - sparsified, binary readout (sparsified time slicing mode), - imaging binary readout mode (5 bit signal depth)	Under control of DAQ system
priority encoder based sparsification circuitry	Automatic hit pixel address generation
dead-time-less and trigger-less operation in both readout modes	
16 parallel serial LVDS output lines (16 groups of 4 × 64 pixels)	
two 5 bit counters per pixel for recording multiple hits per time slice (useable in the imaging mode)	Alternatively used between readout and acquisition phases
high speed frame readout - 160 ns / hit pixel in sparsified time slicing mode (up to 60 hit pixels / 10 μs) - 50 × 10^3 frame/s in imaging mode (5 bit)	

Design of VIPIC



Analog tier (pixel)

Design of VIPIC



Digital tier (pixel)

Design of VIPIC

- **VIPIC readout modes:**

1) Sparsification readout; sparsification engine based on priority encoder

Two options considered: token passing or priority encoder/decoder binary tree (second won: automatic generation of binary addresses, equal response time regardless position in the matrix – but complex readout)

2) Deadtime-less counting

How long should be counters?
- the maximum rate of events that be counted is less than 1 MHz due to 1 μs long pulse duration related to the 250 ns long shaping time,
- assuming 100 MHz serial clock 8 bits (3 bits of starting sign overhead) × 10 ns (serial clock) × 256 (pixels in the group) = 20.4 μs
- assuming deadtime-less operation with two counters/pixel (one counting while second being read out) one readout allows not more than 20 counts

Thus, 5 bit counters are enough allowing counting and outputing data at the maximum speed that is dictaed by the front-end circuitry!!!

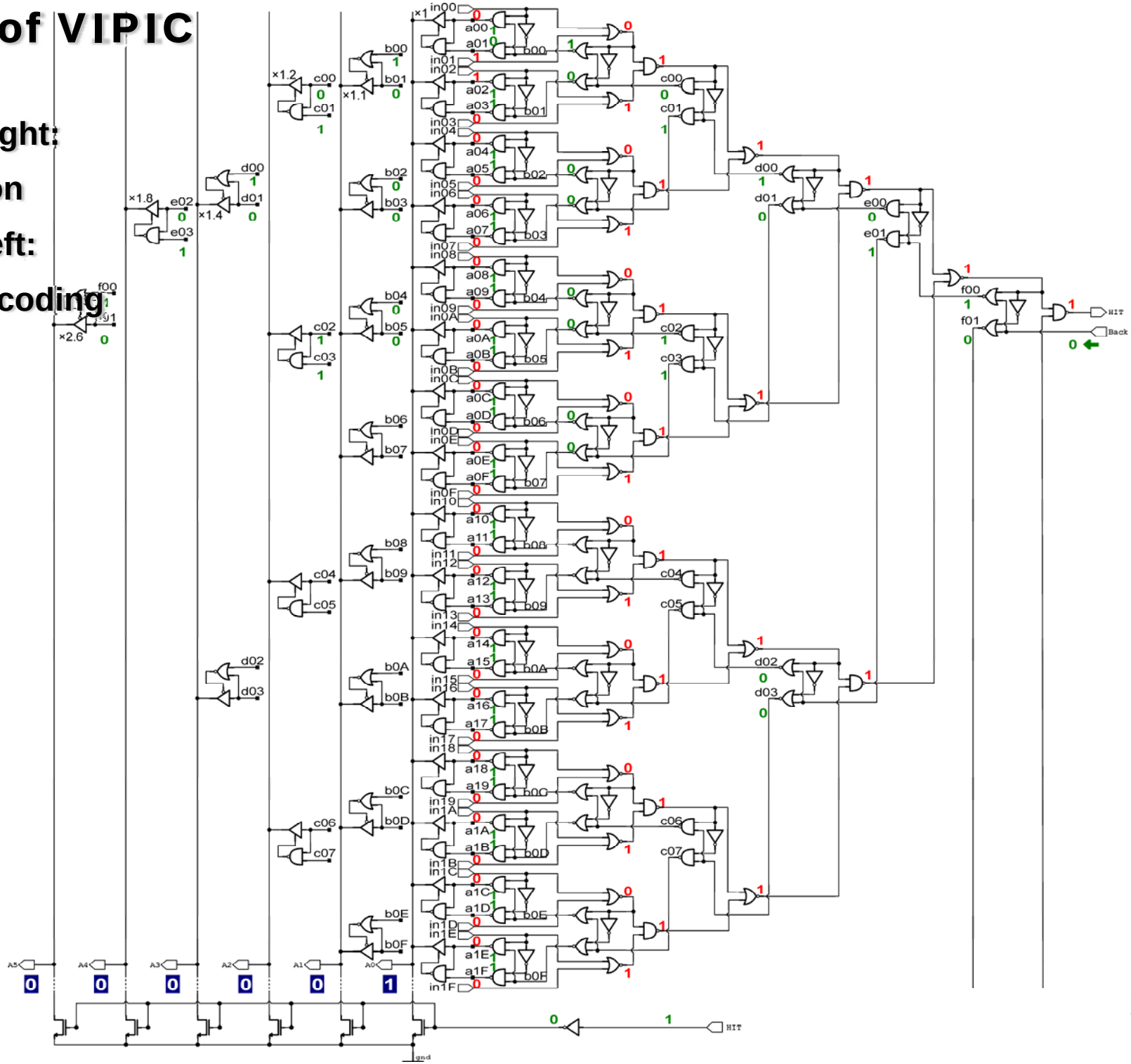
Design of VIPIC

- to the right:

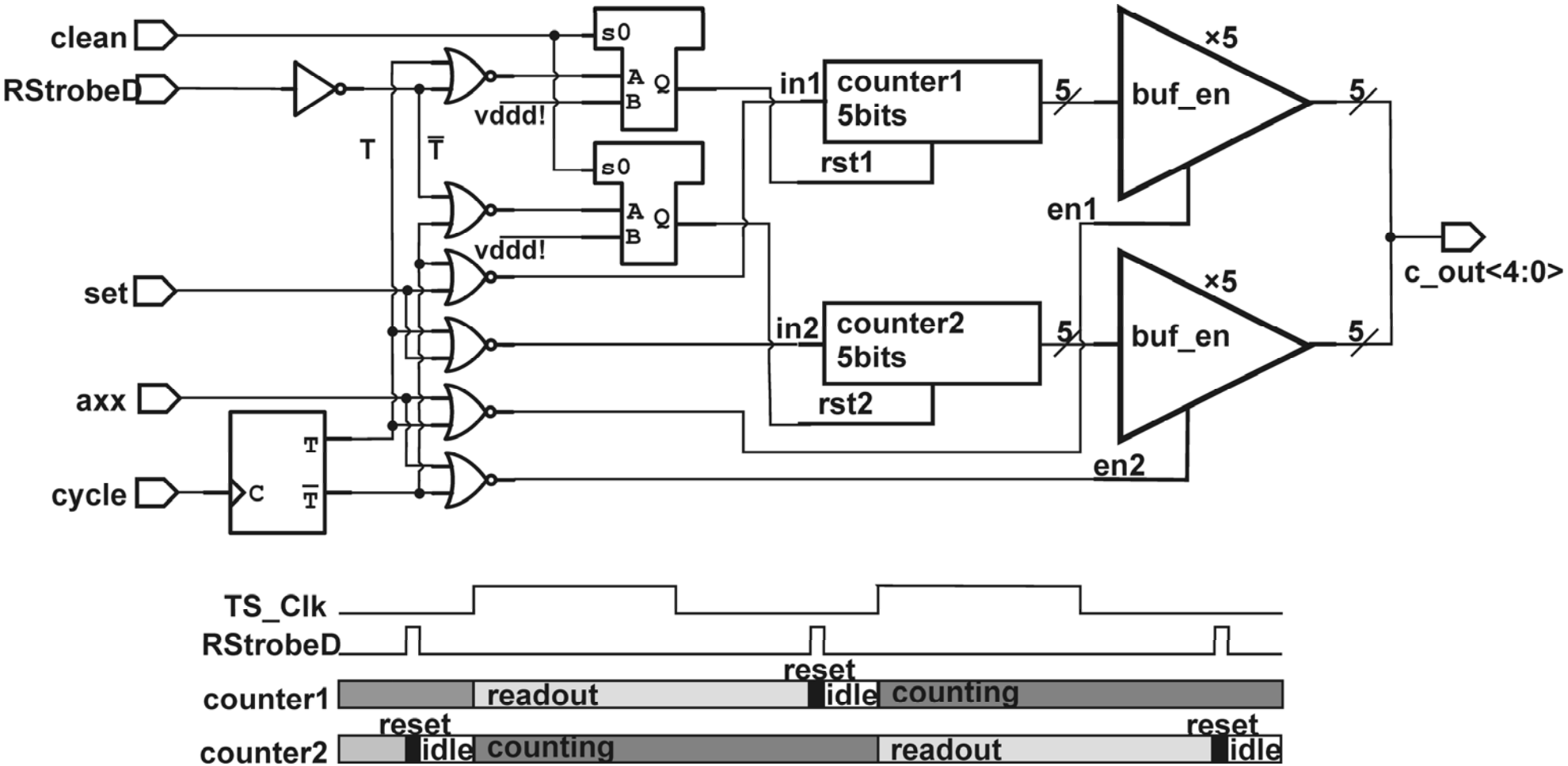
OR function

- to the left:

priority encoding



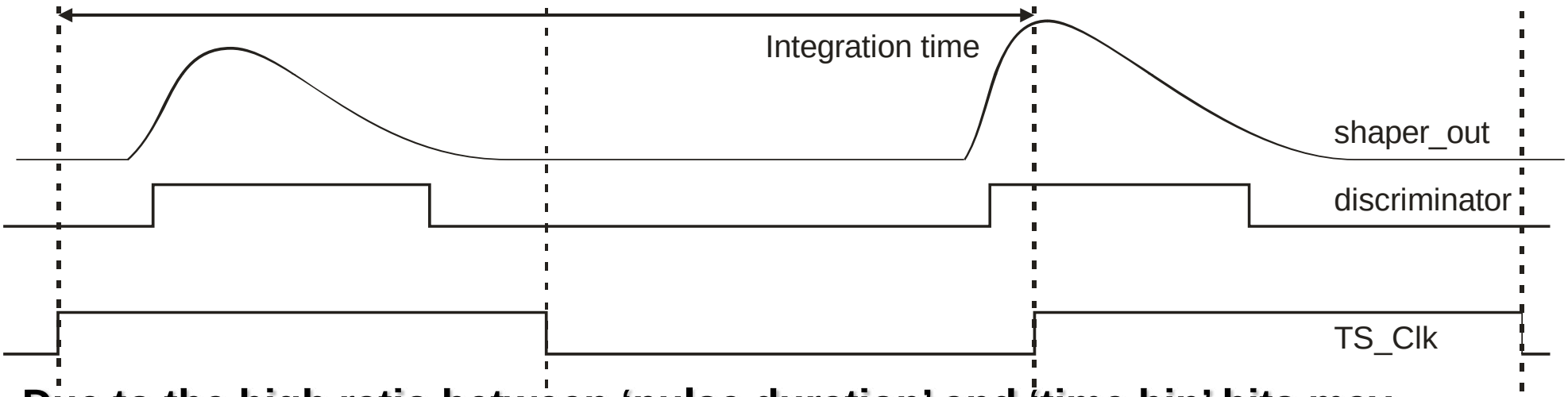
Design of VIPIC



- imaging mode – not primary mode of operation, counters have no overflow protection

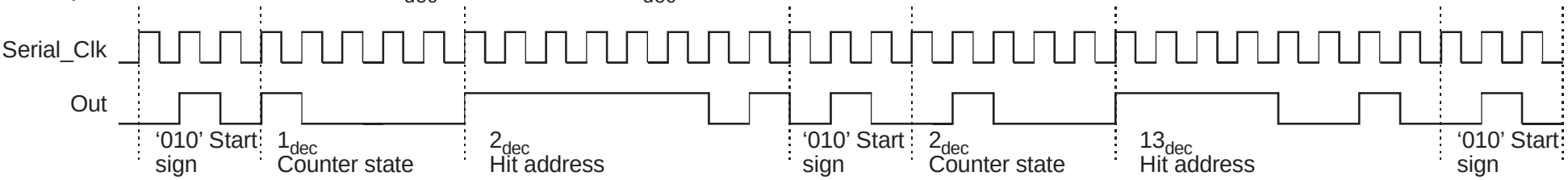
Design of VIPIC

Demonstration of hit spilling between adjacent time slots



Due to the high ratio between 'pulse duration' and 'time bin' hits may overflow, mechanism allowing not allowing double counting of hits occuring at time slots boundaries is implemented

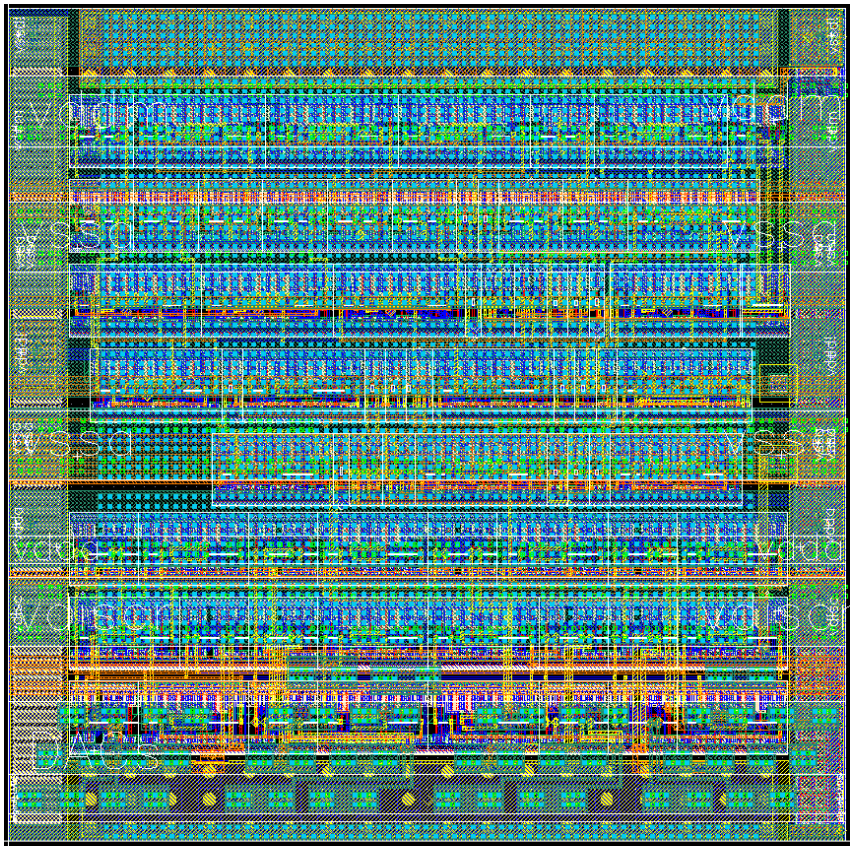
Example of readout: 1 hit @ address 2_{dec}, 2 hit @ address 13_{dec}



Example of readout from 1 out of 16 channels

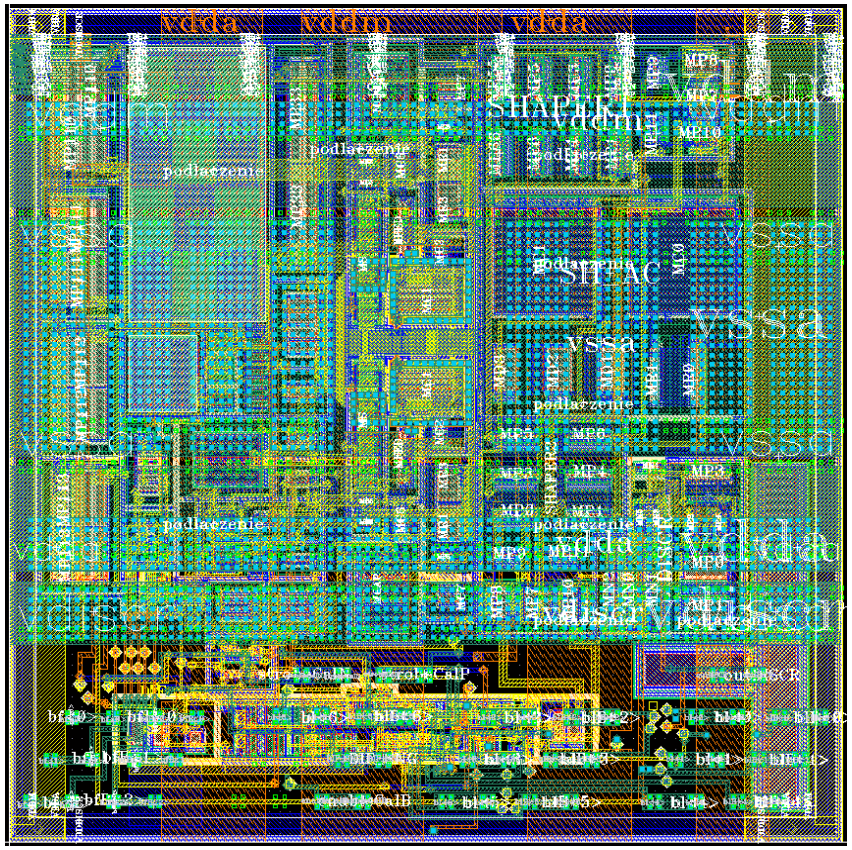
Design of VIPIC

1400 transistors / pixel



Digital part of pixel

280 transistors / pixel

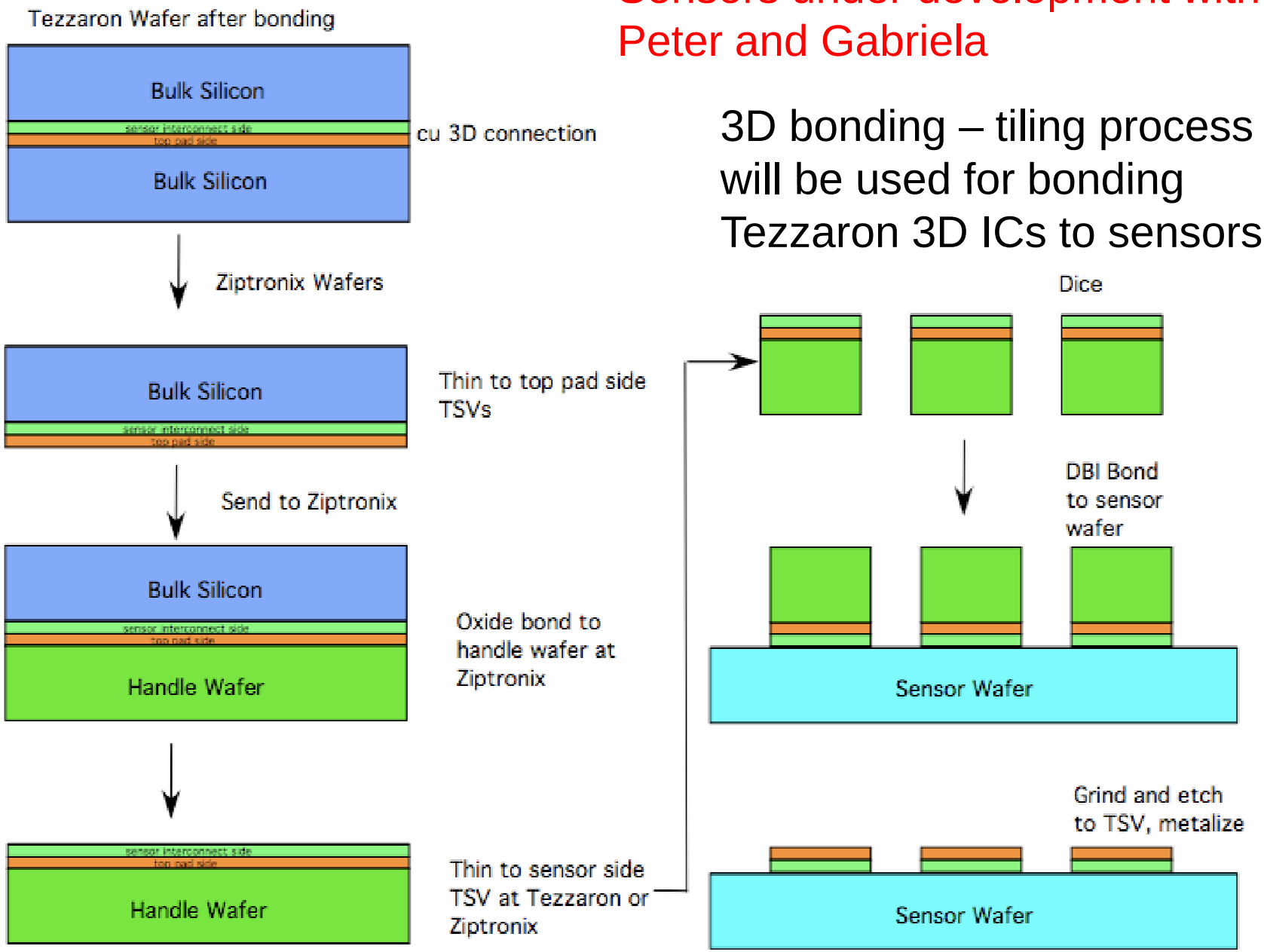


Analog part of pixel

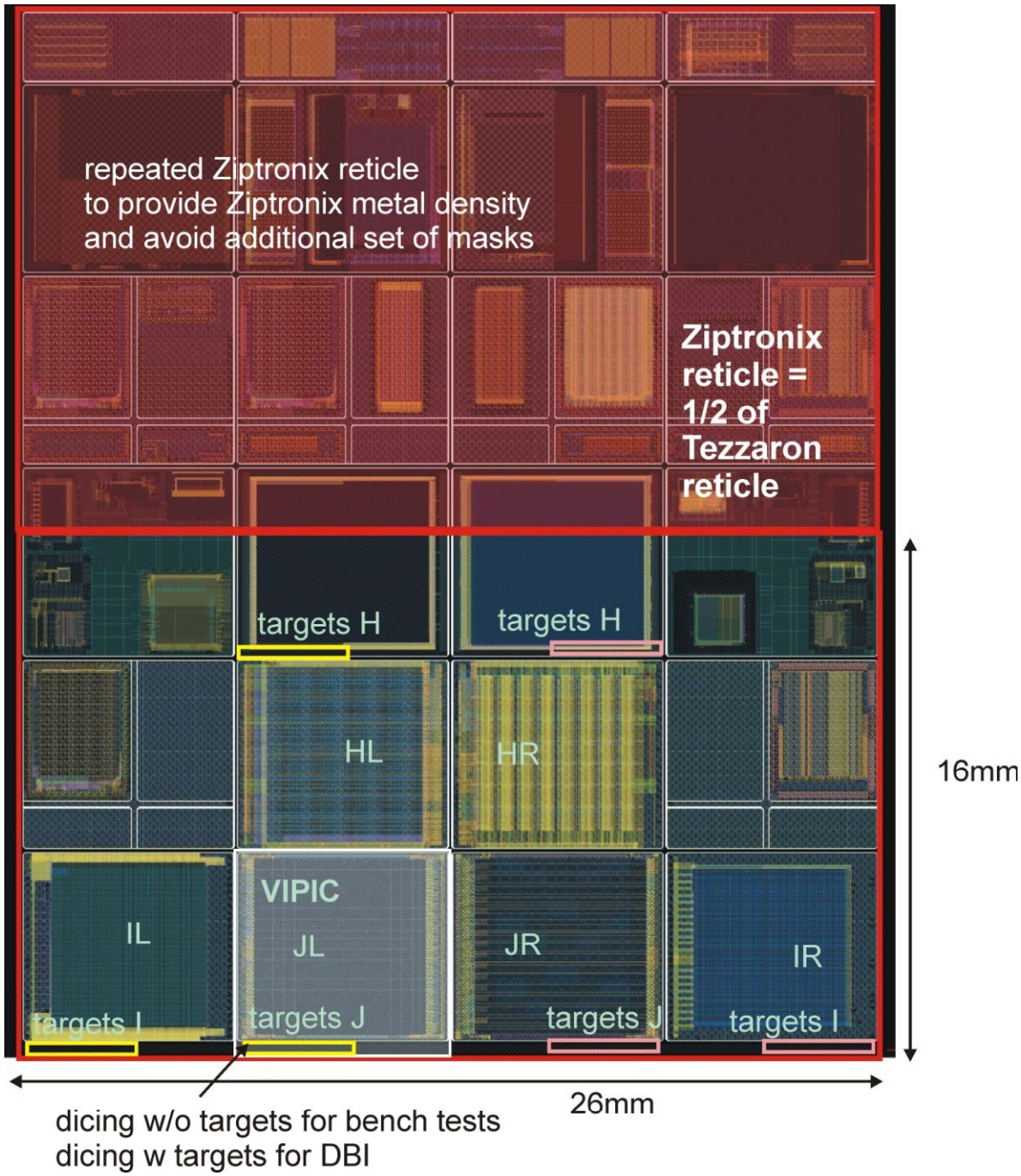
VIPIC and its sensor

Sensors under development with BNL
Peter and Gabriela

3D bonding – tiling process will be used for bonding Tezzaron 3D ICs to sensors

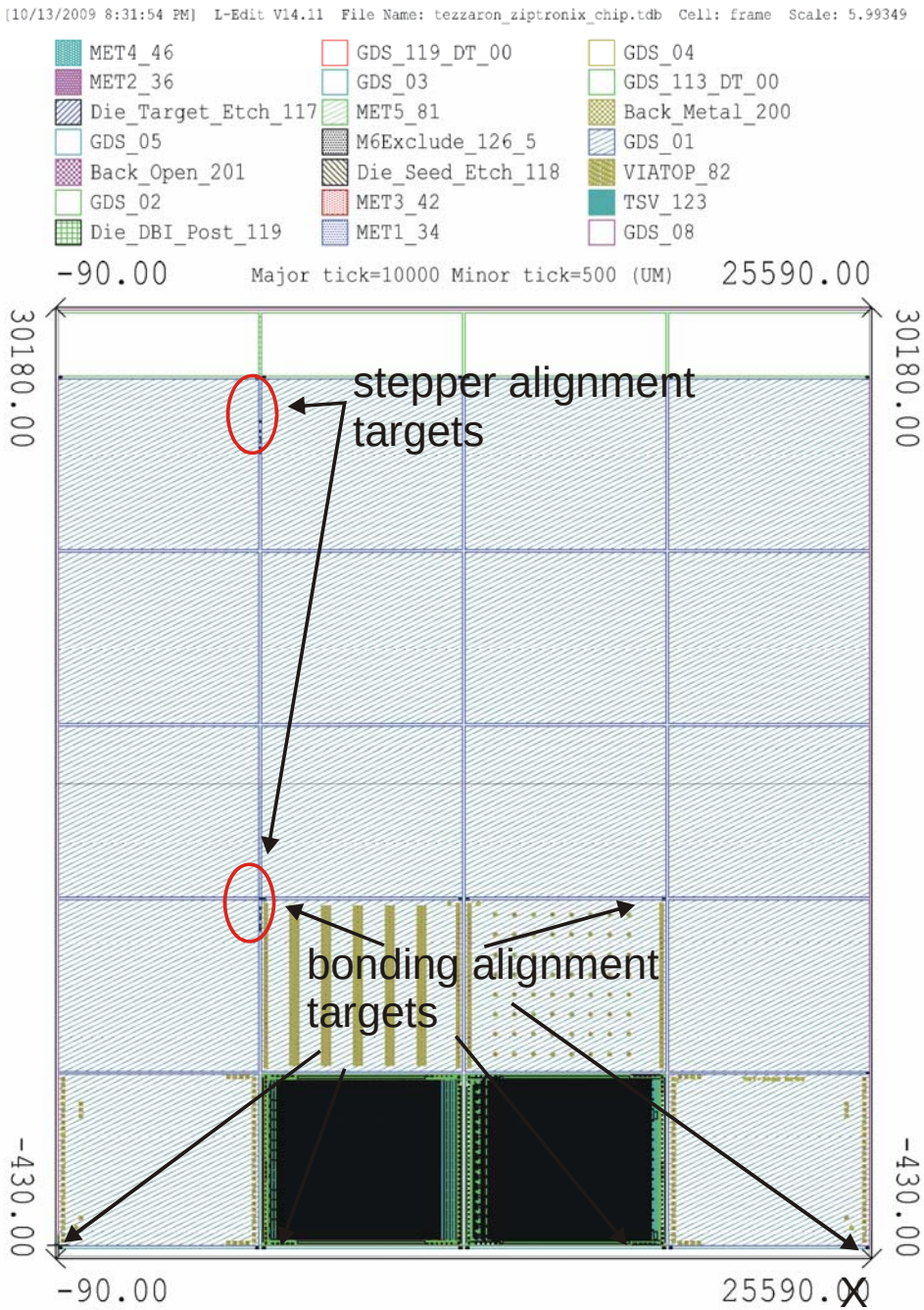


VIPIC and its sensor



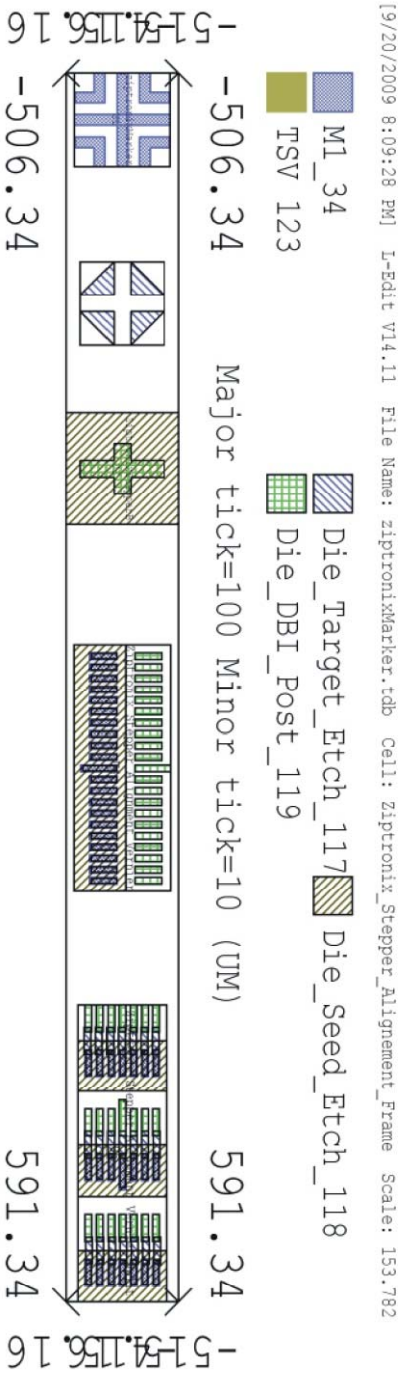
- **Readiness for DBI bonding**
- DBI bonding will be done at Ziptronix
- Chips: H (VIP), I (VICTR) , J (VIPIC) designed for DBI bonding
- Alignment targets required for aligning:
  a) deposition of seed and DBI post metal requires stepper alignment targets
  b) DBI bonding requires bond alignment targets
- Targets placed in two locations:
  a) stepper alignment targets in the first vertical internal dicing street
  b) DBI bonding targets in the dicing streets above the chip H and below chips I and J
- Stepper alignement targets include use of M1 on the frame
- Bonding alignment targets require UR transparency on the frame
- Targets use Ziptronix layers to be deposited on the frame and sensors
- **Singulation of chips**
- Fermilab will dice one 3D wafer for to provide chips for bench testing (no detectors) size 5.5×6.3 mm^2
- Fermilab will deliver 5 wafers for singulation and DBI bonding to the BNL sensors (5.6×6.3 mm^2)

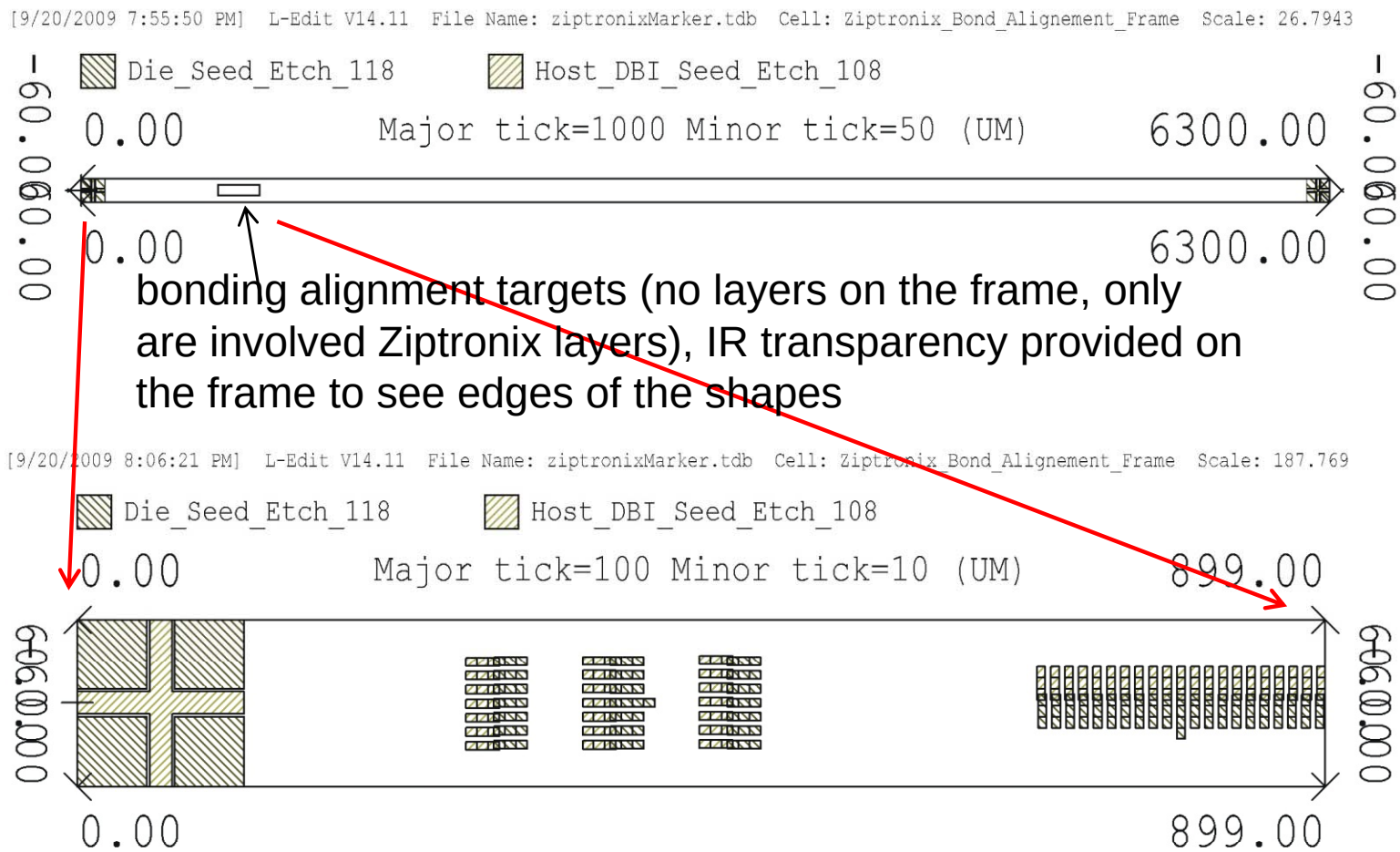
VIPIC and its sensor



- Placing of bonding targets have no influence on the operation of chips (different dicing is however required for chips used in initial bench testing and characterization and DBI bonding)
- Planarity of bonding surfaces is of extreme importance. Surface topograhpy should not exceed 500 nm.
- Sensors are p-on-n, developed for 3 chips at the same time: ILC, CMS upgrade, Light
- Sensor design includes 1 metal layer (used to implement shielding by filling empty spaces between diodes in one option)
- Fanout routing to the extrernal pads realized on Ziptronix
- Stepper aligned to patterns made out of TSVs on ROIC and detector metal on the sensor
- Alignment of chip on the sensor achieved with bonding aligment markers including Vernier lines

VIPIC and its sensor

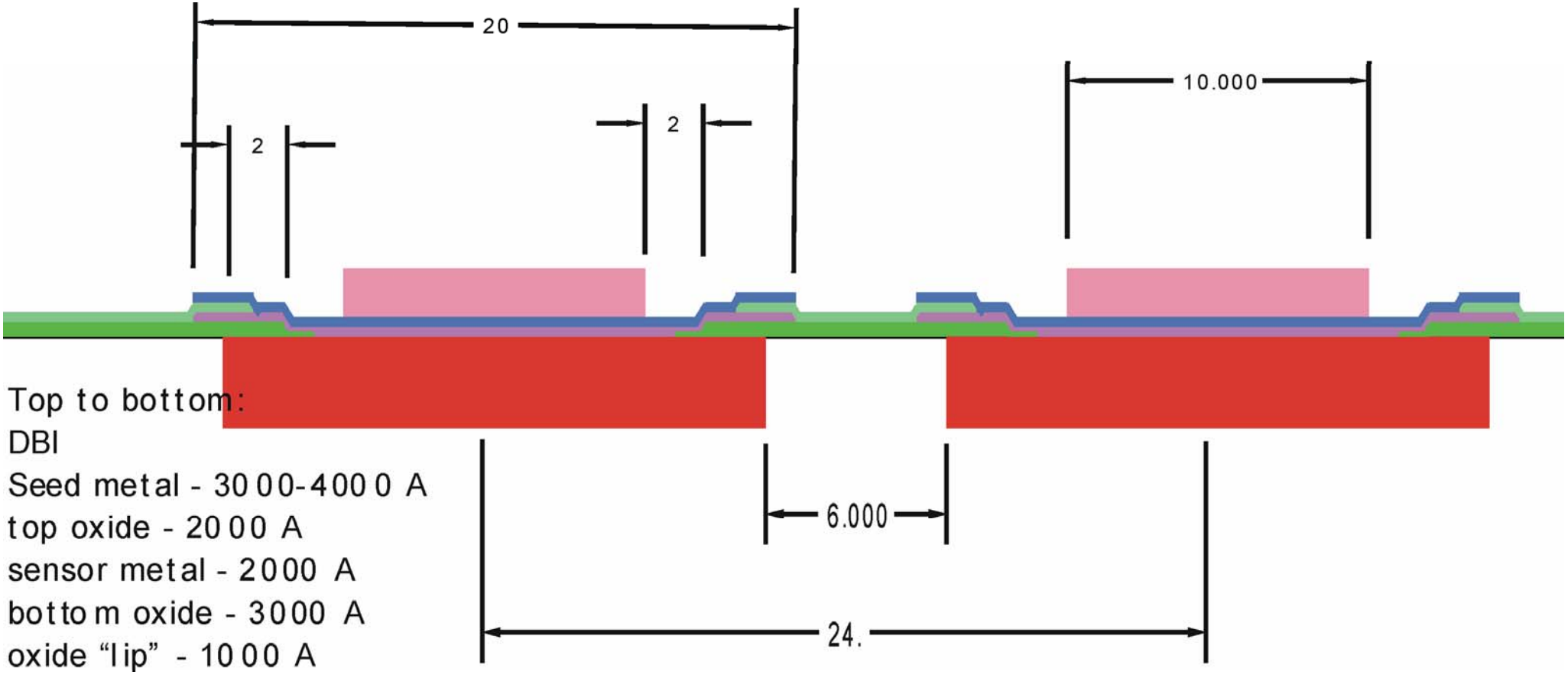


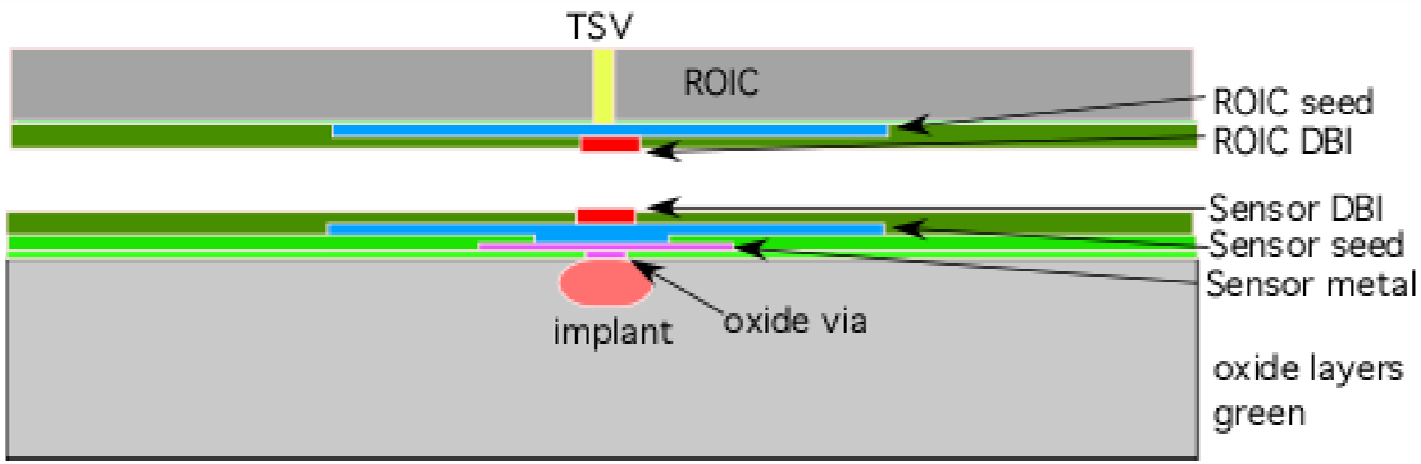


bonding alignment targets (no layers on the frame, only are involved Ziptronix layers), IR transparency provided on the frame to see edges of the shapes

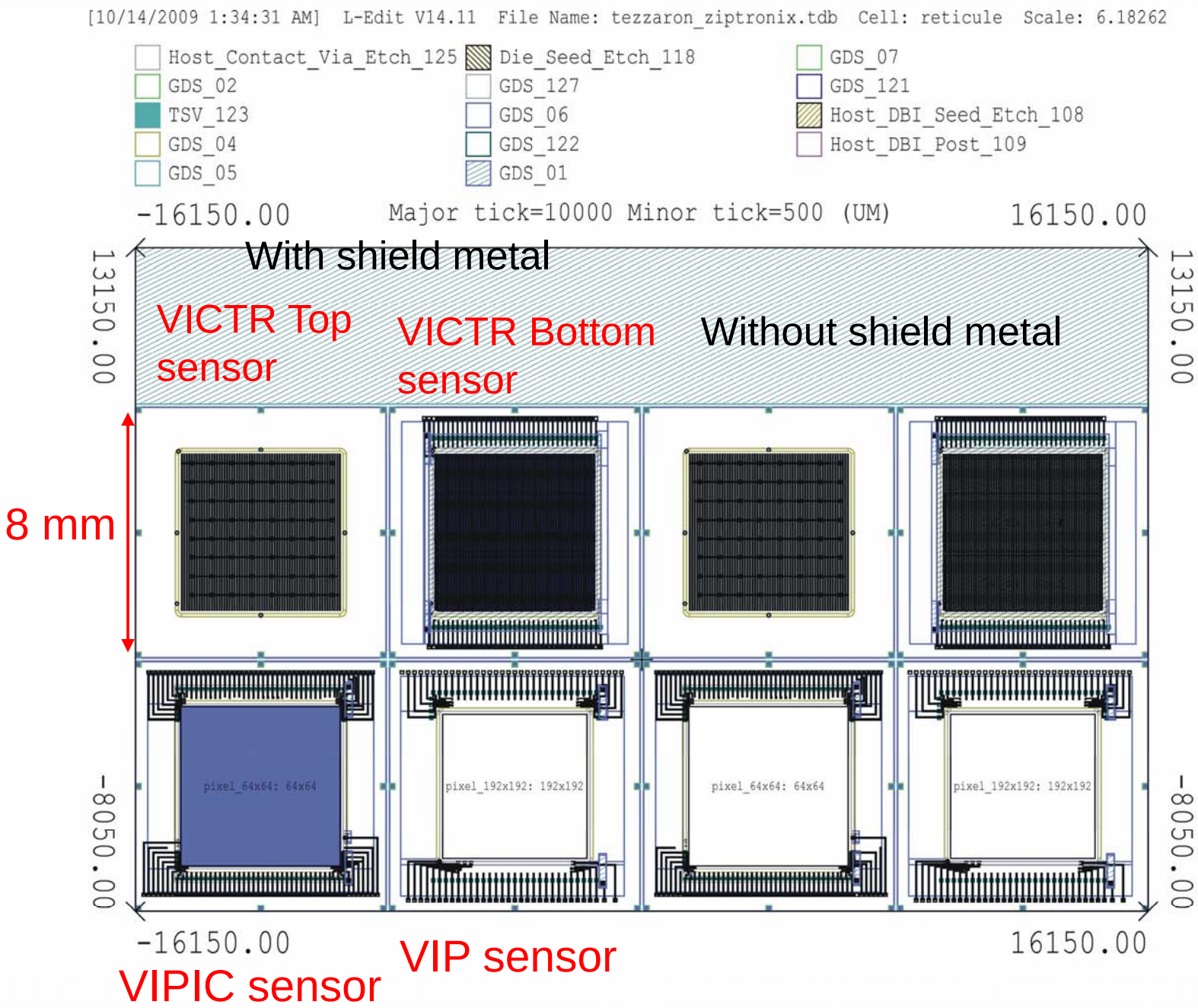
Stepper alignemnt targets (M1 and TSV included on the frame, all other layers are Ziptronix layers)

Surface topography of the sensor





VIPIC and its sensor



Timeline

- First Designers meeting held Dec 11, 2008
- Subsequent meeting in February, March, and May 2009
- All designs initially submitted by mid May
  - Continuous checking of designs by Tezzaron and Fermilab identified numerous problems
    - Inconsistent layer map tables between designs
    - Different DRC violations found with Assura, Calibre, and Magma
    - Non uniform bond interface across all subreticules
    - Via size confusion related to 2 top metals
    - Non mirroring of design in frame
    - Adding of high resistance poly option
    - Computer system crashes at Tezzaron
    - Problems with MicroMagic and Magma
    - Others
  - Items changed during review process
    - Dummy fill program
    - Via density rule
    - Newer DRC versions uploaded.
- Masks started for 31 wafers
- 8 weeks for wafer fabrication.
- 4 weeks for 3D assembly

The Future

- In some sense this HEP MPW run was a learning experience for both the HEP community and Tezzaron.
- Tezzaron is currently planning for a DARPA run due to close December 15
  - 5 tiers, 2-3 tiers of memory (1Gb/tier + 2 tiers of digital)
  - ~25 customers
  - Oversold by 400 %
- New institutions have expressed an interest in joining the 3DIC consortium.
- In part due to our HEP run, both CMP and MOSIS have expressed interest in providing some sort of 3D IC services.
- Consortia hopes to have 1-2 runs in 2010.

Summary

- A group of 17 institutions has come together to participate in the first HEP multi-project run for 3D circuits.
- The designs have been submitted and fabrication is underway at Chartered Semiconductor.
- This run should allow for evaluation of many factors
  - 3D processing
    - Affect of thinning and bonding on device performance
    - Yield of bond connections between tiers
    - Geometry of bond pads between tiers
    - Effect of vias near transistors
    - TSV capacitance and yield
    - Effect of bond pads over circuits
    - Digital coupling from one tier to another tier
    - Comparison of identical 2D and 3D designs in the same technology
  - Chartered process
    - Suitability of process for MAPS
    - Radiation tolerance and noise performance
    - Cryogenic performance/reliability
    - Performance of a large number of different circuits exploring many different operating conditions.
- Tezzaron expected to deliver 2D and 3D wafers later this year.
- Test results to be presented at future HEP meetings