Ideas for a silicon pixel tracker for the International Linear Collider

Chris Damerell (RAL)

The SPT concept was first presented by Konstantin Stefanov at the International Linear Collider Workshop in Sendai, Japan, in March 2008. Shortly afterwards, the UK 'ceased investment' in ILC, but international interest in the SPT has grown, not only for the linear collider.

CONTENTS

- **Design concept**
- **Mechanical simulations**
- **Feasibility – new results with advanced CMOS pixels from:**
  - **Jim Janesick (California) working with Jazz Semiconductors and**
  - **Dave Burt et al (e2V and Open U) working with Tower Semiconductors**

  } *foundries now linked*
- **Next steps**
- **Practical realization for LC and other applications (possibly including GPDs for HL-LHC)**

Design Concept – Linear Collider as an example

- **Goal is to devise a tracker design which significantly reduces the material budget wrt the currently projected leader, the SiD silicon microstrip tracker, which uses the same technology as the LHC GPD trackers**

- **Why push to minimise material in tracker?**

- **In general, we would like:**
  - **photons to convert in the ECAL not in the tracking system**
  - **minimal bremmstrahlung of electrons**
  - **minimal secondary interactions of hadrons**

- **Looking at previous tracking systems, they have all 'gone to hell in the forward region'**

- **This has diminished the physics output in the past, and the penalty will increase with collision energy (LHC at 13 TeV, ILC at 0.5-1 TeV), as the event complexity increases.**

- **The largest pixel tracking system in HEP was till recently the SLD vertex detector with 307 Mpixels (CCDs), now overtaken by the STAR vertex detector with 356 Mpixels (CMOS active pixels).** ***Warmest congratulations!!***

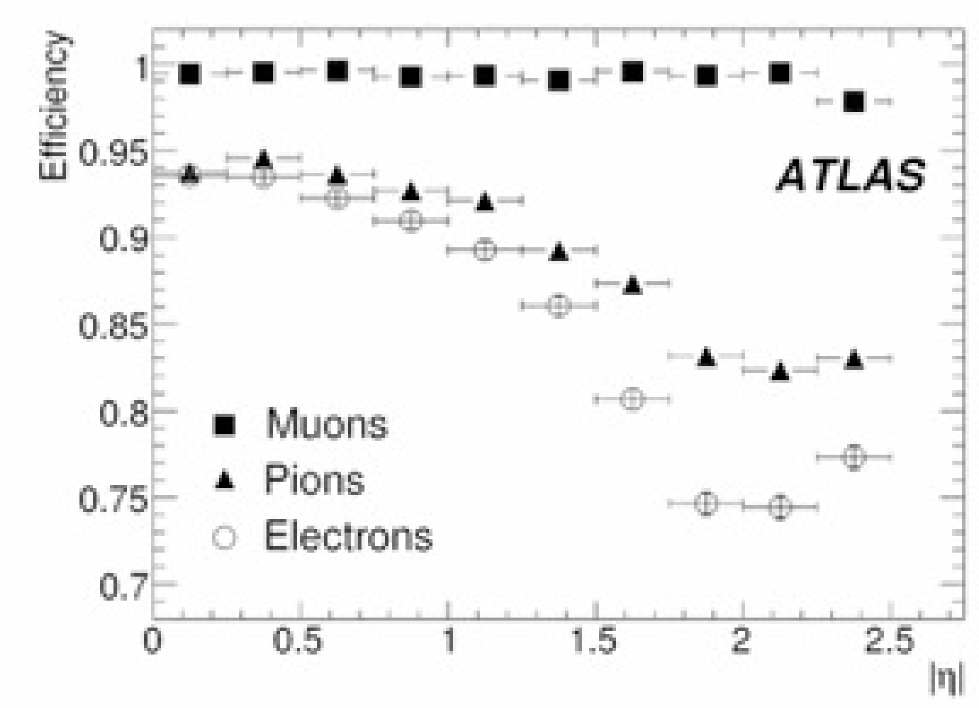
- **Basic SPT concept is a 'separated function' design – precision timing on every track *but not on every point on the track.* So we suggest an optimised mix of tracking layers and timing layers, the latter with single-bunch timing precision**

- **Other key features are binary readout and on-sensor data sparsification, to minimise data flow off the detector**

- **Thin monolithic *charge-coupled CMOS pixels* offer a different 'separated function' feature – evading the link between charge collection and charge sensing given by the *capacitance matching theorem,* with major advantages in terms of power dissipation and noise performance. This 'evasion' is widely exploited in imaging pixel detectors**

- **By working with a *monolithic planar architecture* (CMOS technology) we are confident that systems will be scalable by 2025 (time-early for ILC) to the level of ~40 Gpixels. For large systems, a lot will be gained by avoiding the complexity of hybrid systems, 3-D systems, and other specialised technologies**

Tracking systems at colliders
What's the problem?



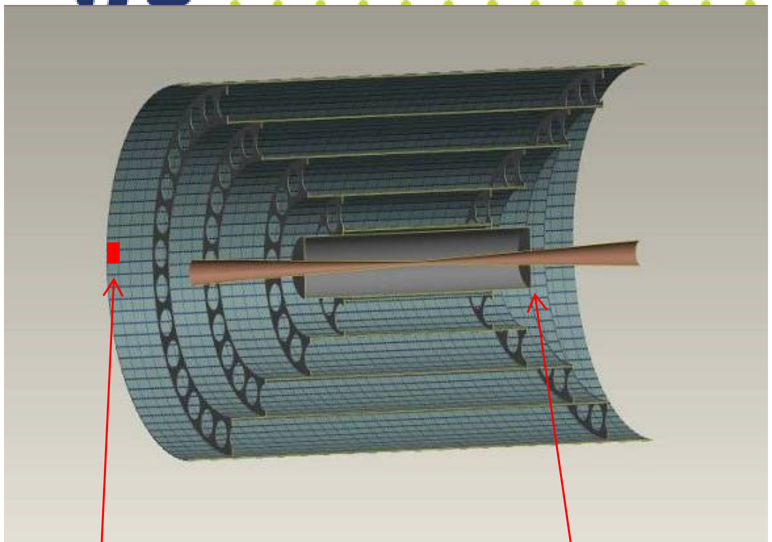
Plot shown by Markus Elsing at Vertex 2011 workshop - *has this changed?*

Pions have almost as much trouble ploughing through the material in the forward region as do electrons

Situation will degrade further if , as is likely, HL-LHC necessitates even more material

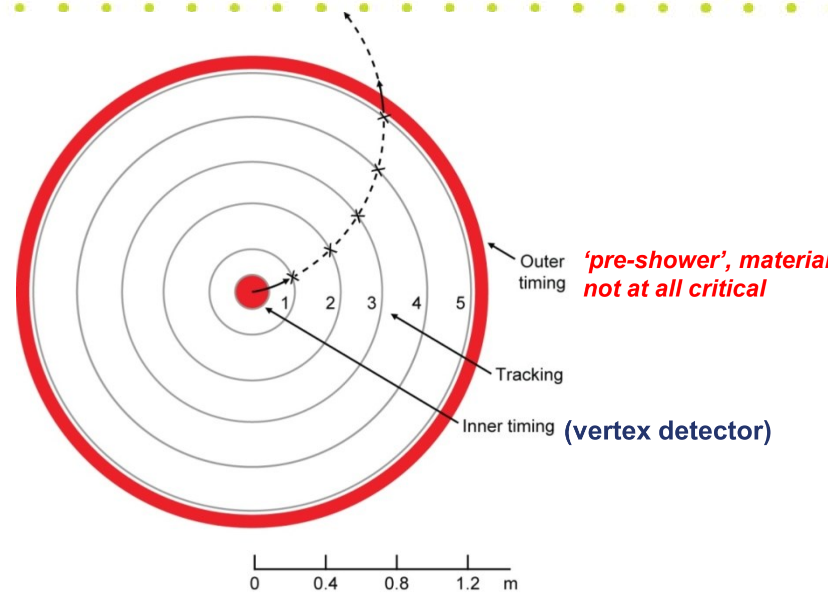
Forward tracking is in particular need of help

Possible layout for the linear collider



Tracking sensor, one of 12,000, 8x8 cm^2, 2.56 Mpixels each

Matching endcaps (only one layer shown)

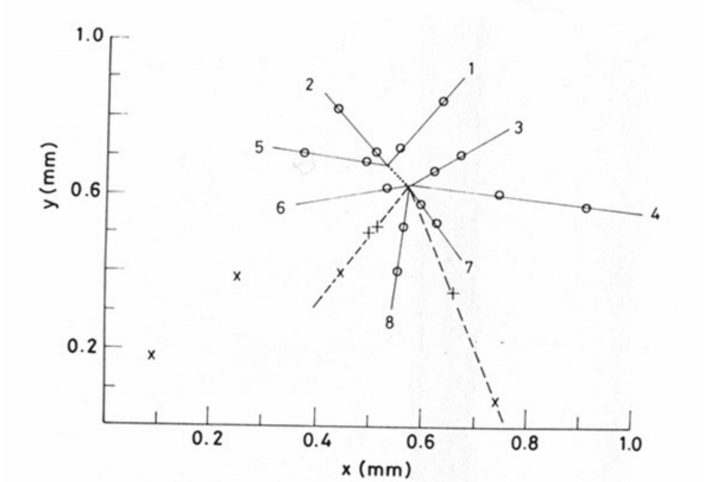


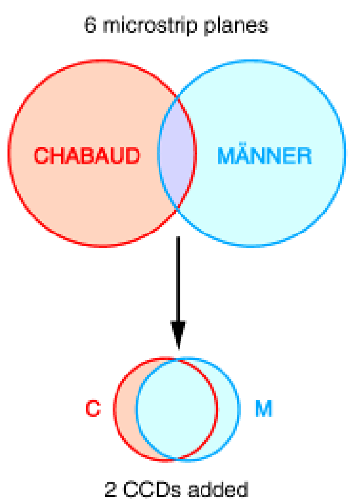
- **Barrels:** SiC foam ladders
  - **Tracking layers:** 5 cylinders, ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range ~50 μm diameter pixels (probably hexagonal)
  - **Outer timing layers:** ~3 cylinders *(also monolithic)* as an envelope, ~2% X_0 per layer if evaporative CO_2 cooling ~150 μm diameter pixels
- **Endcaps:** matching system; 5 tracking and ~3 timing layers, closing off the barrels
- Tracking layers are read out between bunch trains (5 Hz for ILC)

Track reconstruction

- Start with mini-vectors from on-time tracks found in the triplet of outer timing layers, together with an approximate IP constraint. 3 timing layers provide sufficient redundancy
- Work inwards through each successive tracking layer, refining the track parameters as points are added
- Background levels (~7000 out-of-time tracks at CLIC at 3 TeV) appear daunting at first sight, but pixel systems can absorb a very high density of background without loss of performance
- General principle, established in vertex detectors in ACCMOR (1980s) and SLD (1990s): fine granularity can to a great extent compensate for coarse timing. Precision time stamping costs power, hence layer thickness, whereas fine granularity need not
- Back-of-envelope calculations look promising (LCWS Warsaw 2008). Serious simulations may be about to begin (Jan Strube, Tohoku U)
- 'Special methods' are envisaged for low momentum tracks, K-shorts, lambdas and photon conversions
- Track refinement, recovery of tiny inefficiencies, can if necessary be achieved by correlation with tracks found in inner timing layers (vertex detector). Prefer to use tracking layer technology here too, if shown to be possible

Pixel detectors – advantages for track reconstruction





ACCMOR 1984
Fred Wickens

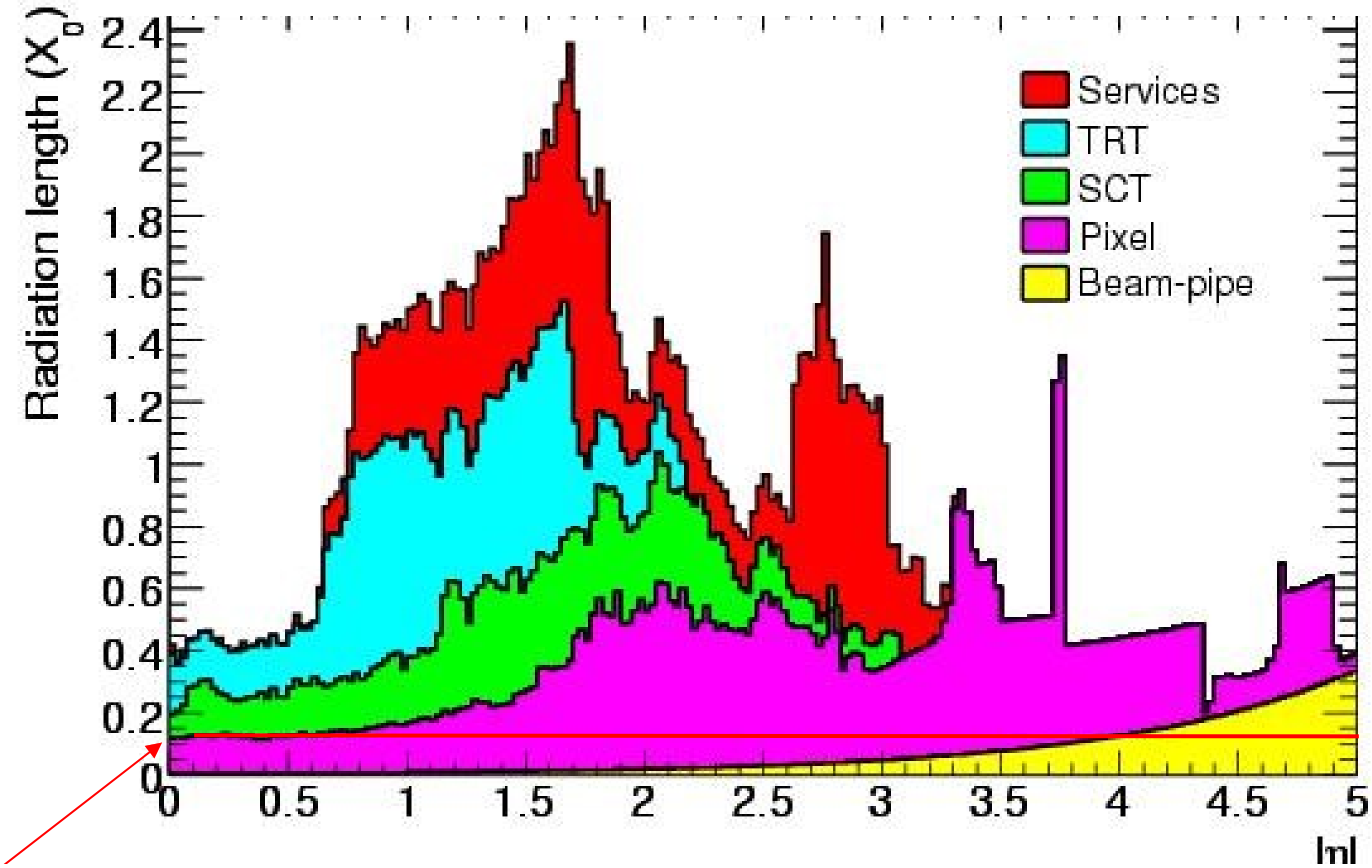
A life-changing experience …

Main challenges

- **Mechanical design – can such large and lightweight structures be made sufficiently stable?**
- **Overall scale - 33 Gpixels for tracking layers, 5 Gpixels for timing layers**
- **Need excellent and prompt charge collection efficiency, non-trivial for these relatively large pixels, which should be fully depleted throughout the epi layer**
- **Need excellent noise performance, to cope with small signals from thin layers. Achievable with extremely low power, due to advances in charge-coupled CMOS pixels – a fast-moving technology**

- **Let's consider these issues in turn …**

Material budget - a major challenge



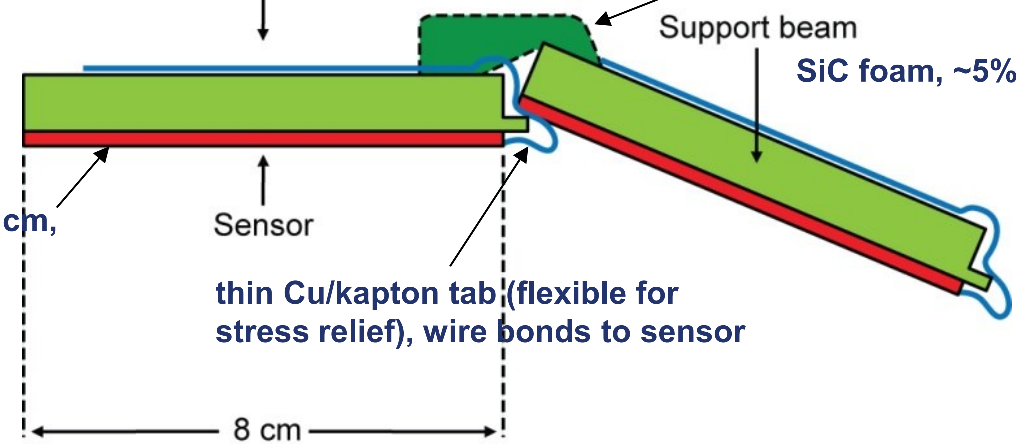
ATLAS tracking system

10% X_0, a frequently-suggested goal for the LC tracking systems (abandoned in 2010 by LCTPC collab, but still hoped-for in SiD collab, who are increasingly interested in the SPT approach)

Our goal is <1% (vertex detector) plus ~3% (tracking layers) ie ~4% total, followed by outer timing layers which may add ~5% [plus the inevitable obliquity factors]

End view of two barrel ladders ('spiral' geometry)

Adhesive-bonded *non-demountable* structure is 'daring' but justified by experience with large gas-cooled systems using monolithic detectors (SLD, astronomy) – very robust, virtually no failures



** copper/kapton stripline runs length of ladder, plus tabs (~5 mm wide) which contact each sensor

Similar stripline runs round the end of each barrel, servicing all ladders of that barrel.

Sparsified data transmitted on demand out of each detector (LVDS then 1 or 2 optical fibres per end), continuously between bunch trains

Continuous (not pulsed) power for tracking layers, hence minimising cross-section of power lines

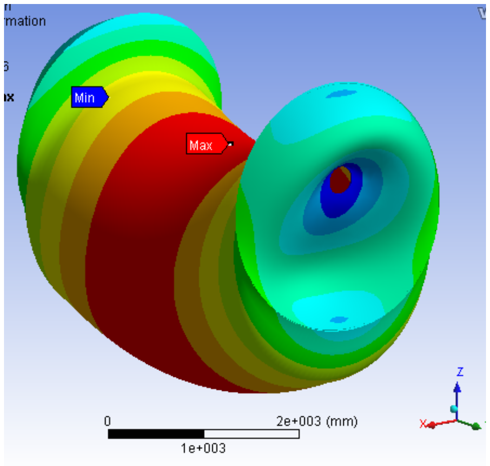
Tracking layers cooled by a gentle flow of nitrogen or air, *hence no cooling pipes* within tracking volume

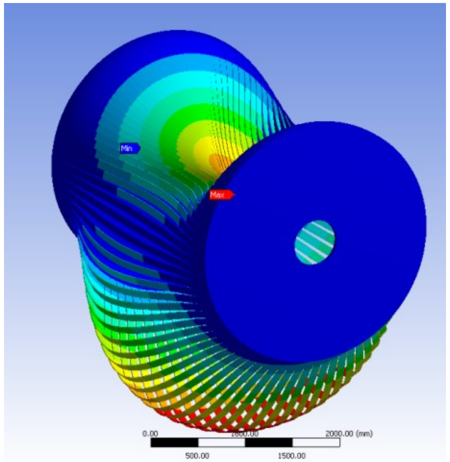
Outer timing layers need pulsed power, and probably evaporative CO_2 cooling, to provide single-bunch timing resolution

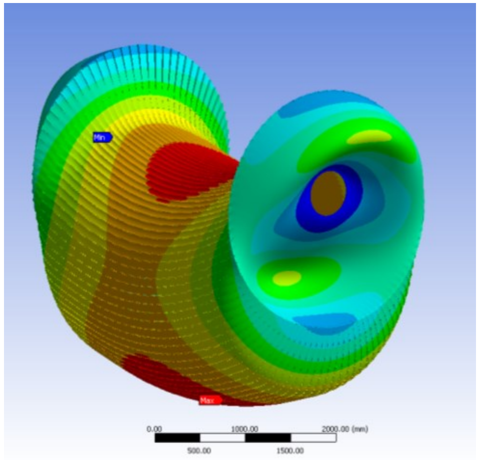
Mechanical structure

- SiC foam favoured wrt 'conventional' CFC sandwich, due to:
  - Homogeneous material, ultra-stable wrt temp fluctuations
  - Accurate match of expansion coefficient to Si, so bonding of large flexible thinned devices to substrate works well
- But what about the lower elastic modulus of SiC? A structure made of discrete ladders supported only at the ends would sag unacceptably under gravity
- Small foam links between ladders, both in the endcaps and in the barrels
- These spectacularly improve the shape stability, almost to the level of a continuous cylinder
- System is assembled layer by layer as pairs of closed half-barrels, sequentially onto the beampipe after the vertex detector
- After assembly, the vertex plus tracking system, mounted on the inner beampipe, is assembled into the overall detector, off the beamline, as part of the ILC push-pull approach for two detectors. Overall weight of this system is only ~200 kg (compare 4.5 tons for current CMS tracker)

ANSYS simulation of Layer 5







- Continuous foam cylinder
- Max deflection 10 μm

- Separate foam ladders
- Max deflection 20.5 mm

- Ladders joined by small foam piece every 40 cm
- Max deflection 20 μm

Steve Watson - *RAL*

System scale

Growth of CCD mosaics

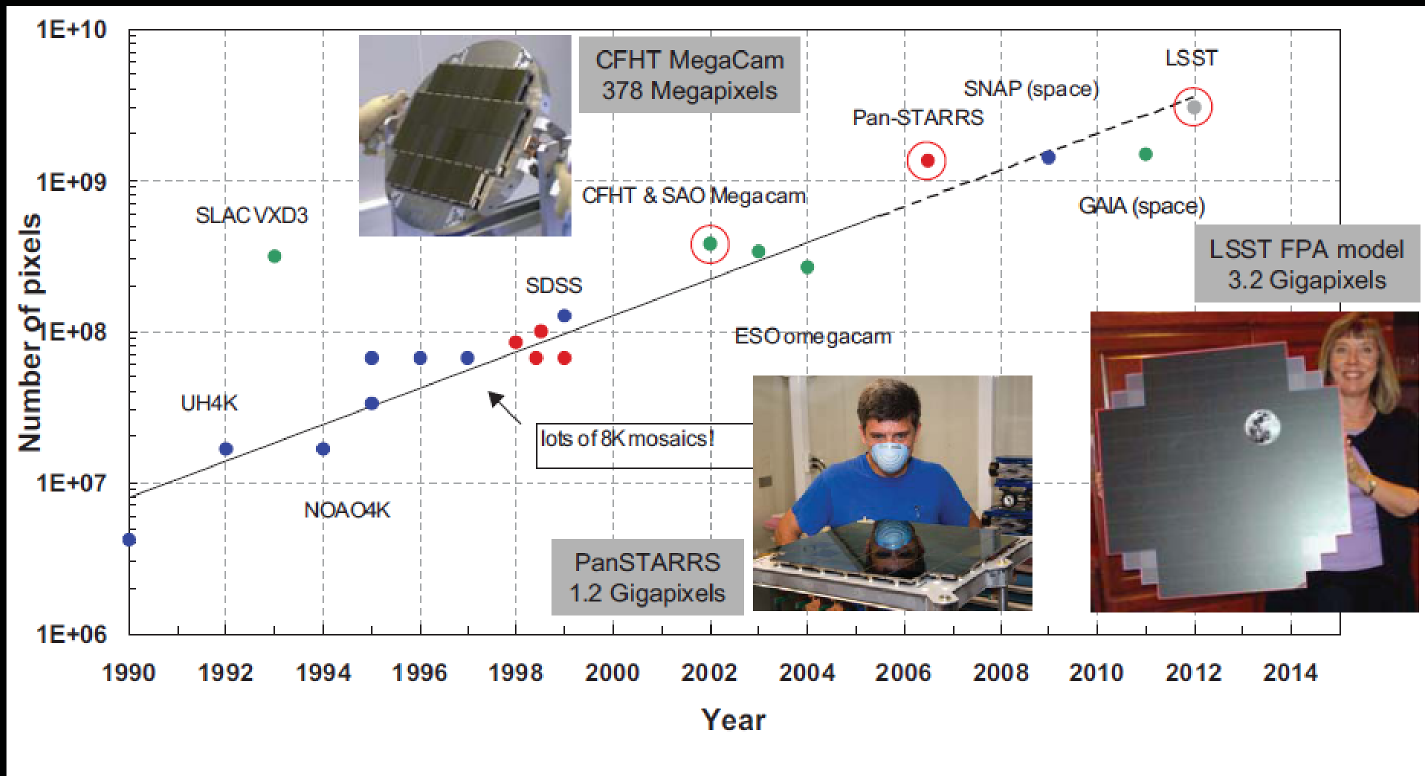


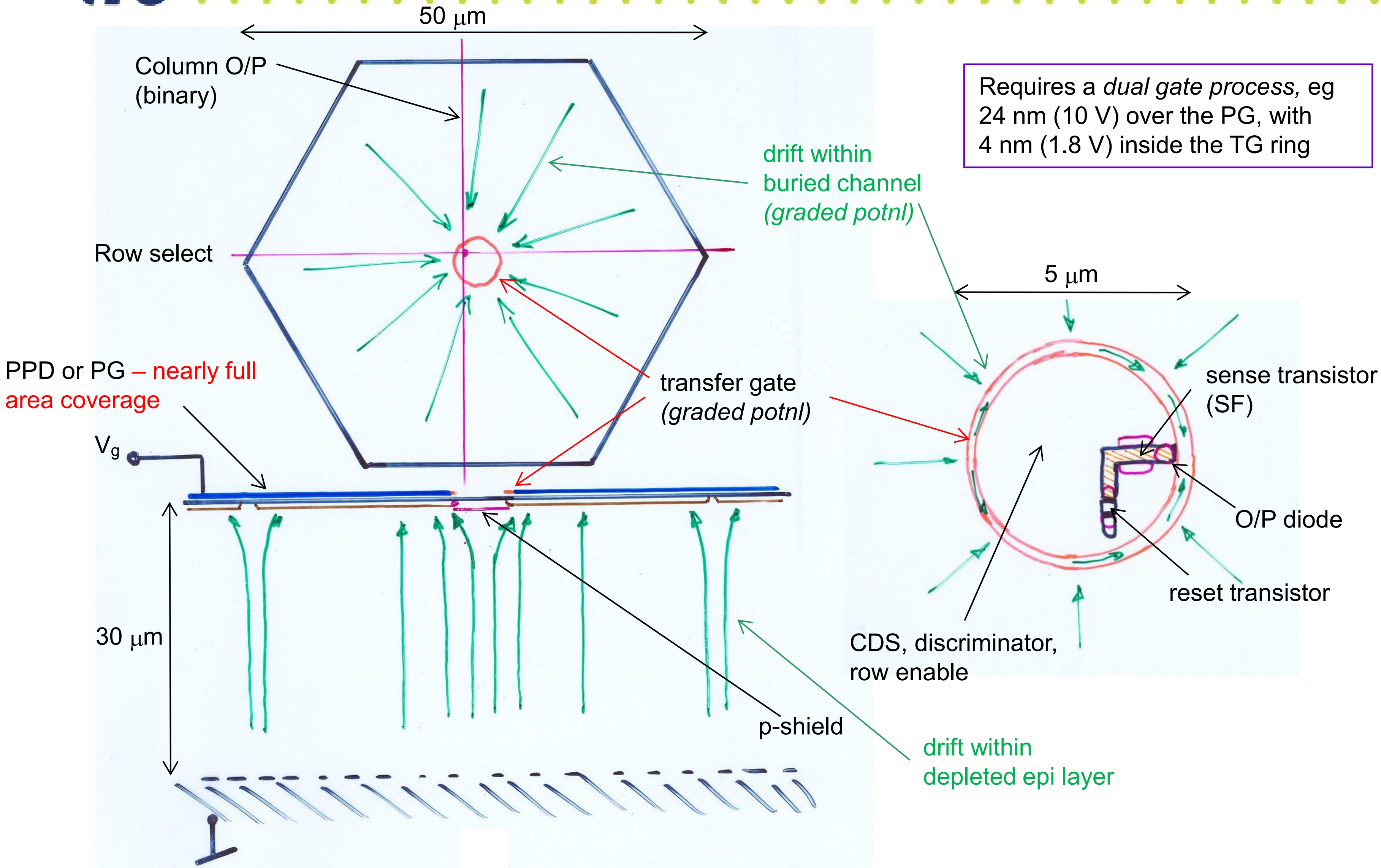
Illustration of large focal plane sizes, from Luppino 'Moore's' law

Focal plane size doubles every 2.5 years

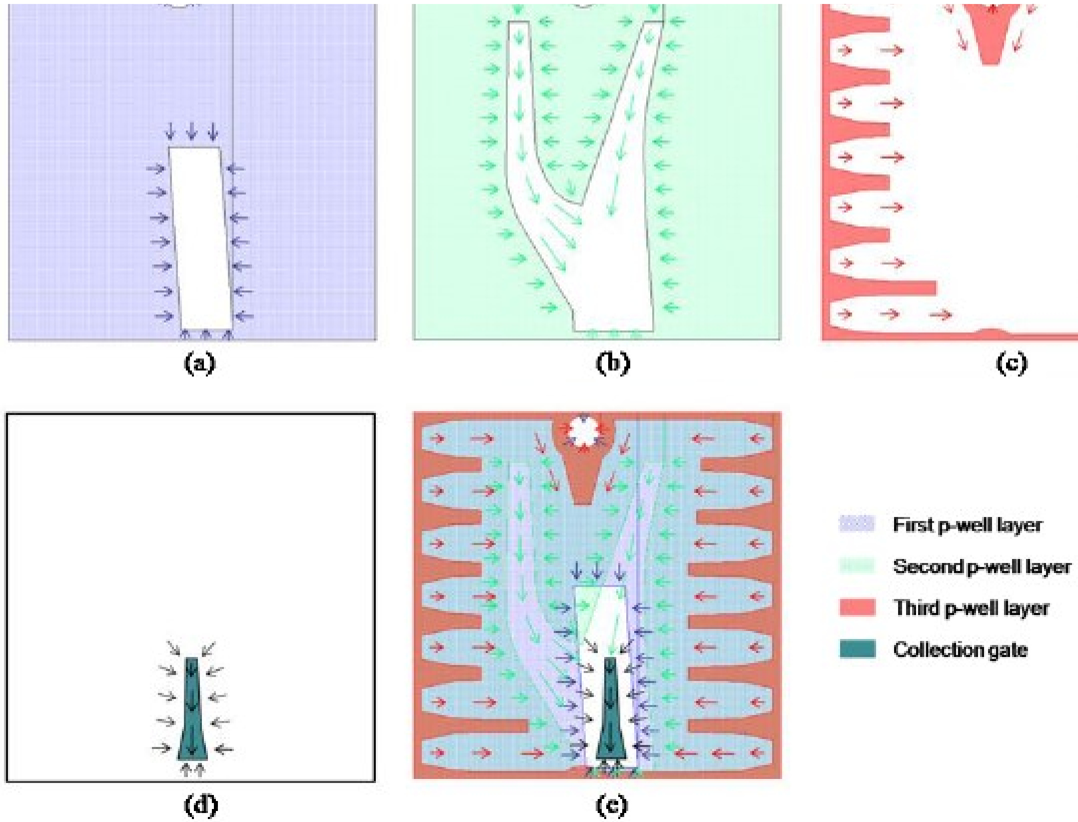
LSST in final stages of prototyping. 40 Gpixels will be 'on the line' by 2020

Note also VXD3

Tracking pixel – unit cell



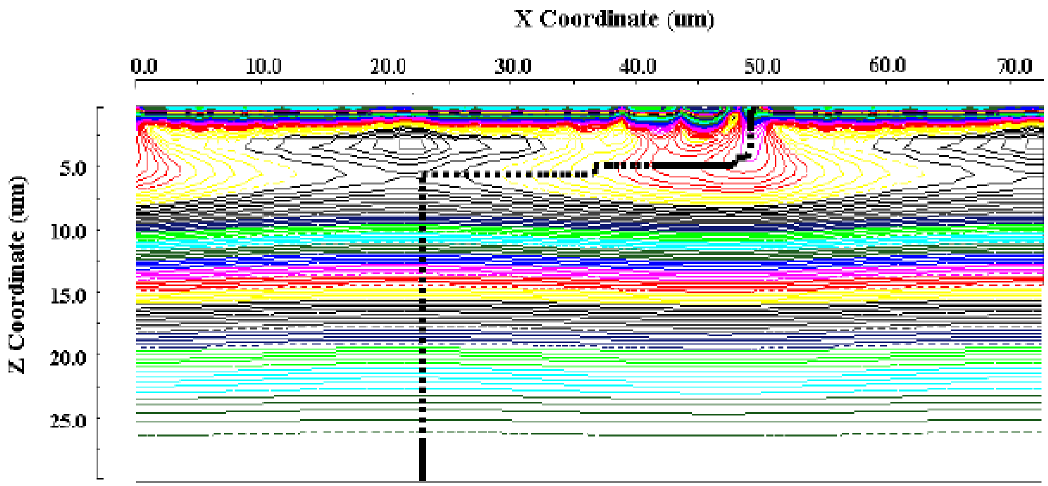
Patterned implants for fast charge collection



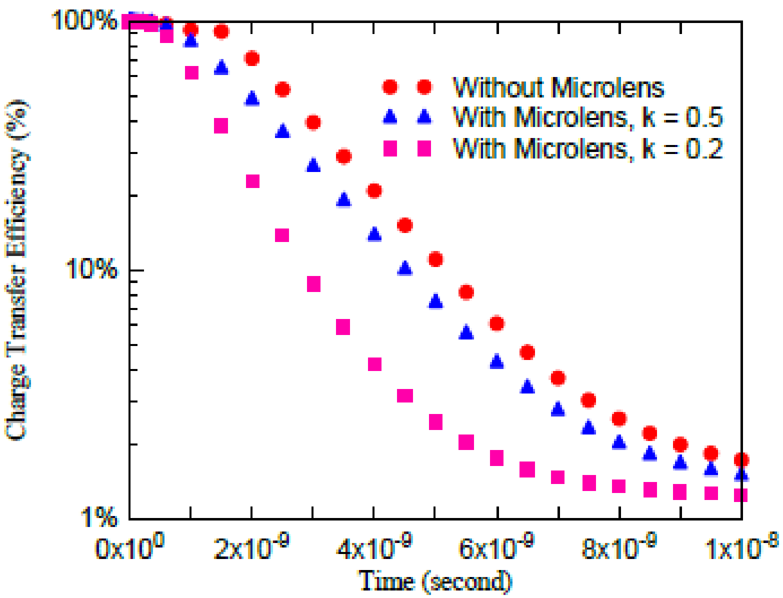
Relatively simple process – all implants can be made at the same energy

Goji Etoh, 2009.

Similar technology available from e2V for CMOS pixels with dual gate thickness

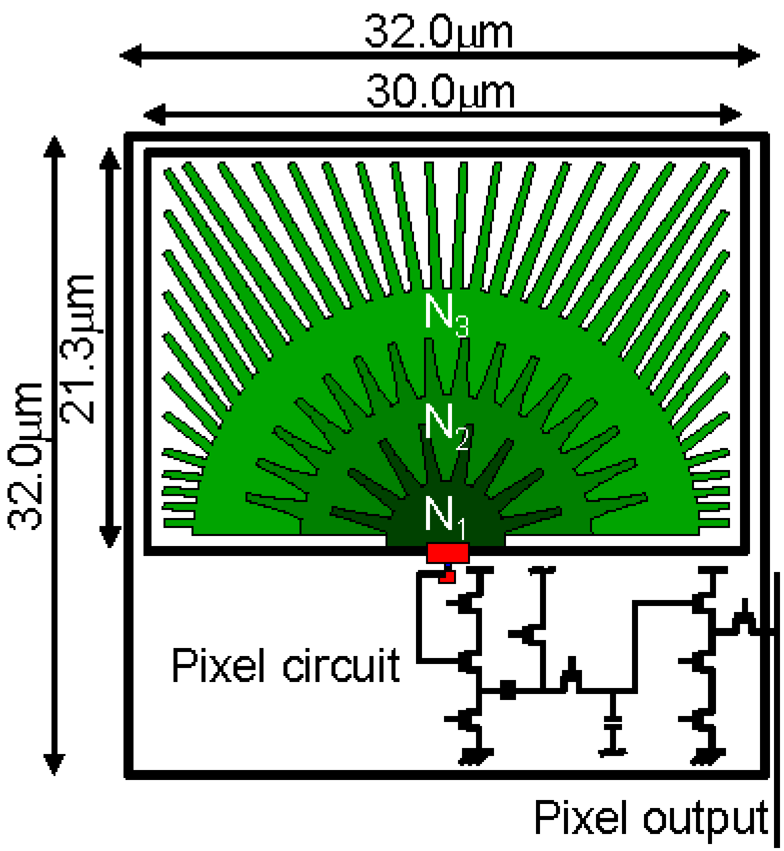


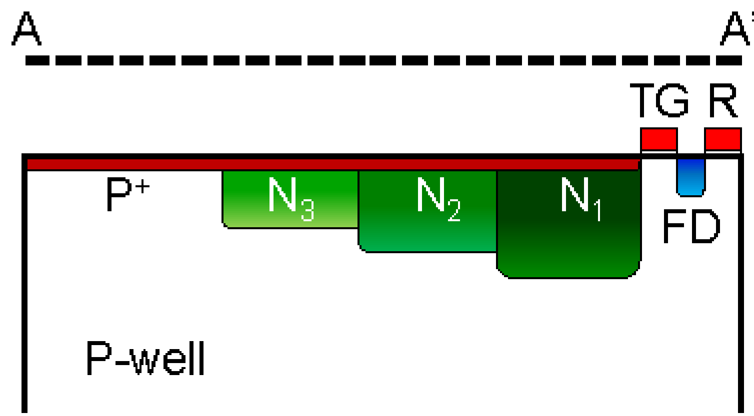
90% charge collection within ~5 ns from uniform illumination of back surface (simulation)



Goji Etoh, 2009

A more recent example, Miyauchi, 2014





Outer timing layers

Regions where 'full' time stamping is needed – 300 ns

There are various technology options (eg hybrid pixels), since material budget is less critical. However, at a quick look, the separated function monolithic pixel appears again to be attractive:

~150 μm diameter pixel should suffice (not needed for precision momentum measurement)

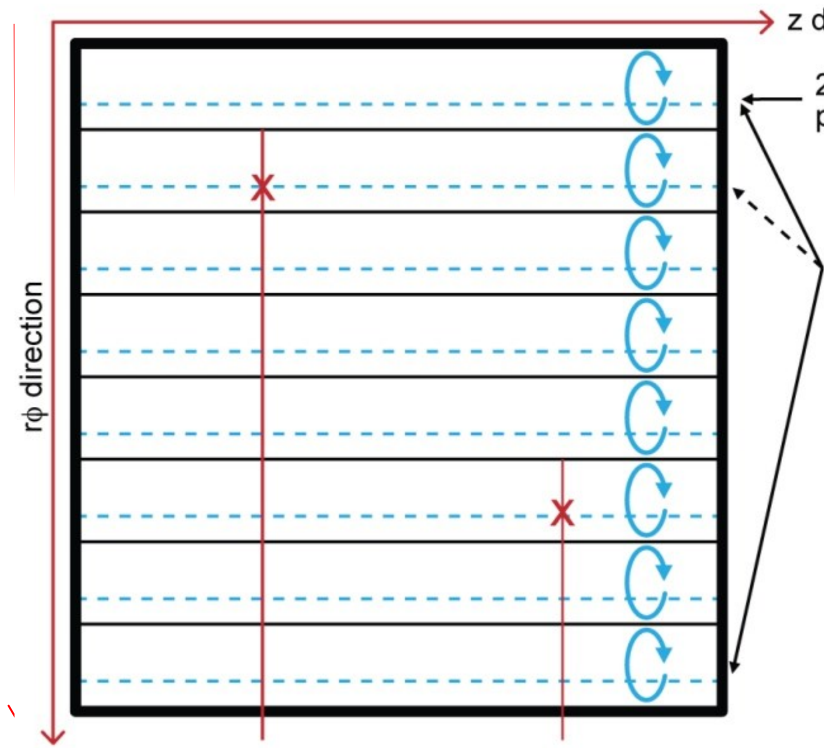
- However, fast charge collection from such large pixels needs careful study and simulation
- Front-end comprises in-pixel sense transistor, CDS and discriminator, as for tracking layers
- But now, CDS spans bunch train (1 ms or 180 ns): Sample-1 before start of train, then open TG. Sample-2 senses the true time of charge collection in pixel
- Add time stamp – send fast column signal to periphery, pick up bunch crossing number and store in edge memory
- Also send to periphery (more leisurely column signal) row address and store that
- Between bunch trains, read addresses and time information of hit pixels
- Continuously active front-end increases power dissipation (from ~300 W to ~1.5 kW)

Possible SPT for LHC

- *Sadly, time has run our for these ideas to be implemented for LS2, so the GPDs are stuck with high power pixel options, implying a high material budget. These ideas could be relevant to a possible far future*
- **Same motivation – greatly reduced material budget. Current LHC physics analyses are degraded by poor tracking performance in fwd region**
- **Remarkably, expected hit rates at luminosity of HL-LHC (from ATLAS colleagues) still allow us to consider the architecture with time-integrating tracking layers, where the tolerable integration time determines the parameters of a rolling shutter**
- **Is radiation hardness of these pixels adequate? It helps that they are already low-resistivity structures (typically below 300 Ω.cm), and we aren't suggesting to go below ~40 cm radius into the 'inferno' of HL-LHC vertex detectors. The fact that CMOS readout chips have to survive there, is surely encouraging (?)**
- **Timing layers with 25 ns resolution and 100% duty factor will need liquid or evaporative cooling, but that's acceptable, close to the ECAL**
- **Track trigger is required: it would be based on mini-vectors from timing layers, linked to the IP**
- **Let's consider one option for the tracking layers, which needs to be more adventurous than for ILC**

Segmented *rolling shutter* readout 'comfortable' example

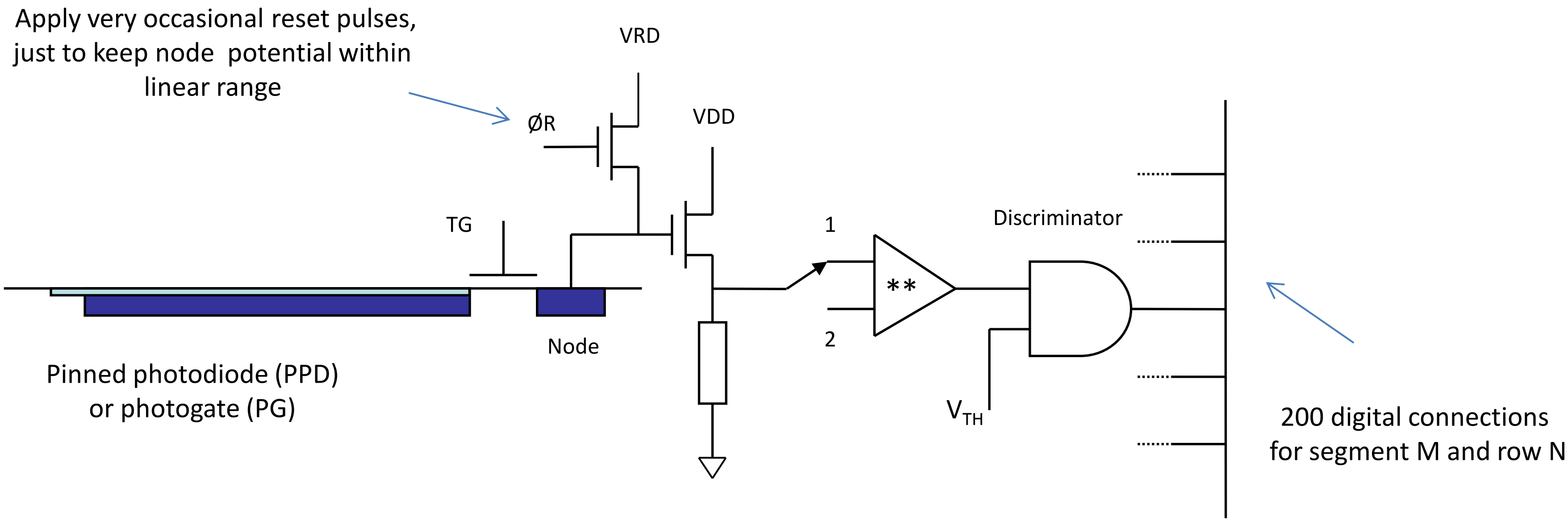
80x80 mm^2
1600x1600 pixels



50 ns per sample, with 200 rows hence 10 μs readout time, 100 k f.p.s

Signals are integrated over 400 BX.

Suggested Pixel logic



**

[V(1) - V(2) (held)] alternating with
[V(2) - V(1(held)]
provides CDS signal with time difference equal to rolling shutter period – certainly adequate noise protection

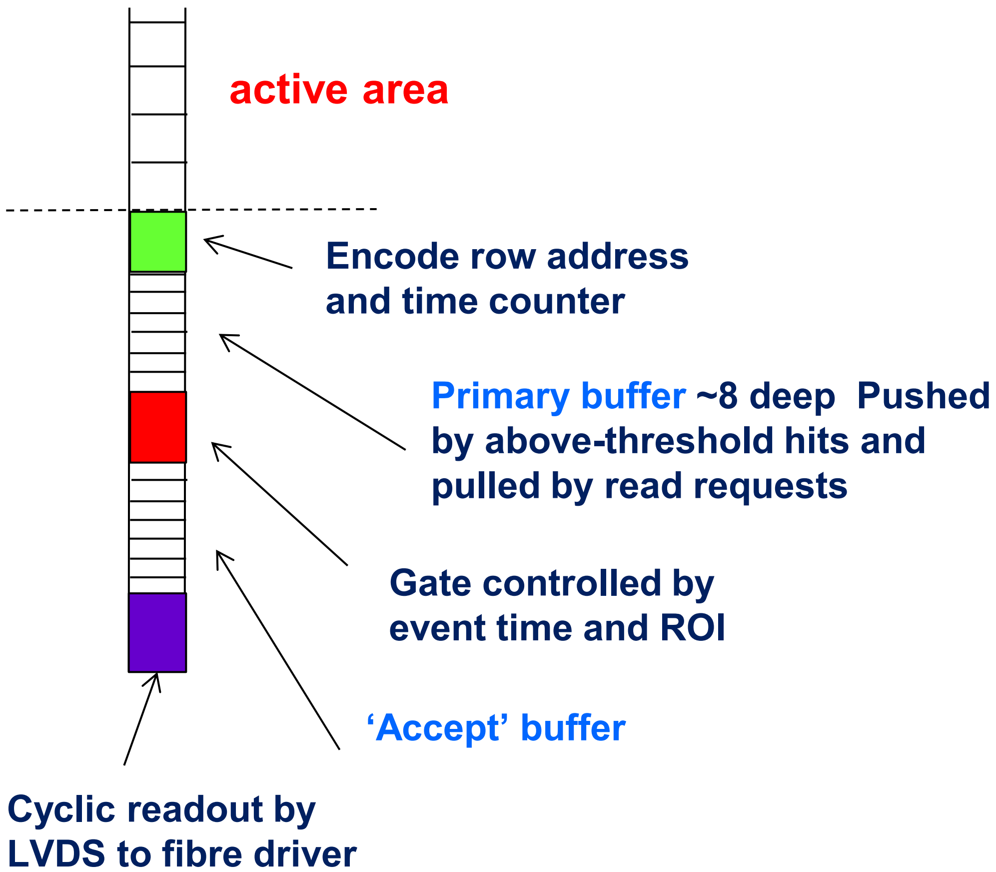
Row-enable switches on VDD, then allows adequate settling time to measure the next voltage sample. Tune S/H timing accurately wrt bunch crossing [Signal charge collection needs to be sufficiently prompt to avoid time-split signals between successive samples]

HL-LHC tracker – power dissipation

- Pixel logic has been simulated in SPICE by Konstantin Stefanov, for 250 and 180 nm CMOS devices. Key points:
- Design requires only 14 transistors per pixel
- FE source follower is operating in subthreshold region
- Signals are stored on 0.1 pF capacitors at input to x4 differential amp (this delivers good noise performance)
- Digital output in pixel has sufficient drive capability for fast signals to chip edge
- --------------------

- Each pixel has power on for only 50 ns each 10 μs. This is the key to achieving low overall power
- Nearly always, the response is ‘nothing there’, so the additional power associated with above-threshold signals is minor
- Average pixel power is 25 nW or 18 nW for 250 or 180 nm technology. This is well below the comfortable limit for gas cooling of 33 nW (1 kW total for tracking layers)
- So one could if needed reduce the integration time below 10 μs
- Might be advantageous to further reduce feature size to 130 nm, 65 nm, or beyond by 2020

Consider readout of one column



- **Case of uniform 10 μs rolling shutter applied to all modules:**

Radius (mm)	Hit density clusters per BX/cm^2	Hit density per 10 μs/mm^2	Layer efficiency* %	Data size (Mb)**
380	0.241	0.964	97.8	16.6
501	0.146	0.584	98.7	13.2
622	0.096	0.384	99.1	10.8
743	0.063	0.252	99.4	8.5
1000	0.028	0.112	99.7	5.1

- **Thanks to ATLAS colleagues (Nikos Konstantanidis, Gordon Crone, …) for estimated hit densities on tracker layers in HL-LHC, 14 TeV, 25 ns bunch interval, luminosity 5x10^{34} cm^{-2} s^{-1}, upgrade layout SLHC_19-13**
- *** Note that background causes loss of *bona fide* hits, but no bias to the track fitting**
- **** 54.2 MB total. This should nearly all be dumped in the sensors. In event building, we would only read data that are in the appropriate time slice and in areas selected by ROIs defined by calorimetry and timing layer vectors. Sipping the appropriate data from the 'LHC firehose' with a 'drinking straw' is probably the greatest challenge.**

- **With these layer efficiencies, 99.9% of tracks with momentum > 10 GeV/c have 4 or 5 good hits on tracking layers**

ROI-based readout

- Using level-1 data, find **mini-vectors** from on-time tracks in the inner and outer timing layers (assume *inner* timing layers will remain obligatory at LHC, but if they too could use tracking layer technology …)
- Find links between these (can be made fast and efficient, given precise 3-D track segments)
- For tracks below some cutoff P_T (possibly ~3 GeV) this is all we need. So for the vast majority of tracks, **the job is done**
- For higher momentum tracks, determine ROIs of ~1x1 cm on the tracking layers, and accept data from these areas, from the data stored in the primary buffers. Data not selected from these buffers are overwritten
- These ROIs will reduce the data volume from the tracking layers from **~54 MB to some tens of kB**
- Even with the hit densities of HL-LHC, the offline association of hits to tracks is highly unambiguous, another advantage of a pixel-based architecture
- Special procedures are envisaged to retain high efficiency for tracks which have no match in the inner timing layers: K-shorts, lambdas and photon conversions (which are relatively rare)

Synergies and next steps

- **Charge-coupled CMOS pixels, developed years ago for high performance cameras, are on the market for scientific imaging as 'scientific CMOS pixels'. Fairchild/Andor/PCO and Hamamatsu are among those active**

- **Jim Janesick's pioneering work with Jazz Semiconductors, and his 'Sandbox' for multi-project wafers, could be very useful for the US community – no longer accessible to European customers, since the Jazz/Tower merger**

- **Jazz were recently awarded a substantial US Government grant to develop advanced imaging devices based on these principles**

- **e2V are developing very similar devices (segmented rolling shutter) for adaptive optics (EELT in Chile) and for weather satellites (observation of lightning)**

- **Next steps for SPT at LHC, would be physics simulations, measurement of rad hardness of existing comparable devices, etc. However, the community is currently focused on options for 2022, as it needs to be. It may be that the HL-LHC option will be studied seriously for the further future, if the SPT becomes established in the less challenging ILC environment**

- **The main message is not to be satisfied with current technologies, but to work toward major improvements**

Conclusions

- The SPT offers the possibility of high performance tracking over the full polar angle range, with a major reduction in material in all directions, particularly the forward region
- For multi-jet physics (where there's nearly always some activity in the forward region) this looks particularly appealing
- In general, having nearly all the photons convert in the ECAL (or just before it, in timing layers), and good quality tracking of electrons, is desirable
- The needed pixel technology may be available, but there are numerous issues, including radiation hardness, to be studied to establish its applicability to tracking systems
- We can profit from the major developments under way for other scientific applications, as well as night vision devices. Goji Etoh, Jim Janesick and others are keen to collaborate. An inter-disciplinary approach to this R&D looks promising
- By 2020, 40 Gpixel systems for science will exist. There has been huge progress in the particle physics community since the first tentative steps with small CCDs of 250 kpixels, in the ACCMOR collaboration 30 years ago, which made major early contributions to the physics of charmed particles, after their (virtual) discovery here at Brookhaven and at SLAC in 1974, 40 years ago next month.

Most recent writeup is in Proceedings of Science, papers from Vertex 2011 workshop: 'New detectors' in http://pos.sissa.it/cgi-bin/reader/conf.cgi?confid=137

SOME EXPERT OPINIONS IN 1980

"Put such a delicate detector in a beam and you will ruin it".

"Will work if you collect holes, not electrons".

"Far too slow to be useful in an experiment".

"It's already been tried; didn't work".

"It will work but only with ≤ 50% efficiency".

"To succeed, you will have to learn to custom-build your own CCDs: investment millions".

"At room temp it would be easy, but given the need to run cold, the cryogenic problems will be insurmountable".

"May work in a lab, but the tiny signals will be lost in the noise (RF pickup etc) in an accelerator environment".

However, Wrangy Kandiah from AERE, Emilio Gatti and Franco Manfredi from Milano, Veljko Radeka from BNL, Joe Killiany from NRL, Herb Gursky from Harvard Smithsonian were supportive

Particle physics funding committee in UK found it 'too speculative'; but Erwin Gabathuler, then director of EP Div in CERN, kindly came to our rescue