Current X-ray detector projects for NSLS-II beamlines

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Detectors for NSLS-II

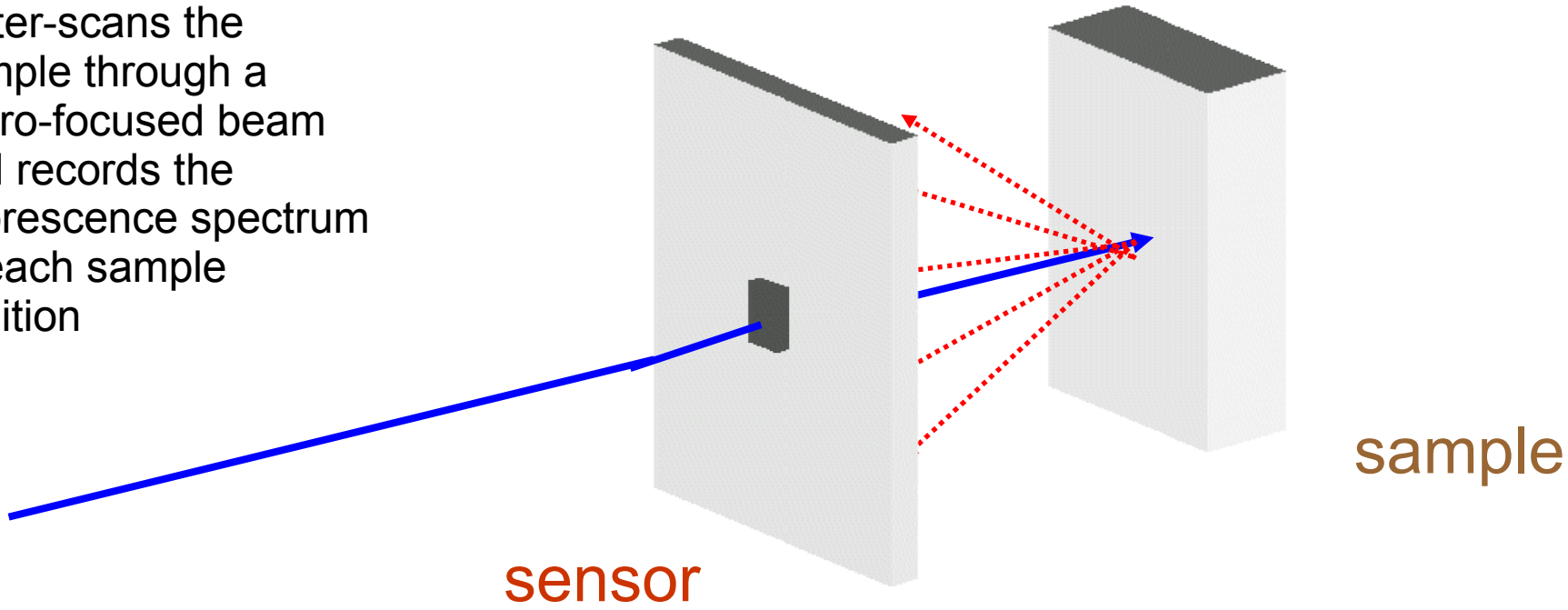
- X-ray spectroscopy
  - Maia: high-throughput elemental mapping
  - HEXID: A “color” x-ray camera
- XCS (x-ray 'speckle') experiments; VIPIC
- Inelastic scattering
- Powder diffraction
  - CZT
  - Scintillator array
  - Germanium

Collaborations

- Photon Science Detector Group is small:
  - Tony Kuczewski, Rich Michta, Abdul Rumaiz
- All of the things described here are the result of collaborations with others:
  - Instrumentation Division
  - Fermilab
  - CSIRO, Australia
  - Semikon Detectors, GmbH
  - LNLS, Brazil

Backscattering geometry for fluorescence microprobe

X-ray microprobe raster-scans the sample through a micro-focused beam and records the fluorescence spectrum at each sample position



- Backscattering geometry allows close approach to sample.
- Provides good solid-angle even for small detector area

Spectral deconvolution → Dynamic Analysis method

PIXE/SXRF spectra are linear combinations of pure element spectral signatures.

Deconvolution cast as a matrix transformation:

$$C = Q^{-1}\,\Gamma\,\mathbf{S}$$

Concentration vector

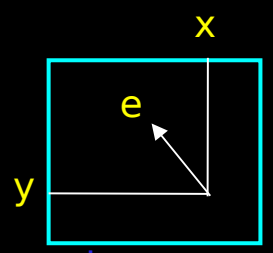
Transform matrix

Spectrum vector

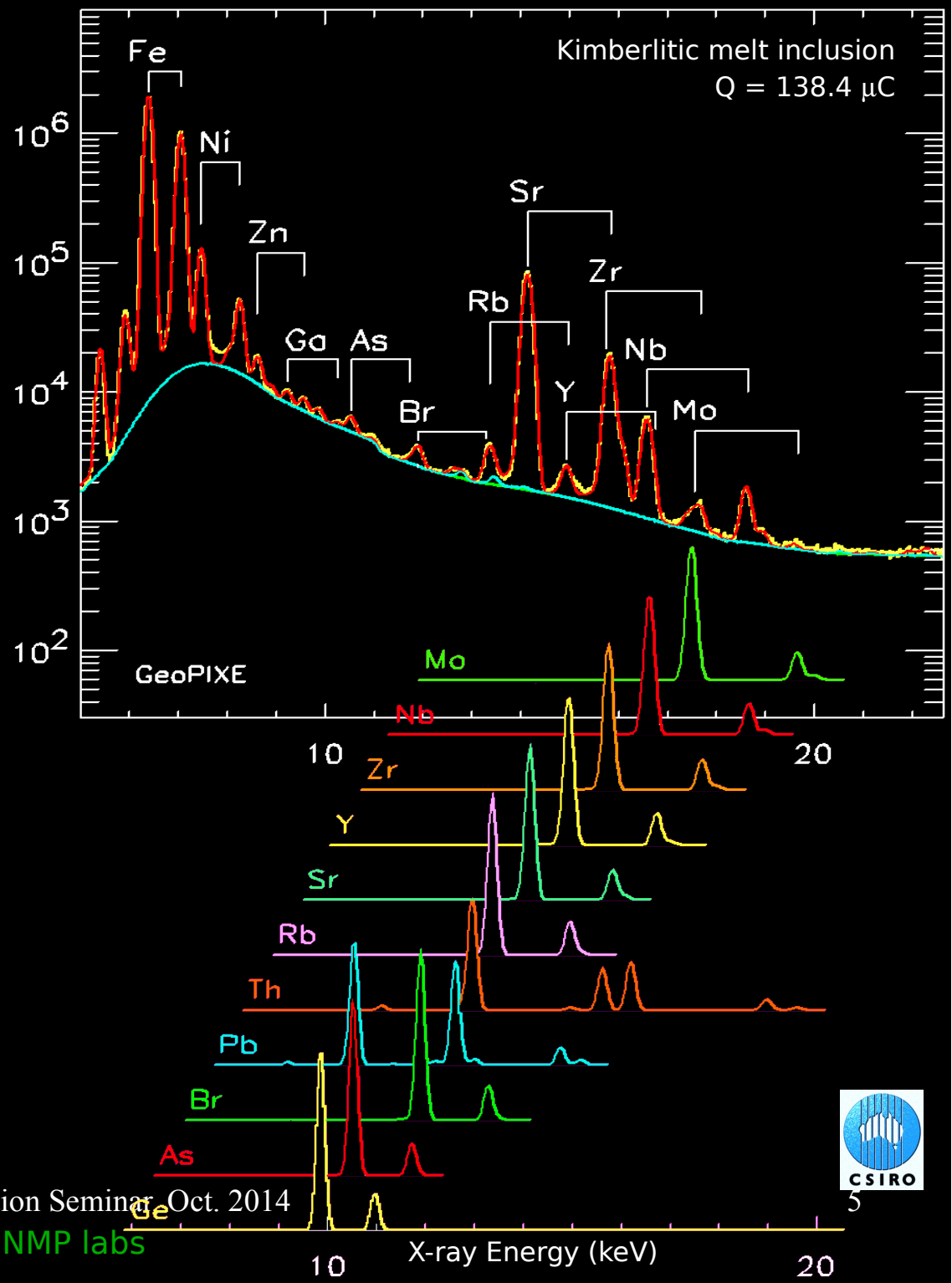
PIXE/SXRF Imaging:

X-ray event: Energy 'e'

Position 'x,y'



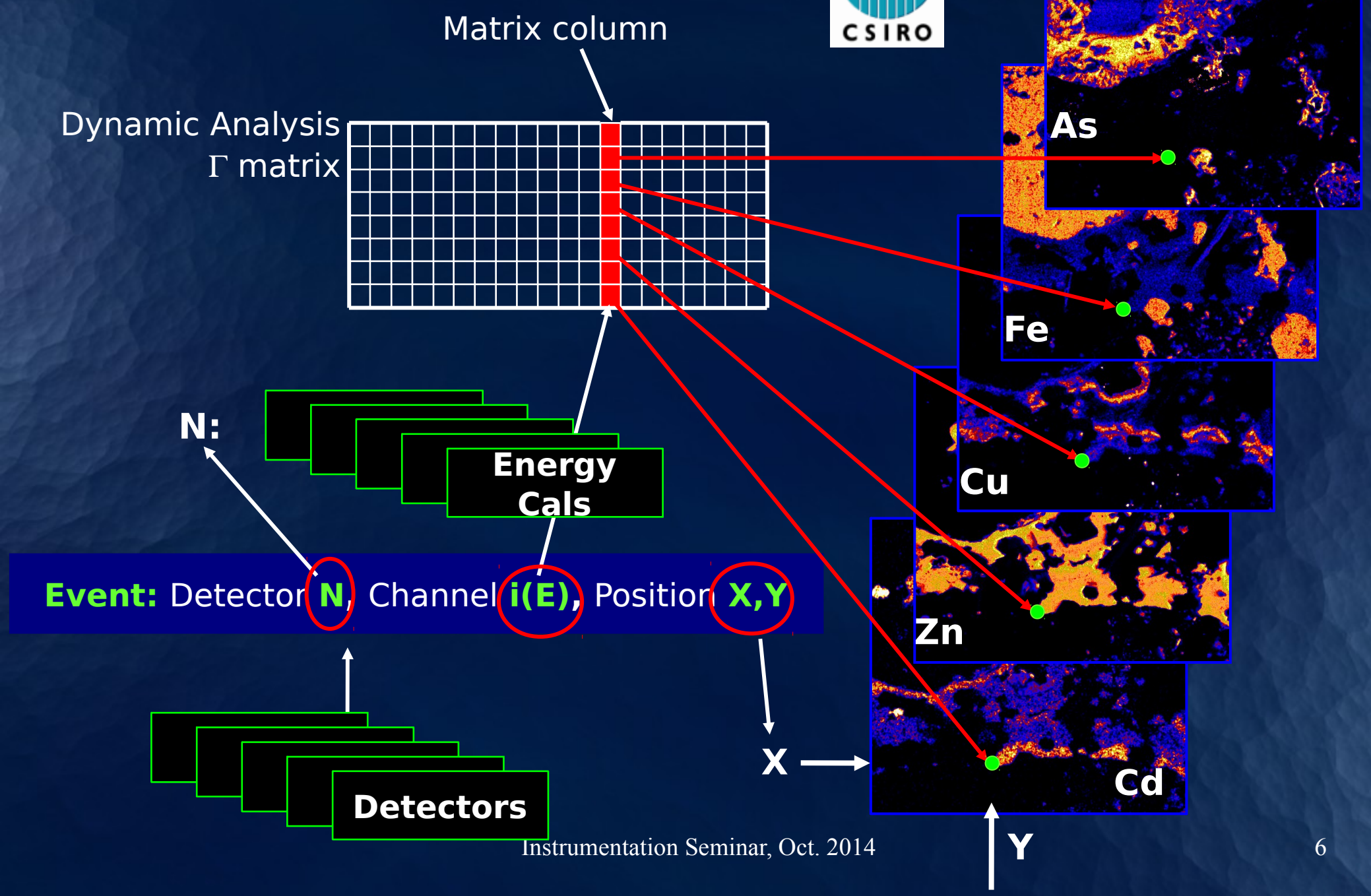
The elements of the Γ matrix for column 'e' are the increments to make to all images at 'x,y'.



GeoPIXE software

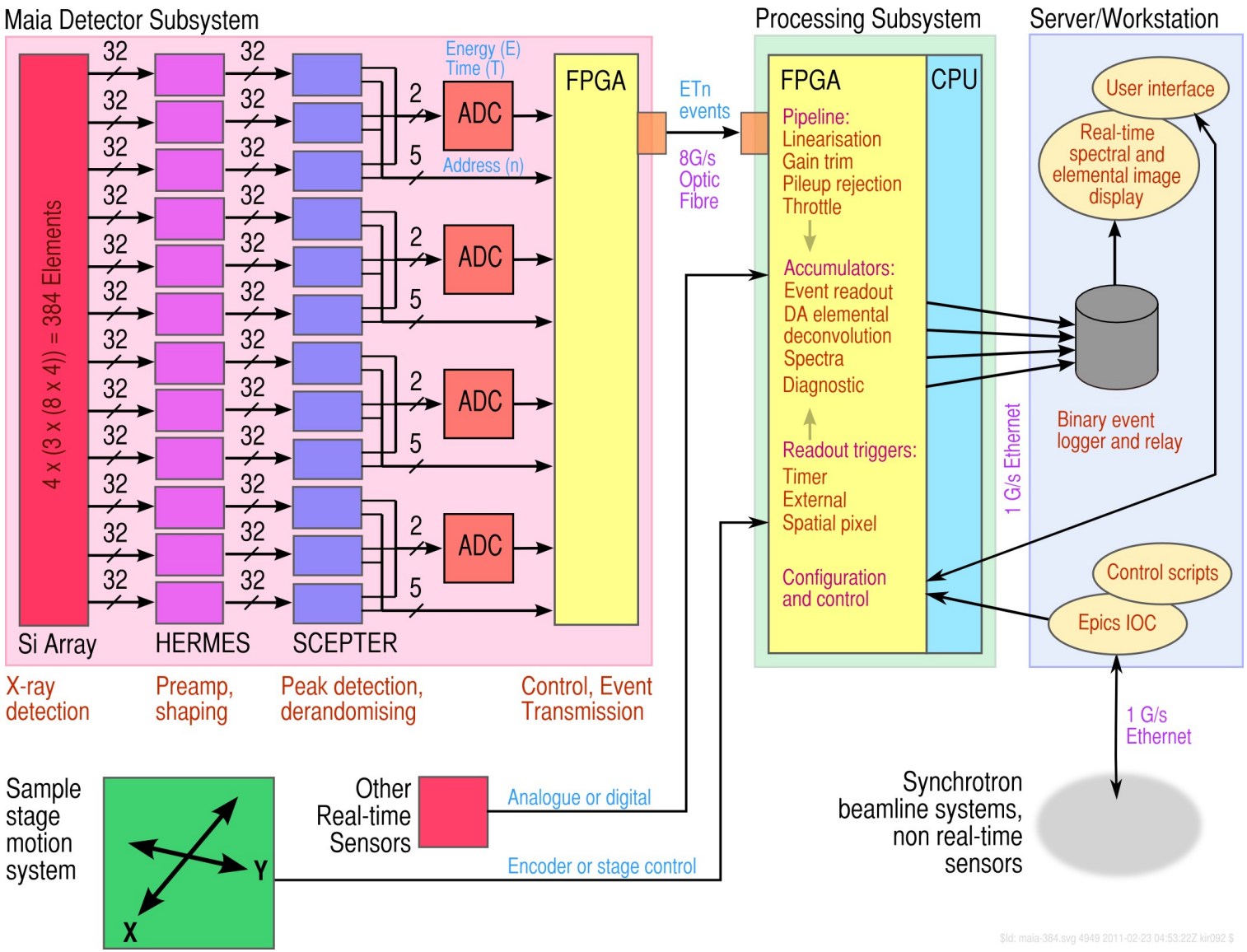
Now at APS, NSLS, CLS, 19 NMP labs

Real-time Elemental Imaging



Block diagram of Maia processing chain

- HYMOD controls stage and reads detector
- Each photon tagged with energy, XY position and pileup status
- Initial coarse scan generates 'average' spectrum which makes DA matrix
- DA technique then presents elemental map as acquisition proceeds.



Sensor +ASICs

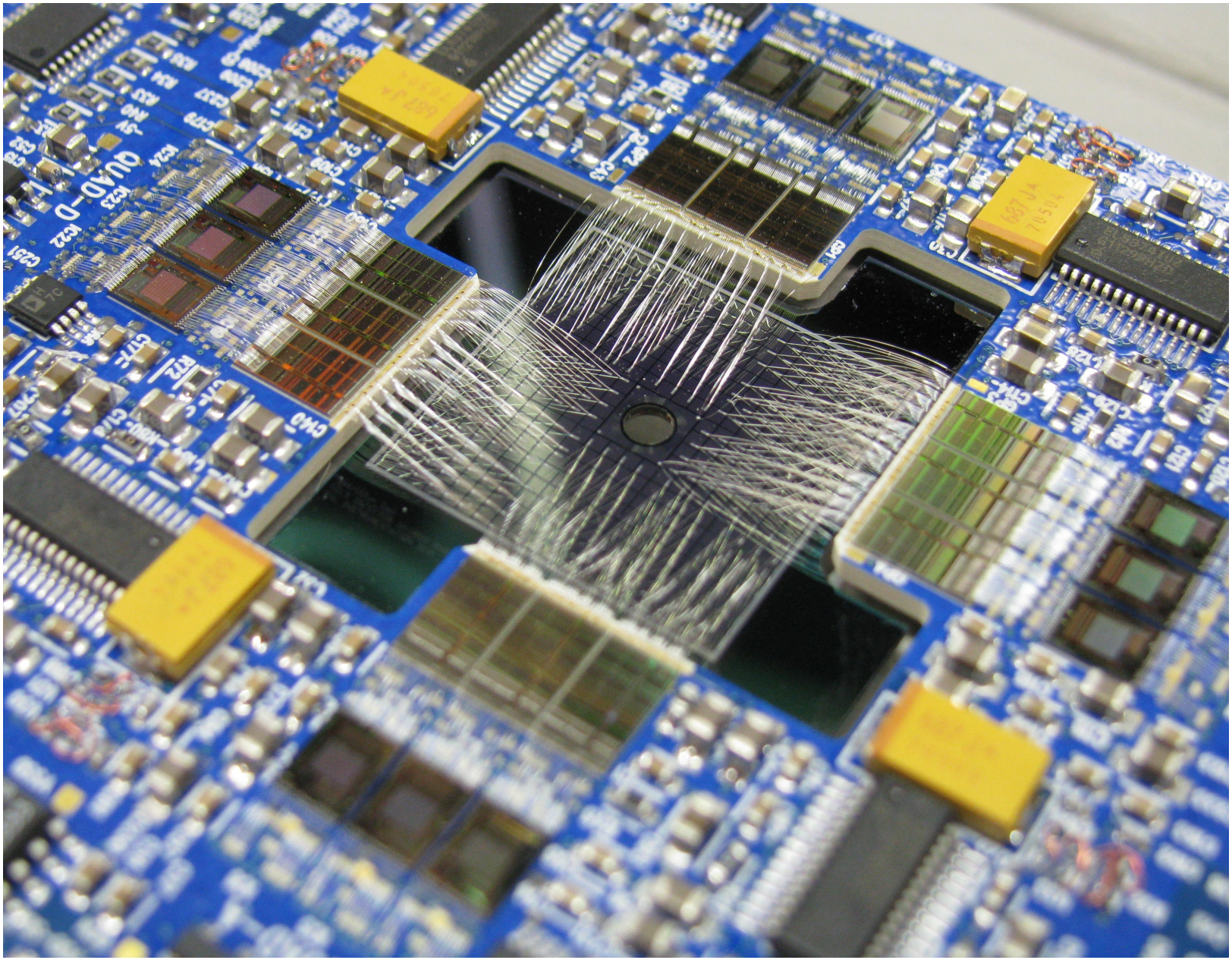
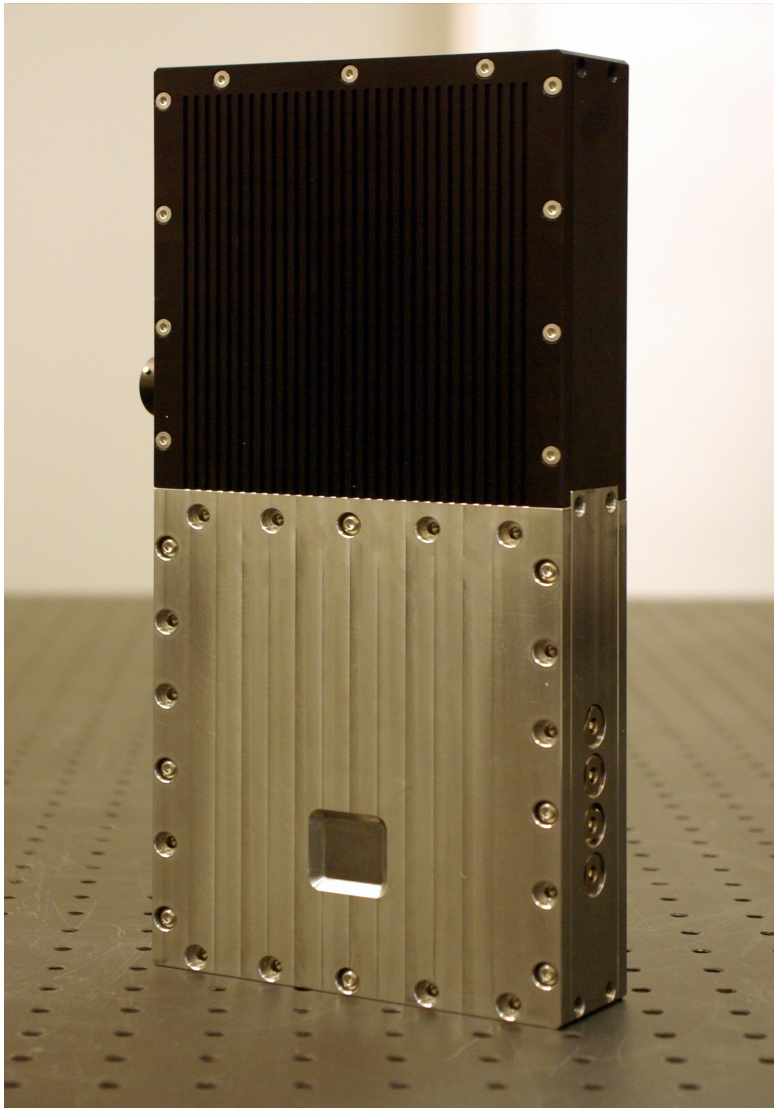
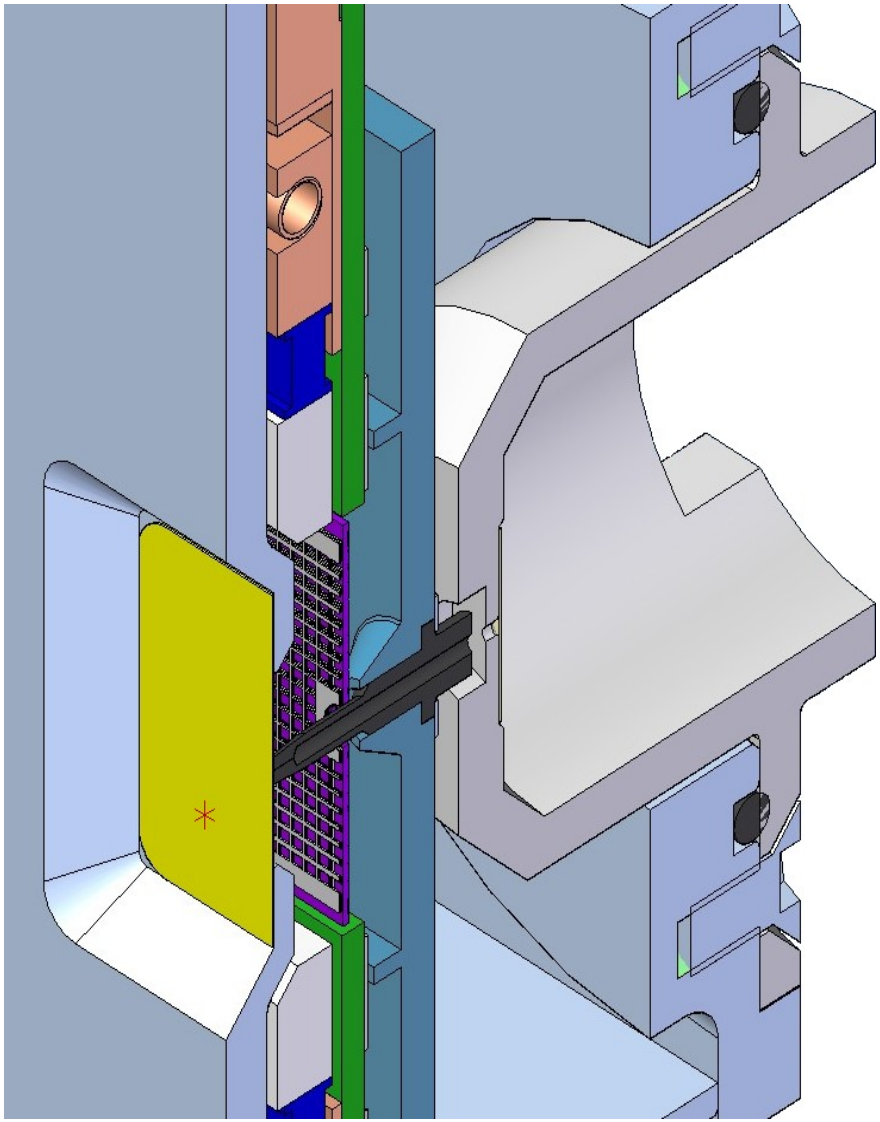


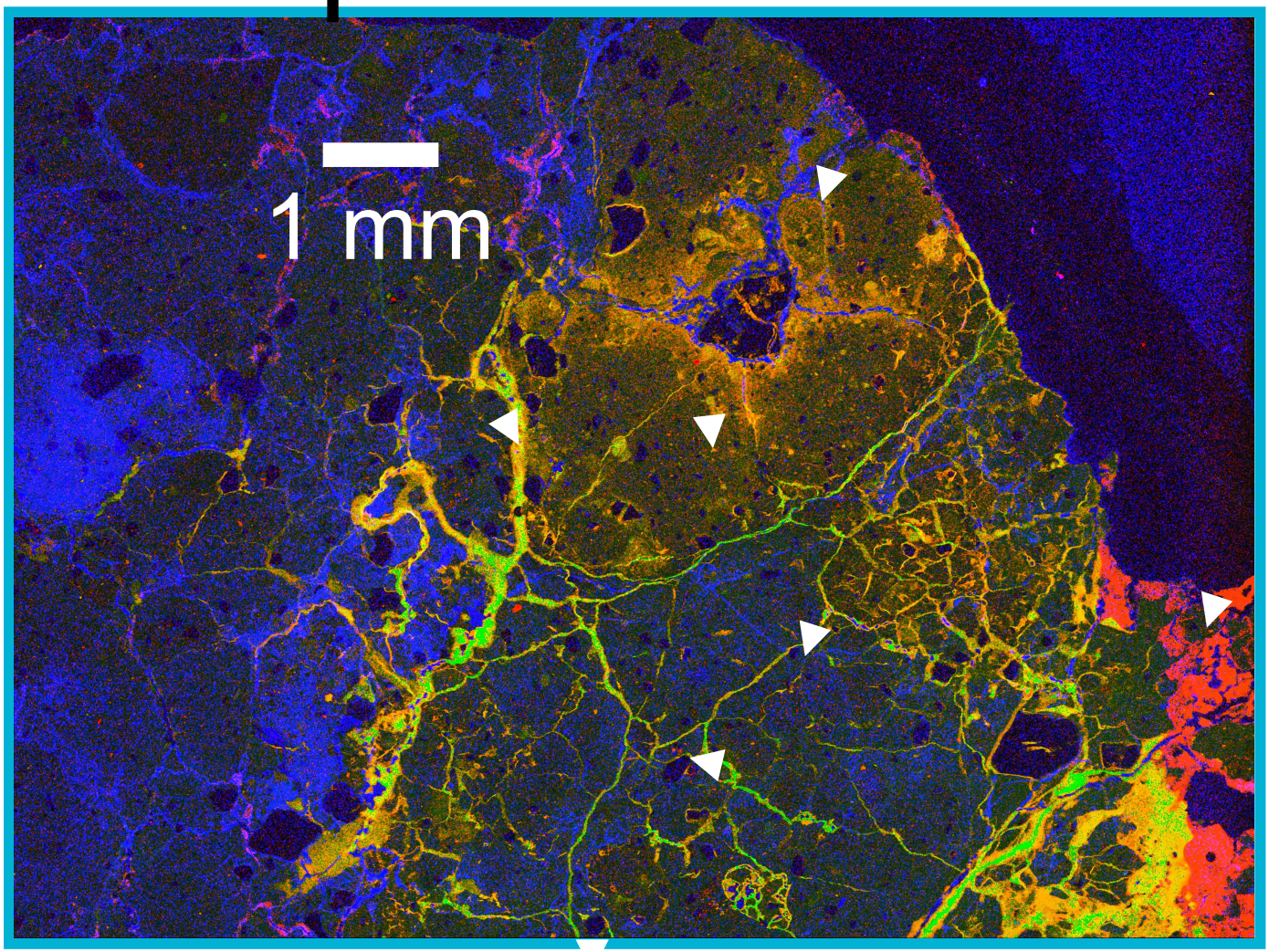
Photo and cross-section





Extremely inhomogeneous samples

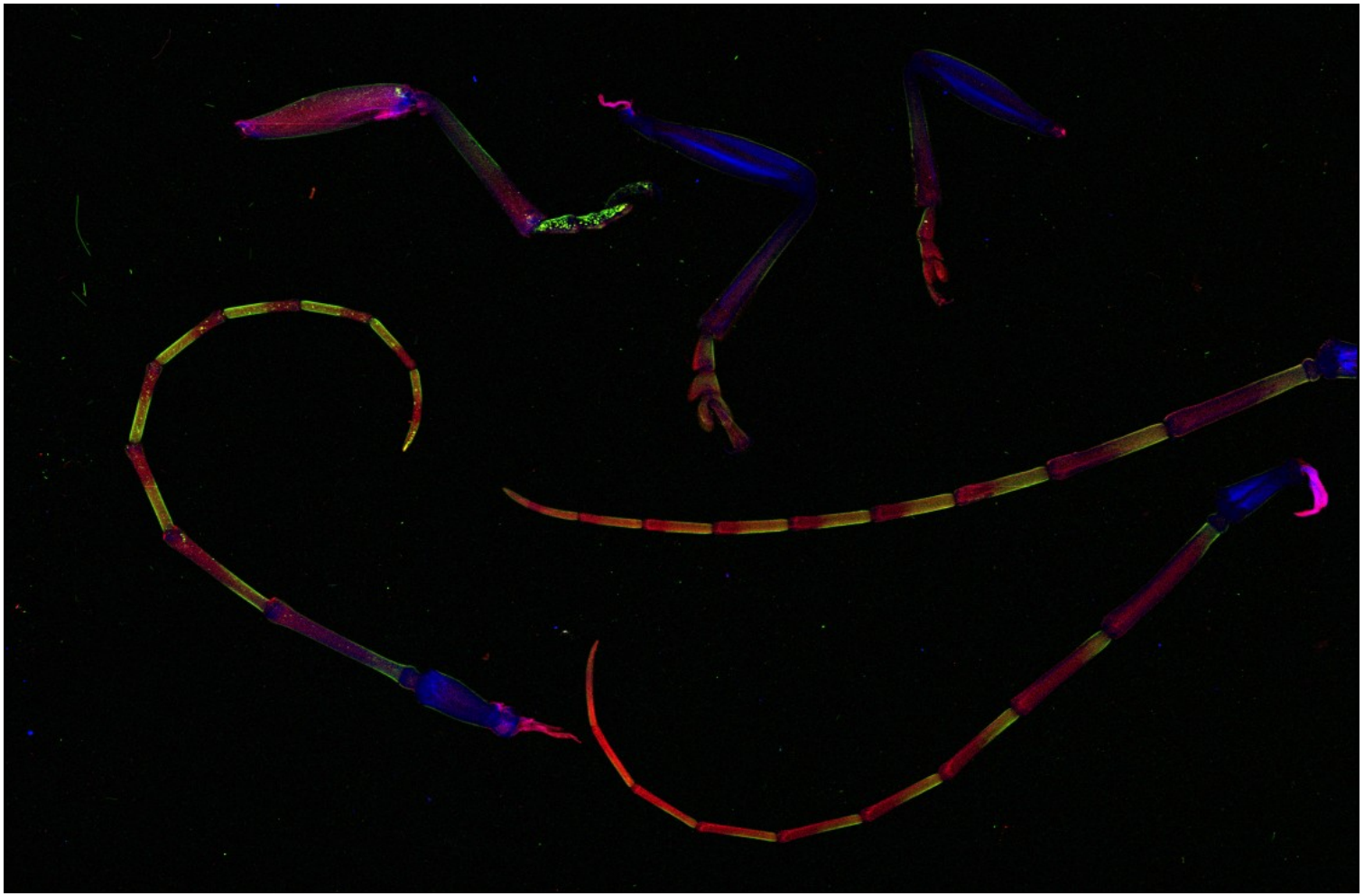
- 9600 x 8000 pixels
- 0.6 ms/pixel
- 1.25 um pixels



Rob Hough, James Cleverley, CSIRO, private communication

Asian Longhorn Beetle Legs and Antennae

- Potassium =red
- Calcium=green
- Zinc=blue
- Sample prepared by Tarryn Goble, Ph.D., post-doctoral associate in the laboratory of Prof. Ann Hajek, in the Cornell Department of Entomology.



Maia development

Limitations of present system:

(a) High capacitance planar diode sensors limit energy resolution

(b) Noise performance of current ASIC (Hermes) could be improved.

Developments underway:

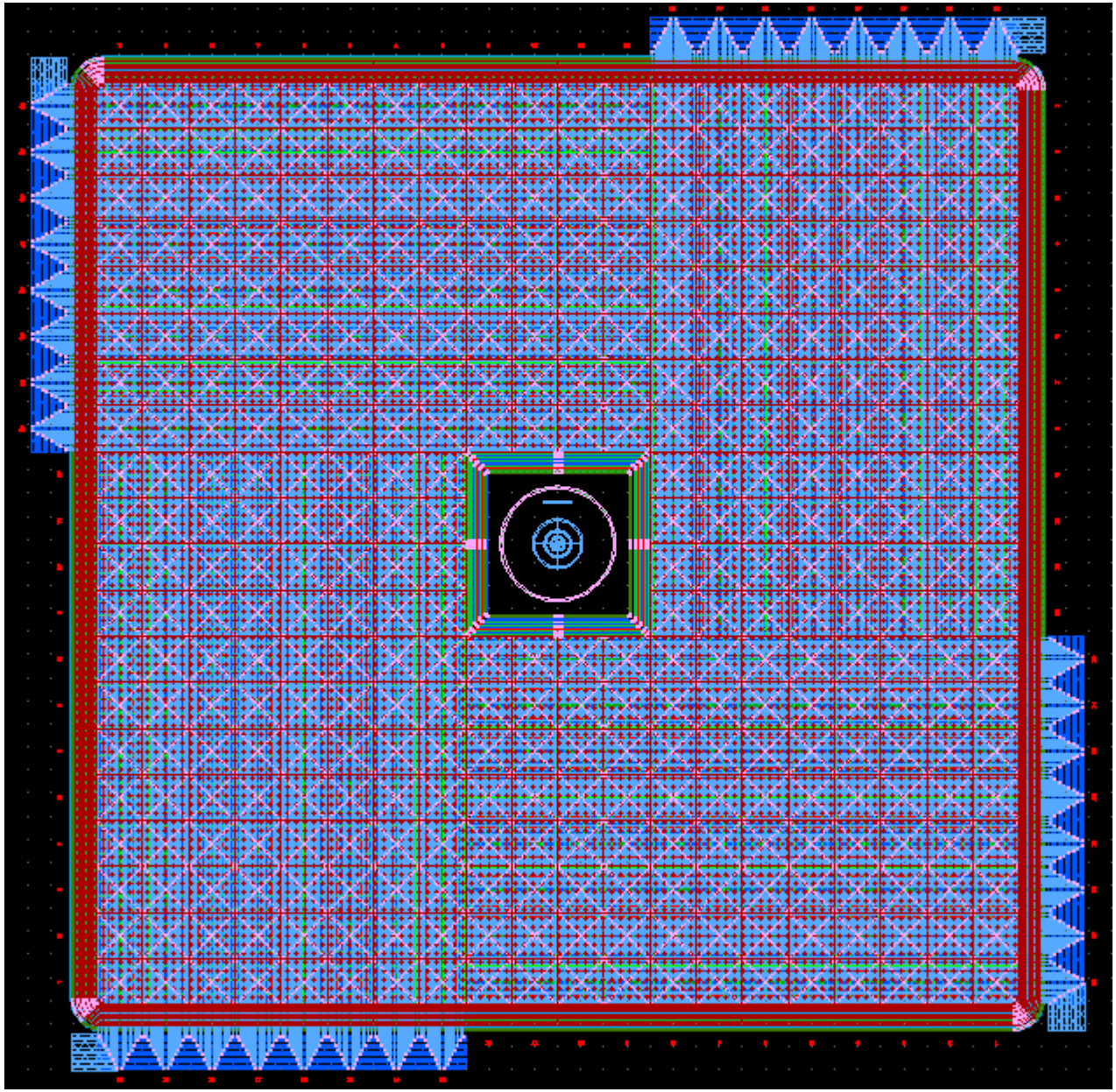
(a) We are looking into arrays of SDDs to provide the ultimate low-capacitance sensor. These are complex structures, so yield in large arrays is an issue (Wei Chen).

(b) MARS, a new amplifier ASIC, has been designed to provide lower noise for lower capacitance detectors and to integrate the functionality of the SCEPTER chip (Gianluigi De Geronimo and Emerson Vernon).

Both of these need to be tested to verify that the ASIC has no bugs and that the new sensors have no unexpected behaviours.

SDD arrays

- 20 x 20 array of 1mm devices (to match Maia's layout)



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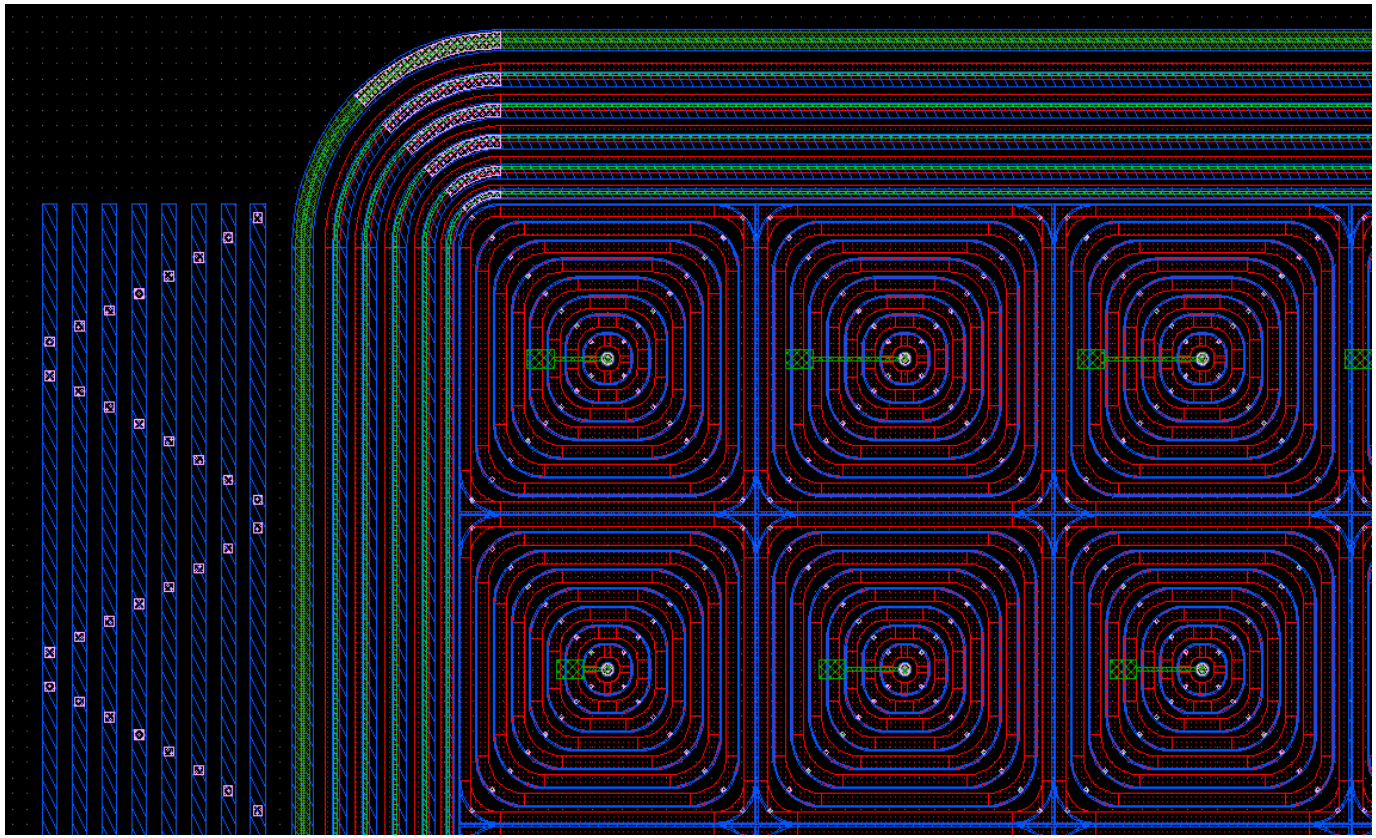

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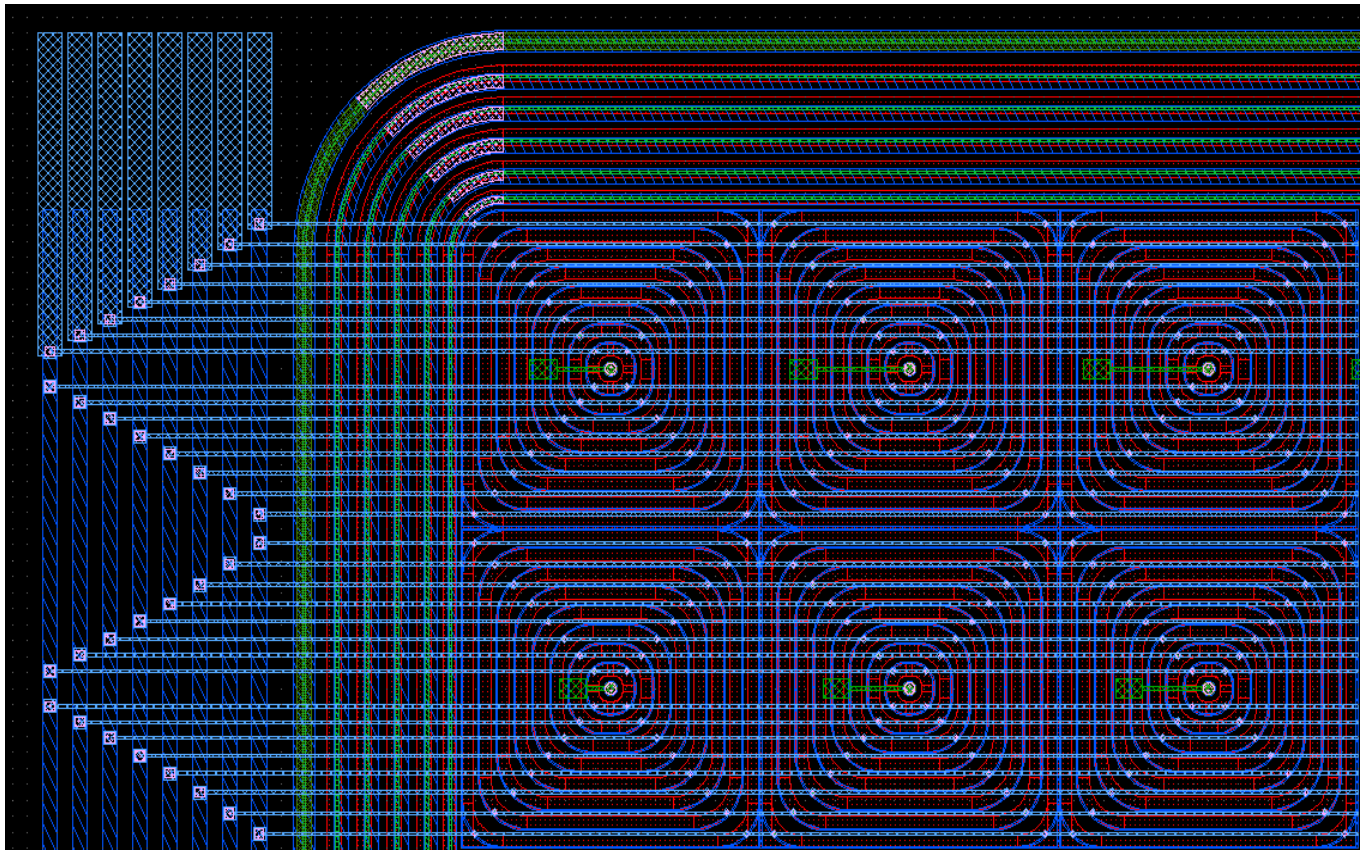
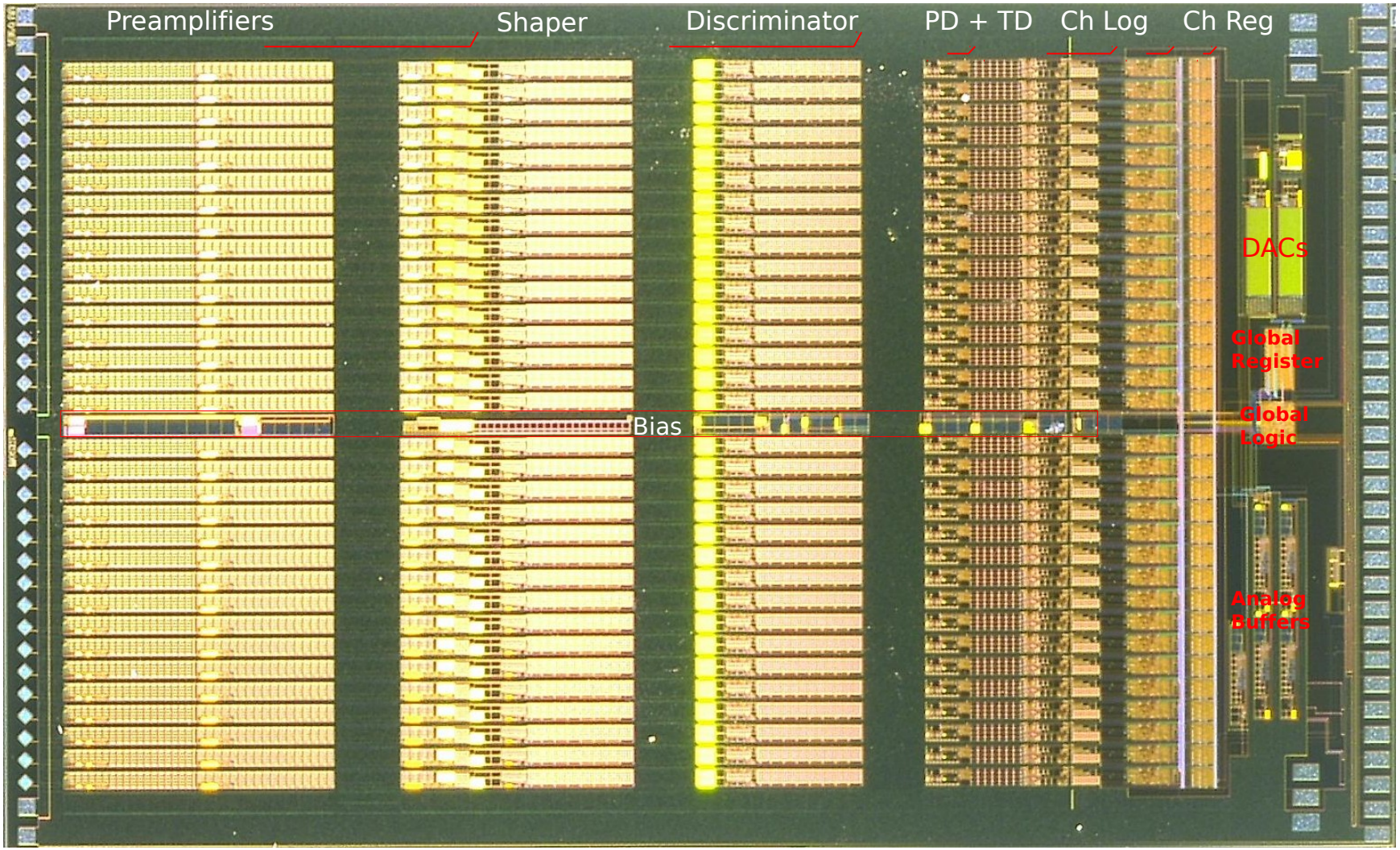


MARS chip

- A new, lower-noise 32-channel amplifier design.
- Peak-detector & time detector per channel.
- Sparsified readout.
- Replaces two chips in Maia design
- Reduces power by >2
- In production, due November. (Emerson Vernon, Gianluigi De Geronimo)

Photo of MARS chip

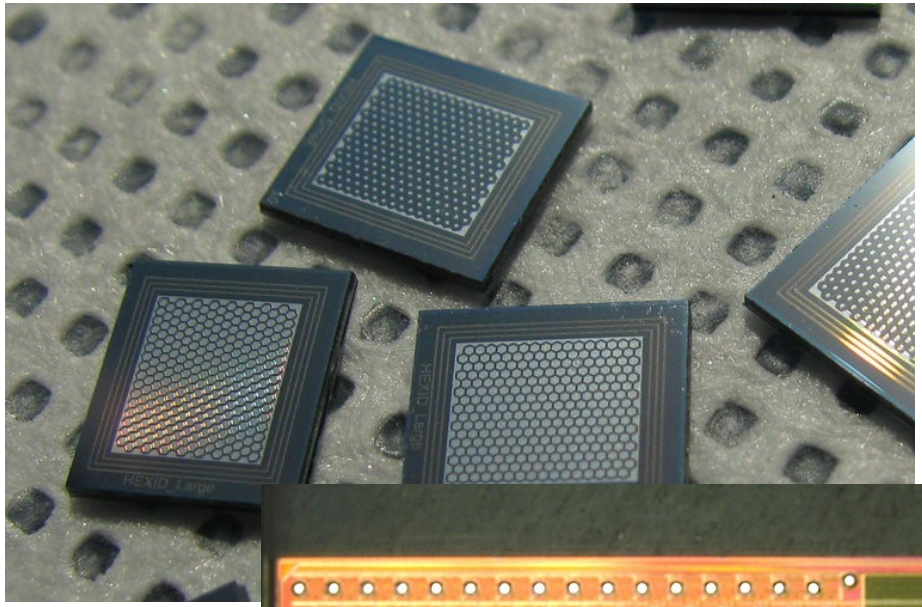


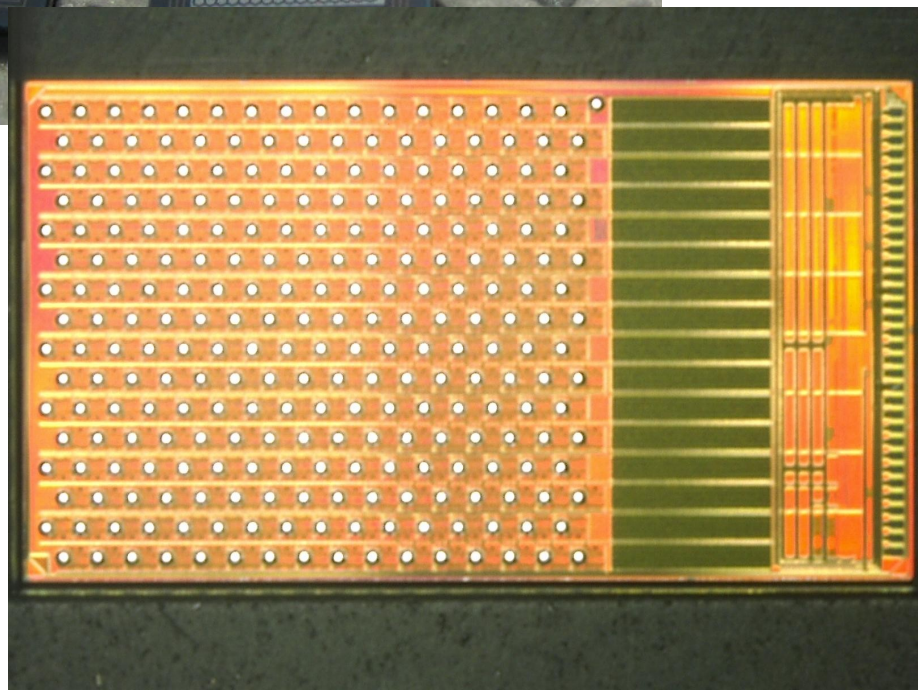
Beyond Maia

- HEXID: A true Color X-ray Camera
  - Hyperspectral Energy-resolving X-ray Imaging Detector
  - “Small” pixels (initially 250um)
  - Full spectrum per pixel
  - High rate per pixel (photon counting, ~50kHz/pixel)
  - Large arrays (~1Mpixel)
- Prototype being fabricated
  - ASIC bump-bonded to sensor array
  - 16 x 16, IBM 130nm, C4NP bump process
  - P-on-N diode array sensor
  - Hexagonal array for simpler handling of charge-sharing

Sensors & ASIC

- Sensors have been fabricated
- Two designs:
- Large implant area
- Small implant area
- ASIC received; being tested (Shaorui Li, Gianluigi De Geronimo).

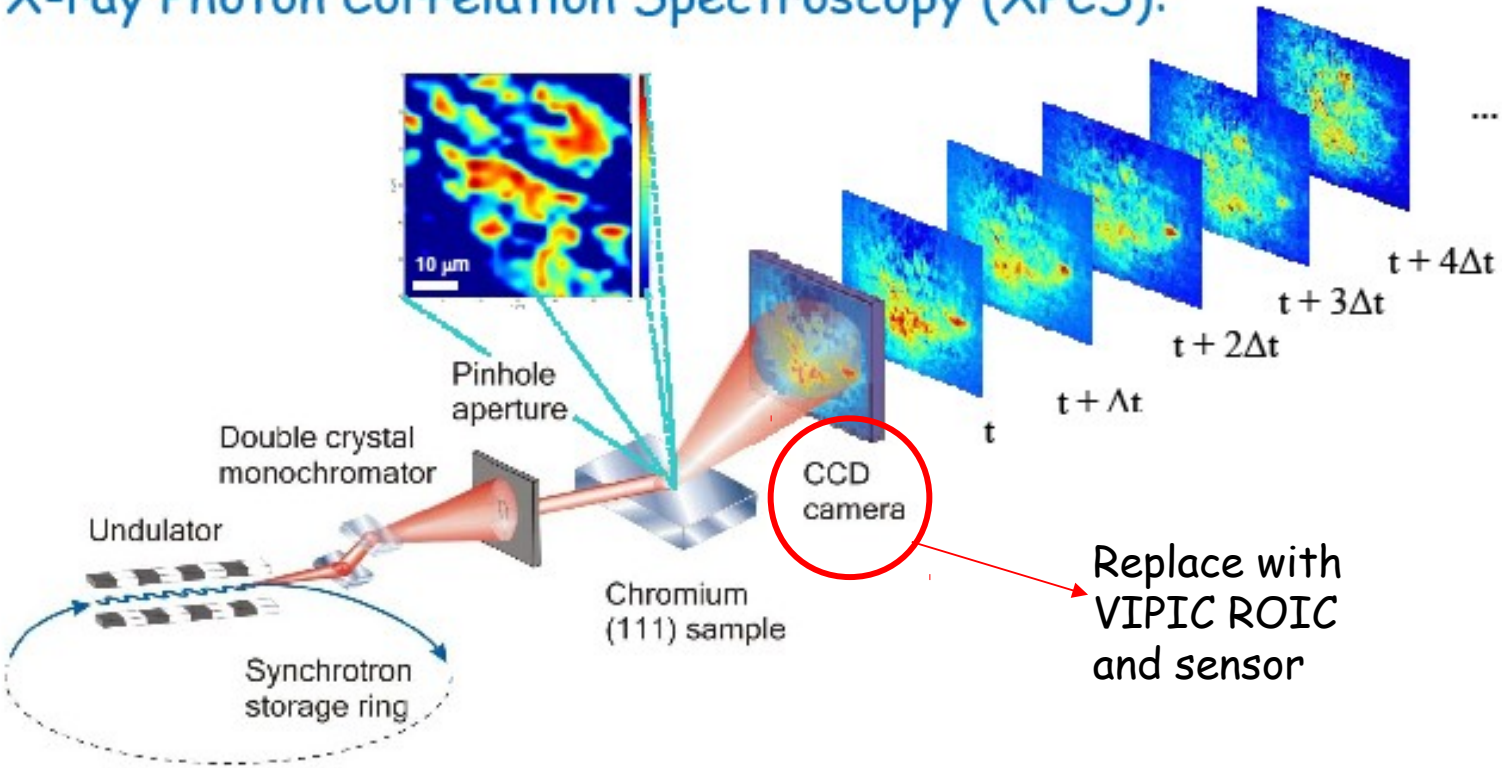


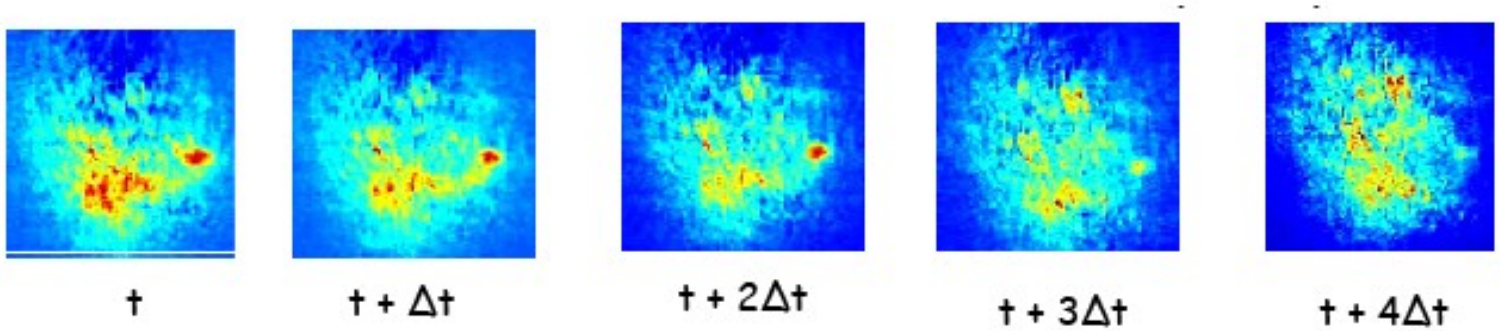


VIPIC

- Custom detector for X-ray correlation spectroscopy
- It's all about timing; the faster the better
- This project pushed the frontiers of semiconductor technology by adopting a method called 3D Integration
  - Three layers stacked atop each other and interconnected
- Collaboration with Fermilab

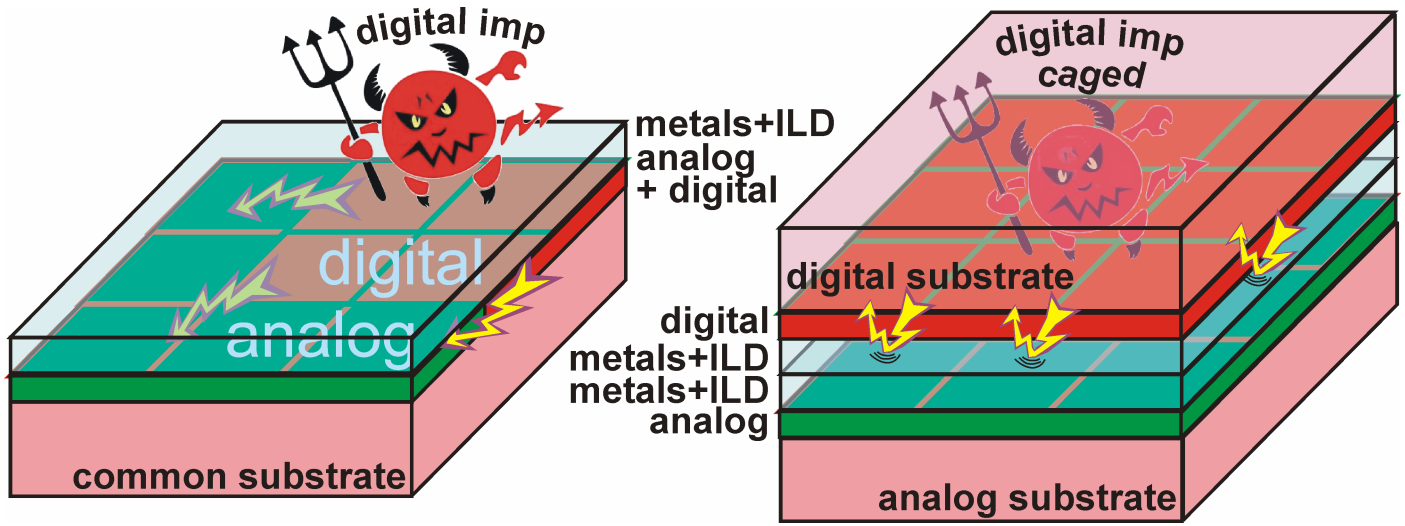
X-ray Photon Correlation Spectroscopy (XPCS):





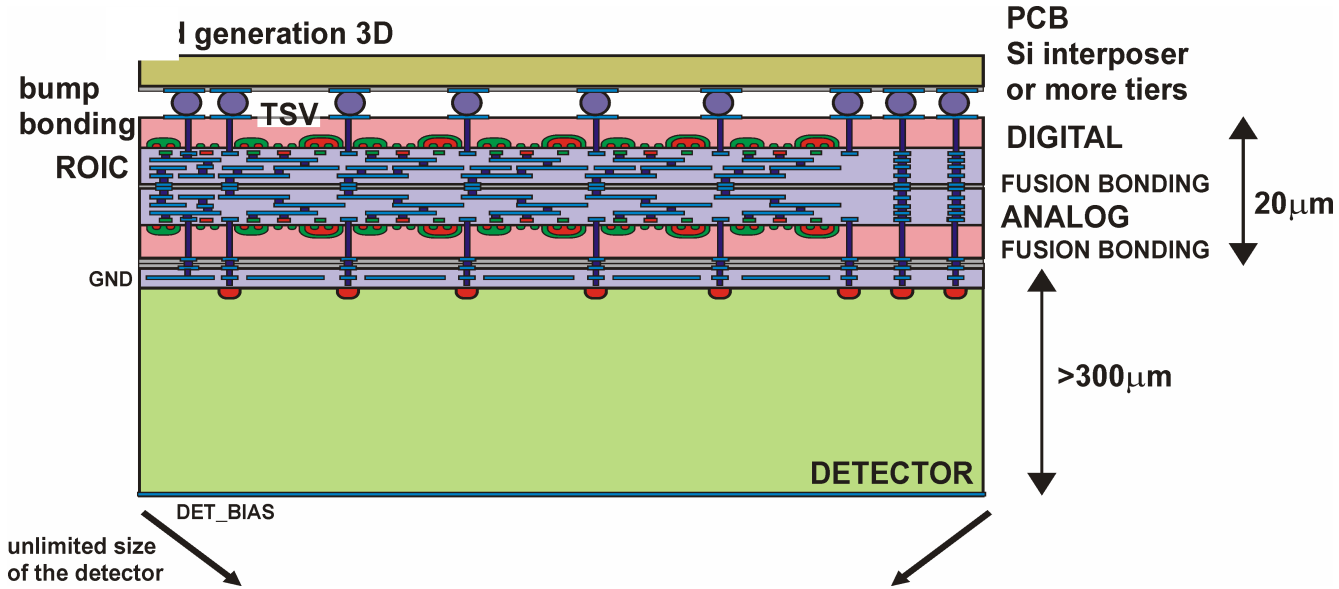
O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

3D integration: What and Why?



- 3D integration refers to the stacking of CMOS circuits in the third dimension as a way to increase device complexity without heroic measures with device feature size.
- Now in production for memory applications, but VIPIC is the first successful mixed-mode design for photon science applications.
- True separation of digital and low-noise analog circuits
  - Allows choice of technology node which is optimal for each function
  - Provides screening of sensitive, low-noise circuits from digital noise
  - Allows easy power distribution to large-area ASICs.

3D opens the door to truly gap-free large-area detectors

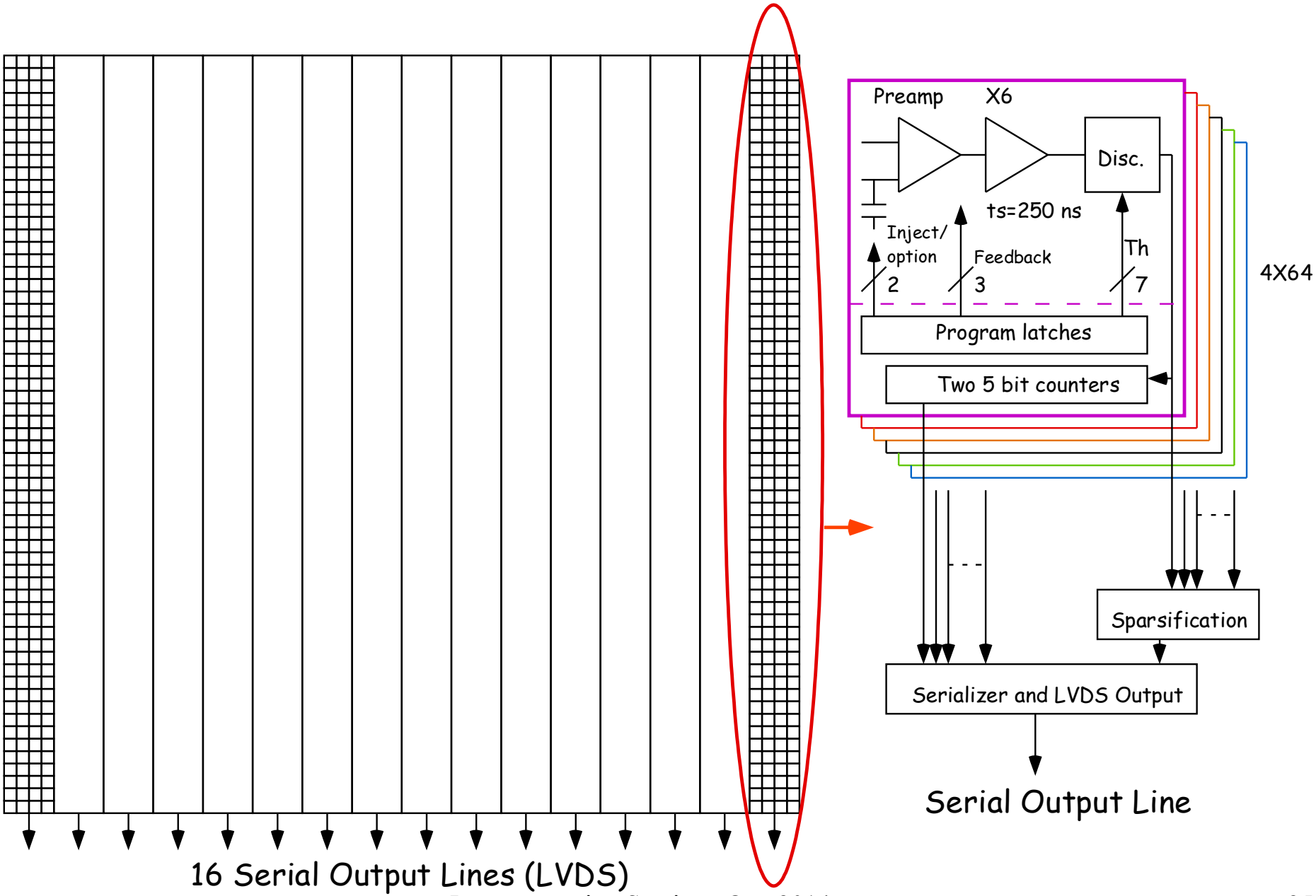


- The availability of Through-Silicon Vias (TSVs) allows direct contact to the circuitry from any point on the device
  - Allows dense interconnection to sensor
  - Allows dense interconnection to outside world
- No need to leave edge-space for wire-bonding and its resulting gap in active area of detector.

VIPIC (Vertically Integrated Photon Imaging Chip)

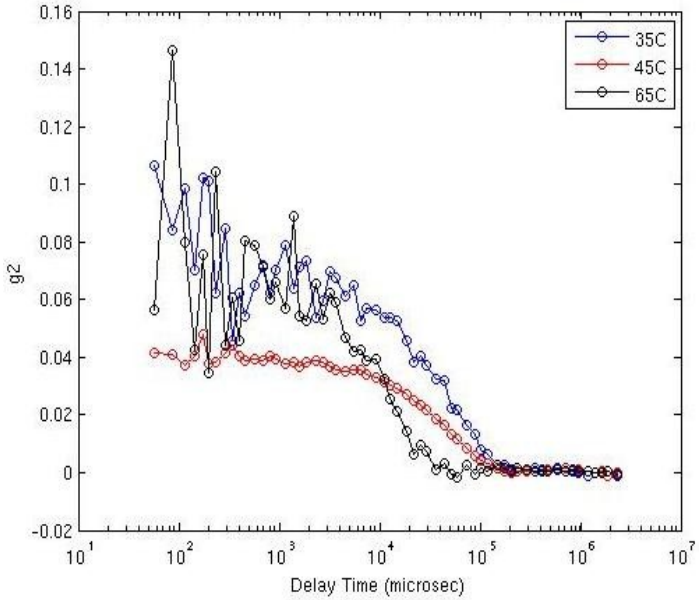
- Specifications
  - 64 x 64 array of 80 micron pixels
  - Dead timeless operation
  - Sparsified data readout
  - Binary readout (no energy information)
  - High speed frame readout time (10 usec min for occupancy ~ 100 photons/cm^2/usec)
  - Optimized for photon energy of 8KeV
  - Triggerless operation
- Features (5.5 x 6.3 mm die size)
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Address generated by circuit without hard coding
  - Constant pixel address readout time (5 ns) regardless of hit pixel location by means of binary tree principle.
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tier readout chip with separate analog and digital sections
  - Adaptable to 4 side buttable X-ray detector arrays

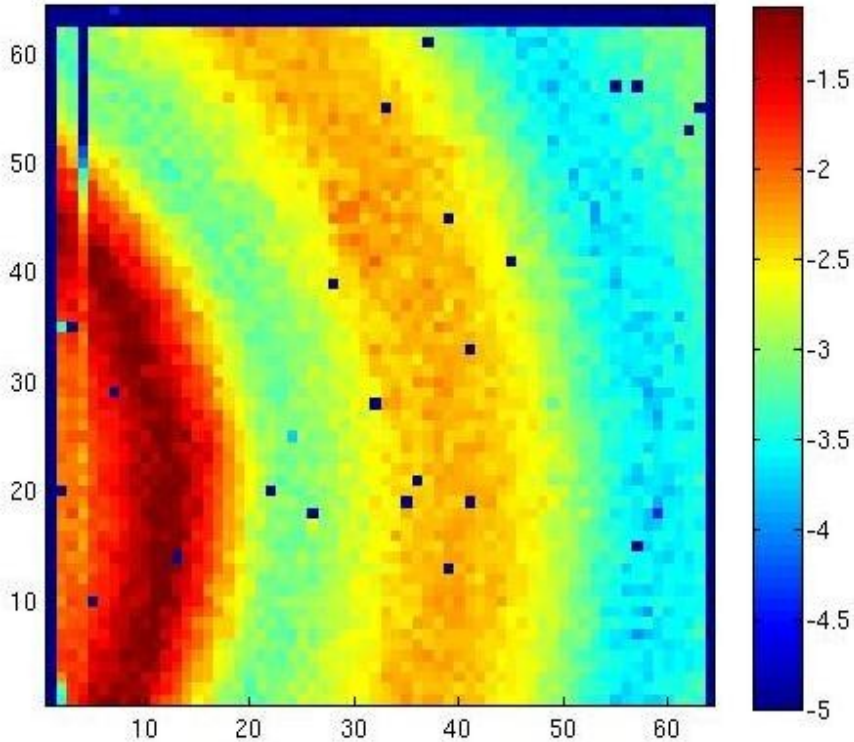
VIPIC Block Diagram



First beam data from chip

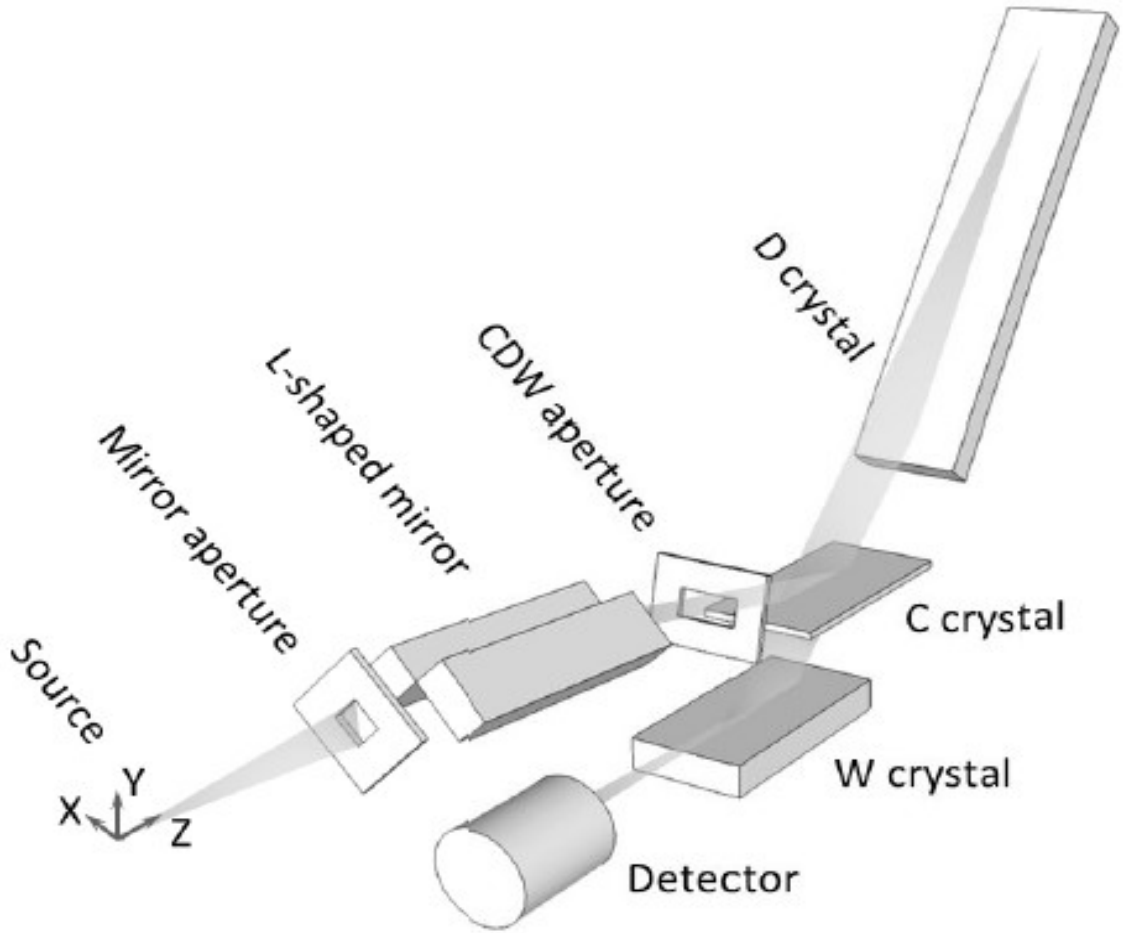
- Still being analyzed
- Small-angle scattering from a latex sample





IXS optical setup

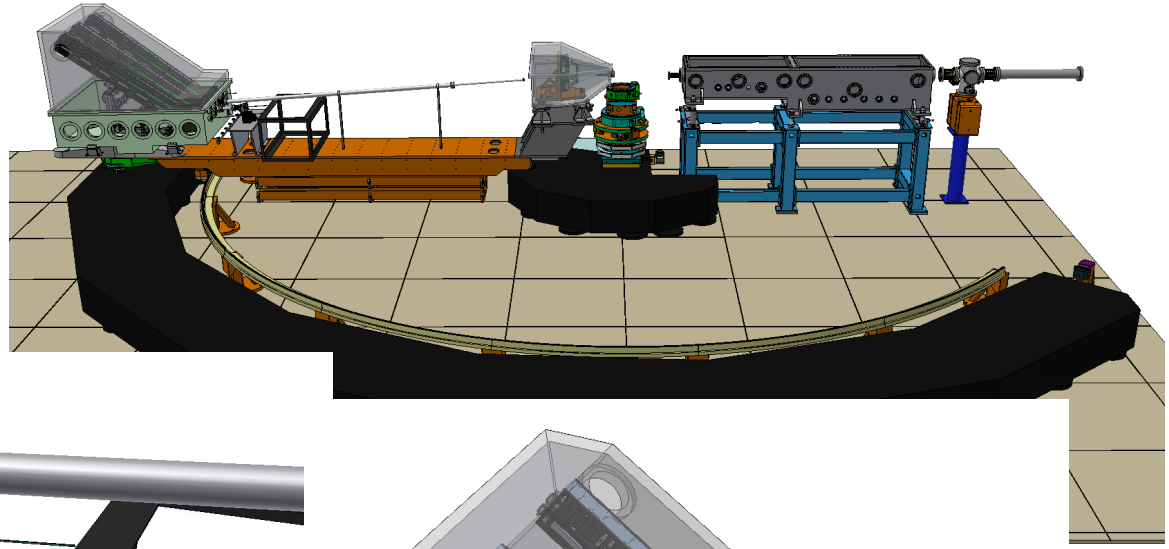
- Based on an idea by Y. Shvydko
- Asymmetric back-reflection adds additional dispersion

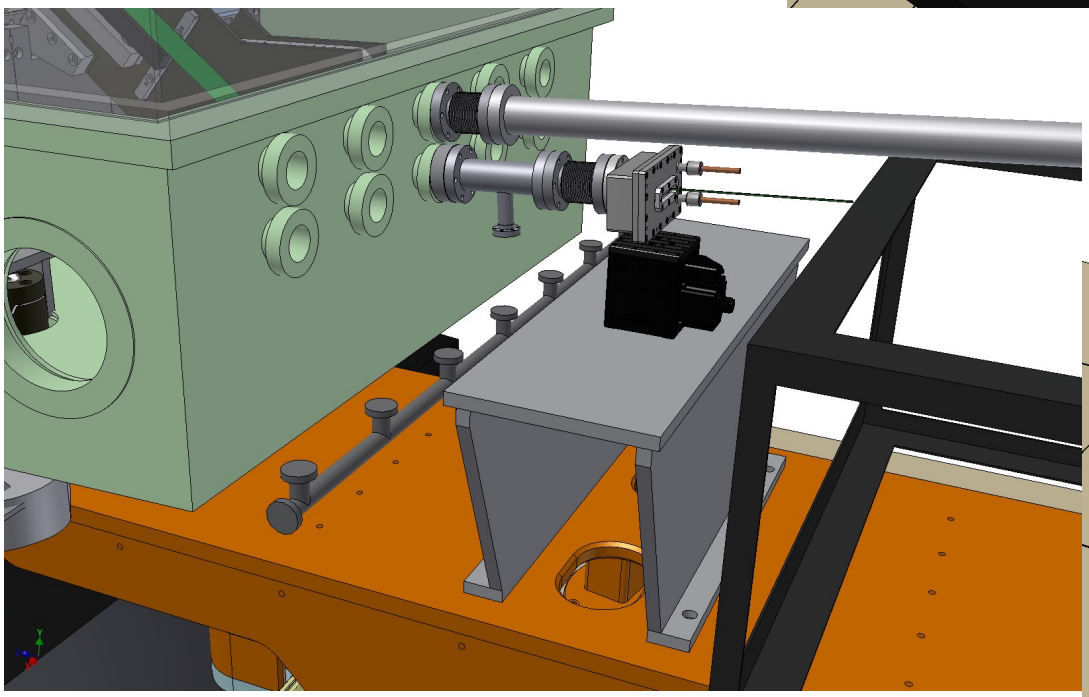


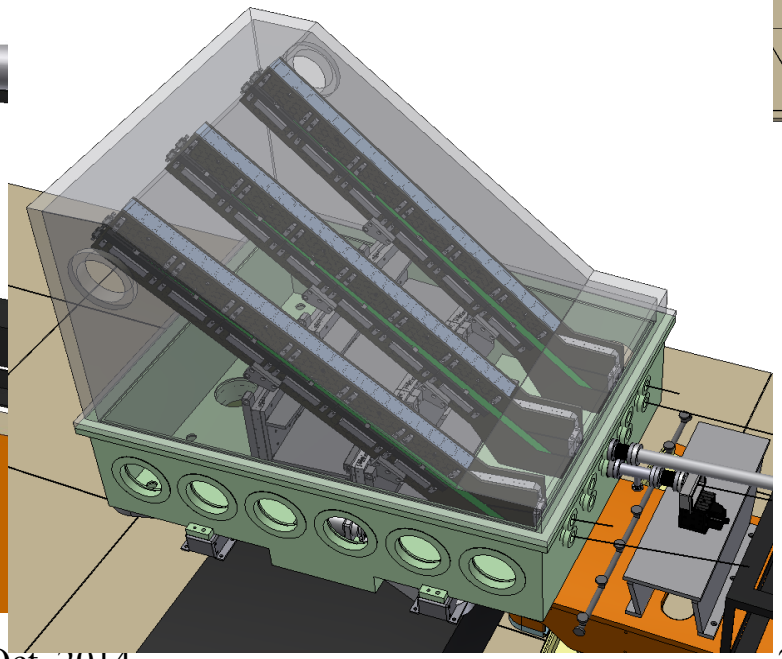
IXS beamline

(Yong Cai)

- Novel optical system for IXS.
- No bent crystals
- < 1mV resolution

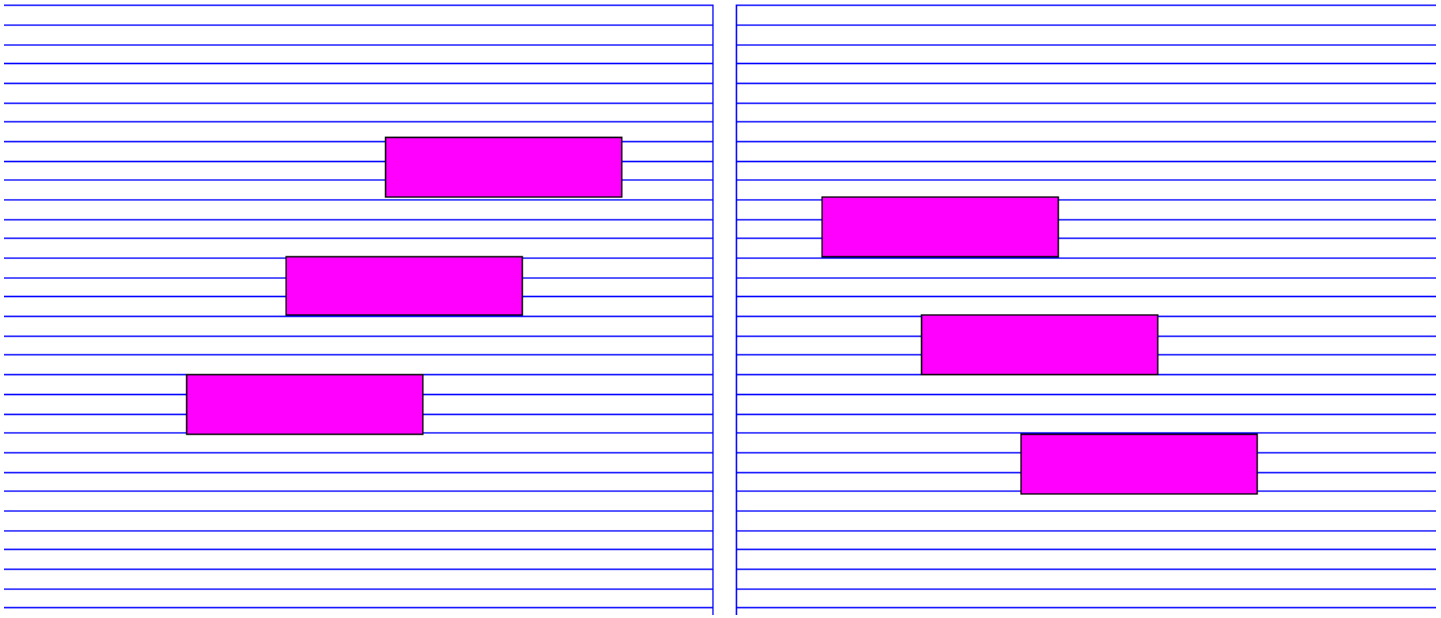






The “Tagma” Detector Concept

The **D** crystal phi angle can be exploited to steer the beam horizontally, with minimal energy shift within 0.5-1.5 mrad, allowing isolation of nominally adjacent beamlets.



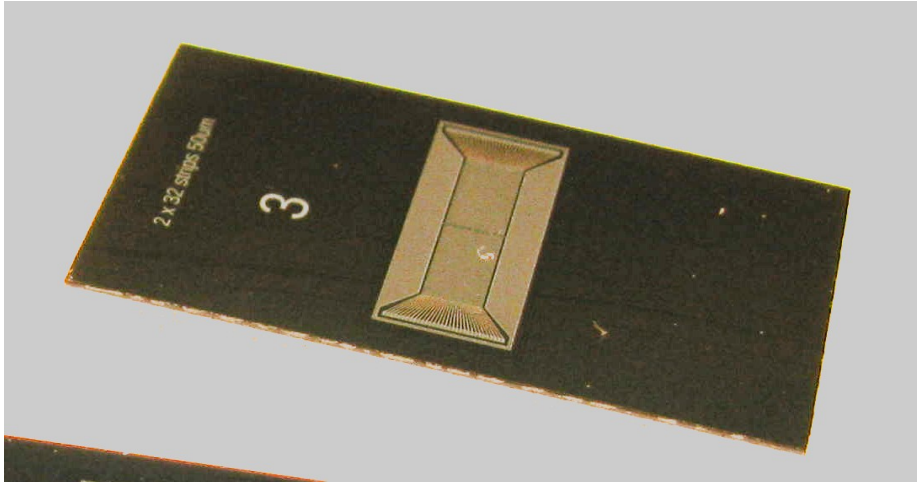
- In biology, a ***tagma*** is a specialized grouping of multiple segments into a coherently functional unit, as in the head, thorax, and abdomen of insects.

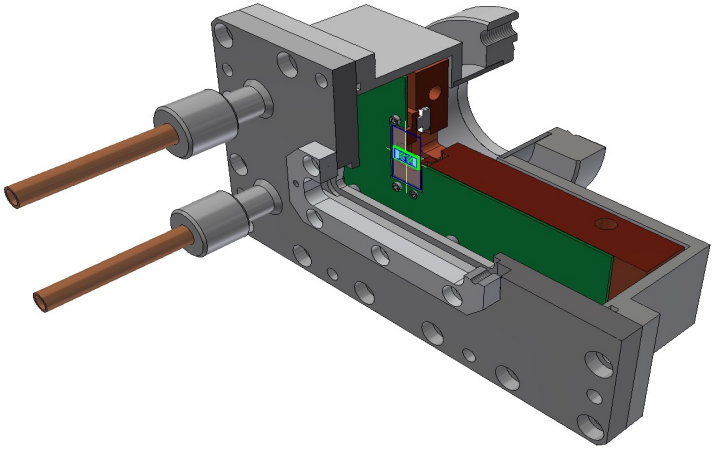
- For the NSLS-II IXS beamline, ***Tagma*** is a detector providing minimally complex segmentation for isolation of multiple beamlets from the D crystals of the dragonfly analyzer.

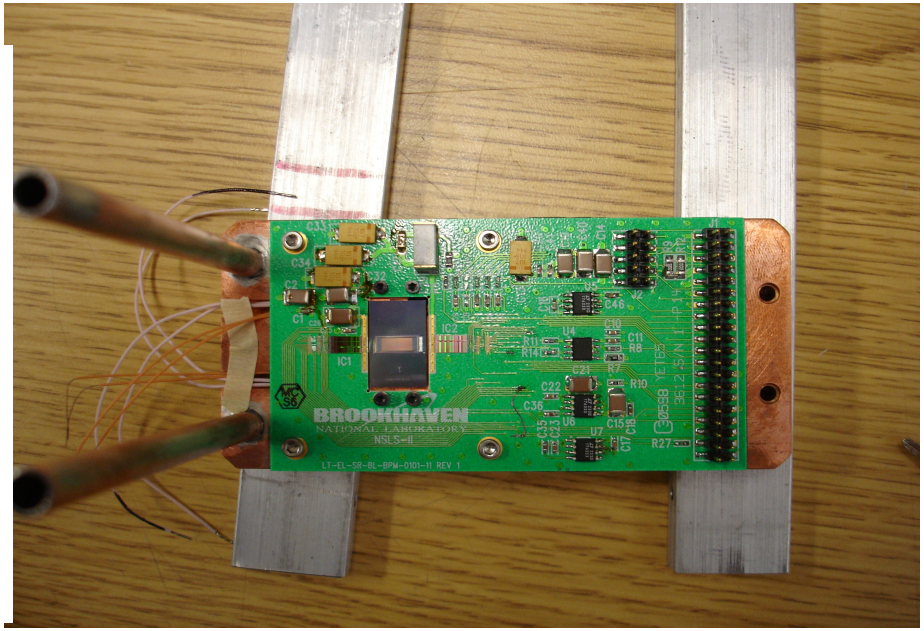
  (“pseudo-2D”; 18 used channels)

IXS microstrip detector

- 32 + 32 strips, 4mm x 80um
- Uses same front-end chip (Hermes) as Maia and BNL x-ray strip detector
- Chip has built-in counters and SCAs





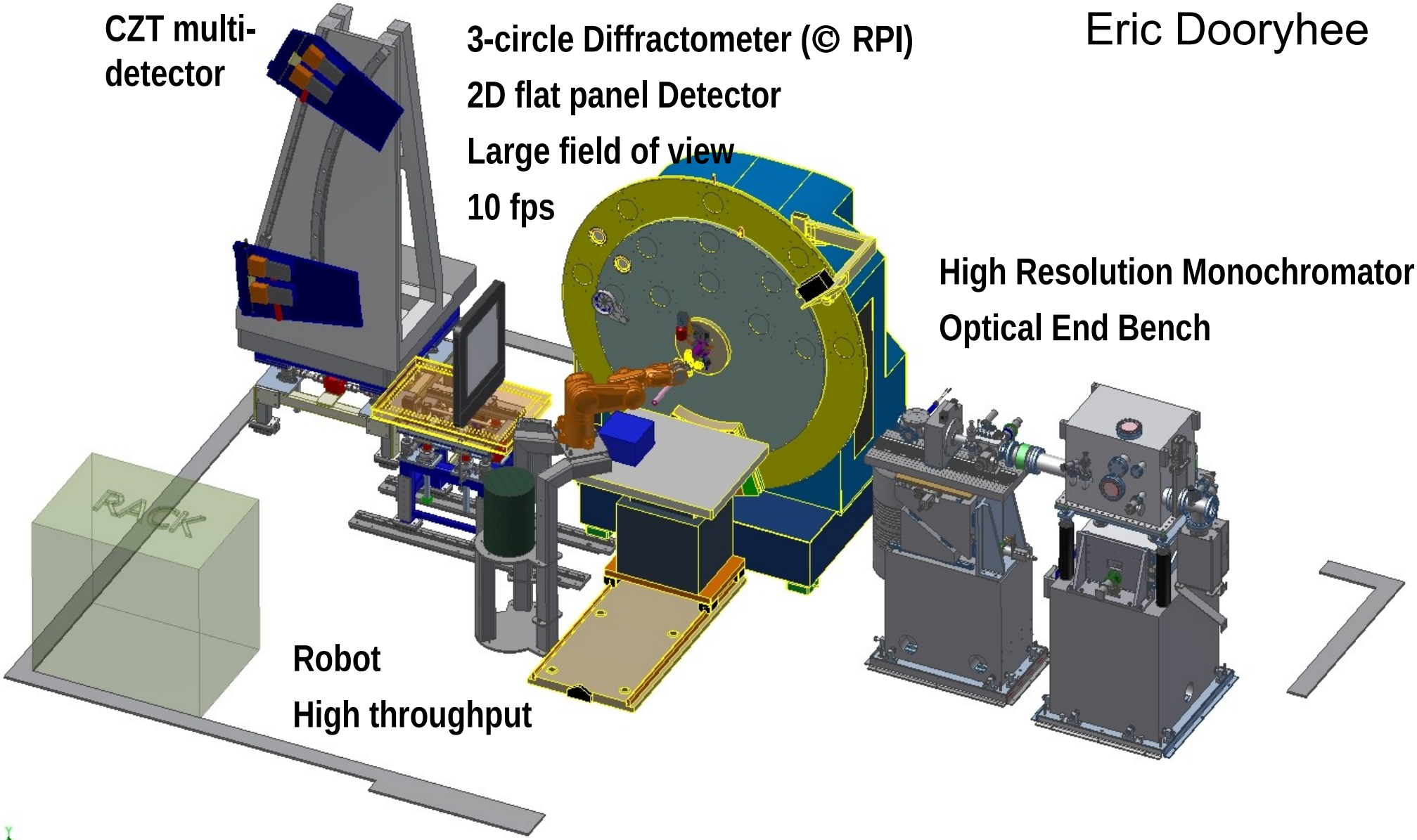


Powder Diffraction

- CZT multi-detector for multi-crystal analyzer
- Scintillation counter array
- Germanium multi-detector for Energy-Dispersive Diffraction
- Germanium microstrip detector for monochromatic diffraction

XPD End Station Day-1 Configuration

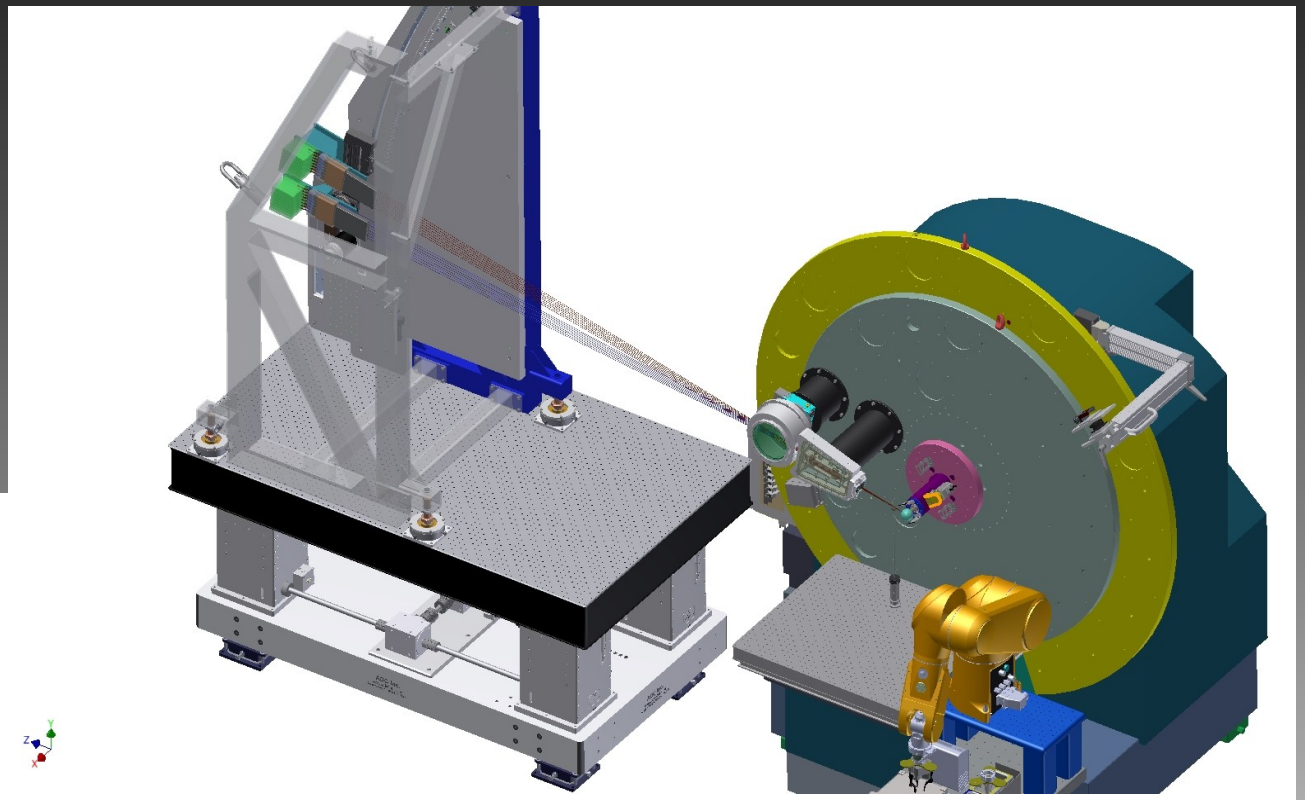
Eric Dooryhee

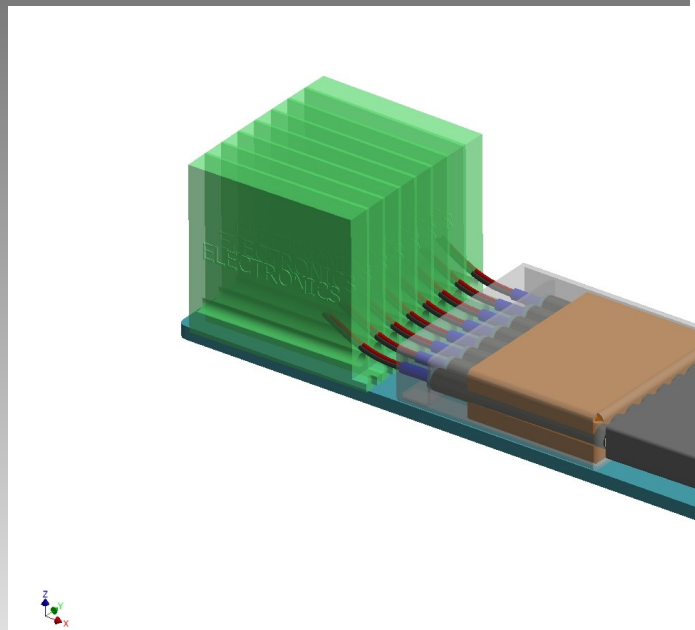


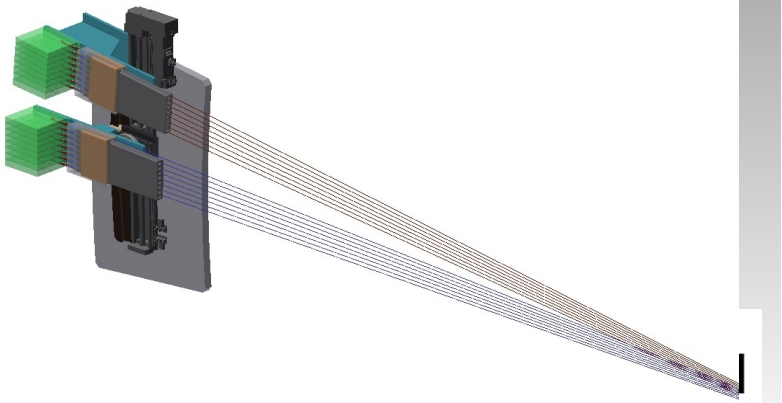
Basic suite of sample environments (flat plate furnace, hot air blower, cryostream)
User custom sample cells

title

- text

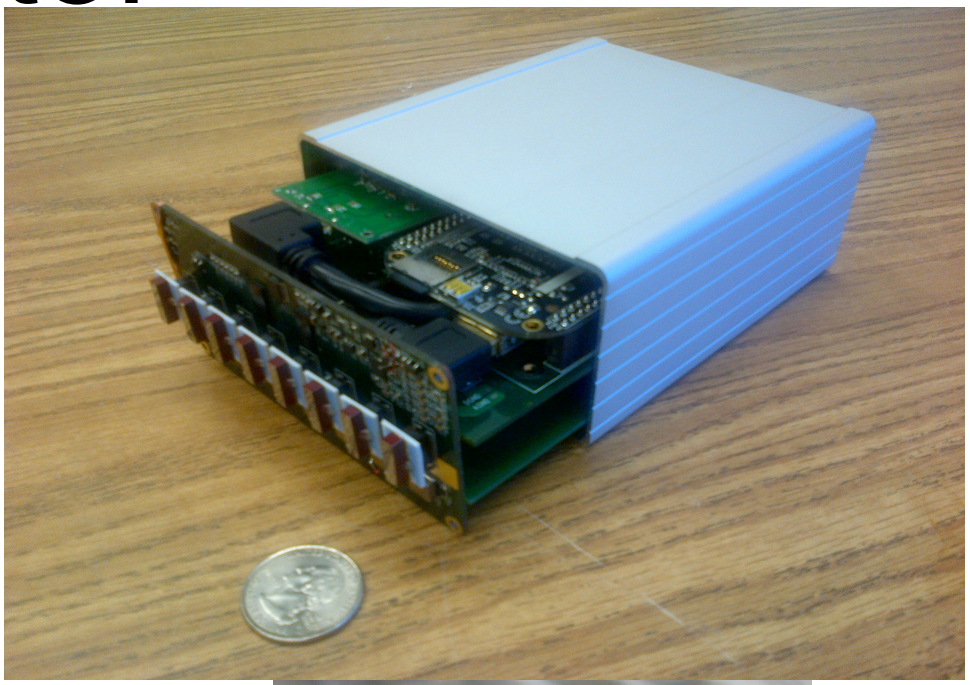




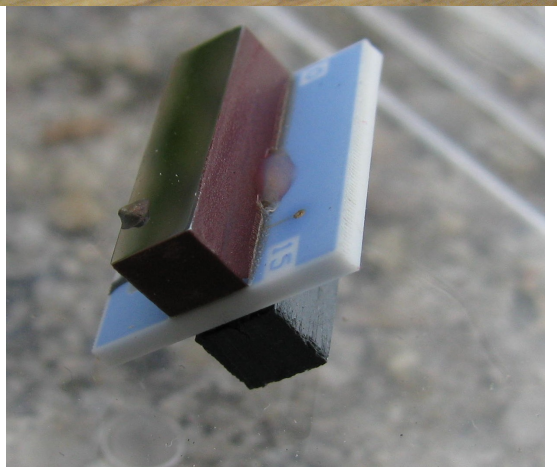


U.S. DEPARTMENT OF ENERGY

XPD high-energy multi-detector



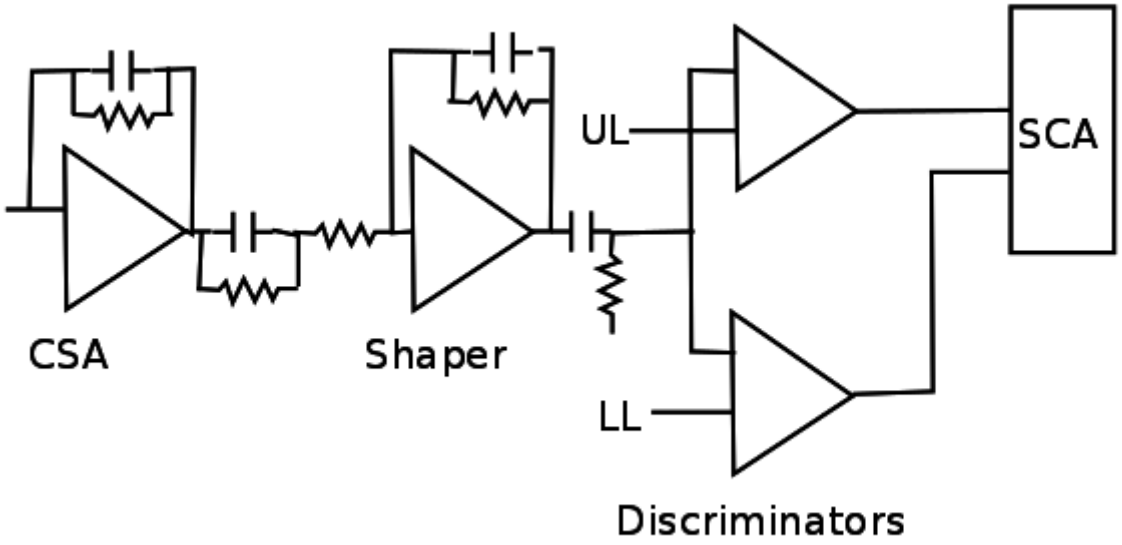
- CZT-based
- Self-contained detector system
- Uses 2 BNL-designed 64-channel readout chips
- Uses commercial CZT sensor
  - 16 strips per sensor
  - 8 sensors
  - 128 channels



Scintillation counter for 50keV x-rays.

- Need fast scintillator
- GYSO seems optimal
  - High density (6.7 g/cm^3)
  - <100ns scintillation decay time
- 1cm diameter x 3mm thick
- Hamamatsu tube

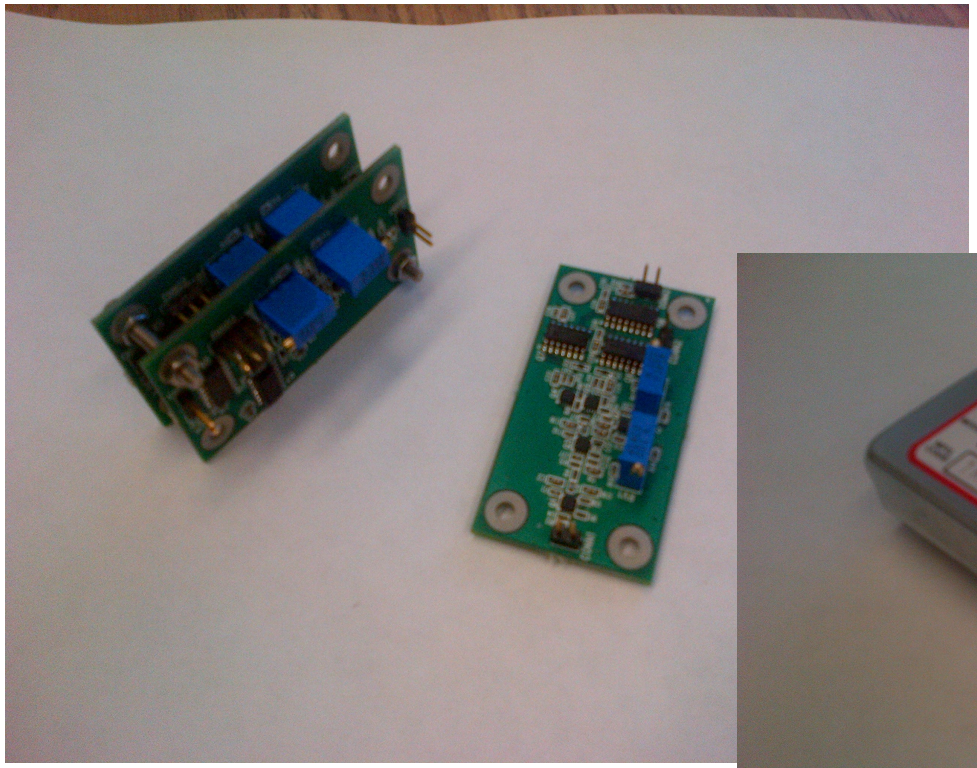
Custom electronics

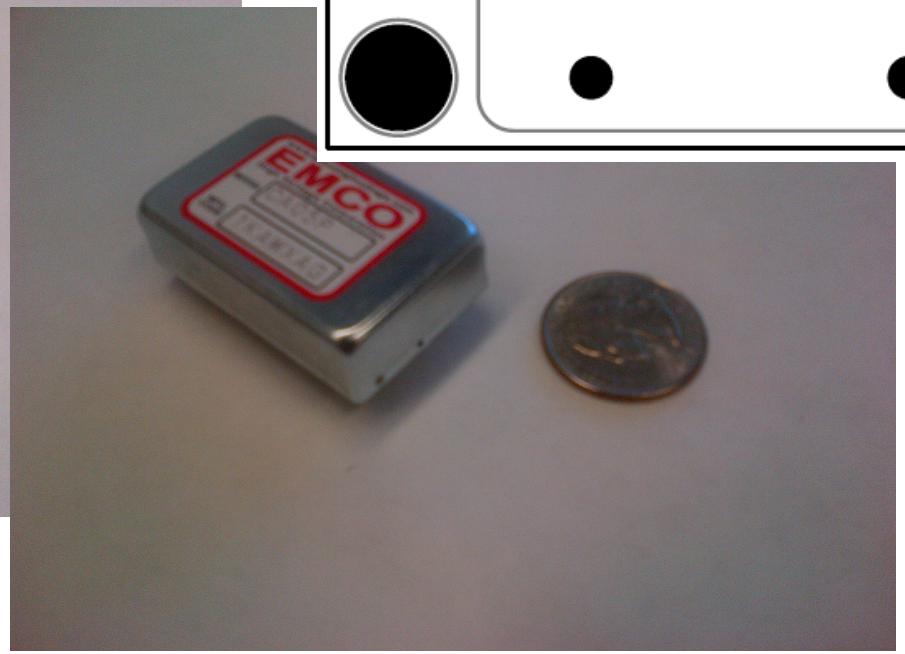


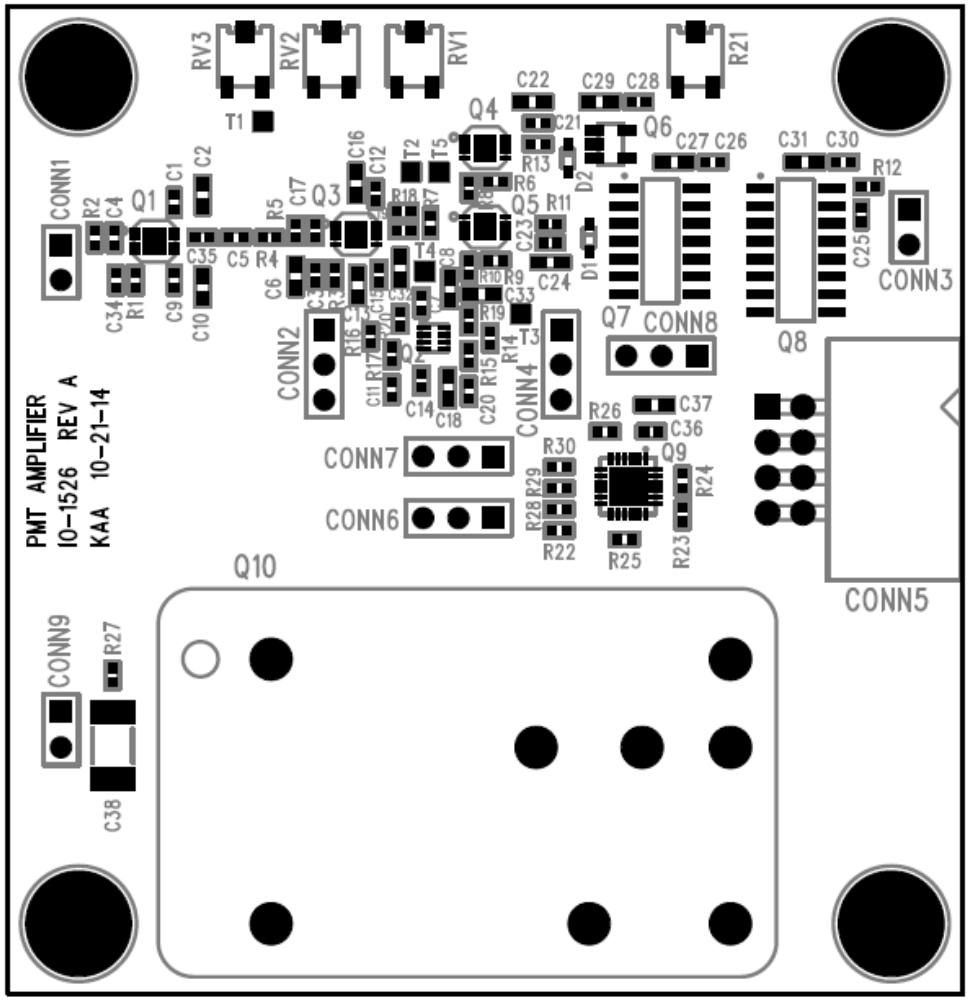
- Conventional chain:
  - Charge-sensitive preamp
  - Shaping amplifier
  - Upper and Lower level discriminators with SCA logic
  - Uses ADA4587 fast op-amp for analog functions

Boards

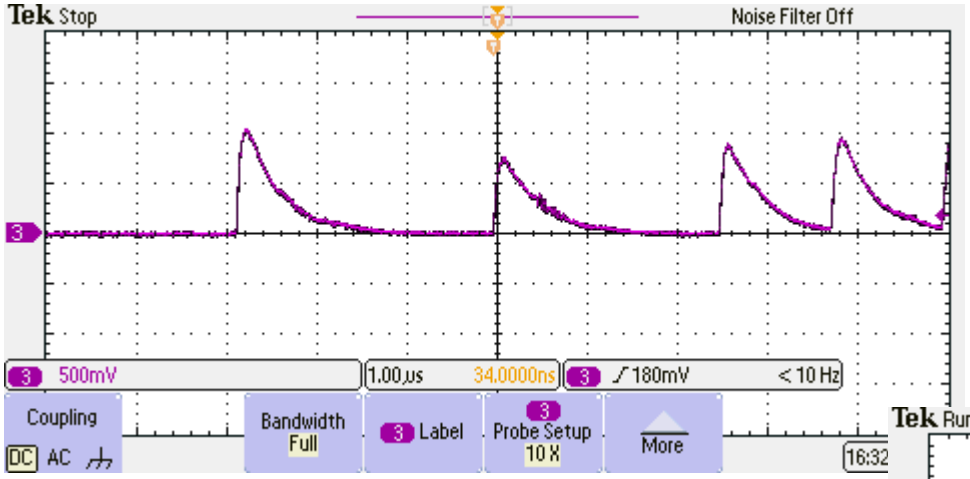
- Prototype board verifies design
- Final design includes HV supply
- Complete scintillation counter electronics in 2” x 2” x 0.75”
- Manual or DAC bias and threshold adjust.

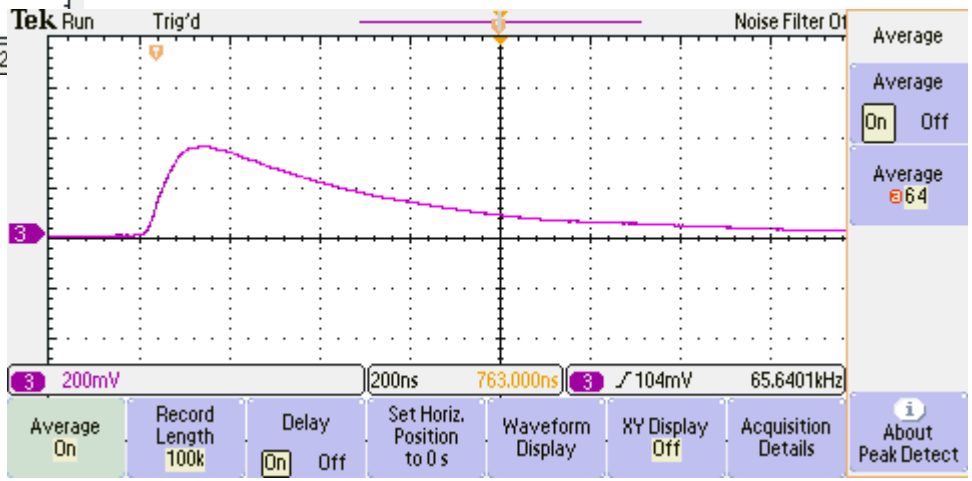






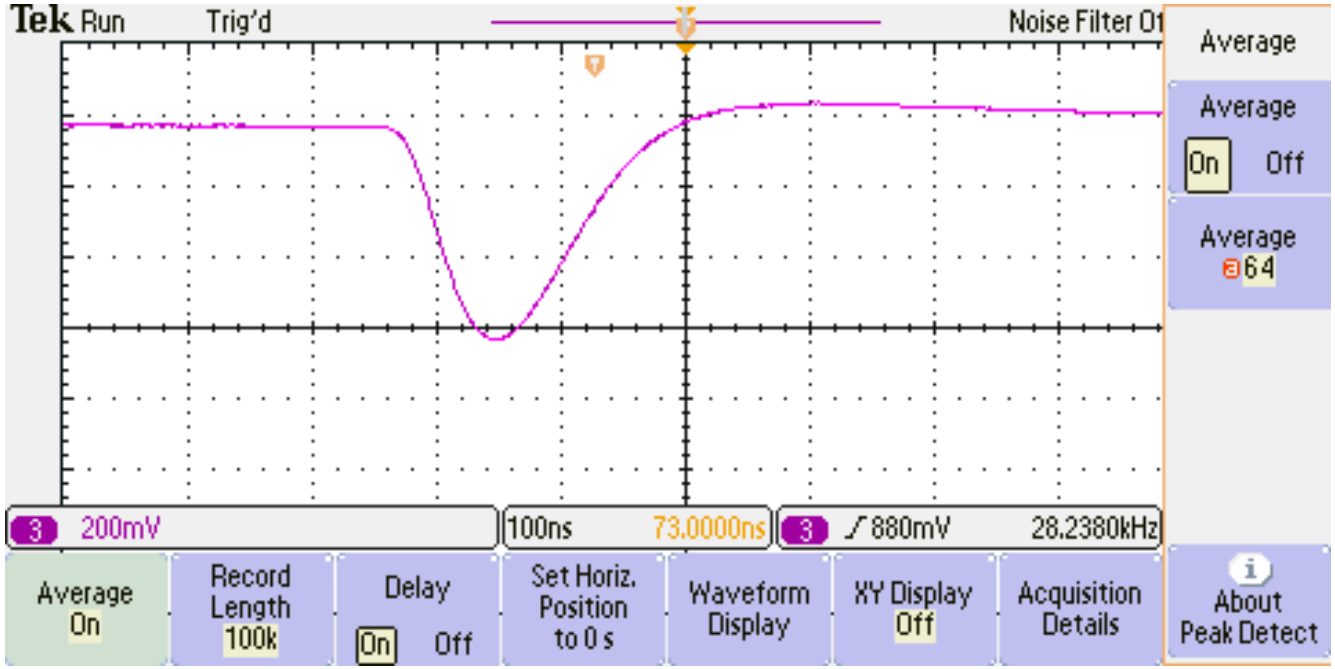
CSA output





- 241 Am source
- ~300kHz

Shaper output



- ~100ns FWHM.
- ~0.6V pulse height @ 700V bias.

Digital Interface

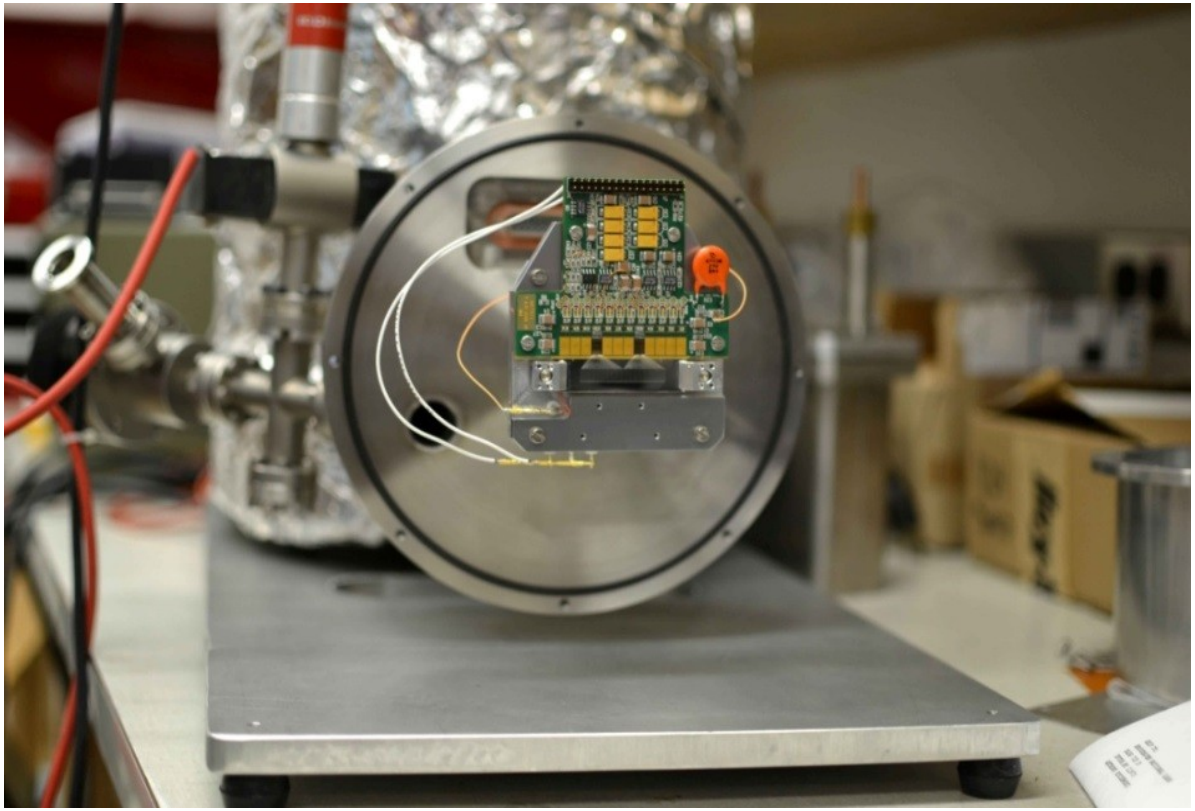
- Digital interface based on MicroZed FPGA board.
- Dual-core Arm processor plus FPGA logic
- Existing logic designs for 32-bit counter.
- Implement two banks of eight, to allow dead-time-free counting.
- Linux system installed on Arm processors
- Built-in Ethernet interface.

Germanium detectors

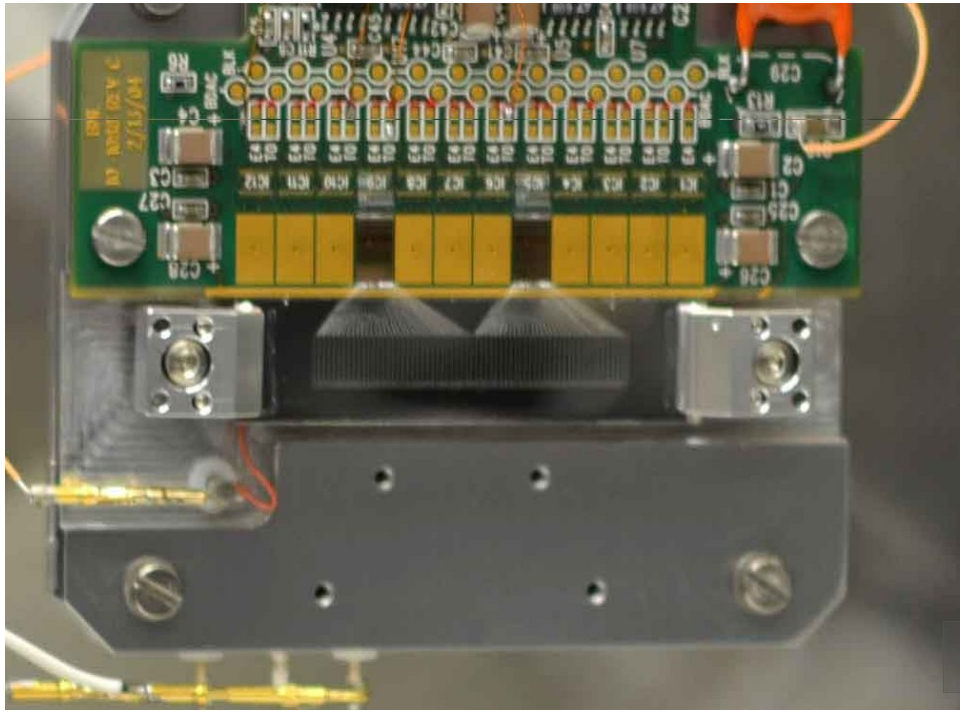
- Efficient at high photon energies
- Spectroscopic quality material
  - Energy-dispersive diffraction
  - Low-noise position-sensitive detectors
- Collaboration with Semikon Detectors GmbH

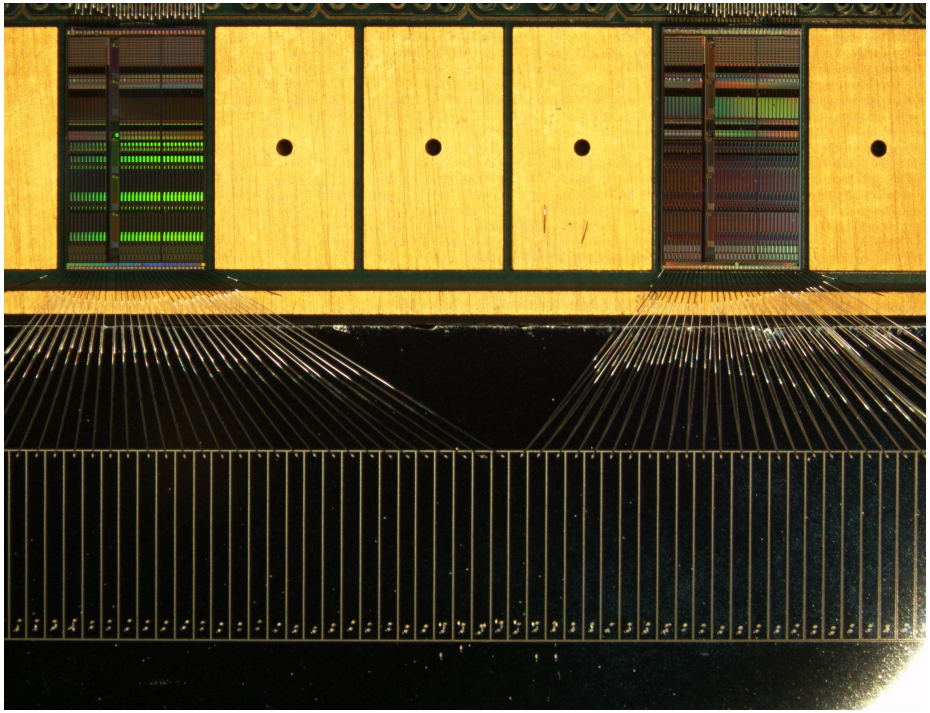
EDX multi-element Prototype

- Try to re-use as much as possible to provide a test vehicle quickly and economically
- 64 detectors, each 0.5mm x 5mm
- Two HERMES chips mounted on a modified existing board, with some creative wirebonding
- Mounted in an existing LN2 cryostat with a large volume cold-finger housing.



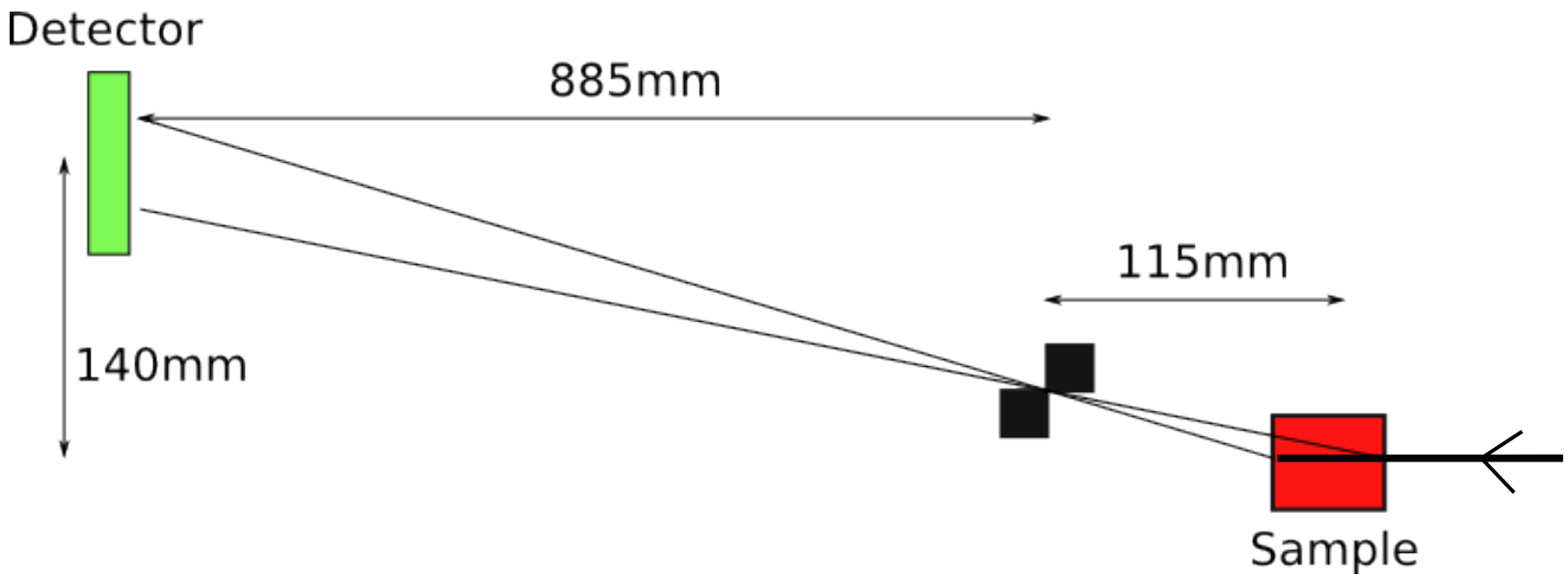
Electronics





- PCB holding 2 ASICs mounted on the cold plate, showing the 64 wirebonds connecting the sensor strips to the ASICs.
- The PCB is mounted on thermally-insulating standoffs, allowing its temperature to float to around 223K (-50C). The sensor settles at around 100K with the electronics under power.

Diffraction sectioning: experimental setup



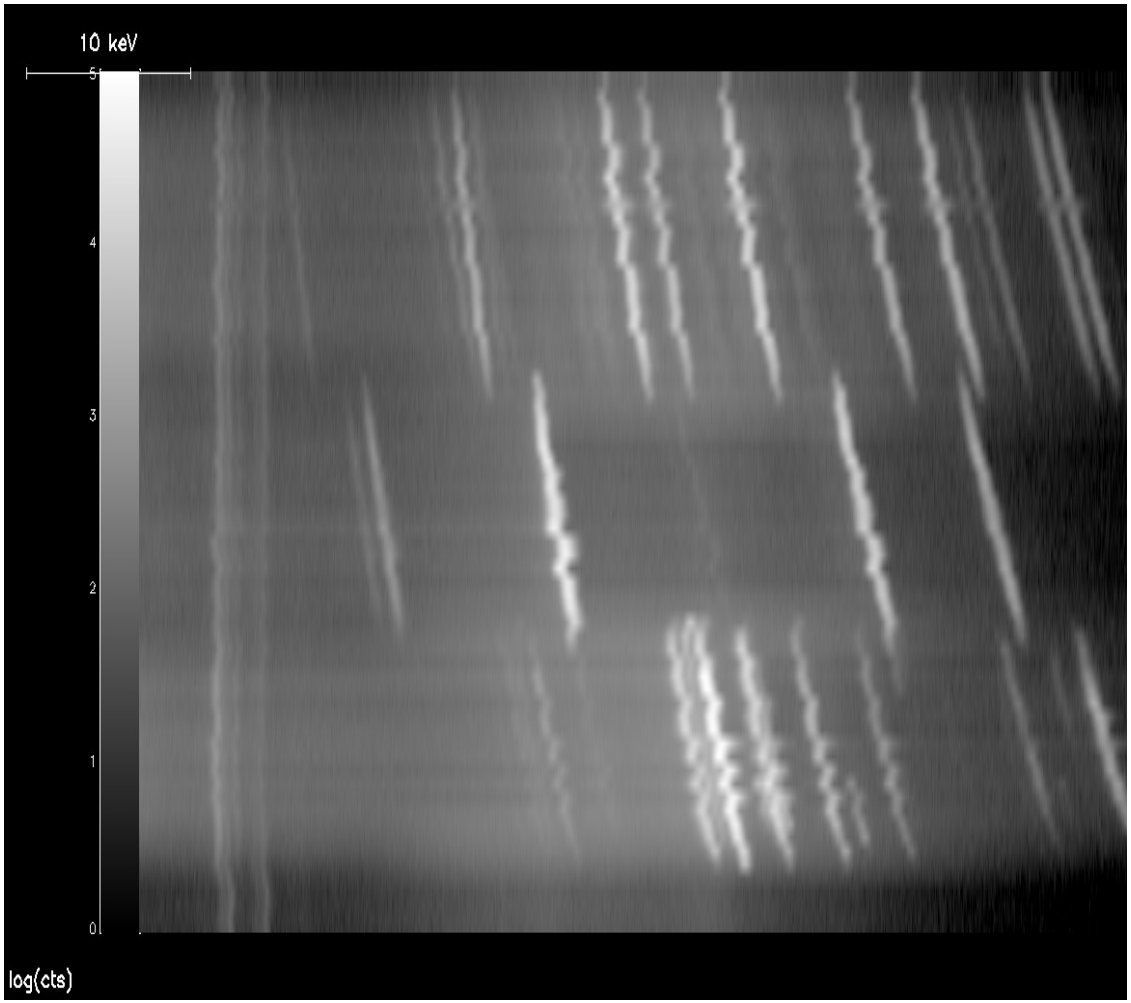
- 100um white beam enters from right
- Slit projects scattered beams onto strip detector
- Each detector element collects spectra (i.e. diffraction pattern) from one region of sample.

Test Sample

- Three low-Z samples in cuvettes with two thicknesses
  - ~1 cm
  - ~5 mm

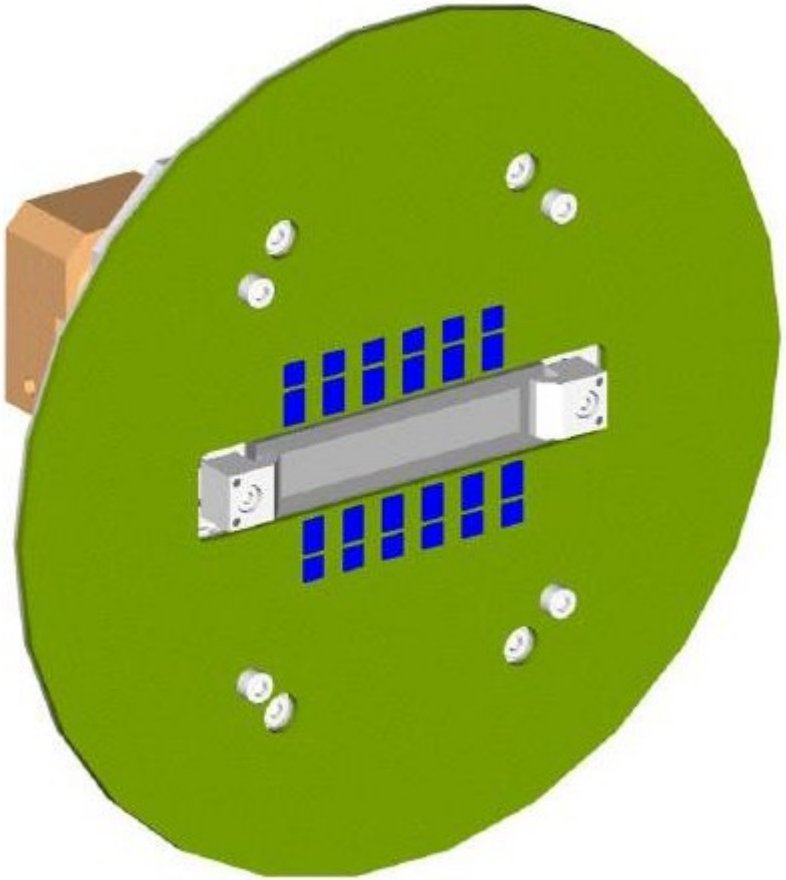
Test sample

- We only had access to a bending-magnet beamline for these measurements, limiting us to an energy range of <70keV.
- We made a test sample consisting of three low-Z compounds, SiC, Si and Al2O3.
- The three ~1cm sections can clearly be seen in the plot.



Ge Microstrip detector

- Currently under construction
- Collaboration with Argonne
- 384 detectors
  - 8mm x 0.125mm
  - Read out using modified Maia electronics

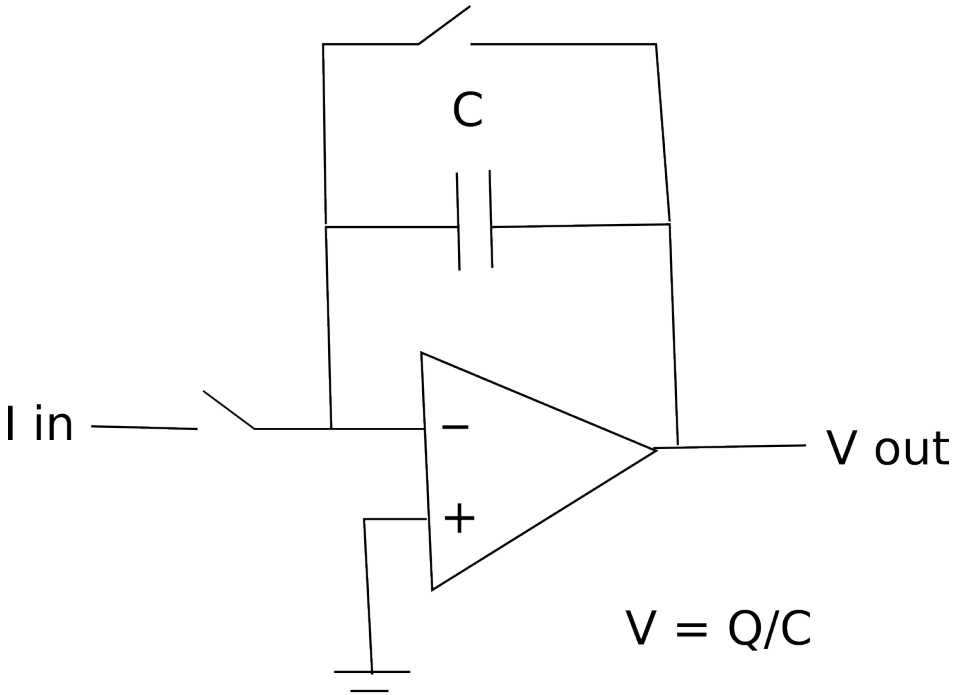


Quad low-current readout

- Many years ago, my group designed a 4-channel V-F converter with LED display (significantly pre-EPICS).
- We made many of them, and gave the design to a couple of companies; you can still buy them.
- The classic low-current signal path was:
  - Keithley electrometer
  - V-F converter
  - Counter
  - Computer.
- I always thought this was a dumb way to do it, so when I came across a chip specifically designed for low-current measurements I asked Rich Michta to build something based on it.

Charge Integrator

- Operational amplifier in “virtual ground” configuration forces inputs to same potential.
- Current on input is integrated on capacitor
- V = I.t / C
- Small capacitor and / or long integration time → high sensitivity.

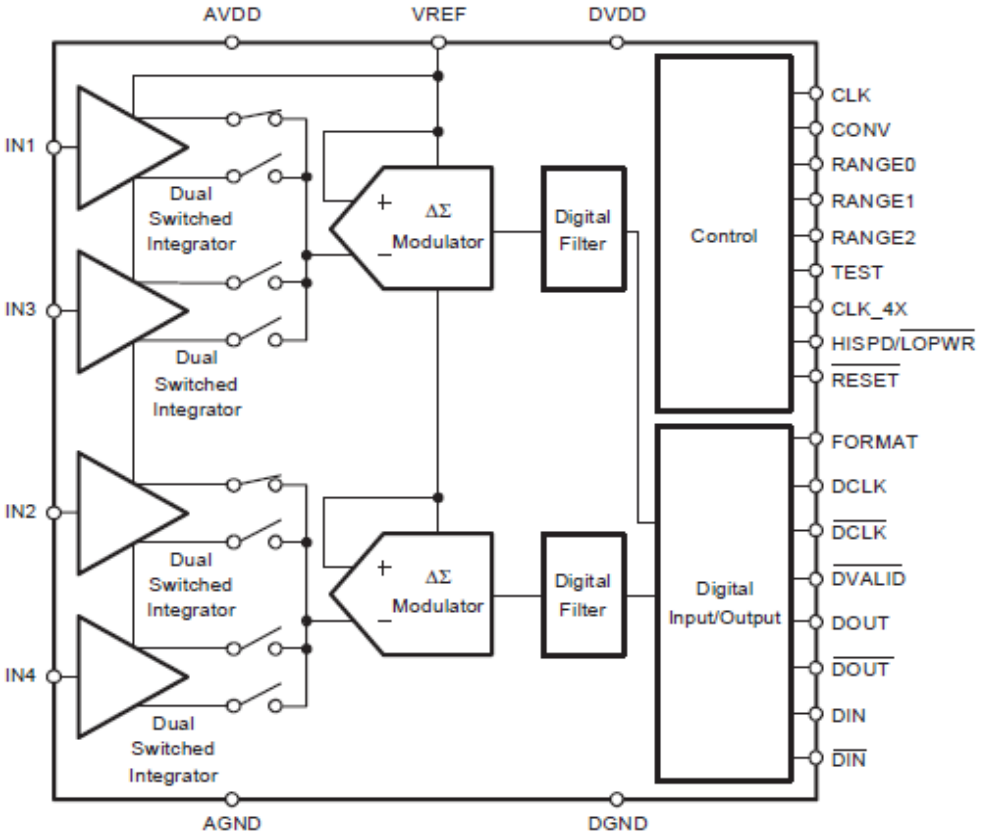


V = Q/C

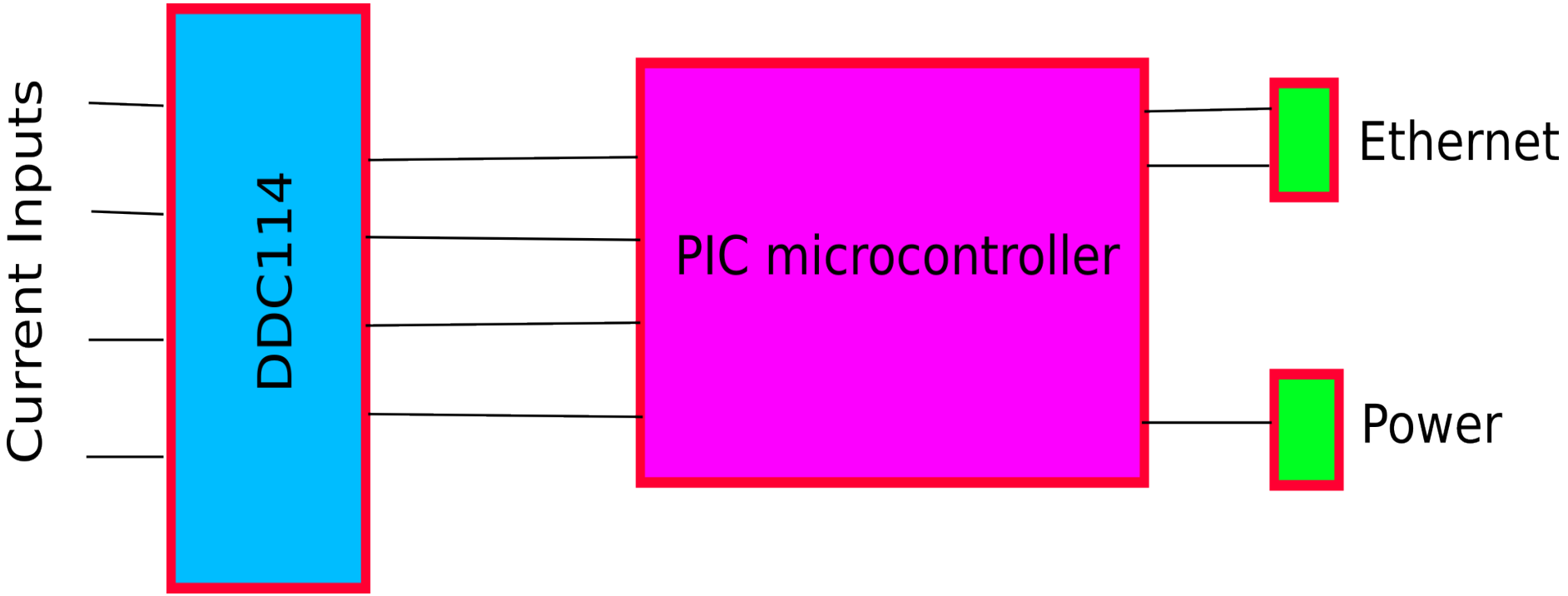
Q = I.t

DDC114

- FEATURES
  - SINGLE-CHIP SOLUTION TO DIRECTLY MEASURE FOUR LOW-LEVEL CURRENTS
  - HIGH PRECISION, TRUE INTEGRATING FUNCTION
  - INTEGRAL LINEARITY:
  - ±0.01% of Reading ±0.5ppm of FSR
  - VERY LOW NOISE: 5.2ppm of FSR
  - LOW POWER: 13.5mW/channel
  - ADJUSTABLE DATA RATE: Up to 3.125kSPS
  - PROGRAMMABLE FULL SCALE



Black box contents



- Our module consists of a PCB to hold the DDC114 chip and it's associated services, plus a connector for a commercial microcontroller module from the PIC family, which provides chip control and Ethernet capability.

The end result

- 4 input connectors
  - Max input ~800nA
  - Positive input only
- Ethernet
- Power (9V adapter)
- ASCII protocol via TCPIP sockets
- Available soft EPICS IOC

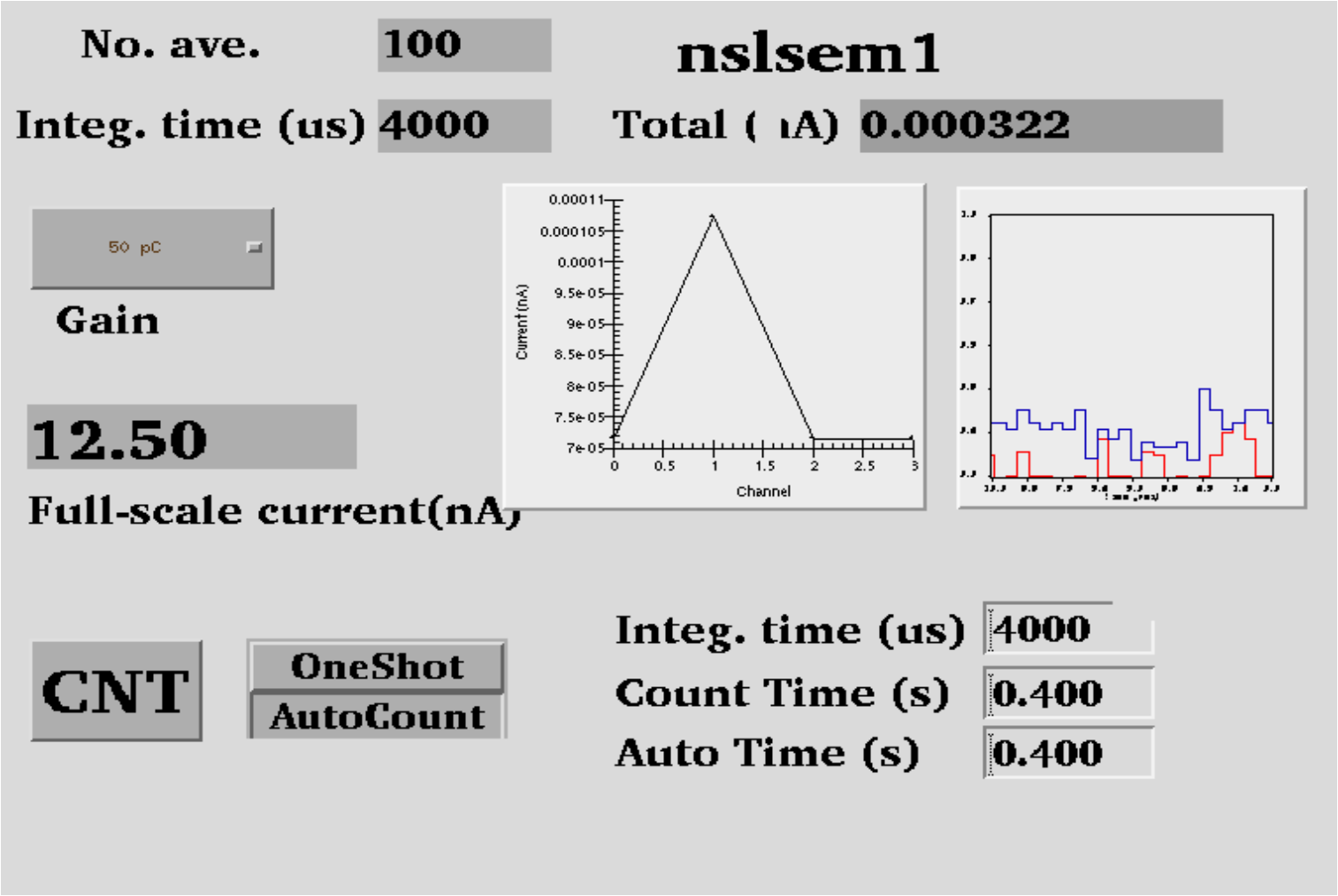
Simple ASCII protocol

- Communication with the device is via TCP/IP sockets.
  - An input stream which sends function controls to the device
  - An output stream sending out data
- Data can be output continuously, or following a software trigger
- Maximum output rate is 2,500 samples / sec using this interface.
- Device can average multiple samples
- Output is raw ADC counts, ASCII, four values per line.
- Operation is not intuitive

Soft IOC controls

- Based on SynApps Scaler record
- More complicated than scaler because:
  - Sensitivity depends on integration time and integration capacitor
  - Need to choose both sensitivity and effective acquisition time
    - Ability to average many readings to decrease noise
- IOC also converts raw ADC counts to Amps
- Calculates (A-B)/(A+B) for two pairs to form simple 2-D BPM.

Screenshots



- Example of MEDM screen for electrometer.

Summary

- Many thanks to all of our collaborators
- NSLS-II will keep us busy for the foreseeable future
- Even simple devices, made to fit, can significantly ease the life of a beamline scientist!