Scientific Detector Workshop

Florence Oct. 7-11, 2013

FOCAL PLANE ELECTRONICS SESSIONS

P. O'Connor
Instrumentation Division Seminar
Nov. 13, 2013

The Scientific Detector Workshop

7-11 October 2013
Florence, Italy
SDW 2013

- **5-day workshops held every 3-4 years**
  - *"These 5-day workshops gather the world experts in the field of detectors for astronomy and **are filled with lively discussions and debates** during oral and poster sessions and interactive roundtables. The discussions continue during informal interactions promoted by the social and cultural events that take advantage of the features of the workshop location.**The workshop formula is tailored to keep the atmosphere informal** and conducive to the exchange of information and the establishment of long-lasting relationships and collaborations."*
  - *Hawaii 1996*
  - *Cozumel 1999*
  - *Taormina 2002*
  - *Garching 2009*
  - *Florence 2013*
- **Topics:**
  - *Status and plans for astronomical facilities and instrumentation (ground & space)*
  - *Earth and Planetary Science missions and instrumentation*
  - *Laboratory instrumentation (physical chemistry, synchrotrons, etc.)*
  - *Detector materials (from Si and HgCdTe to strained layer superlattices)*
  - *Sensor architectures – CCD, monolithic CMOS, hybrid CMOS*
  - ***Sensor electronics***
  - *Sensor packaging and mosaics*
  - *Sensor testing and characterization*

http://www.inst.bnl.gov/~poc/SDW

Focal plane electronics sessions

- **New Generation IV Controllers for CCD and CMOS Arrays -** *Bob Leach, SDSU*
- **A Compact, Low Power Digital CDS CCD Readout System[1] -** *Armin Karcher, LBNL*
- **LSST ASICs for Sensors Control and Readout[2]** *- Herve Lebbolo, LPNHE*
- **Prototype ASIC for Space Large Format NIR/SWIR Detector Array[2,3,4]** *Benoit Dupont, ESA*
- **Lessons Learned from a Decade of SIDECAR ASIC Applications[2,3,4]** *Marcus Loose, Markury Scientific*
- **In Situ Testing of CCD and NIR Detector Controllers** *Roger Smith, Caltech*
- **Control System for EUCLID-NNISP Mission Infrared Focal Plane[3,4]** *Favio Bortoletto, INAF Padova*
- **System Tests of LSST Integrated Readout Chain** *Paul O'Connor, BNL*
- **Theoretical Comparison of CCD Video Processors[1]** *Simon Tulloch, Univ. Sheffield*
- **Roundtable: Digital Correlated Double Sampling, ASICs**
- **+ 11 posters**

Themes:

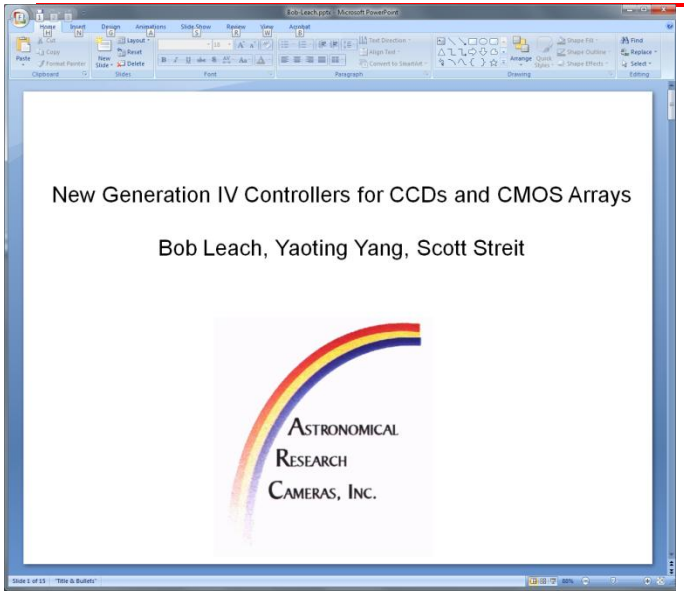
[1]Digital Correlated Double Sampling

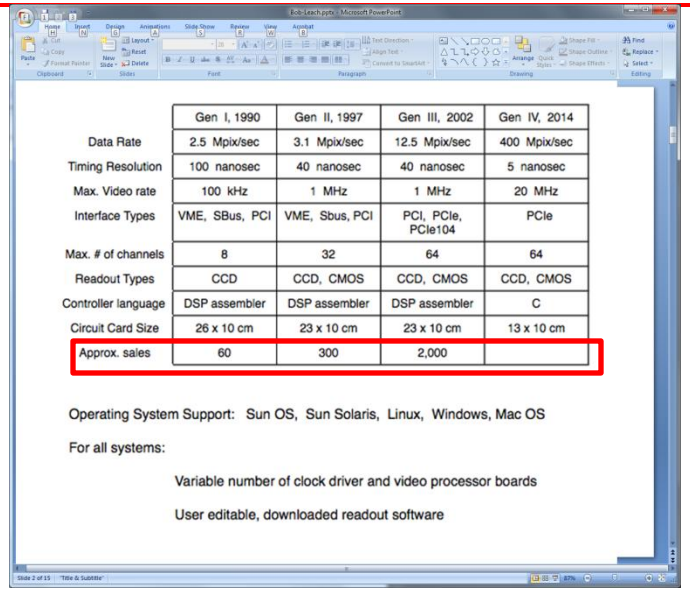
[2]ASIC

[3]Hybrid CMOS

[4]Space

Bob Leach – Gen IV controller





	Gen I, 1990	Gen II, 1997	Gen III, 2002	Gen IV, 2014
Data Rate	2.5 Mpix/sec	3.1 Mpix/sec	12.5 Mpix/sec	400 Mpix/sec
Timing Resolution	100 nanosec	40 nanosec	40 nanosec	5 nanosec
Max. Video rate	100 kHz	1 MHz	1 MHz	20 MHz
Interface Types	VME, SBus, PCI	VME, Sbus, PCI	PCI, PCIe, PCIe104	PCIe
Max. # of channels	8	32	64	64
Readout Types	CCD	CCD, CMOS	CCD, CMOS	CCD, CMOS
Controller language	DSP assembler	DSP assembler	DSP assembler	C
Circuit Card Size	26 x 10 cm	23 x 10 cm	23 x 10 cm	13 x 10 cm
Approx. sales	60	300	2,000	

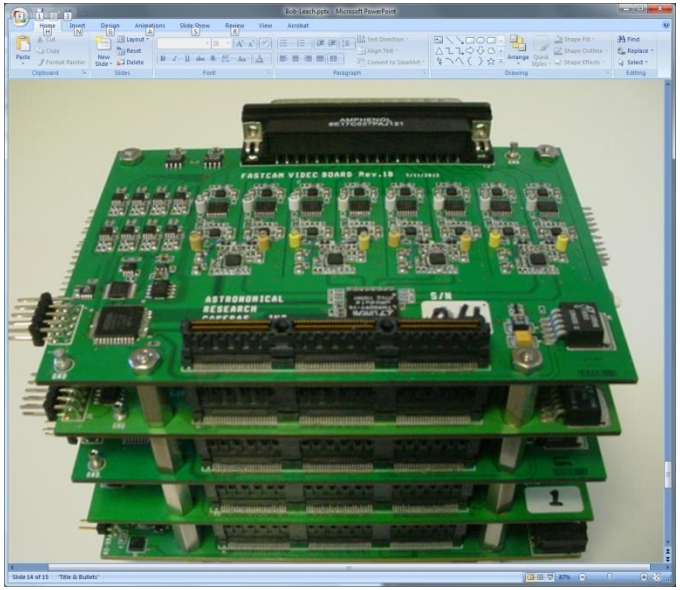
Operating System Support: Sun OS, Sun Solaris, Linux, Windows, Mac OS

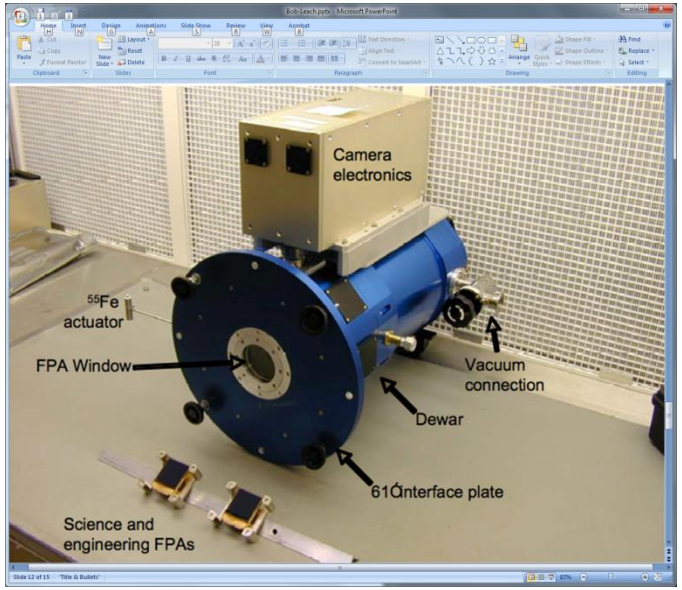
For all systems:

Variable number of clock driver and video processor boards

User editable, downloaded readout software

- Popular "turnkey" CCD and CMOS controller
- Analog CDS



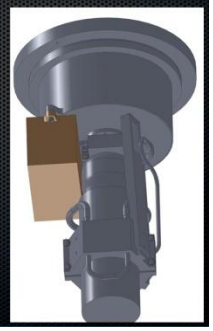


Armin Karcher – readout for DESI spectrograph

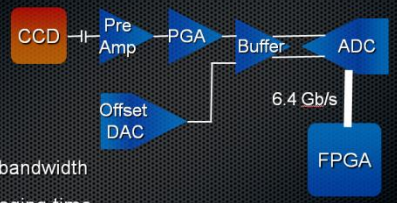
Armin Karcher – readout for DESI

Hardware Requirements

- Low Noise
- Compact / Low Power
- Flexible
  - P type and N type CCDs
  - 3 and 4 phase clocking
- Commercial interface
  - TCP/IP over Ethernet



Video Architecture



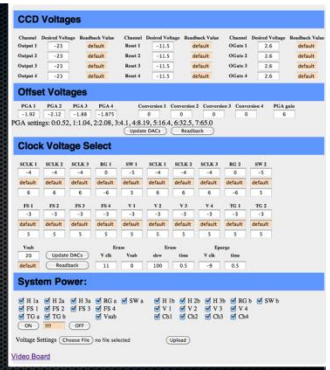
- Digital CDS
- High analog bandwidth
- Flexible averaging time
- Few analog components
- High speed 16 bit ADC (100MHz)
- Large data bandwidth to FPGA

FPGA Board

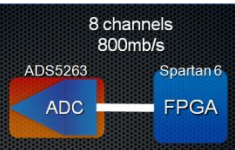
- Commercial board reduces routing effort
- Includes DRAM, FLASH, Power, Ethernet phy
- Ultra compact SO-DIMM form factor
- Upgrade path to new, pin-out compatible boards with next generation FPGAs
- Uses MicroBlaze soft-core@100MHz for PC communication.
- State machine reads timing table from internal memory and generates clocks, reads ADC data, and transmits CDS data to Micro Blaze.

Software

- User Interface is web based.
- No PC software is needed.
- All configuration files are stored on the controller in flash.
- Images can be acquired/read out by sending requests from the browser or any user program.
- Image files are sent in fits format.



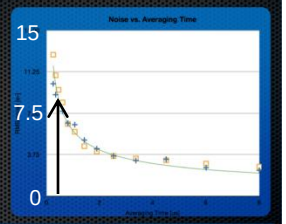
Digital CDS

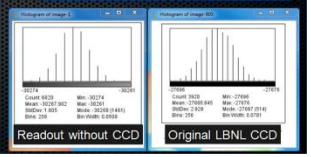


- Simple approach to DCDS was chosen.
- A programmable number of Reset and Signal samples are added in two 26bit accumulators.
- The difference is right shifted by a programmable number of bits and 16 bits are read-out.
- A digital gain can be chosen by setting the shift number.
- This allows simple tuning of settling and averaging times.
- More complex approaches may now be investigated after fully understanding the current system performance.

Performance with LBNL CCDs

- Performance is identical to the best we have seen on this CCD with the ARC Gen2 system.
- Newer low capacitance output transistors bring down noise.
- Lowest achieved noise in test system:
  - 1.76 e- @ 100kHz
  - 1.59 e- @ 50kHz



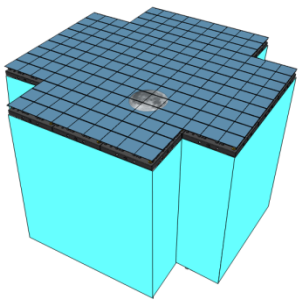


Small form-factor controller using modern components and packaging.

P. O'Connor – LSST integrated readout: design

The problem

- Electronics to ***control CCDs*** and ***process an aggregate of 1.5Gpixels/s*** must fit into 1/6m³ behind the focal plane
- Inclusive of thermal and mechanical FPA support
- ***Everything in cryostat***



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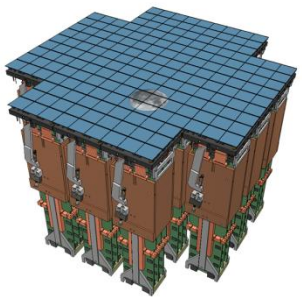
The solution

- A modular system of 21 "raft towers".
- Each is an autonomous, fully-testable 12K x 12K imager.
- Roughly the same size and power envelope as a 16-channel SDSU controller.
- Keys to compactness and low power:
  - ***Shortest possible CCD-electronics interconnect length***
  - ***Analog CDS***
  - ***ASIC-based clock, bias, and video processing***



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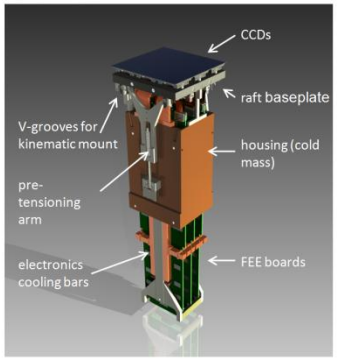
Raft Tower Module



- Complete 144-Mpixel imager
- Support sensors mechanically to meet strict coplanarity and piston tolerances
- Thermal management of sensors and electronics
- Protect sensor surfaces from condensable contamination
- Provide bias, timing, and control signals for CCD operation
- Low noise analog signal processing
- Digitizing, multiplexing of pixel data
- Diagnostics and slow controls

Optimized for

— *Compactness*

— *Low power*

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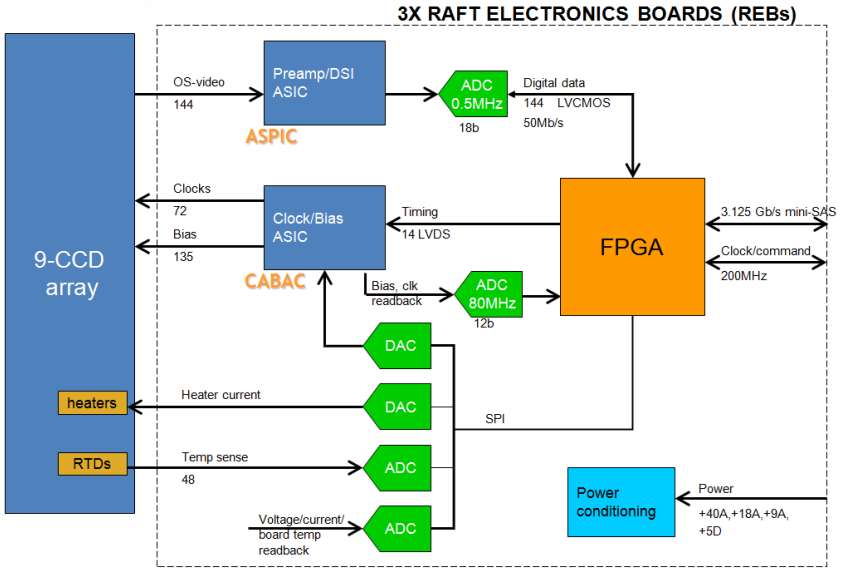
Raft tower electronics



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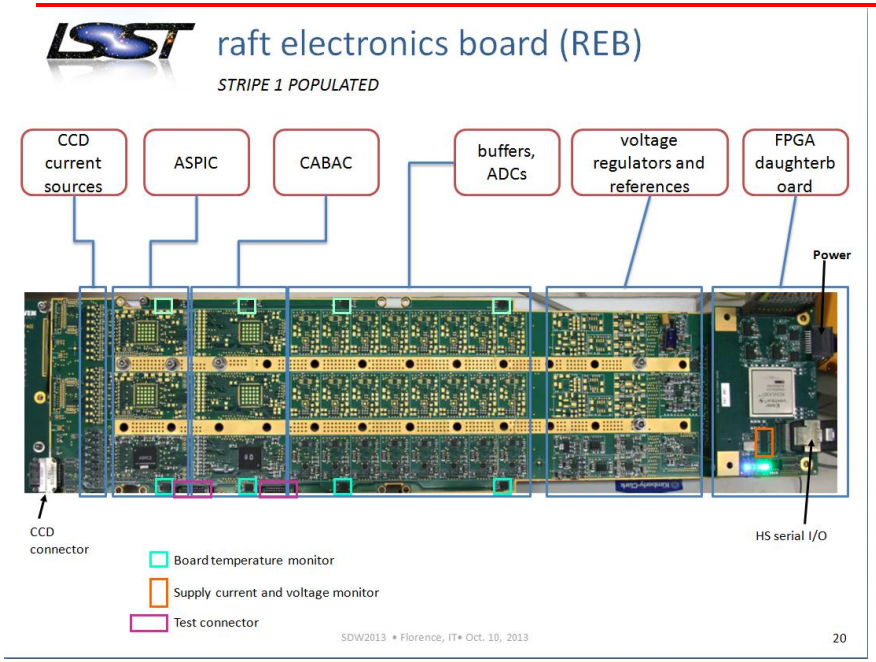
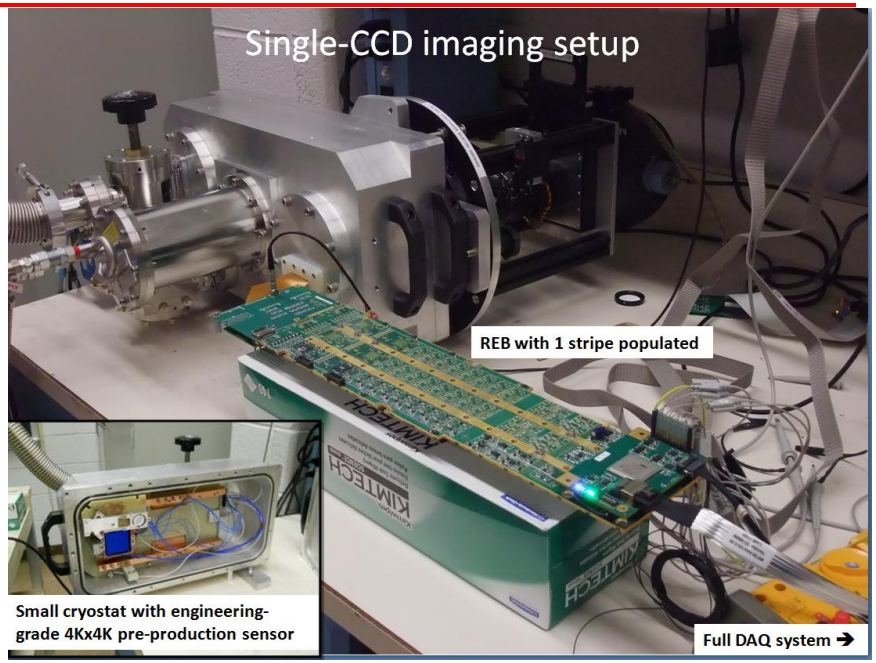
Raft electronics key requirements

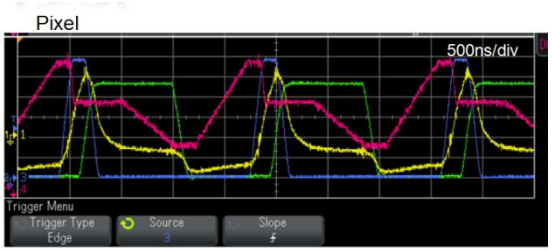
CCD bias	Provide programmable voltages for all CCD biases, except back depletion voltage
CCD clocking	Provide switches and programmable rail voltages/slew rate for all CCD clocks
Sequencer	Timing generator for CCD clocks, CDS switches, ADCs. ***Independent state machines for each CCD.***
Video processing	CDS by dual slope integration for 48 video channels Pixel rate ***545kpix/s*** ***Noise <9e-*** ***Crosstalk <0.2%*** Nonlinearity < 2%, 1 – 90ke- Max signal 175ke-
Data acquisition	***18b sampling***, 48 channels @545kpix/s Serialize with ECC. No frame buffer on REB 3.125Gbps Cu link to optical TX/RX
Slow controls and monitoring	Configure ASICs Monitor board and CCD temperatures, P/S current and voltage Read serial ID chip CCD protection
Special diagnostic port	Read back CCD bias voltages 80MSa/s ADC to monitor CCD clocks via mux on CABAC
Environmental	Vacuum operation; -40C coldsink.; low outgassing; ***power ≤ 350mW/chan***

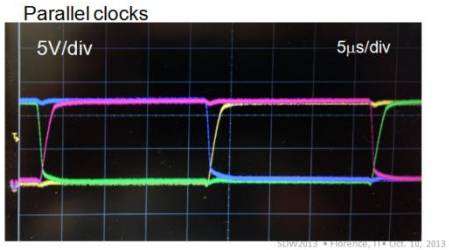
P. O'Connor – LSST integrated readout: implementation

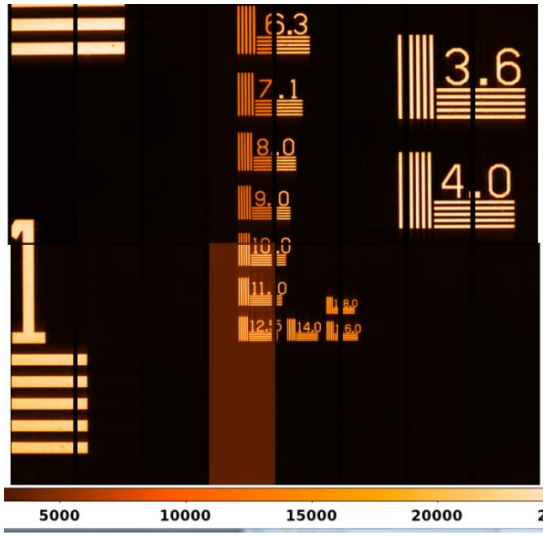




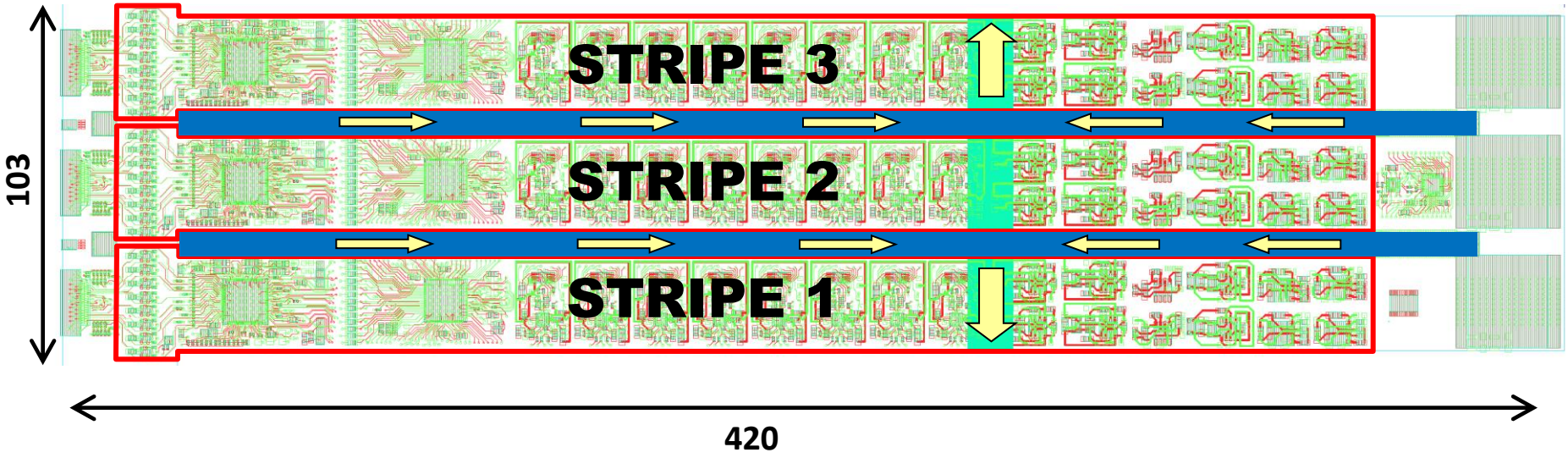
- Each REB serves 3 CCDs of 16 channels each.
- 12 ASICs for video processing, clock and bias generation
- T,V,I monitors
- 18b SAR ADCs (48)
- Virtex5 FPGA
- 3.125Gbps link







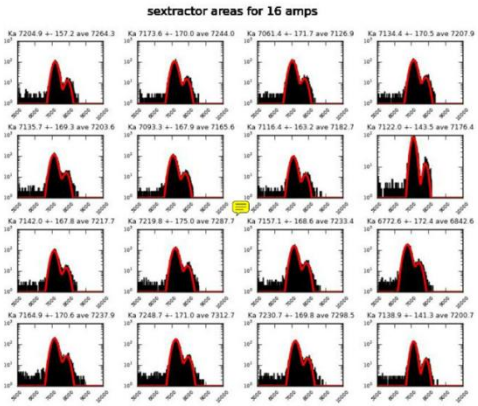
raft electronics board (REB)



P. O'Connor – LSST integrated readout: results

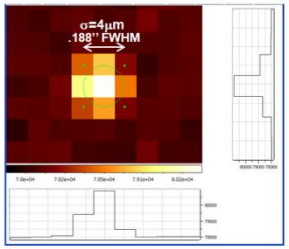
^{55}Fe xrays, -50V substrate bias

Spectra with Kα, Kβ peaks

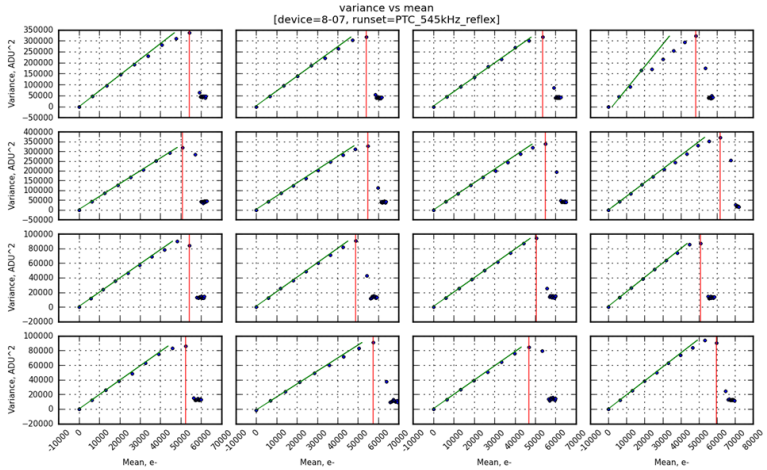


Gain dispersion 1.5%

Single cluster (zoom)



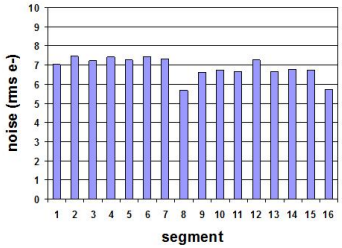
photon transfer



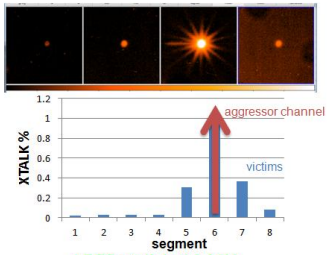
Full well capacity of CCD is ~140ke-; dynamic range of REB1 limited to ~ 60-80ke$^-$ withcurrent gain setup

Noise, crosstalk, nonlinearity

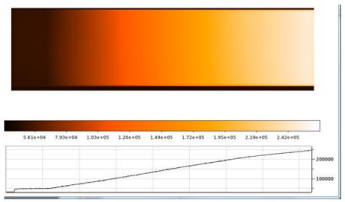
480kpix/s

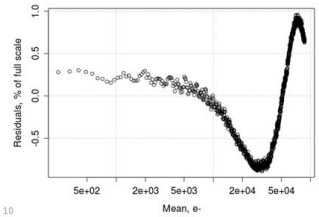


** REB noise is 1.5 -2.2 e-*



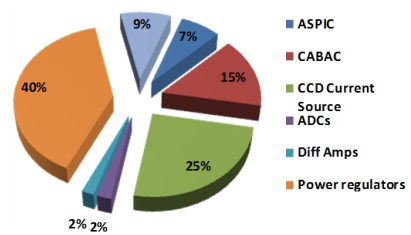
** REB xtalk is ≤ 0.04%*





Electronics power dissipation

Source	Peak power dissipation, W	
	Per REB	Per channel
CCD current source	4.21	.088
Video ASIC	1.20	.025
Clock/bias ASIC	2.52	.053
ADC differential buffer/driver	0.31	.0065
ADC	0.36	.0075
Power Regulators	6.63	.138
Control FPGA	1.50	.031
TOTAL Electronics Power	**16.73**	**0.349**

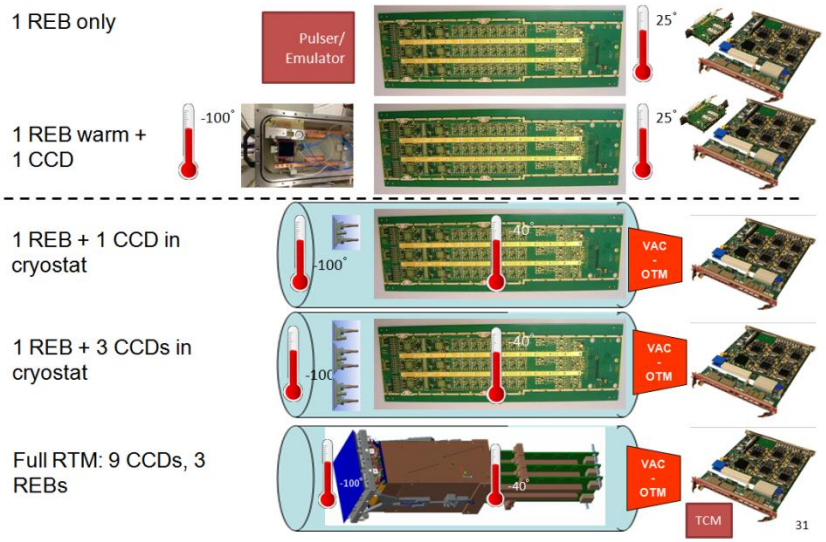


Measured (on single-stripe REB)	
Expose	6.98W
Readout	8.96W

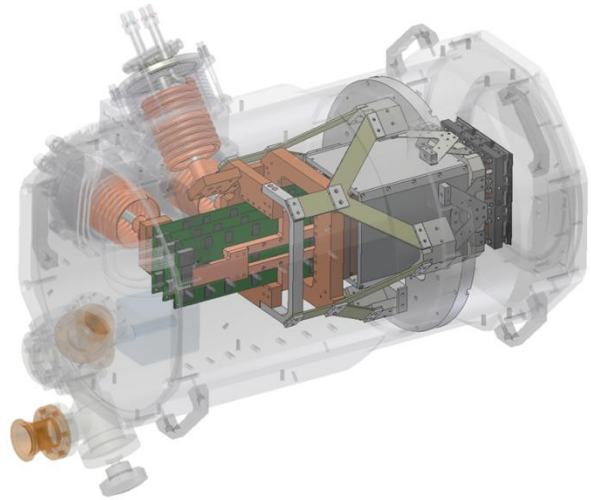
Ave(LSST cadence) ~ 7W
30% power common
≈.35W/chan for fully-populated REB ✓

P. O'Connor – LSST integrated readout: plans

Next steps



mechanics and thermal



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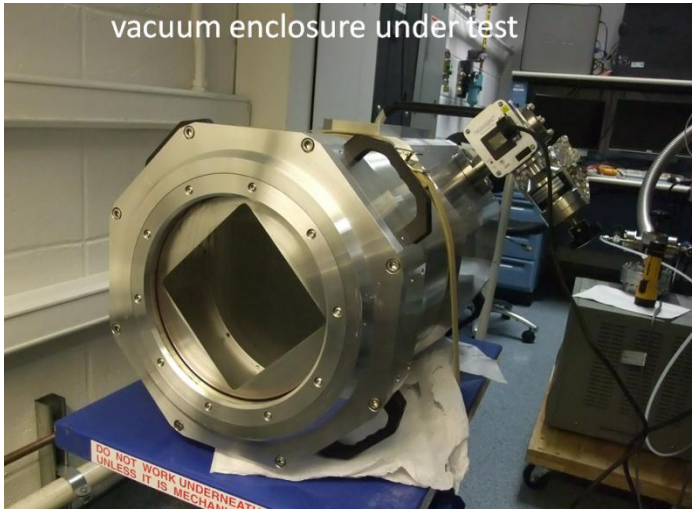
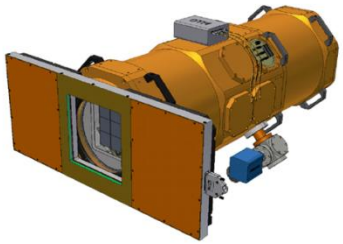
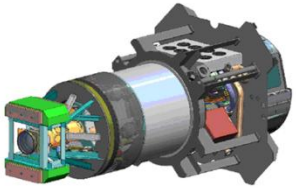


proposed LSST commissioning camera (ComCam)

- Raft test cryostat with 9 engineering-grade CCDs, full electronics and DAQ, LN2 cooling, shutter, corrector + filters
- Installed on camera hexapod/rotator at LSST 3-mirror focus prior to full Camera readiness
- 30 arcmin field on-axis
- Early commissioning studies





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Digital Correlated Double Sampling

- **Required to remove kTC noise from reset of imager sense node**
- **Advantages:**
  - *Reduce analog circuitry to minimum (DC restore and antialiasing filter)*
  - *Synthesize arbitrary weighting function*
  - *Increase effective bits by sample averaging*
  - *Convenient diagnostic output*
  - *Intriguing possibilities for offline analysis*

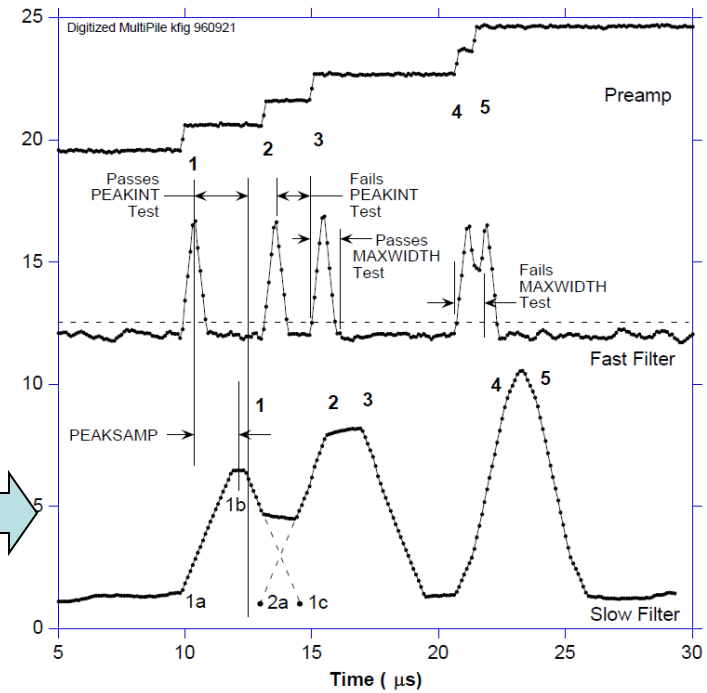
- **Drawbacks:**
  - *ADC sample rate > 10X pixel rate*
  - *Data volume, data bandwidth, power dissipation impact*

- **Design choices:**
  - *ADC sample rate*
  - *Analog bandwidth (upper and lower cutoff frequencies)*
  - *Sample weighting function*

DCDS pros and cons

Paul O'Connor 10/10/13

1. **"Digital CDS" is a special case of digital filtering, which has been used for a long time in a wide range of research instrumentation to approach optimal filtering, or to apply multiple filters to the same digitized waveform, or to implement time-adaptive filters:**
   - *W. Cleland, E. Stern, "Signal processing considerations for liquid ionization calorimeters in a high rate environment", Nucl. Instrum. Methods A338, 467(1994)*
   - *W. Warburton et al., "Digital pulse processing: new possibilities in nuclear spectroscopy", Appl. Rad.Isotopes 53(4), 913 (2000)*
2. **It is well established that the simple differential averager (SDA) is the optimal filter for detecting a step signal in the presence of white noise;**
   - *D. Hegyi, A. Burrows, AJ85(10), 1980*
   - *G. Hopkinson, D. Lumb, J. Phys. E15,1214(1982)*
3. **When 1/f noise is significant, the shape of the optimal filter changes but SDA remains near-optimal.**
4. **The SDA is easily implemented in the analog domain (dual-slope integrator).**
5. **DCDS advantage only when noise is non-white and pixel rate is low.**



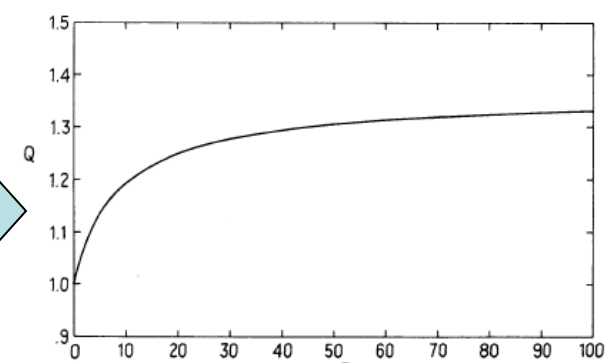
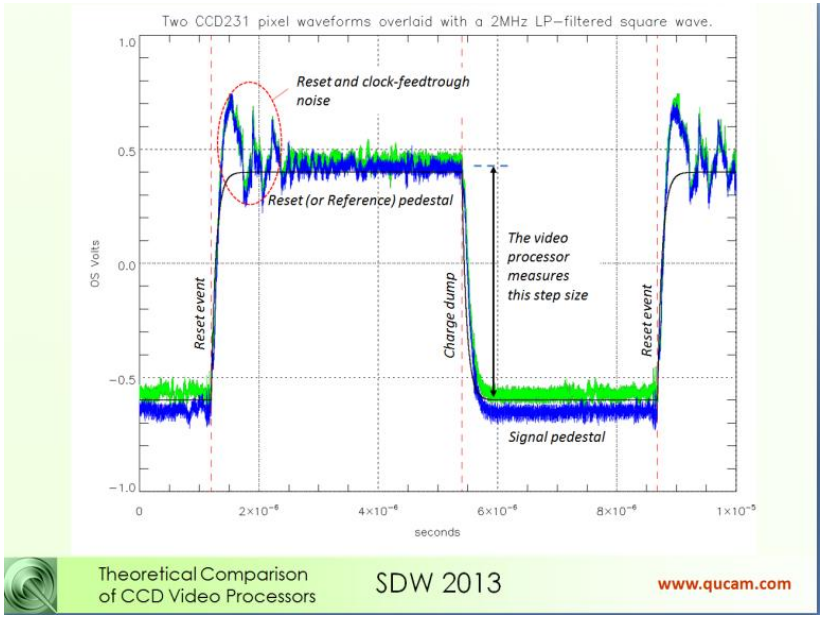
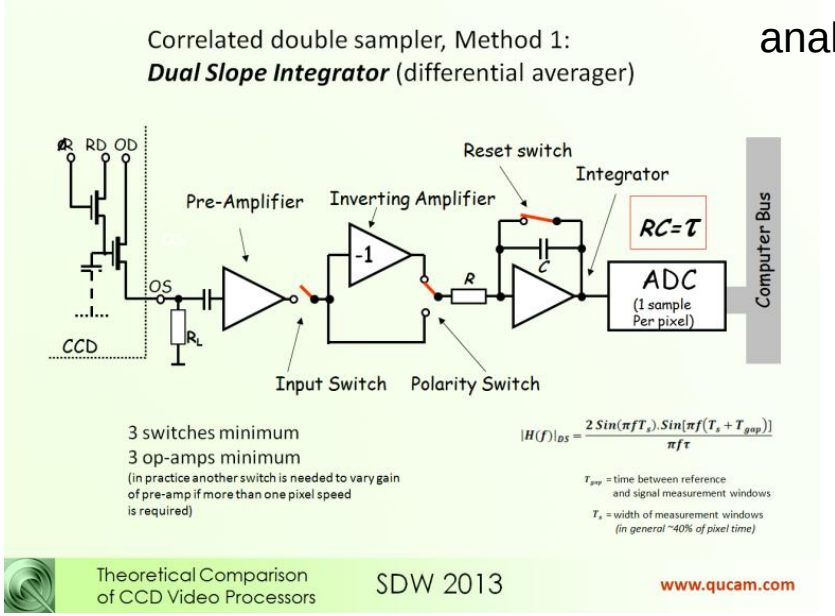
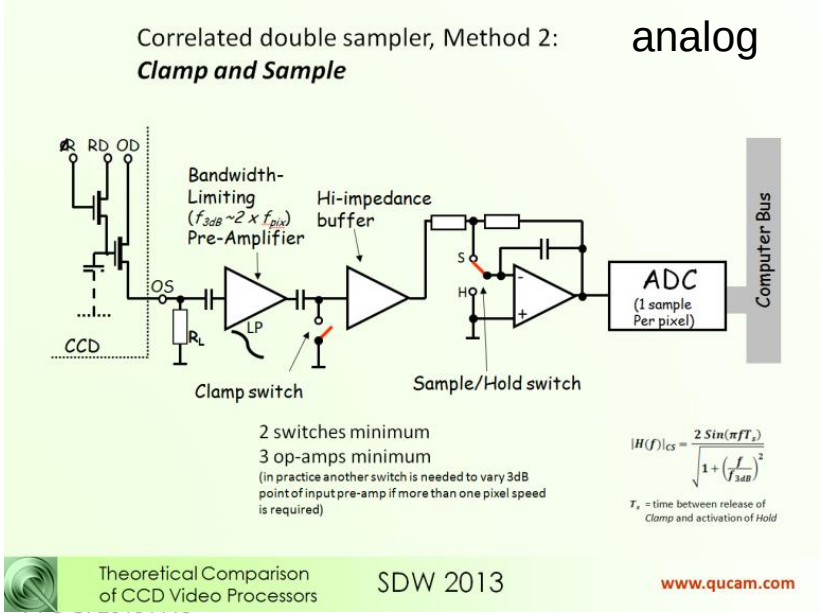


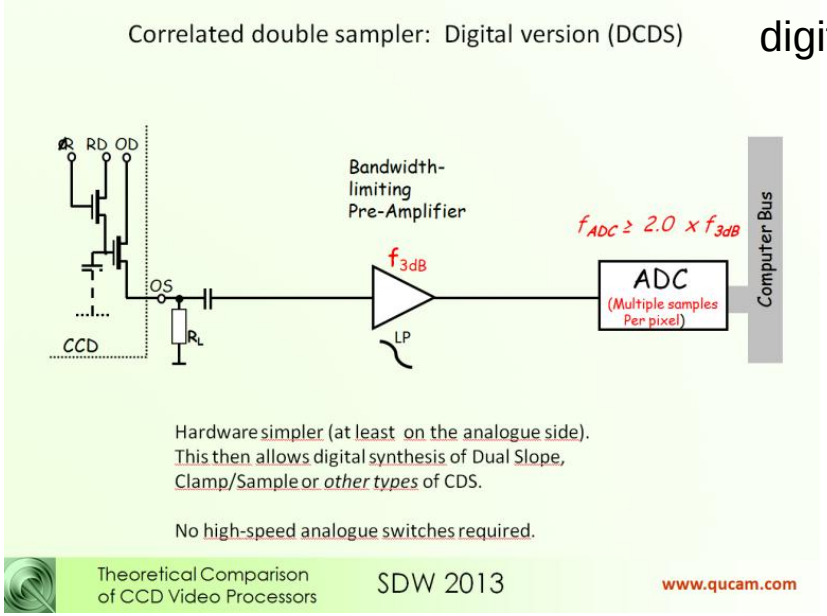
FIG. 2. The quotient Q of the signal-to-noise ratio obtained with a matched filter to that obtained with the differential averager vs α, where $\alpha = F_0\tau/2W_0$.

Simon Tulloch – DCDS numerical model



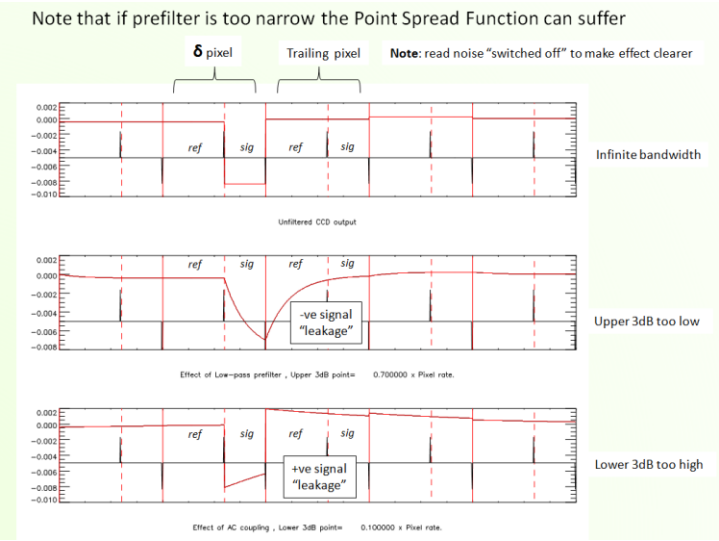


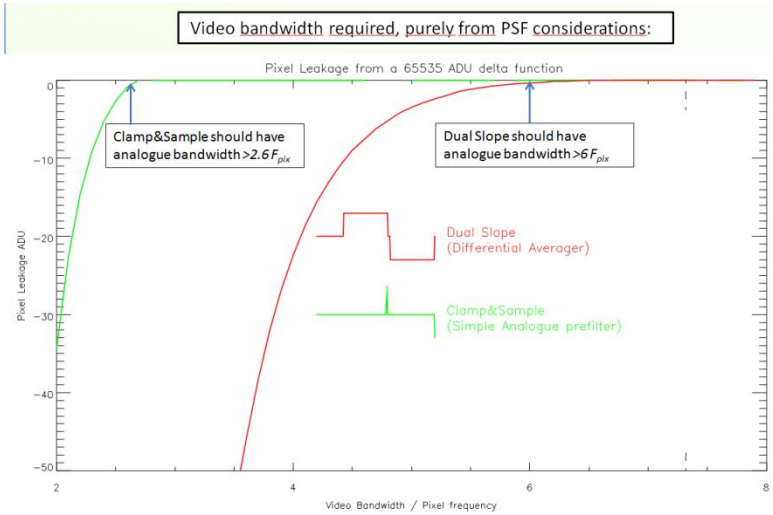




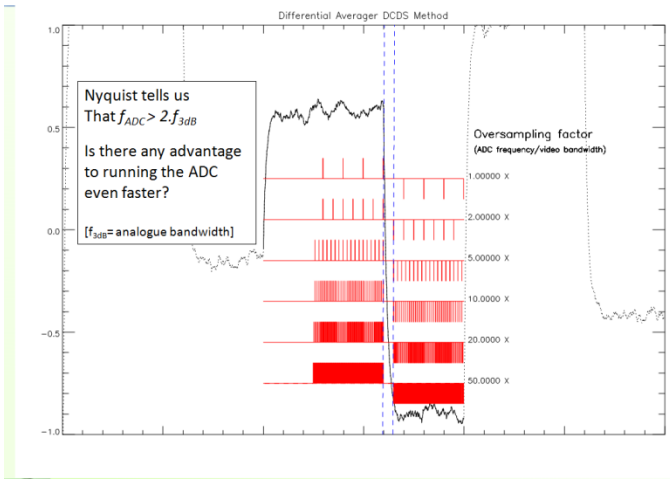
Simon Tulloch – DCDS bandwidth/sample rate

required analog bandwidth

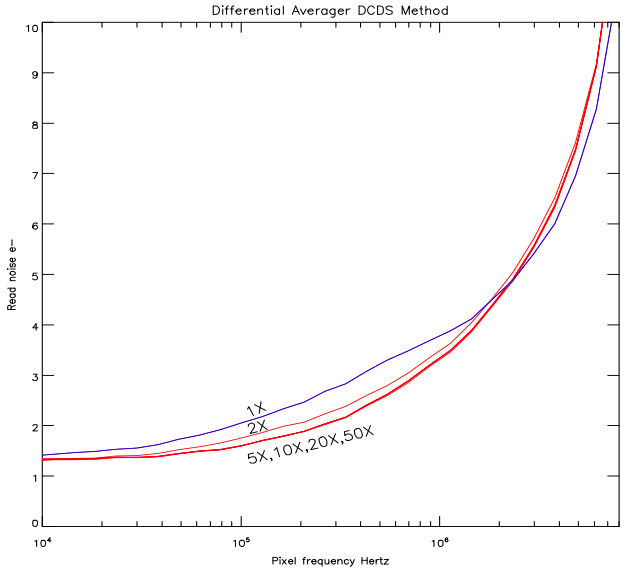




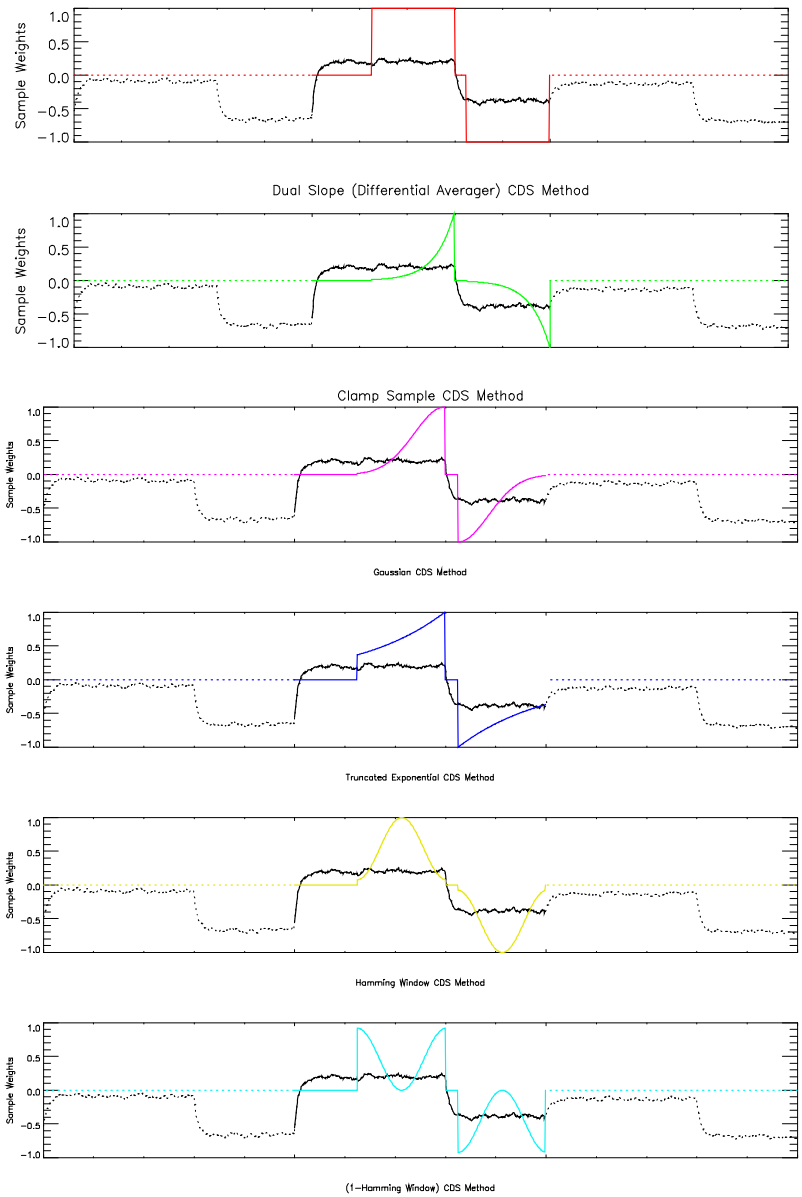
increased oversampling

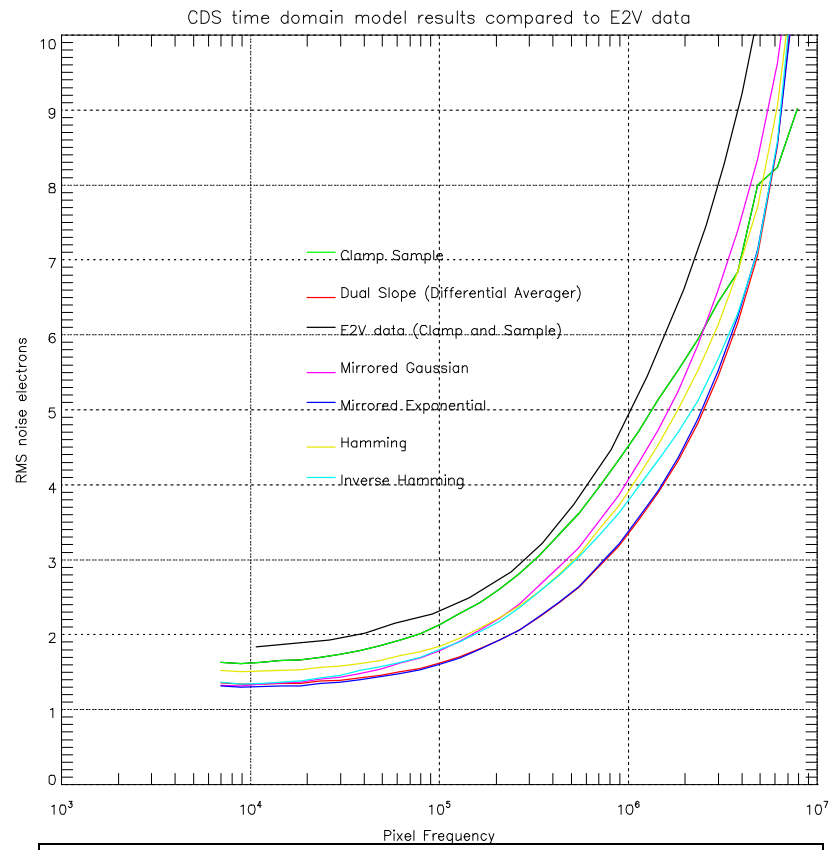


noise vs. pixel rate vs. oversampling



Simon Tulloch – DCDS weighting function





- Differential Averager (Dual Slope Integrator) is the best all-round performer.
- Clamp&Sample is the poorest performer at all pixel rates
- Mirrored Gaussian and mirrored exponential methods give tiny advantage at low-signal end

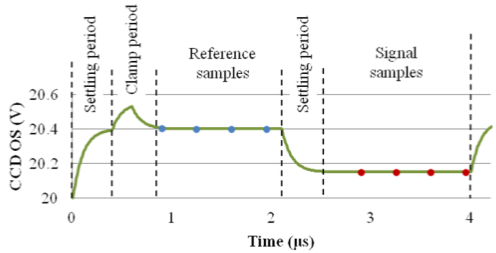
Confirmed experimentally (Clapp 2012 SPIE)

Paul Jorden – Digital Correlated Double Sampling

Paul Jorden – DCDS

DCDS Processing

e2v



- Limited to sampling the settled output voltage
- Sample frequency/pixel frequency > 14
  - 16-bit accuracy
  - System bandwidth at ADC nyquist frequency
  - 10% clamp period

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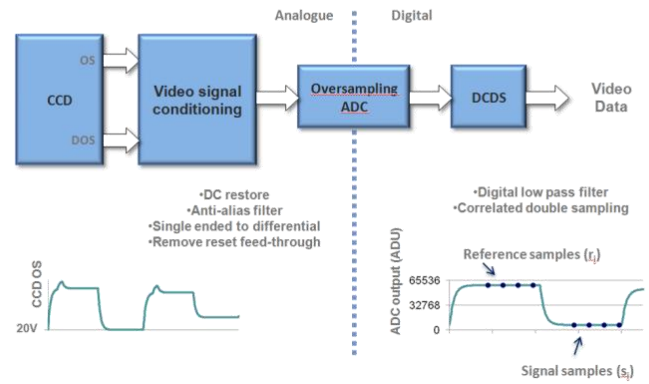
Video Chain

e2v

- Digital Correlated Double Sampling (DCDS)



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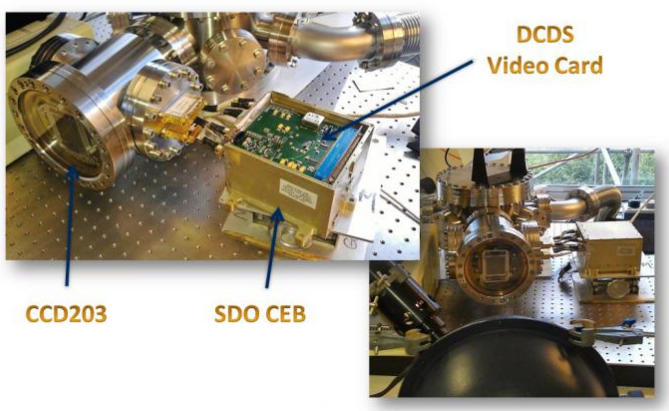
DCDS Prototype

e2v



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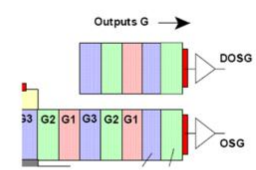
Concept for J-PAS

e2v

- **Use differential signals** for best common-mode noise rejection

  Get √2 noise increase



- **Use DCDS for optimal noise** of system
  - 100 MHZ sampling frequency; 500 kHz pixel rate
  - DCDS better than analogue CDS and recovers some of the loss of differential mode.

$f_{sample} = 200\ f_{pix}$

??

References

- Clapp SPIE 2012, 8453-49 DCDS
- Jorden et al. SPIE 2012, 8453-20. J-PAS

© e2v Slide 8

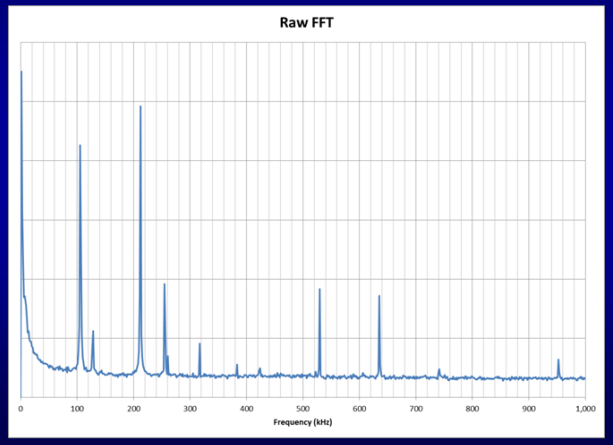
Greg Bredthauer – DCDS roundtable

ADC Evolution

Controller	Year	ADC	Sample Rate (MHz)	Bits	Noise (LSB RMS)	Power (mW / Ch)	Notes
FlexCam	2006	AD9824	30	14	2.0	153	Analog CDS
Firefly	2007	LTC2208	130	16	2.9	1500	
Tapestry	2008	LTC2208	130	16	2.9	1500	
CCTapestry	2009	ADS5562	80	16	1.4	865	
Aura	2009	LTC2262	150	14	1.2	149	
Reflex	2010	AD9268	125	16	2.3	375	Dual
Reflex B	2011	AD9650	105	16	1.5	328	Dual
Archon	2012	ADS5263	100	16	1.0	355	Quad
	2013	AD7960	5	18	1.1	46	SAR

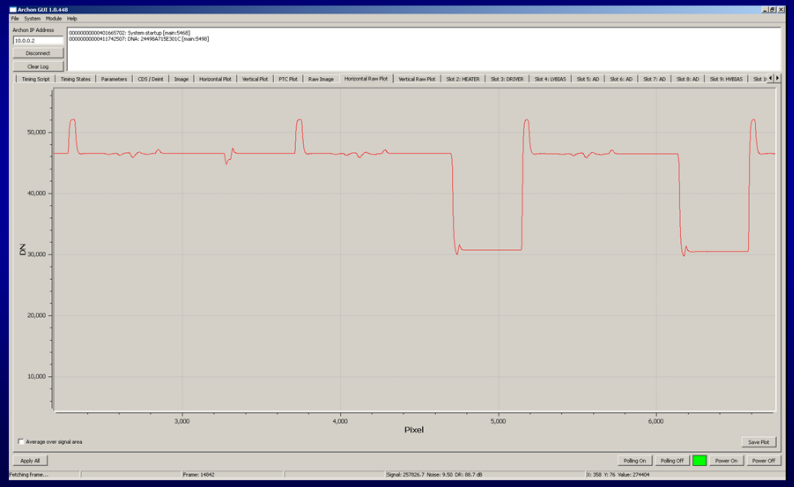
2

Diagnostics



3

Analytic Possibilities



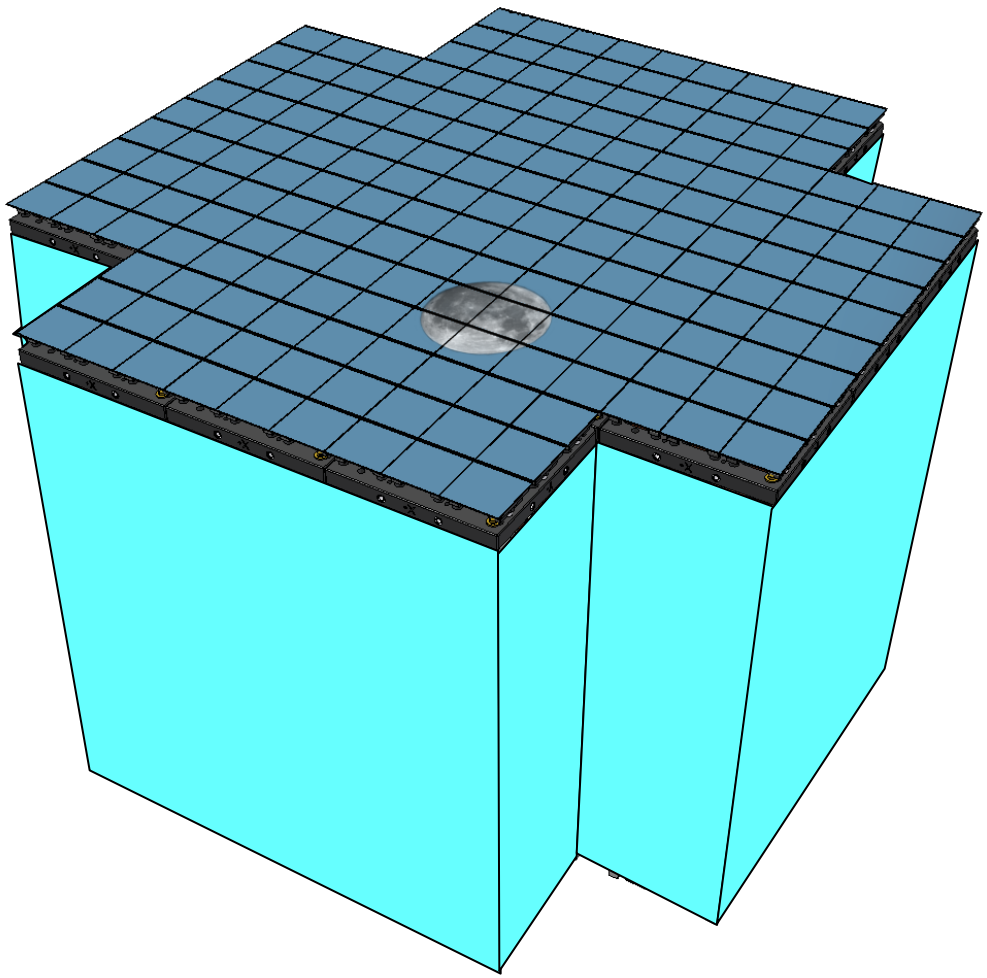
Digital CDS Experience

- High sampling rates let you see subtle features (How fast is the CCD output settling? Is it ringing?)
- For higher frequencies (1 MHz), every extra sample averaged lowers noise, close to theory
- For lower frequencies (100 kHz), balance with 1/f noise – samples prefer to be close to SW transition
- Higher analog bandwidth gives faster settling, easier to avoid subtle non-linearities
- ADC power falls with sample rate – use lower frequencies in production after tuning

BACKUP

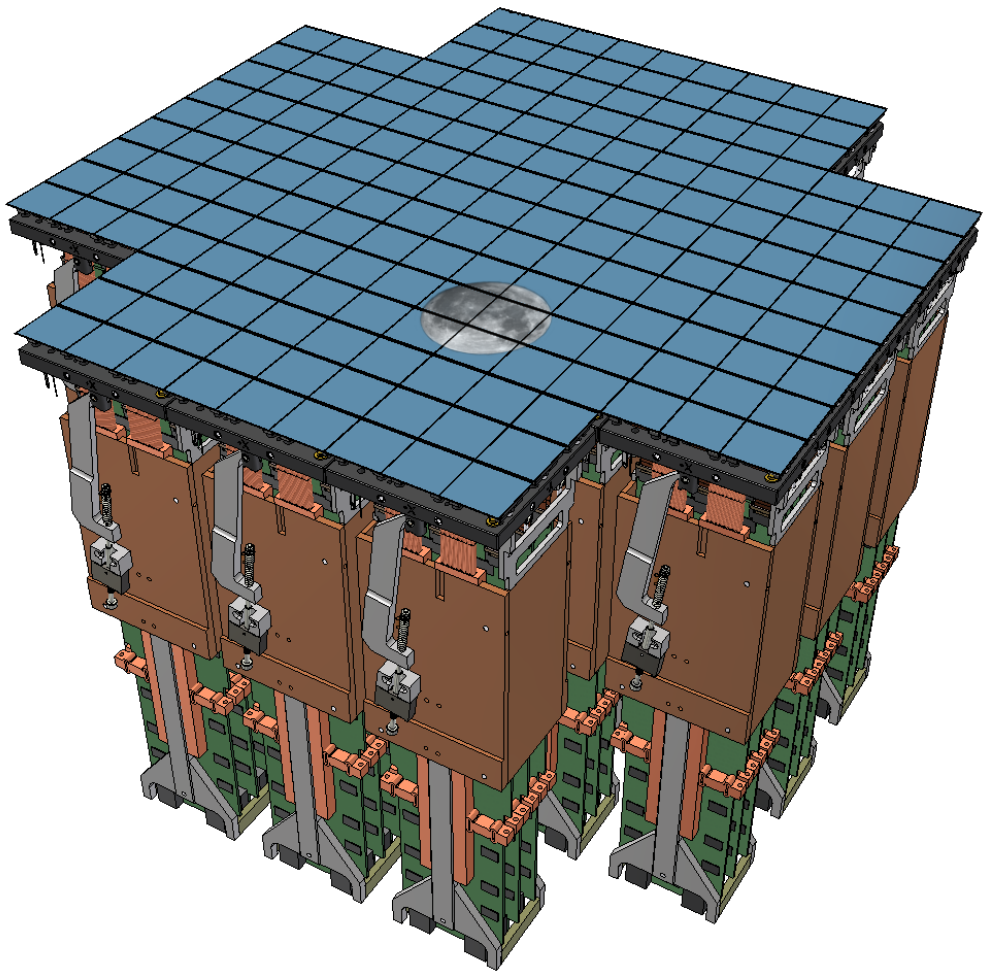
The problem

- Electronics to ***control CCDs*** and ***process an aggregate of 1.5Gpixels/s*** must fit into 1/6m^3 behind the focal plane
- Inclusive of thermal and mechanical FPA support
- ***Everything in cryostat***

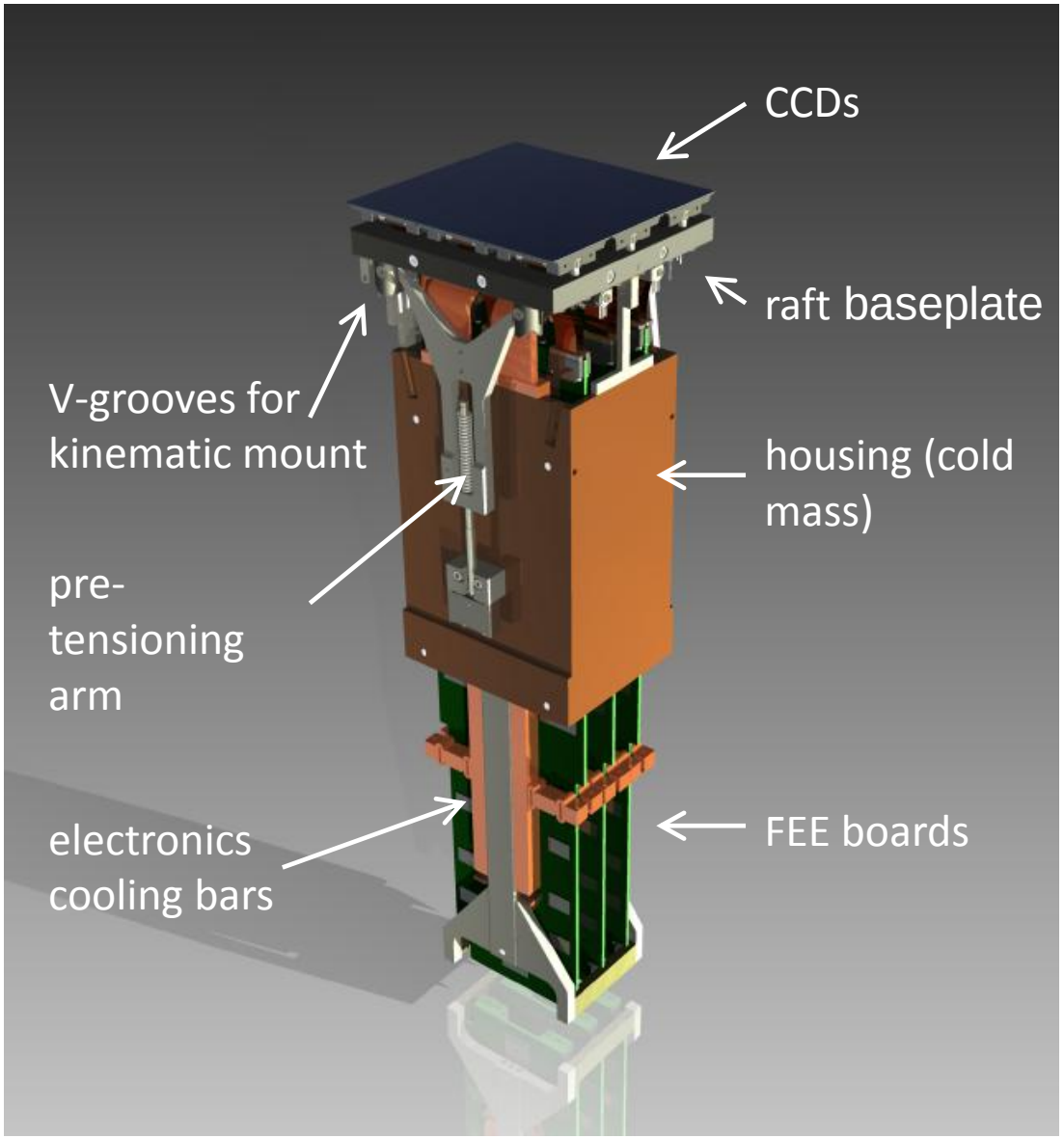


The solution

- A modular system of 21 “raft towers”.
- Each is an autonomous, fully-testable 12K x 12K imager.
- Roughly the same size and power envelope as a 16-channel SDSU controller.
- Keys to compactness and low power:
  - ***Shortest possible CCD-electronics interconnect length***
  - ***<u>Analog</u> CDS***
  - ***<u>ASIC-based</u> clock, bias, and video processing***



Raft Tower Module

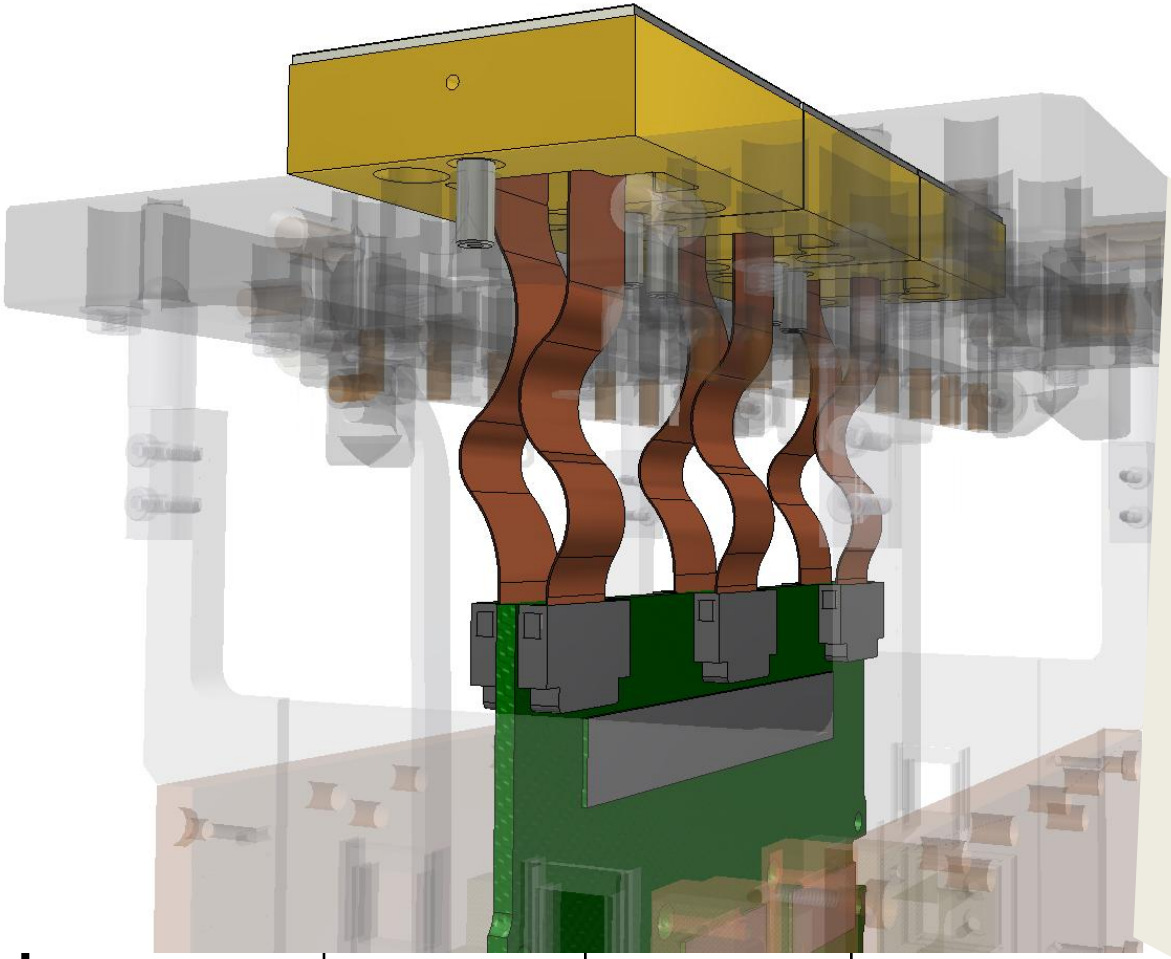


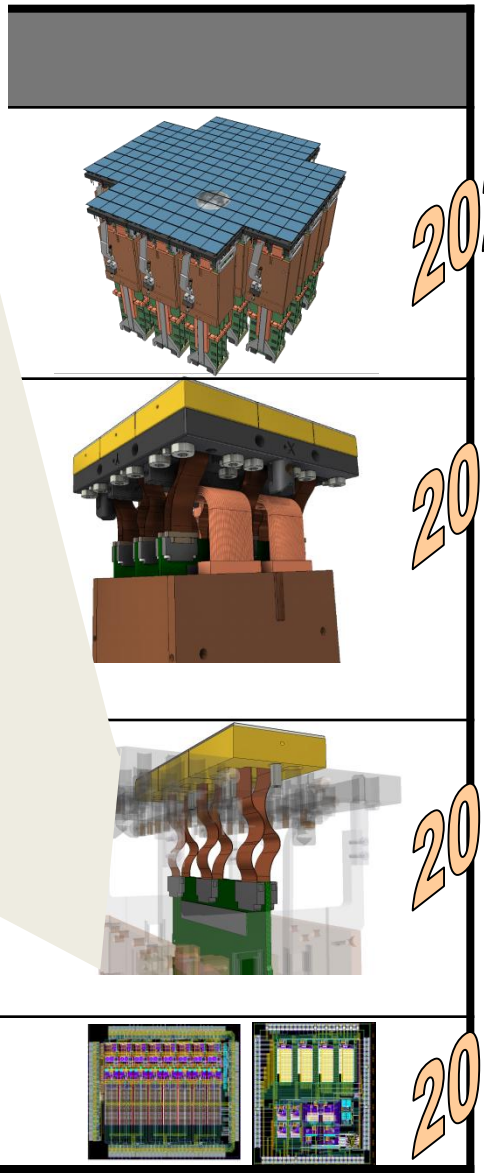
- Complete 144-Mpixel imager
- Support sensors mechanically to meet strict coplanarity and piston tolerances
- Thermal management of sensors and electronics
- Protect sensor surfaces from condensable contamination
- Provide bias, timing, and control signals for CCD operation
- Low noise analog signal processing
- Digitizing, multiplexing of pixel data
- Diagnostics and slow controls

Optimized for

— *Compactness*

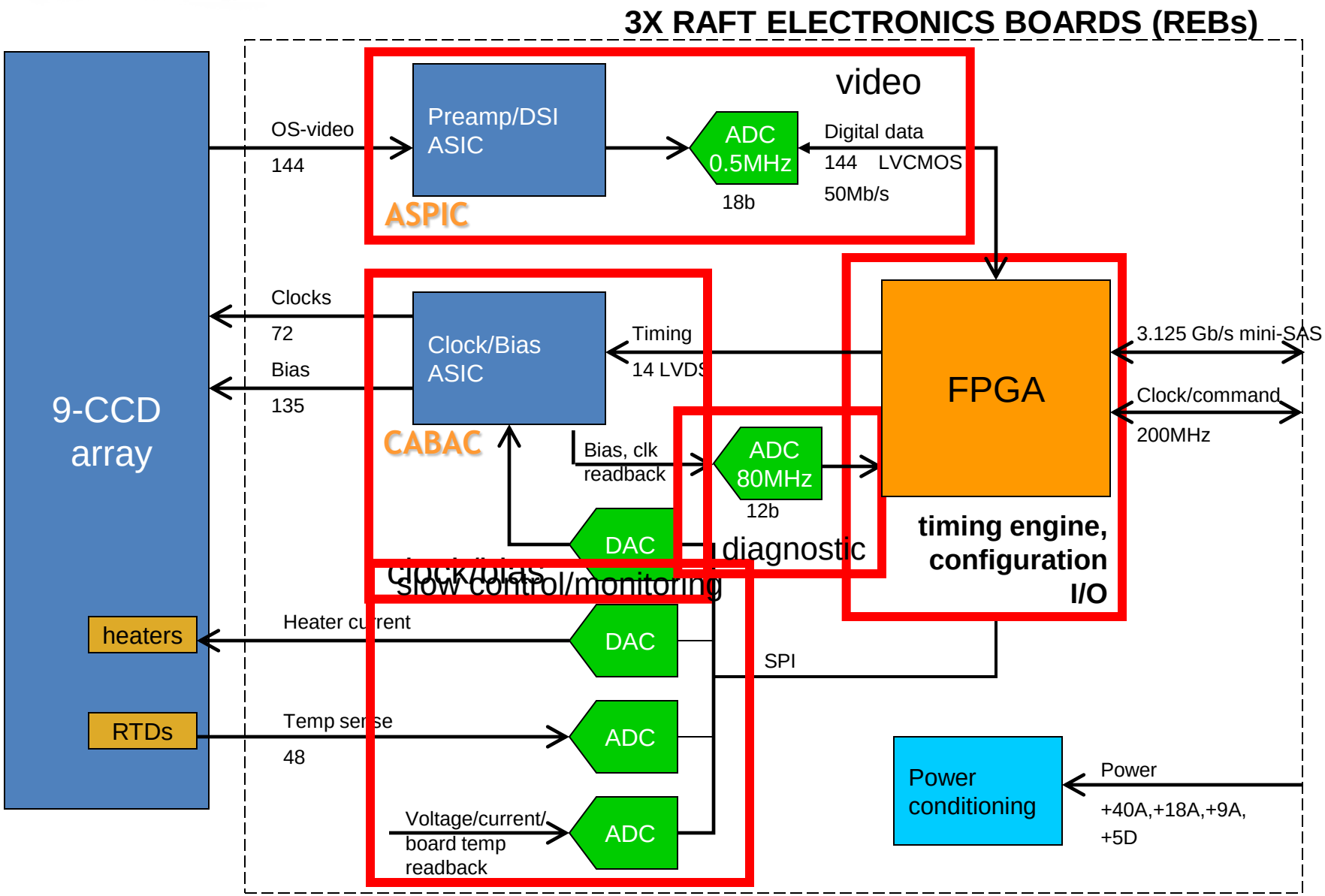
— *Low power*





REB	**63**	**3**	**48**	
ASIC	**378**	**½**	**8**	

Raft tower electronics

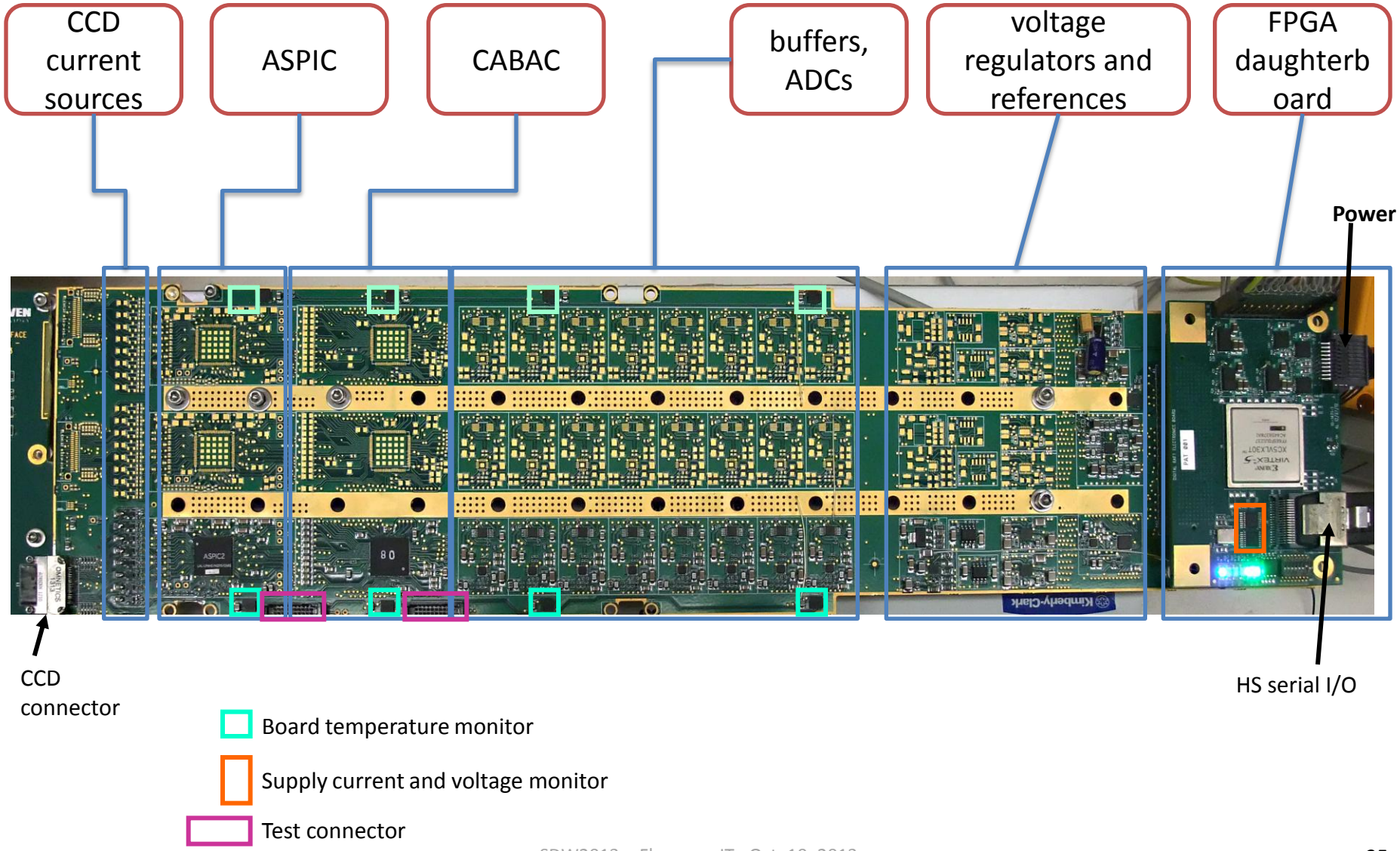


Raft electronics key requirements

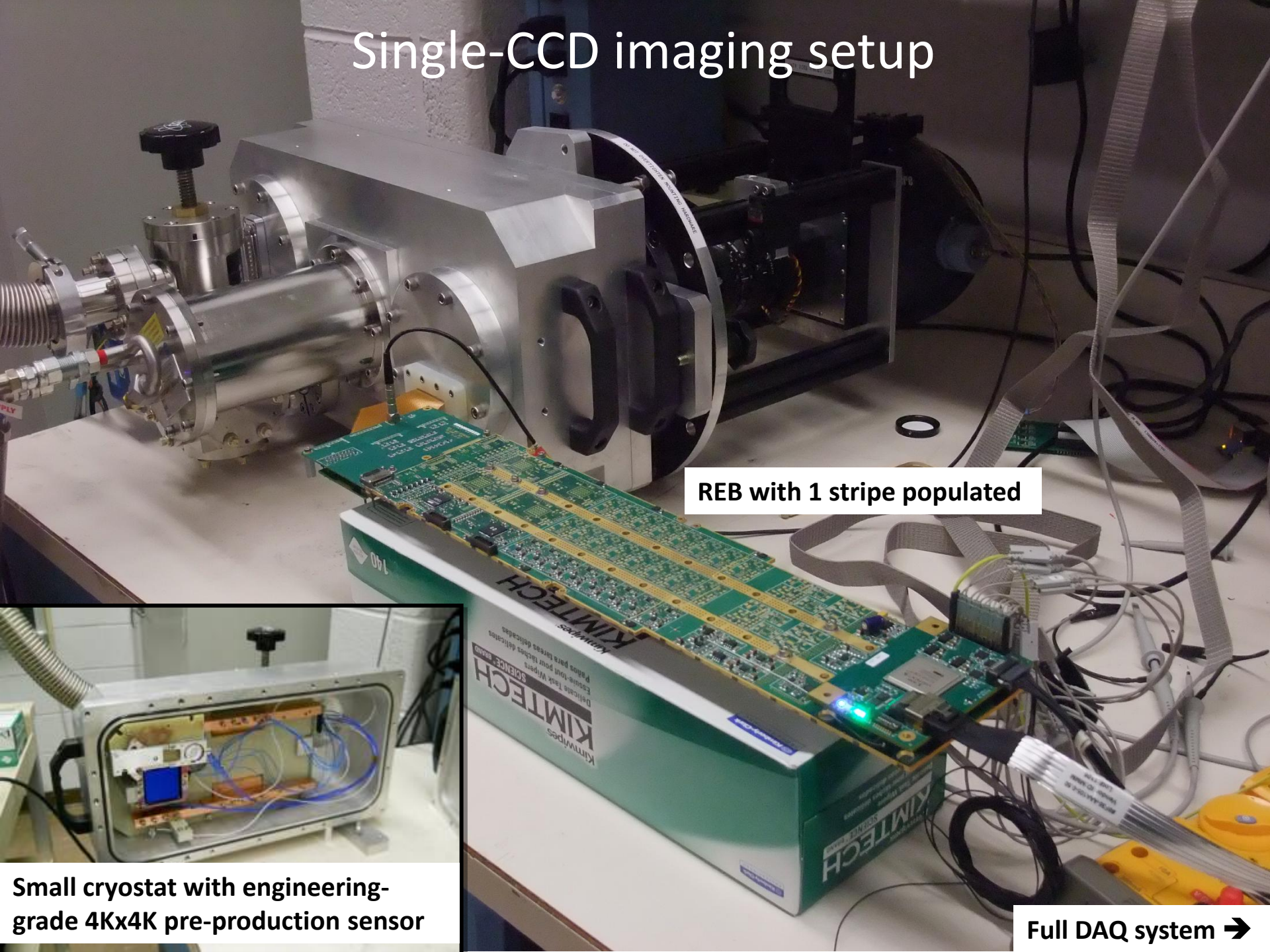
CCD bias	Provide programmable voltages for all CCD biases, except back depletion voltage
CCD clocking	Provide switches and programmable rail voltages/slew rate for all CCD clocks
Sequencer	Timing generator for CCD clocks, CDS switches, ADCs. ***Independent state machines for each CCD.***
Video processing	CDS by dual slope integration for 48 video channels Pixel rate ***545kpix/s*** ***Noise <9e-*** ***Crosstalk <0.2%*** Nonlinearity < 2%, 1 – 90ke- Max signal 175ke-
Data acquisition	***18b sampling***, 48 channels @545kpix/s Serialize with ECC. No frame buffer on REB 3.125Gbps Cu link to optical TX/RX
Slow controls and monitoring	Configure ASICs Monitor board and CCD temperatures, P/S current and voltage Read serial ID chip CCD protection
Special diagnostic port	Read back CCD bias voltages 80MSa/s ADC to monitor CCD clocks via mux on CABAC
Environmental	Vacuum operation; -40C coldsink.; low outgassing; ***power ≤ 350mW/chan***

raft electronics board (REB)

STRIPE 1 POPULATED

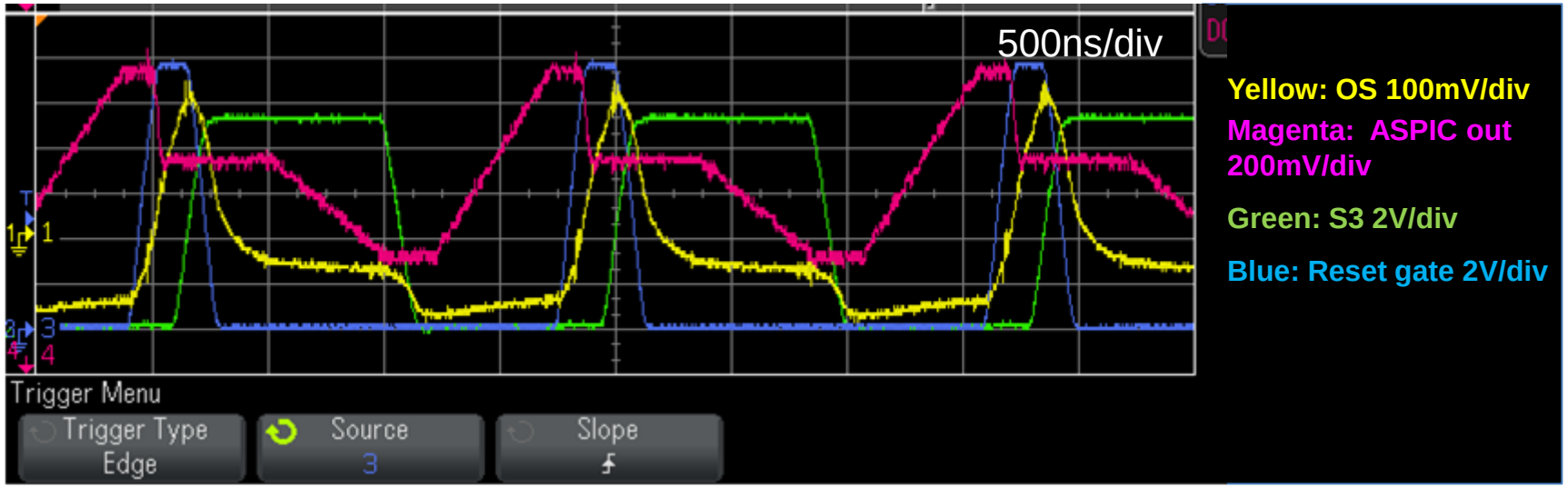


Single-CCD imaging setup

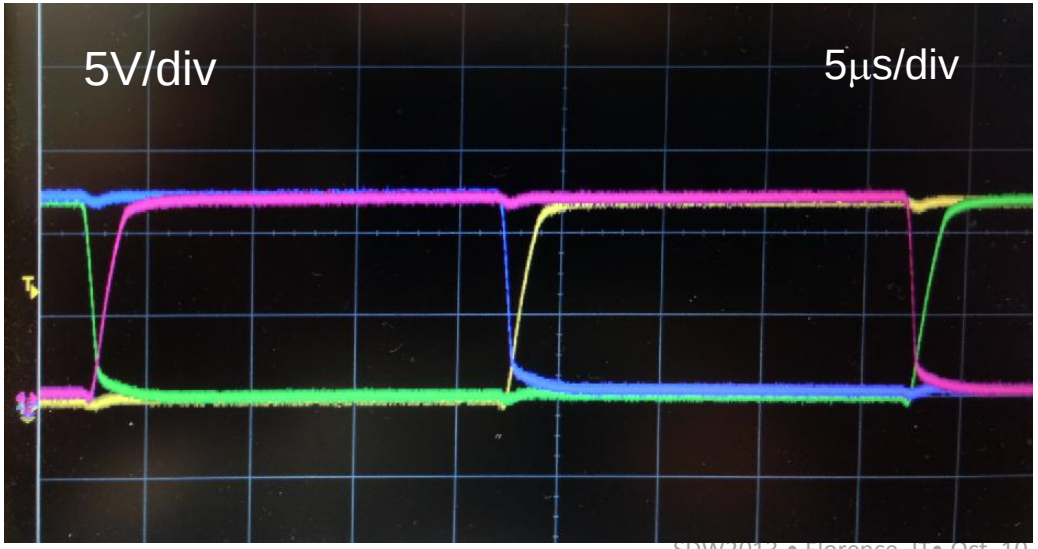


waveforms

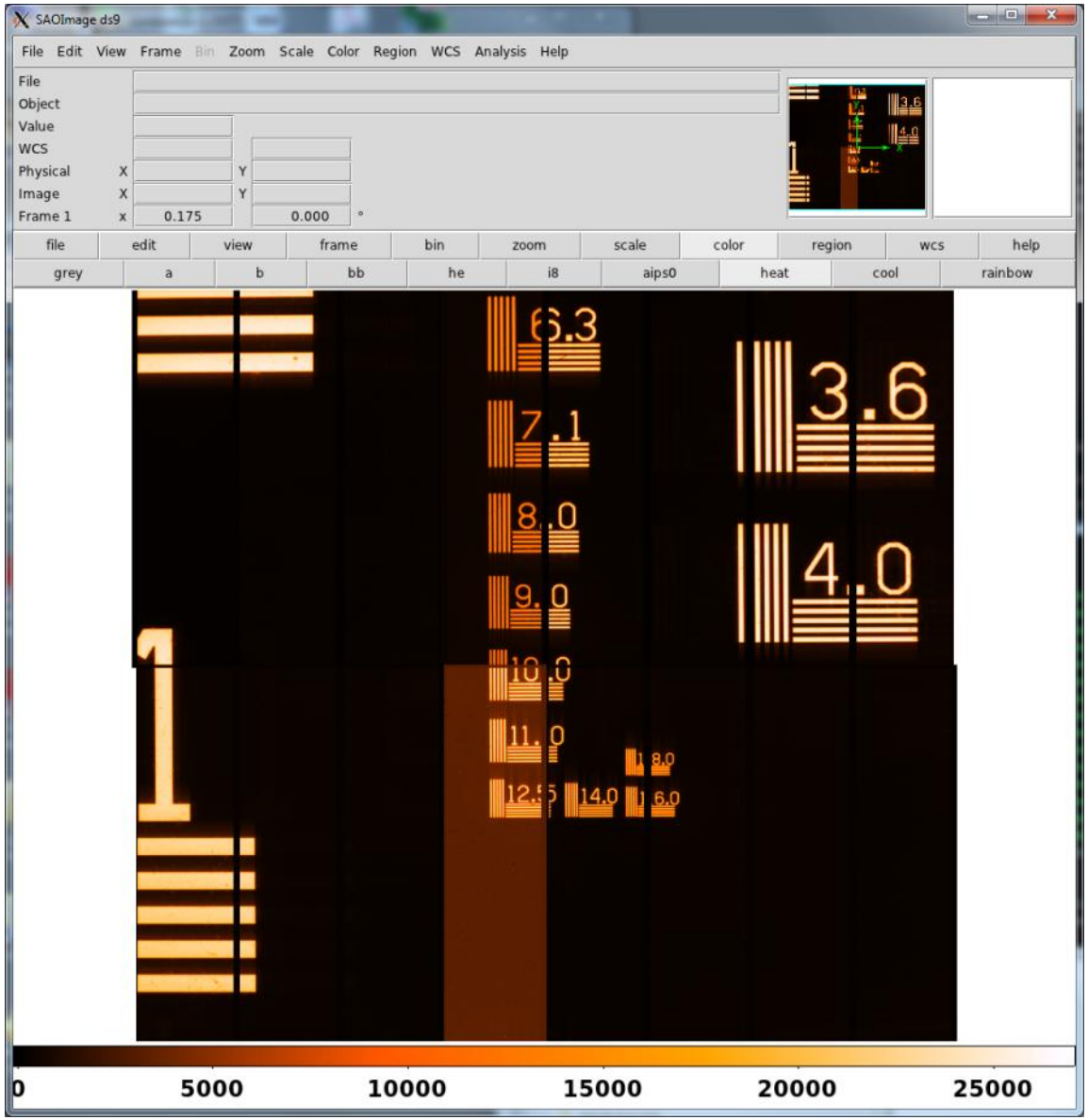
Pixel



Parallel clocks



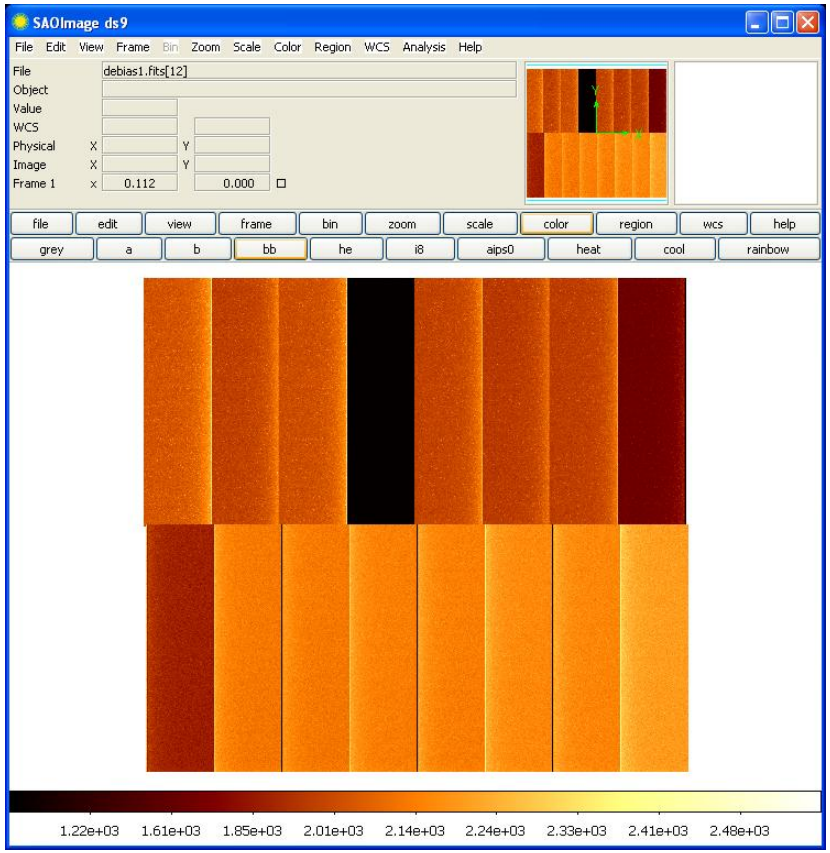
target image



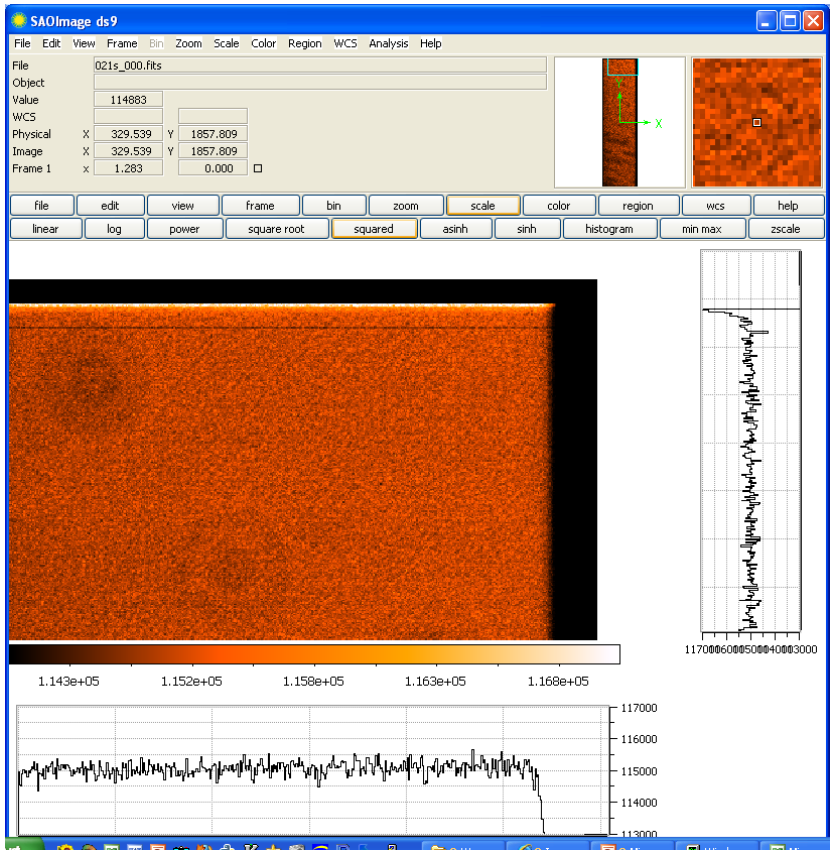
8000 e-
650nm

Bias and flatfield

Bias

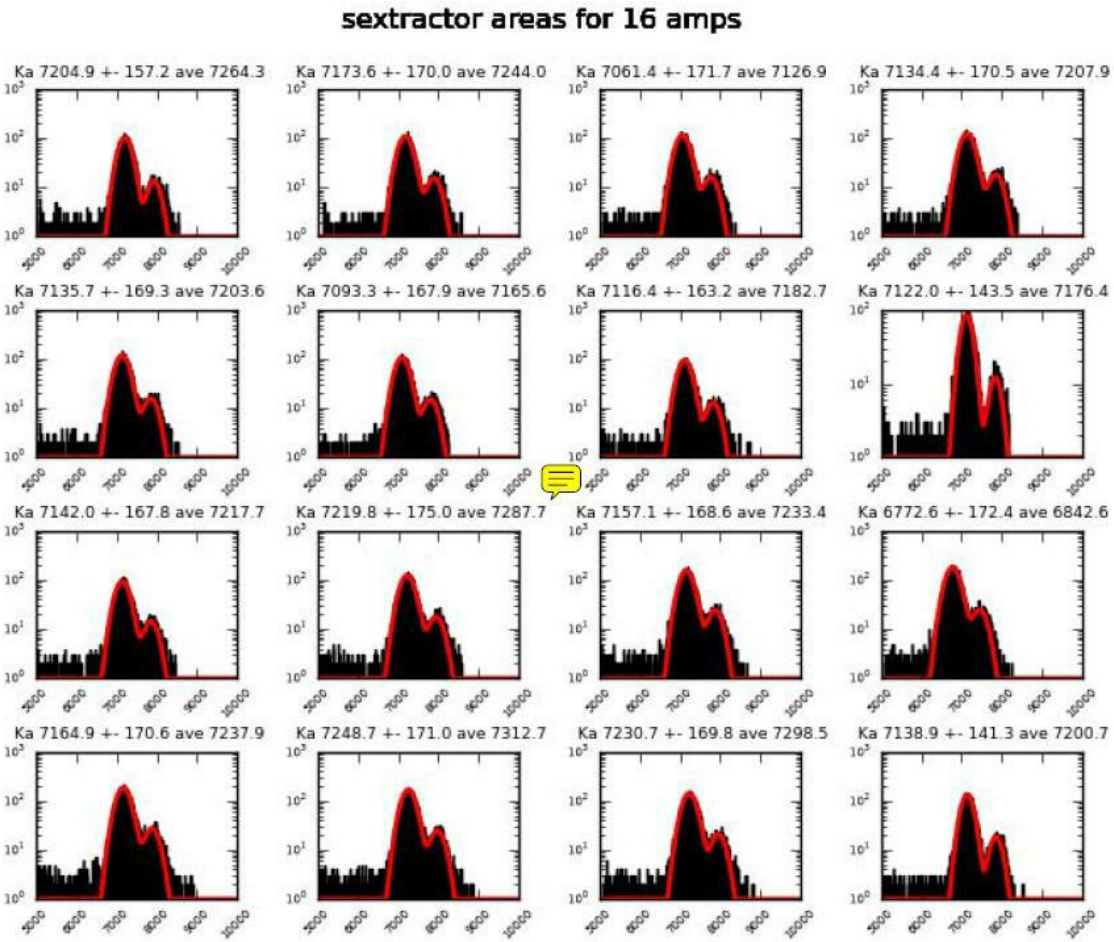


650nm flat



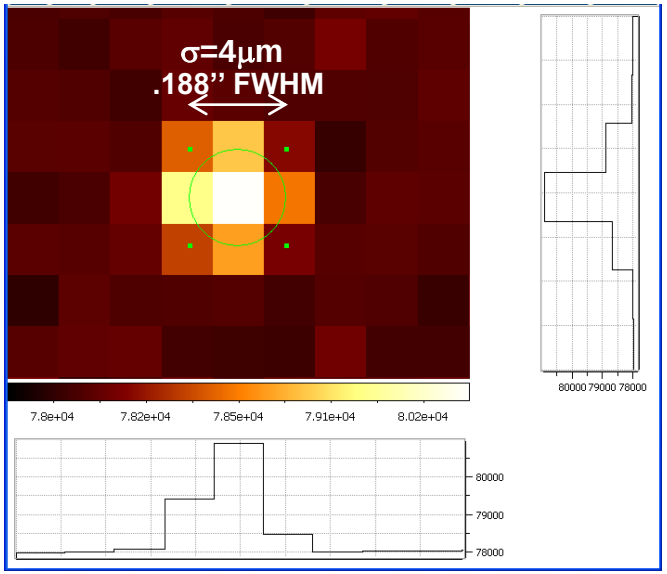
^{55}Fe xrays, -50V substrate bias

Spectra with Kα, Kβ peaks

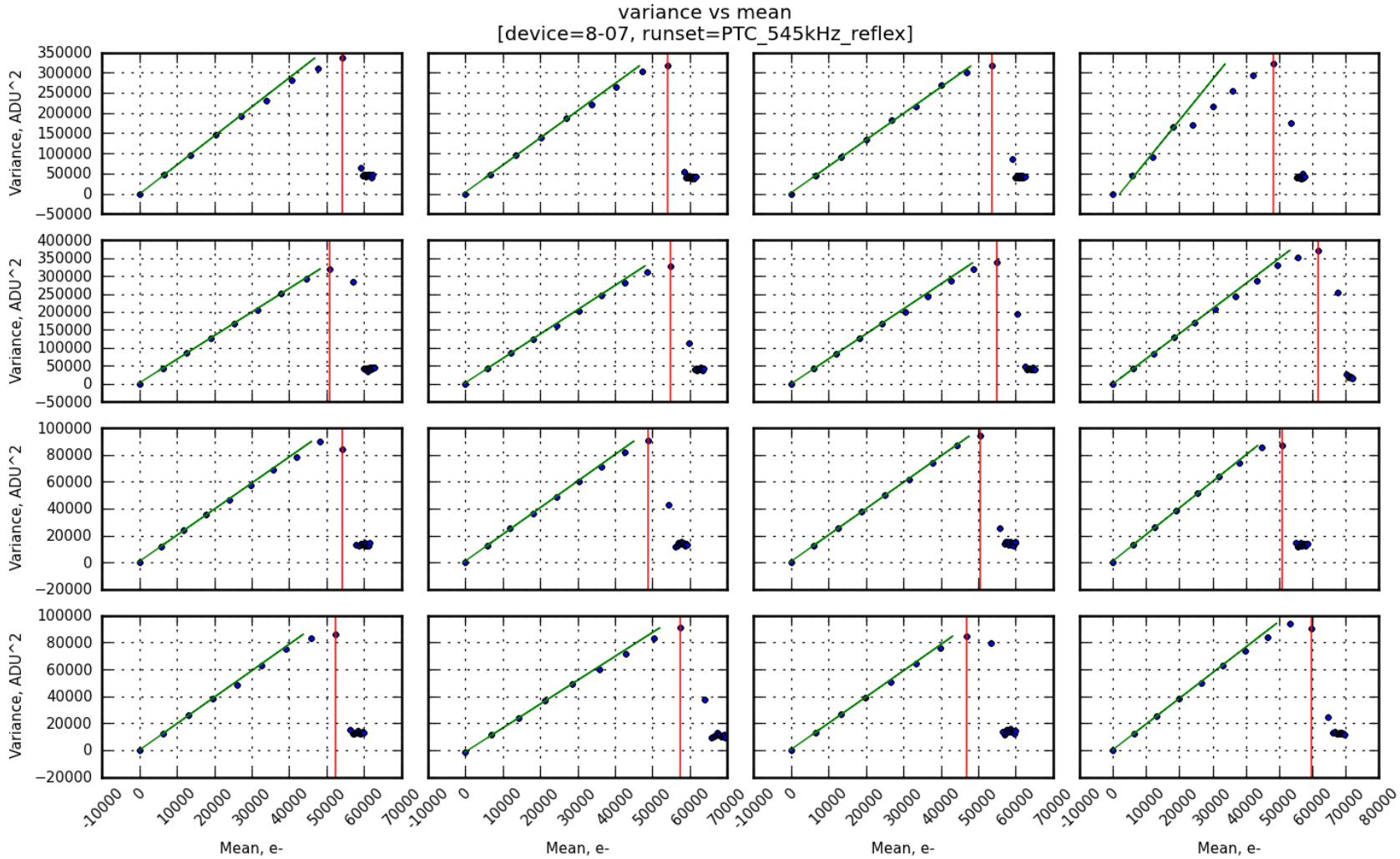


Gain dispersion 1.5%

Single cluster (zoom)



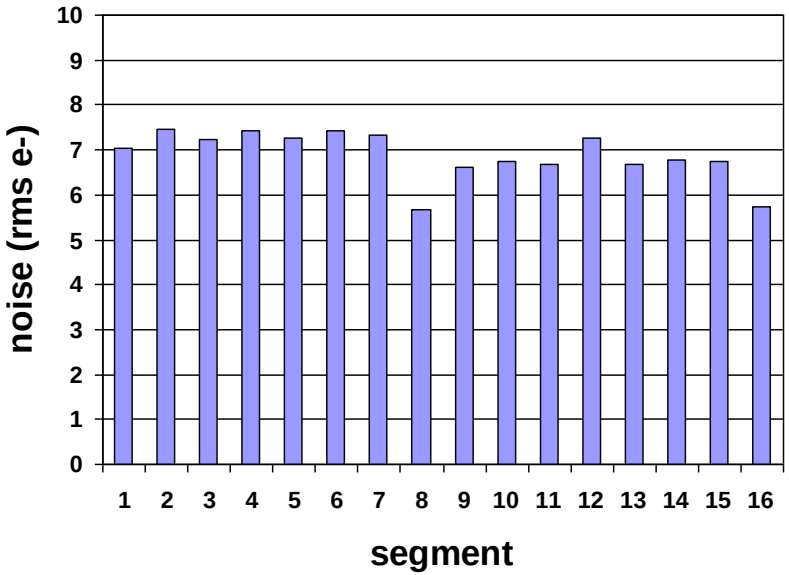
photon transfer



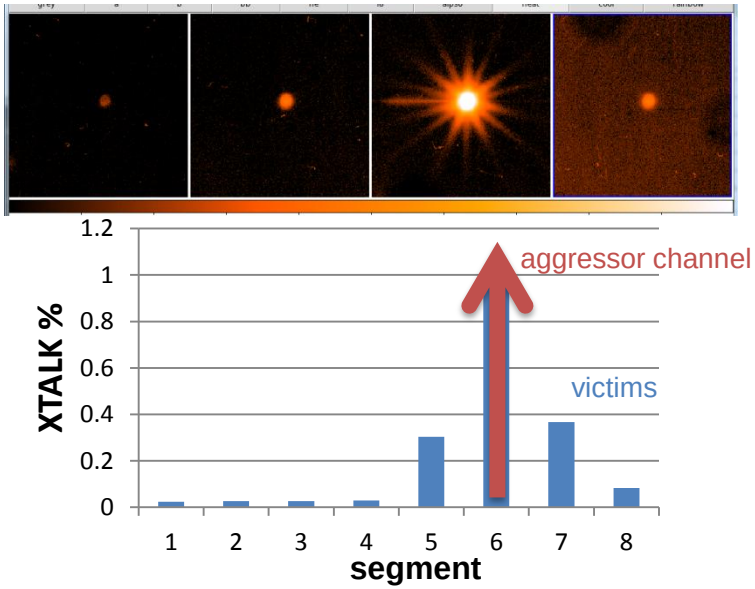
Full well capacity of CCD is ~140ke-; dynamic range of REB1 limited to ~ 60-80ke$^-$ withcurrent gain setup

Noise, crosstalk, nonlinearity

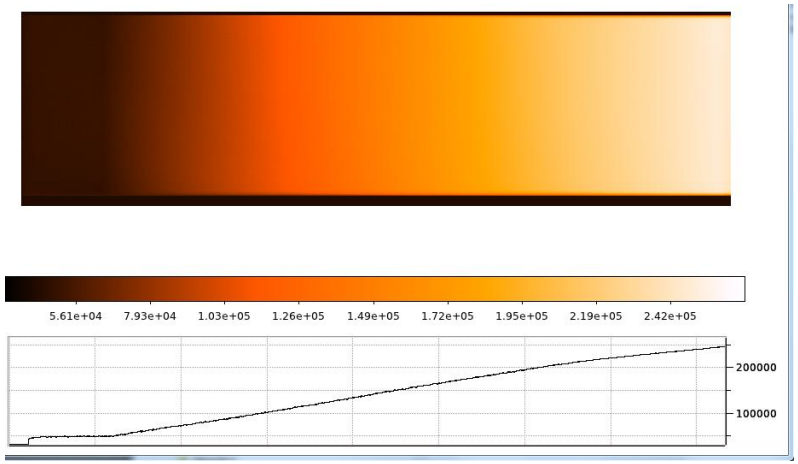
480kpix/s

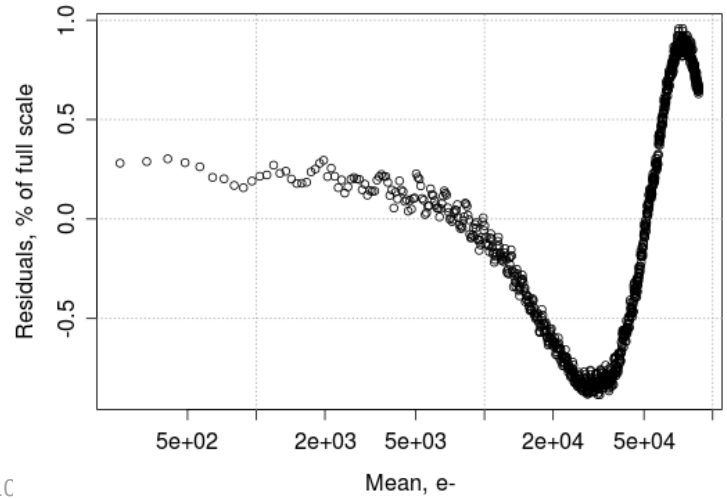


** REB noise is 1.5 -2.2 e-*



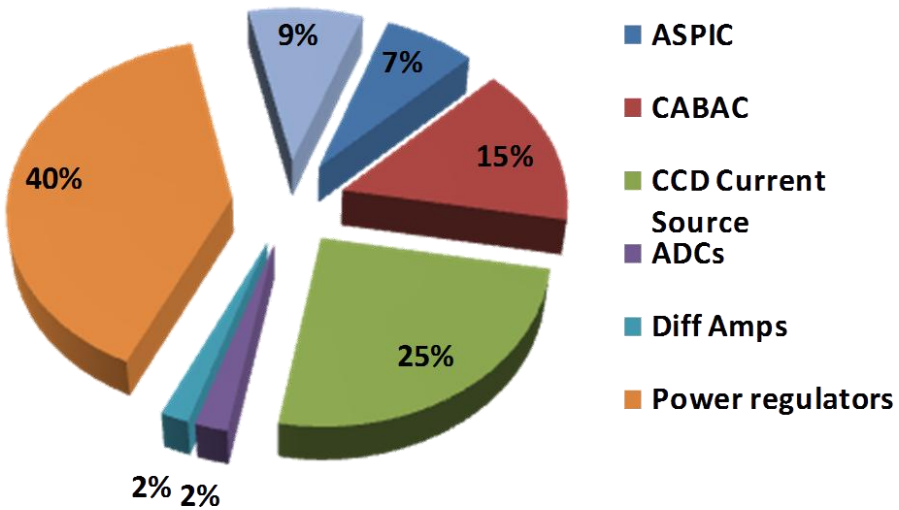
** REB xtalk is ≤ 0.04%*





Electronics power dissipation

Source	Peak power dissipation, W	
	Per REB	Per channel
CCD current source	4.21	.088
Video ASIC	1.20	.025
Clock/bias ASIC	2.52	.053
ADC differential buffer/driver	0.31	.0065
ADC	0.36	.0075
Power Regulators	6.63	.138
Control FPGA	1.50	.031
TOTAL Electronics Power	**16.73**	**0.349**

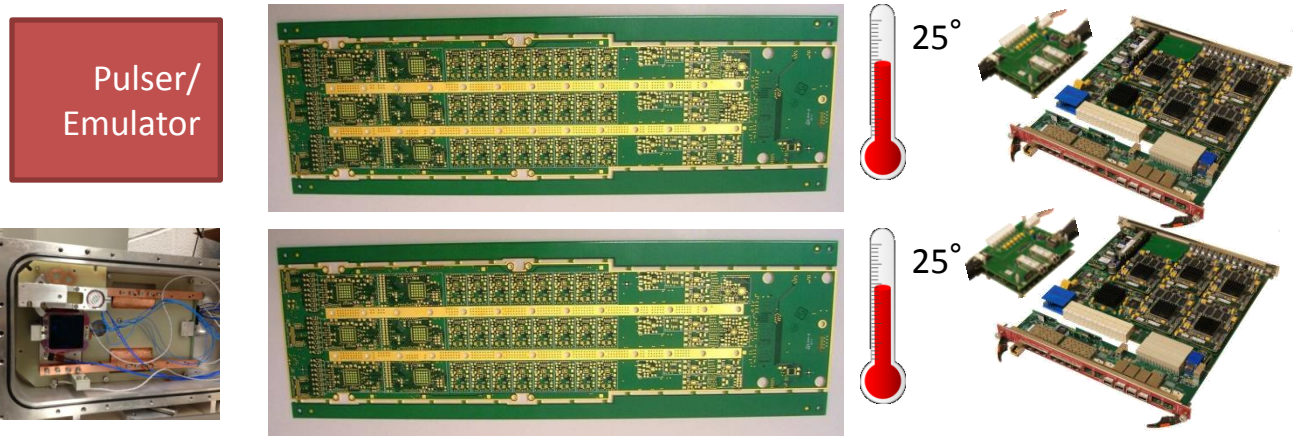


Measured (on single-stripe REB)	
Expose	6.98W
Readout	8.96W

Ave(LSST cadence) ~ 7W
30% power common
≈.35W/chan for fully-populated REB ✓

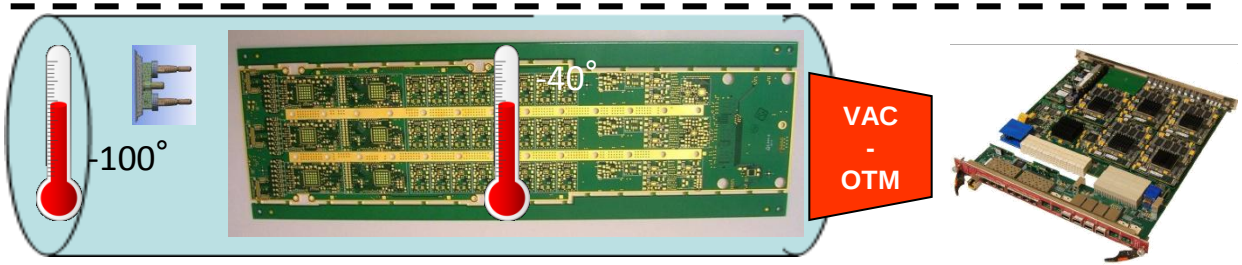
Next steps

1 REB only

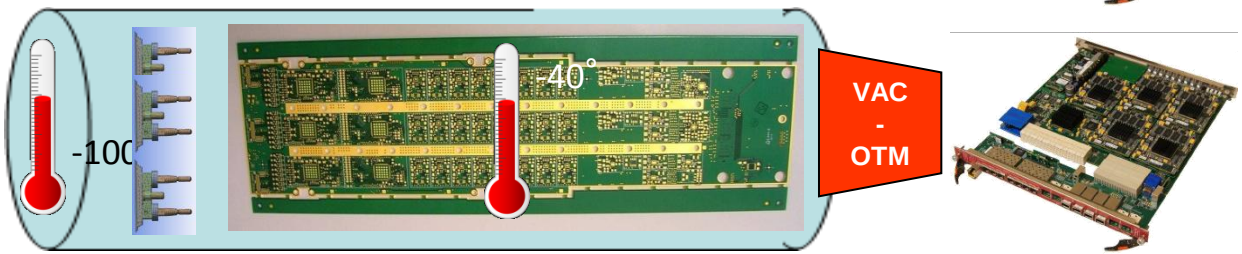


1 REB warm +
1 CCD

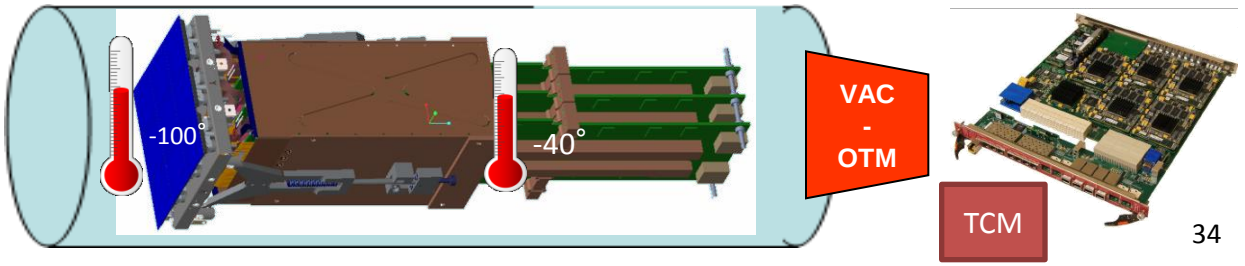
1 REB + 1 CCD in
cryostat



1 REB + 3 CCDs in
cryostat

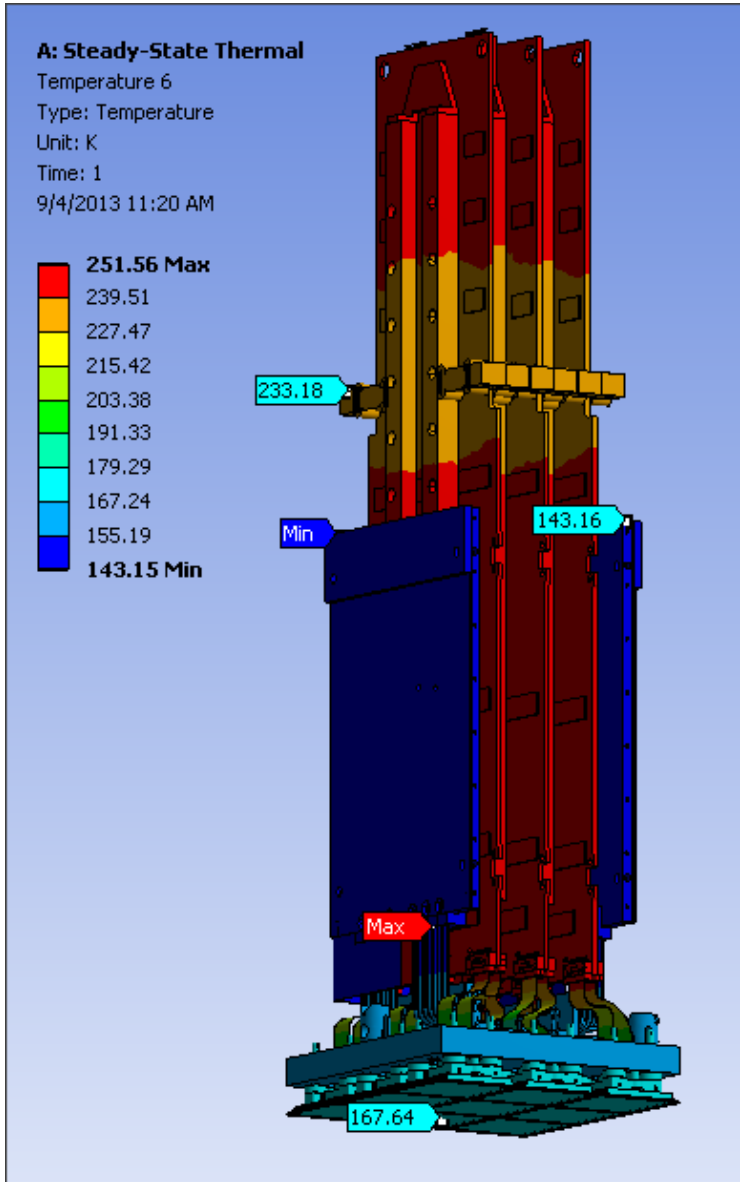


Full RTM: 9 CCDs, 3
REBs

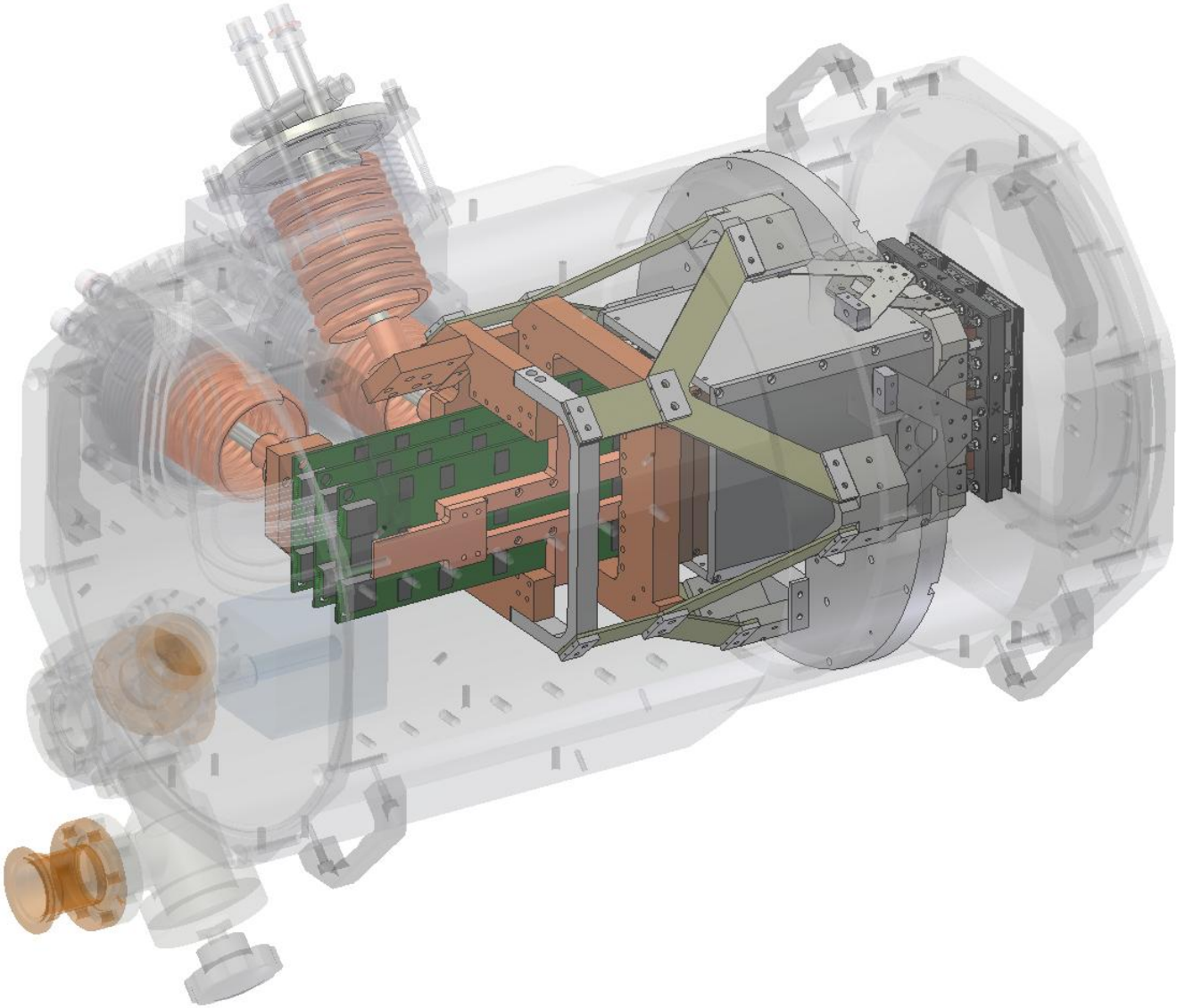


Robust FEA Model: Complete RTM Assembly

- Nominal thermal loads from: electronics, radiation from L3, conduction through materials, etc.
- Expected thermal contact at all interfaces
- Raft rim heaters at 1.0 Watts each (slightly less than ½ max)
- Cryoplate at 143K
- ColdPlate at 233K



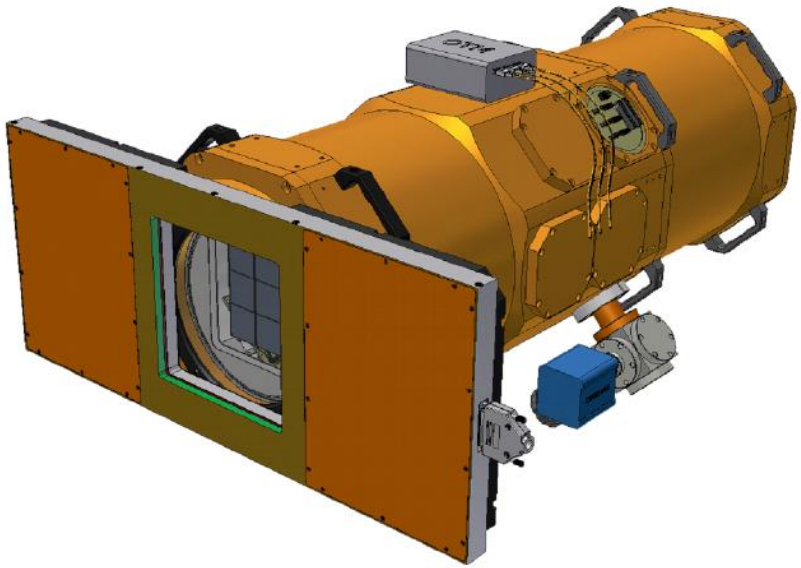
mechanics and thermal

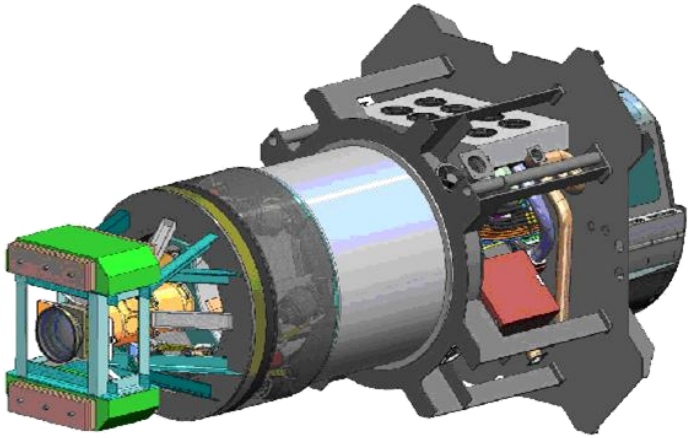


vacuum enclosure under test

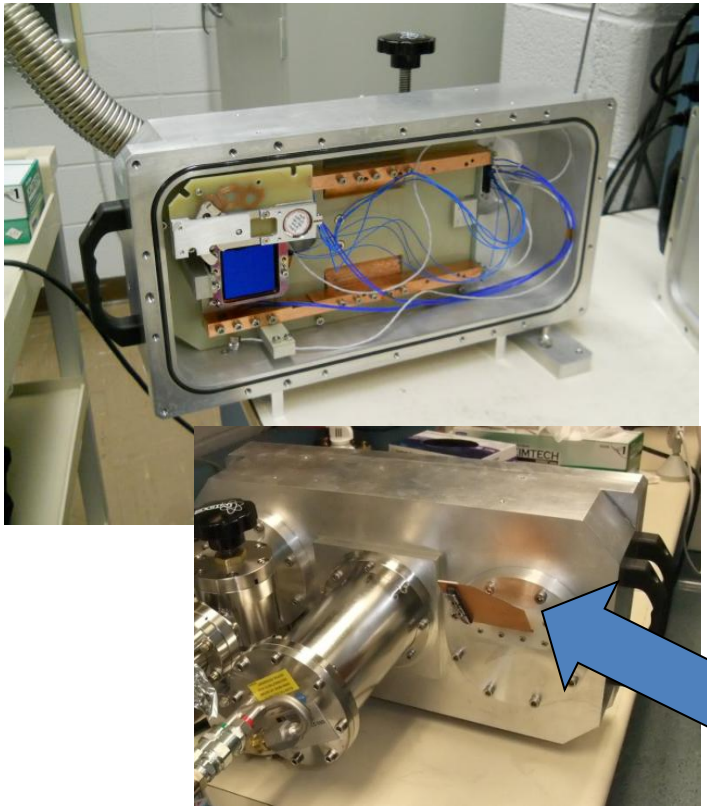
proposed LSST commissioning camera (ComCam)

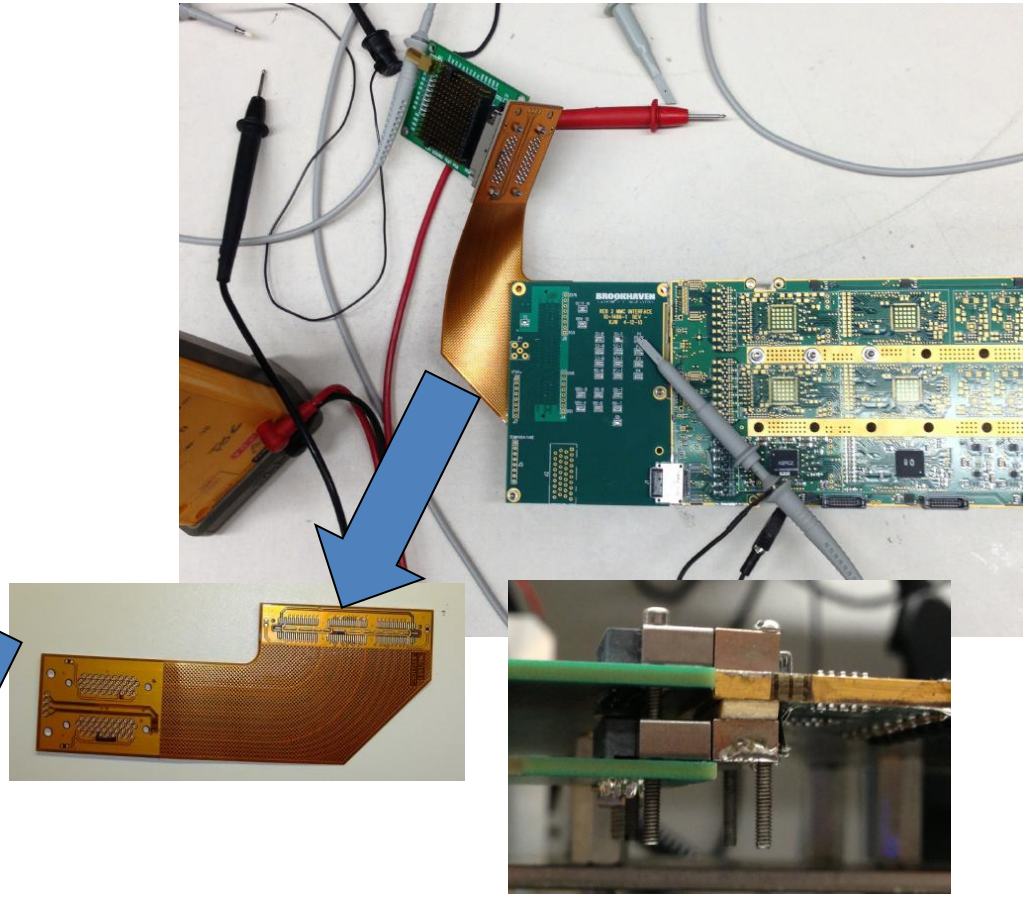
- **Raft test cryostat with 9 engineering-grade CCDs, full electronics and DAQ, LN2 cooling, shutter, corrector + filters**
- **Installed on camera hexapod/rotator at LSST 3-mirror focus prior to full Camera readiness**
- **30 arcmin field on-axis**
- **Early commissioning studies**





REB + CCD test bench components





Multimode cryostat with CCD, xray source, thermal control and monitoring

REB with adapter PCB and through-vacuum rigidflex cable