

Register Transfer Level Approaches to Radiation Hardening



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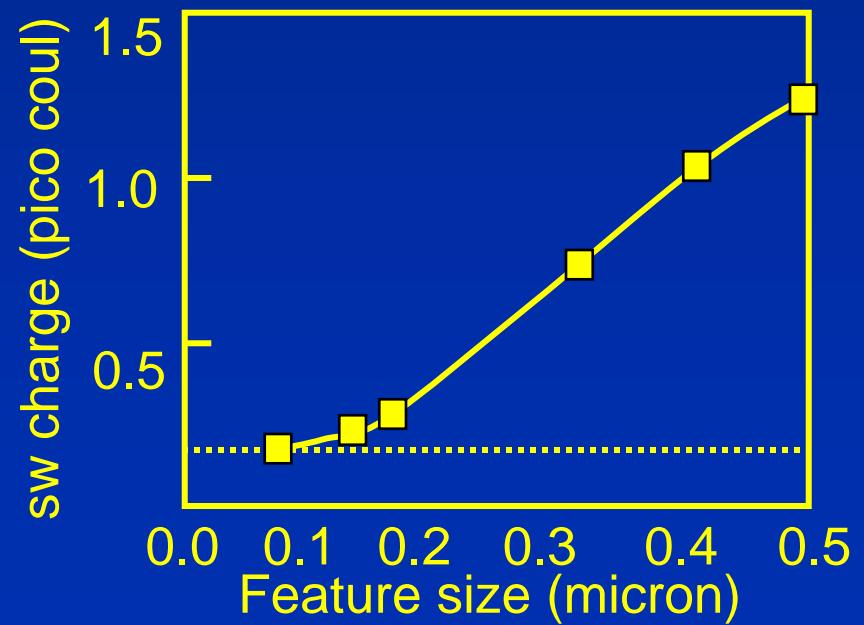
Outline

- Radiation Hardening: Motivation
- Register Transfer Level Design
- RT Level Radiation Hardening
- Experimental Results
- Concluding remarks

Motivation

- Increased likelihood of single event upsets (SEU)
 - ↳ small node cap. + small voltage \Rightarrow small quantities of stored charge
 - ↳ small quantities of energy is sufficient to introduce SEUs
 - ↳ energy of neutrons at sea levels can cause SEUs
 - ↳ effect of neutrons at flight altitudes is even worse

Minimum sized CMOS inverter
Load Capacitance = 2x Gate Capacitance



Motivation

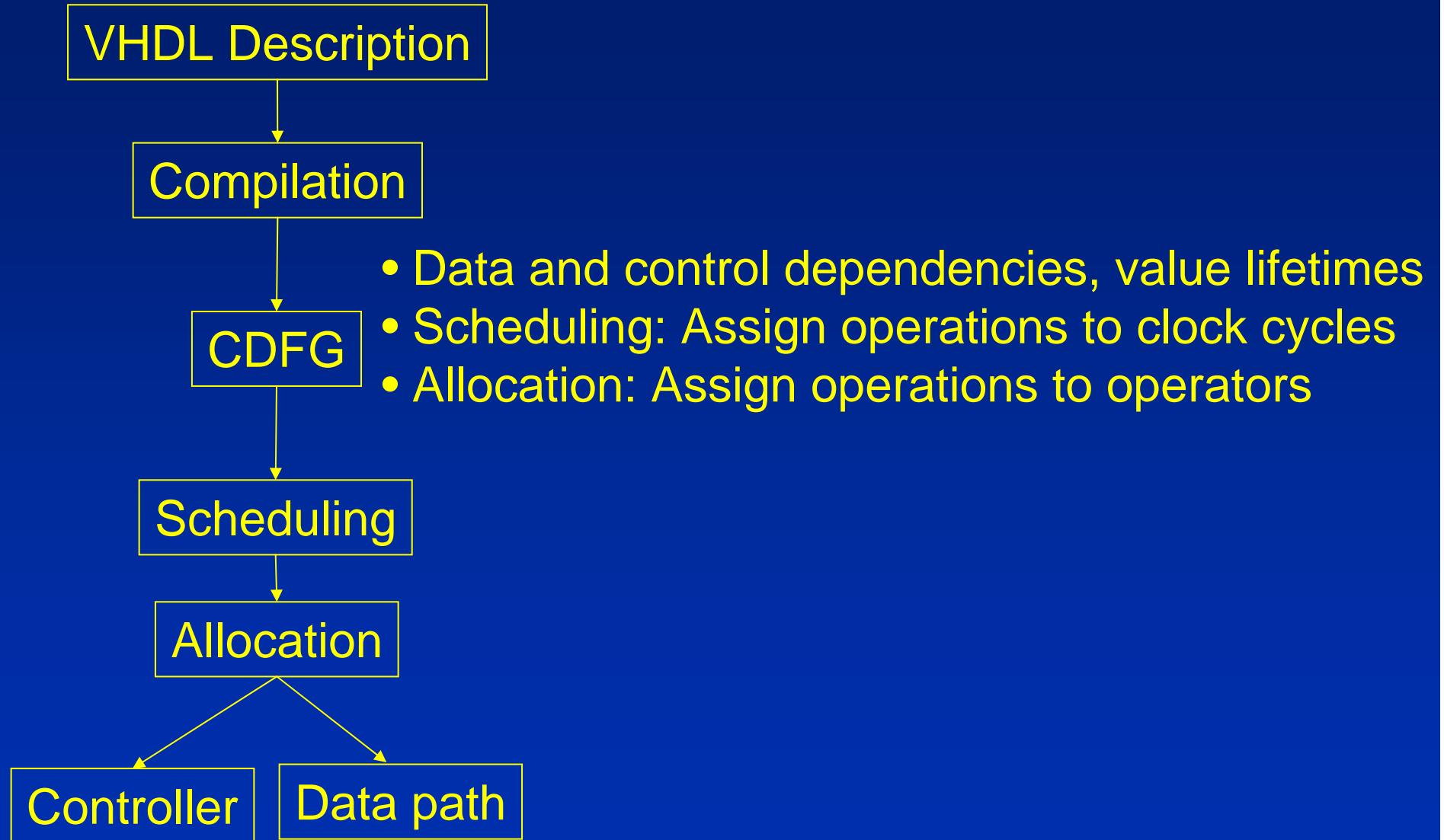
- Increased likelihood of SEU propagation
 - ↳ At Ghz, THz clock rates, SEU effects propagate through combinational logic.
 - ↳ Increased clock frequency \Rightarrow higher prob. of latching an SEU \Rightarrow increased window of vulnerability
- Small interval between successive clock pulses
 - ↳ Pulse width of SEUs pico-seconds
 - ↳ Not enough time for SEU transient to die down
 - ↳ Strong as well as weak SEU transients will be latched

Motivation

- V_t does not scale well in VDSM technologies. If subthreshold slope is $\sim 80\text{mV/decade}$
 - ↳ on-off current ratio of 6 $\Rightarrow V_t = 0.48 \text{ V}$
 - ↳ on-off current ratio of 3 $\Rightarrow V_t = 2.4 \text{ V}$
 - ↳ Low on-off current ratio \Rightarrow Leakage current \uparrow
 - \Rightarrow Noise margin \downarrow
 - \Rightarrow tolerance to variation in device params \downarrow
 - \Rightarrow Sensitivity to α -particles \uparrow

source: A. H. Johnston, “Radiation effects in advanced microelectronics technologies”, IEEE Trans on Nuclear Science, vol. 45m no. 3 Jun 1998.

RT Level Design Flow



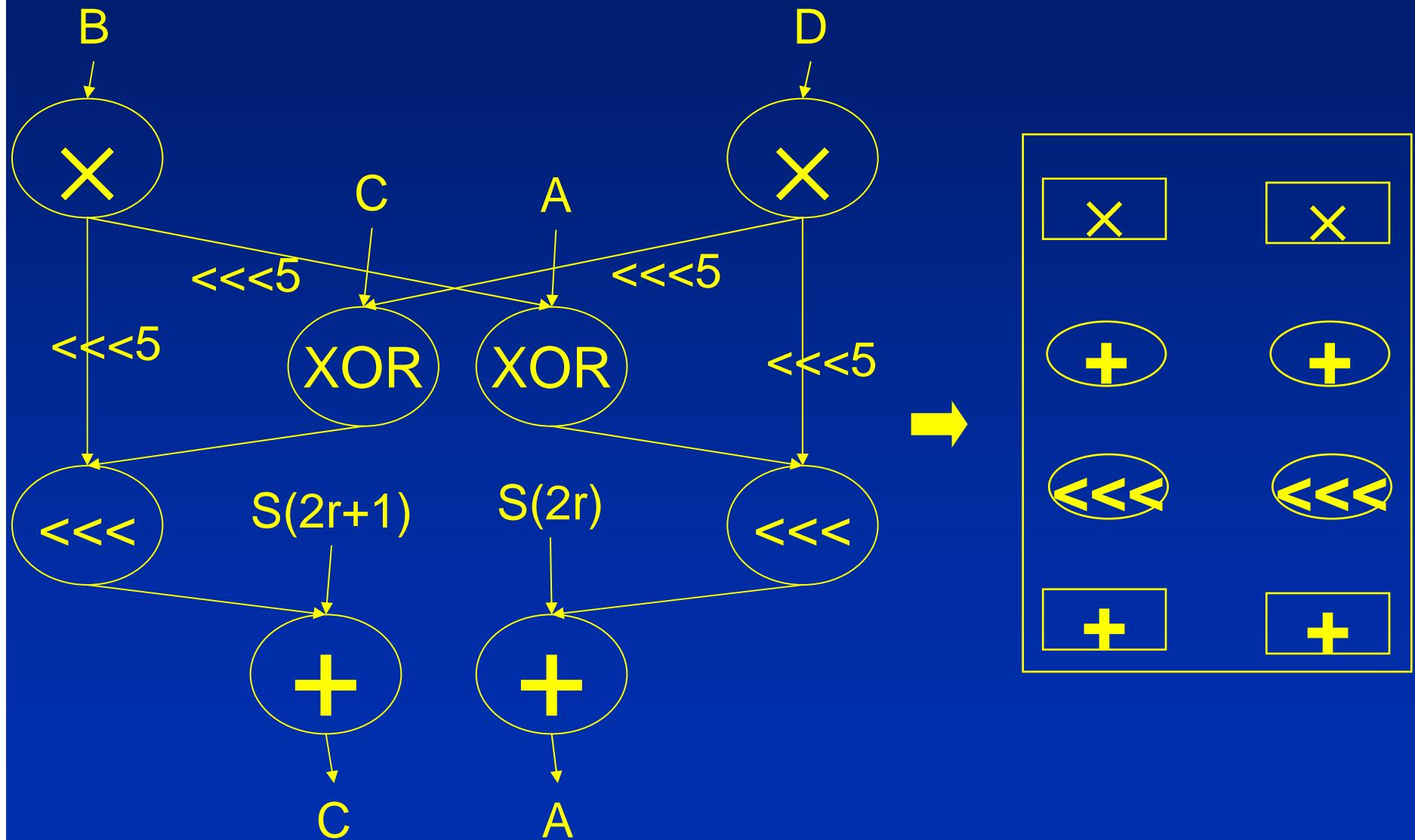
RC6 Encryption Algorithm

```
B = B + S[0];
D = D + S[1];
for i = 1 to 20 do {
    t = (B*(2B+1)) <<< 5;
    u = (D*(2D+1)) <<< 5;
    A = ((A xor t) <<< u) + S[2i];
    C = ((C xor u) <<< t) + S[2i +1];
    (A, B, C, D) = (B, C, D, A);
}
A = A + Key [42];
C = C + Key [43];
```

Input: 128-bit plain text stored in 32-bit registers A
round keys Key[0], Key[1], ..., Key[43]

Output: 128-bit cipher text

RT Level Design (step 1): RC6 CDFG

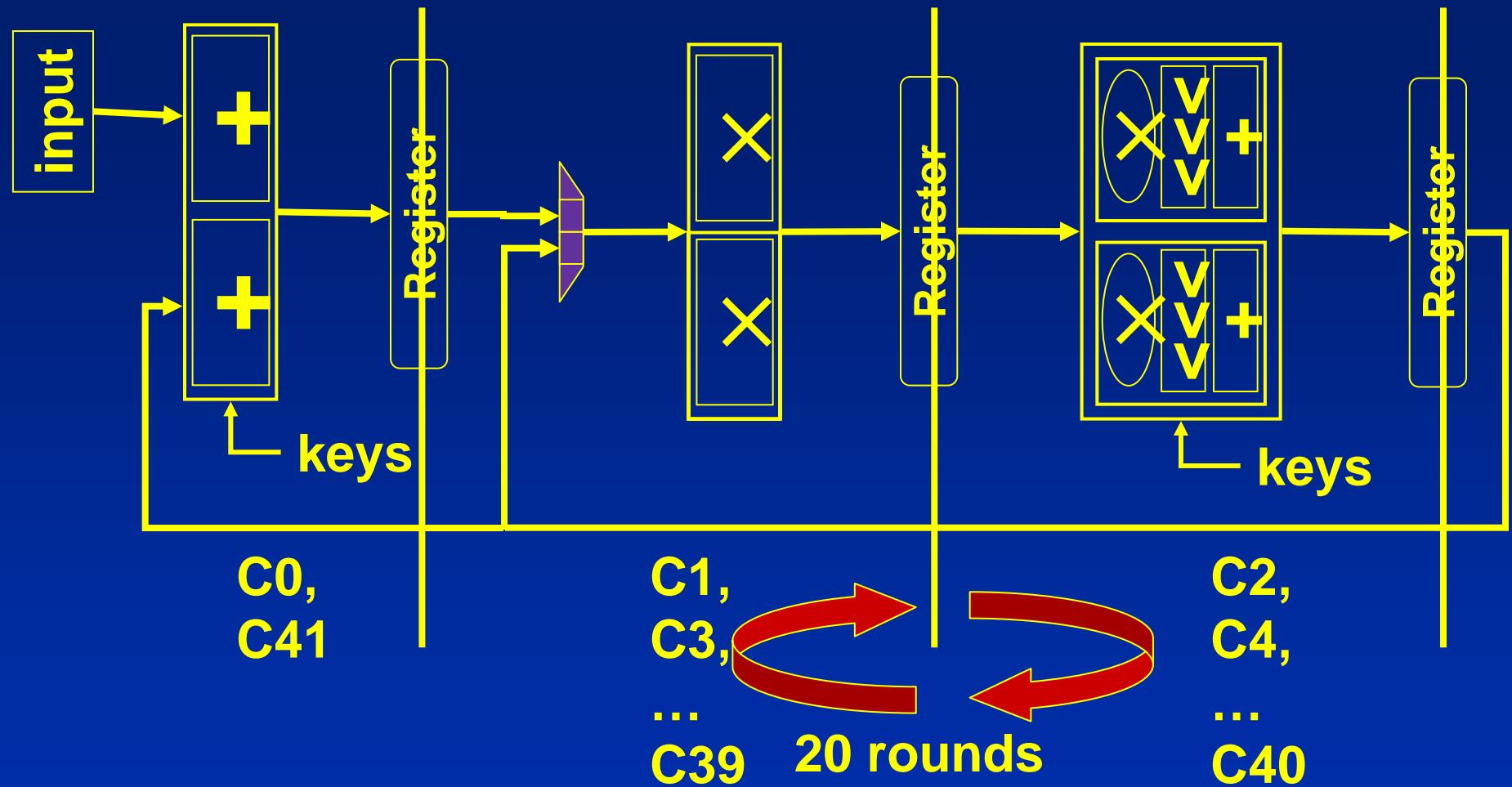


RT Level Design (step 2):Scheduling

	M1	M2	O1	O2
C1	X	X		
C2			+<<<+	+<<<+
C3	X	X		
C4			+<<<+	+<<<+
C5	X	X		
C6			+<<<+	+<<<+

Resource constraint: 2x, 2 [$\oplus <<<+$] operators
2 cycles/round x 20 rounds = 40 cycles
2 cycles each for pre and post whitening = 4 cycles

RT Level Design (step 3): Allocation



Fold RT Level schedule:
3 additional registers and 1 multiplexer

FPGA Implementation

Data Latency	44 cycles
Area	3193 slices
Frequency	26.818 MHz
Throughput	312.1 Mbps

RT Level Radiation Hardening

- Concurrent Error Detection
- Recovery
- Faulty unit Diagnosis
- Reconfiguration around the faulty unit

RT Level Radiation Hardening (CED)

- Time Redundancy based CED
 - Idle Cycles Based CED
 - Data diversity based CED
 - Allocation diversity based CED
- Hardware redundancy based CED

RT Level Radiation Hardening (CED)

Idle Cycles Based CED

Idle Cycles in a Design

	M1	M2	O1	O2
C1	X	X		
C2			+<<<+	+<<<+
C3	X	X		
C4			+<<<+	+<<<+
C5	X	X		
C6			+<<<+	+<<<+

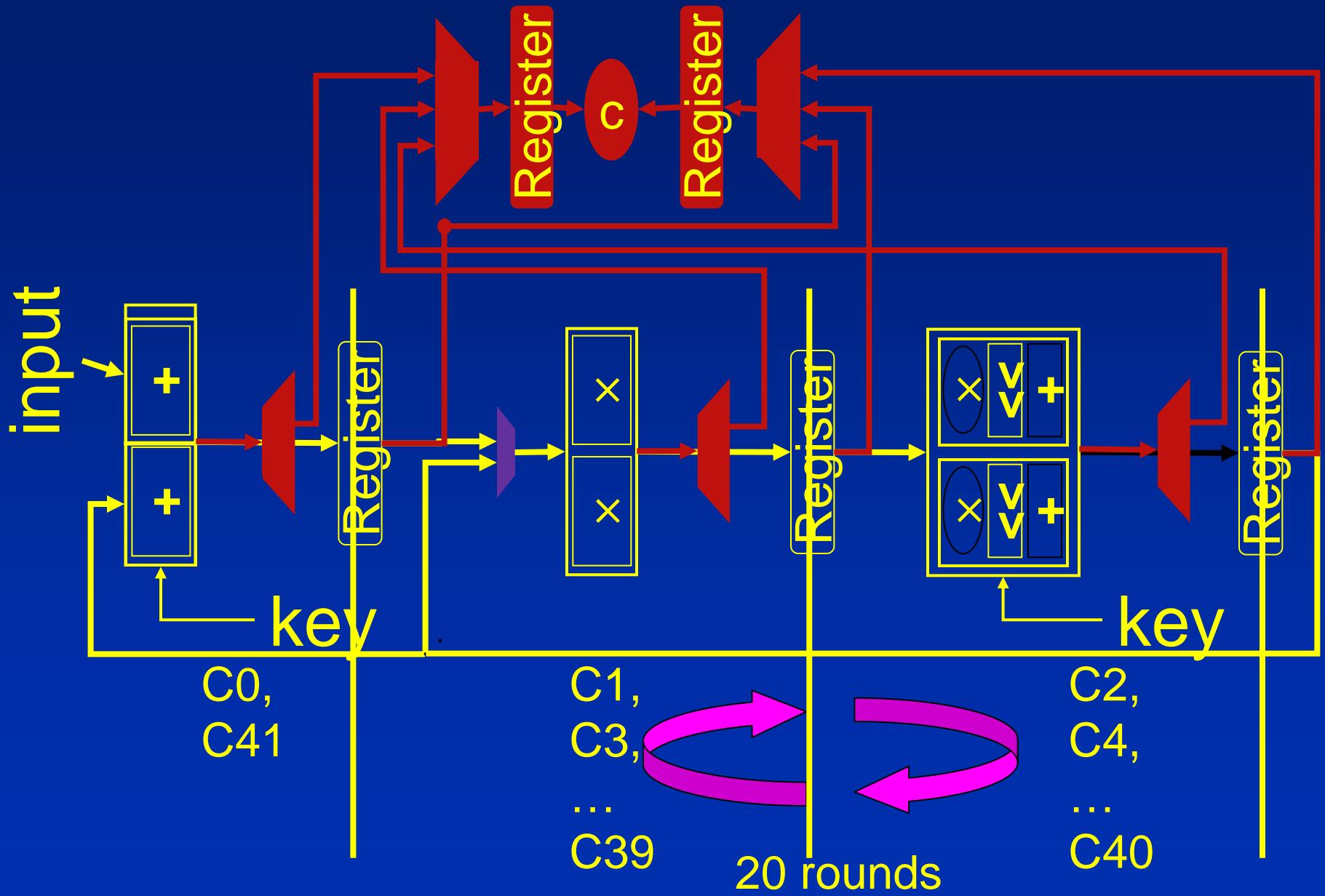
RC6 schedule using 2 multipliers and 2 [$\oplus <<<+$] ops
Multipliers idle in C2, C4, ...
[$\oplus <<<+$] ops idle in C1, C3, ...

Use Idle cycles for CED

	M1	M2	O1	O2
C1	X	X		
C2	X	X	$\otimes <<+$	$\otimes <<+$
C3	X	X	$\otimes <<+$	$\otimes <<+$
C4	X	X	$\otimes <<+$	$\otimes <<+$
C5	X	X	$\otimes <<+$	$\otimes <<+$
C6	X	X	$\otimes <<+$	$\otimes <<+$

Re-do multiplications in C1 in C2 and compare

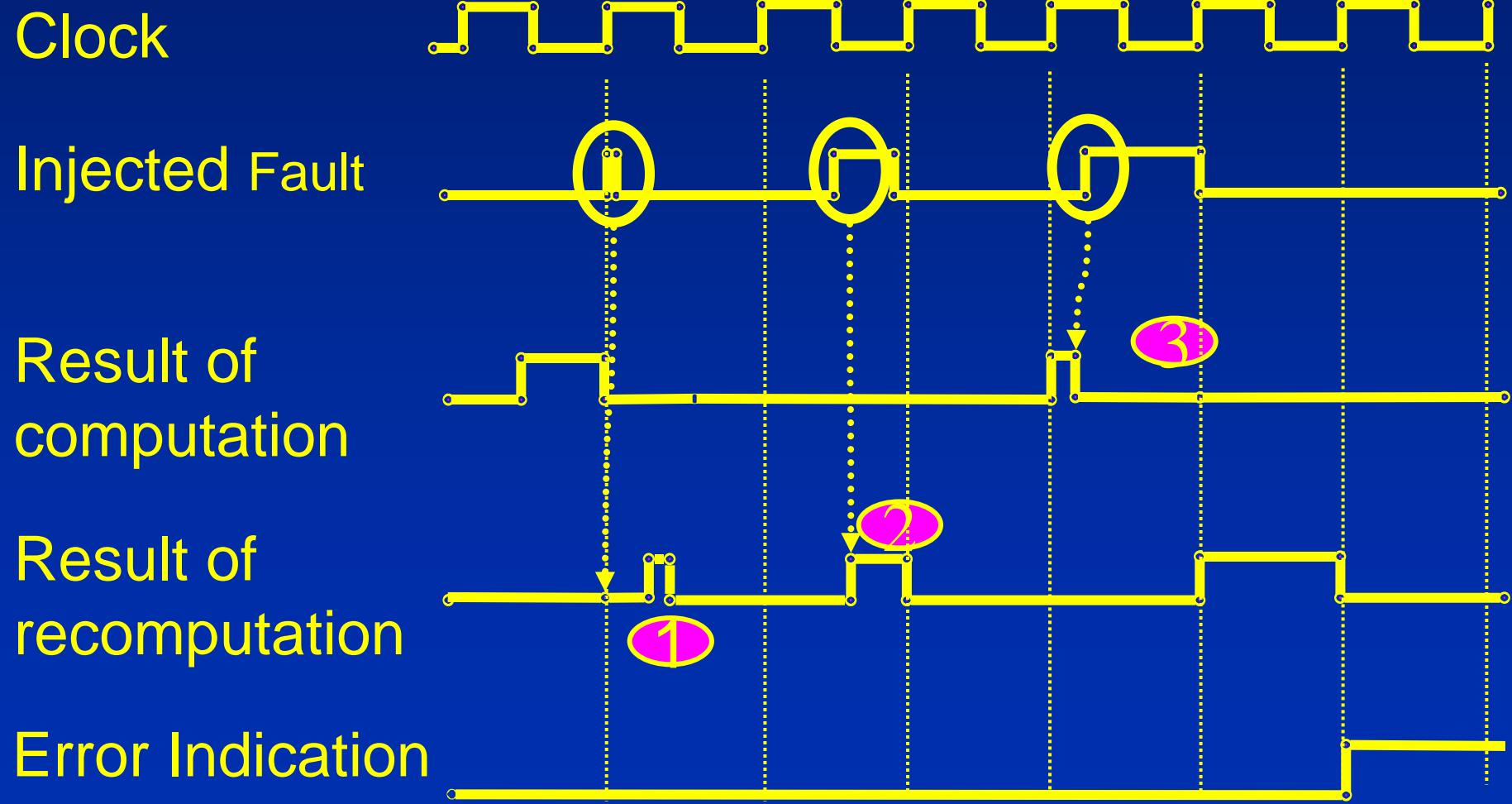
RC6 Datapath with idle cycles based CED



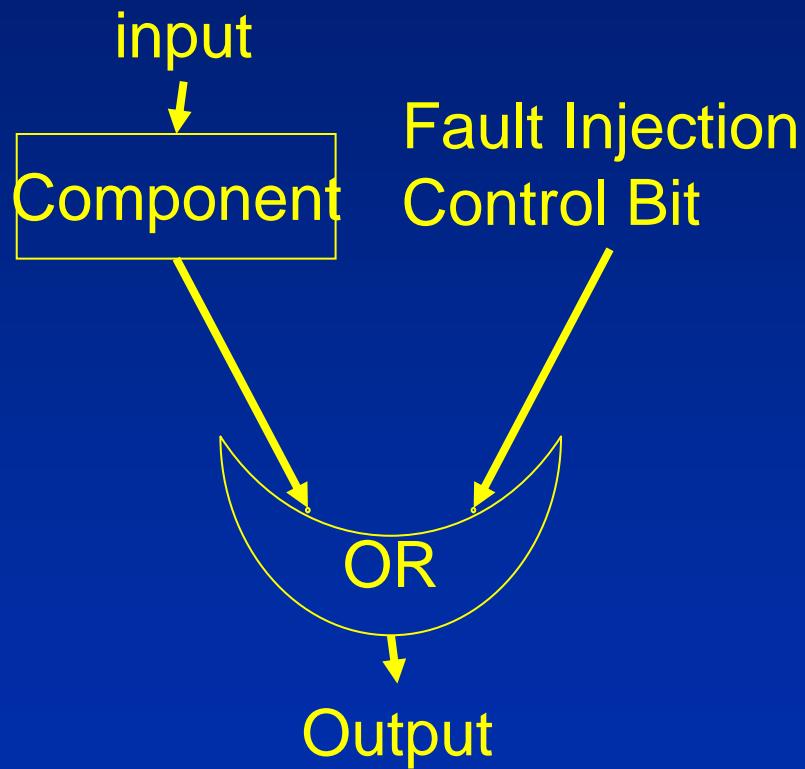
RC6 Implementation

FPGA Implementation	Basic design	CED design	
		Hardware Duplication	Idle cycles
Full duplex	Yes	Yes	Yes
2-stage pipelining	Yes	Yes	No
Data Lat. (Cycle)	44	45	44
FD Lat. (Cycle)	N/A	1	2
Area (slices)	3193	6277	4673
Frequency (Mhz)	26.818	26.680	21.143
Throughput (Mbps)	312.1	303.6	123.0

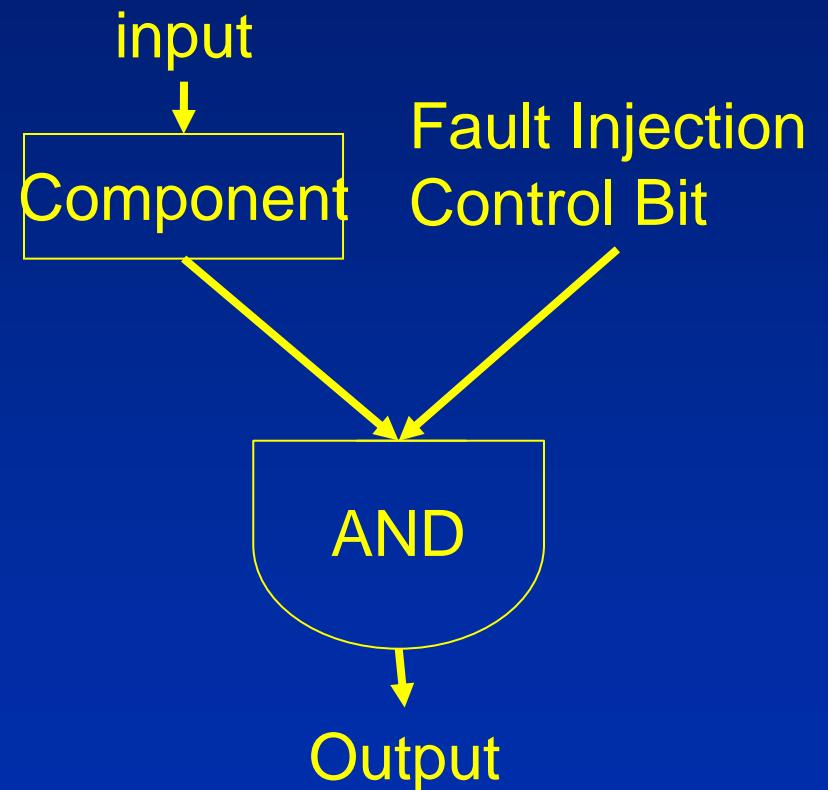
RC6 Fault injection study: some CED scenarios



RC6 Fault Injection

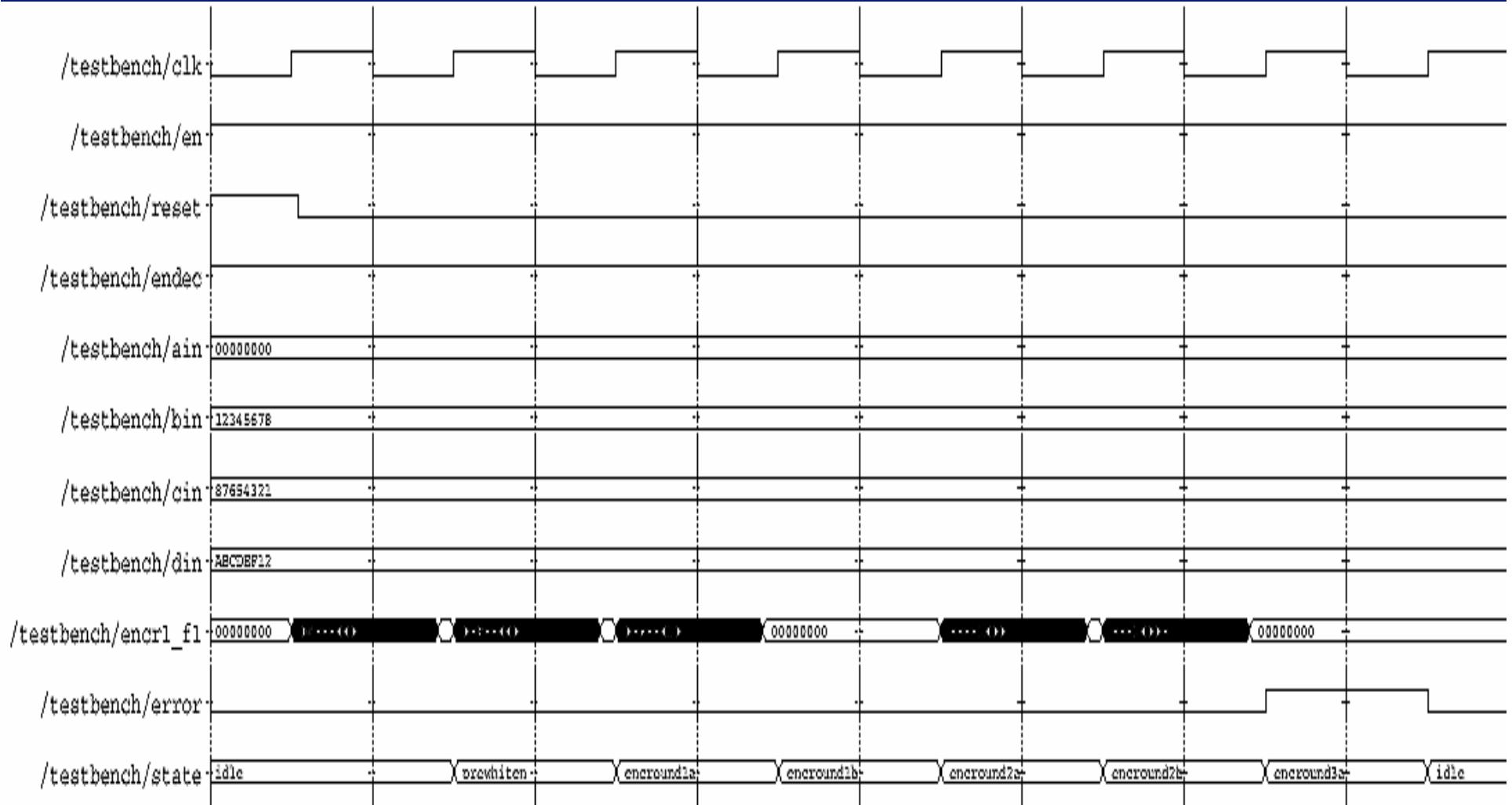


Inject stuck-at-1 fault



Inject stuck-at-0 fault

RC6 Fault injection simulation

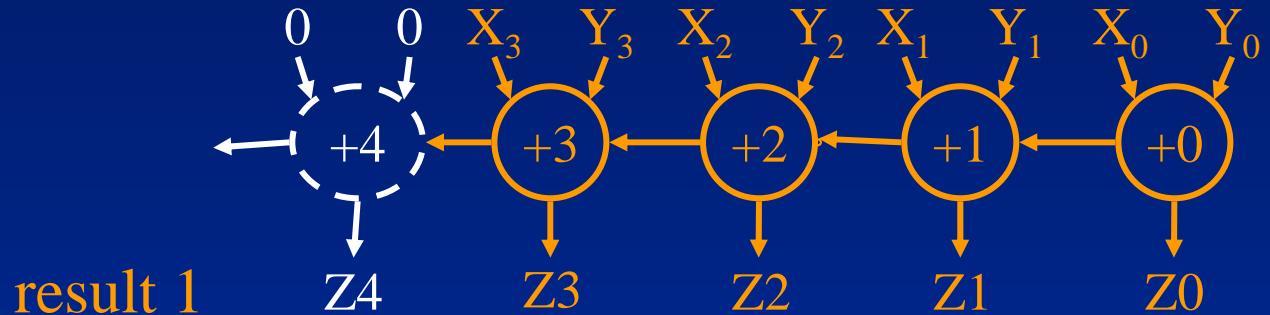


RT Level Radiation Hardening

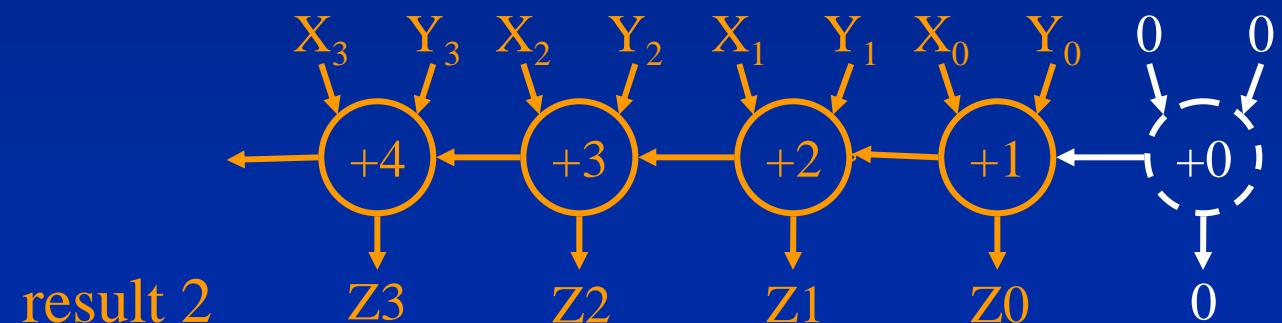
Data Diversity based CED

Recomputing with Shifted Operands (Logic RESO)

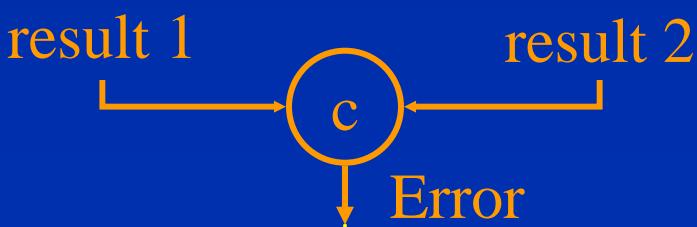
1. Perform basic computation



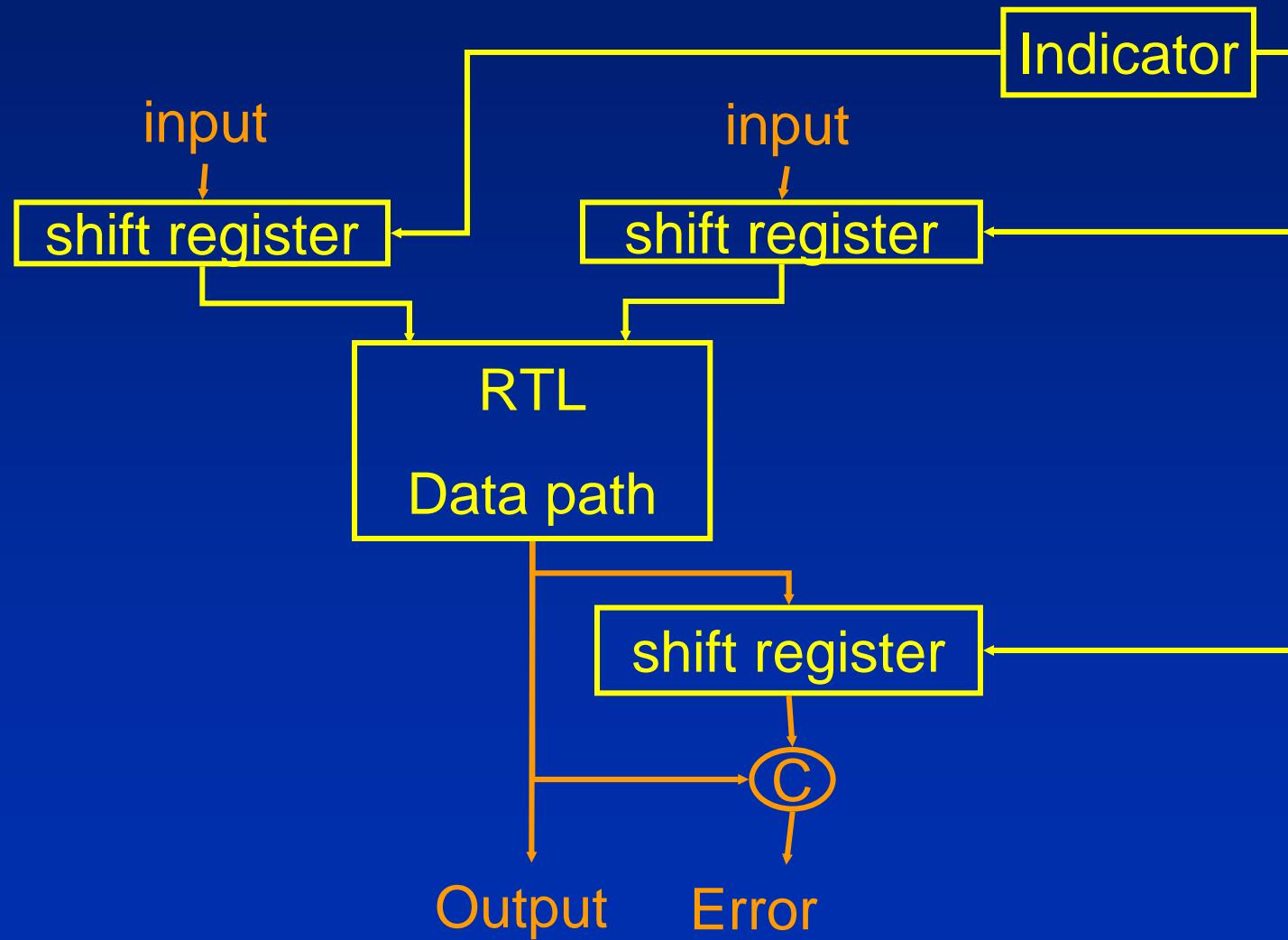
2. Repeat computation with 1-bit shifted operands



3. Compare results

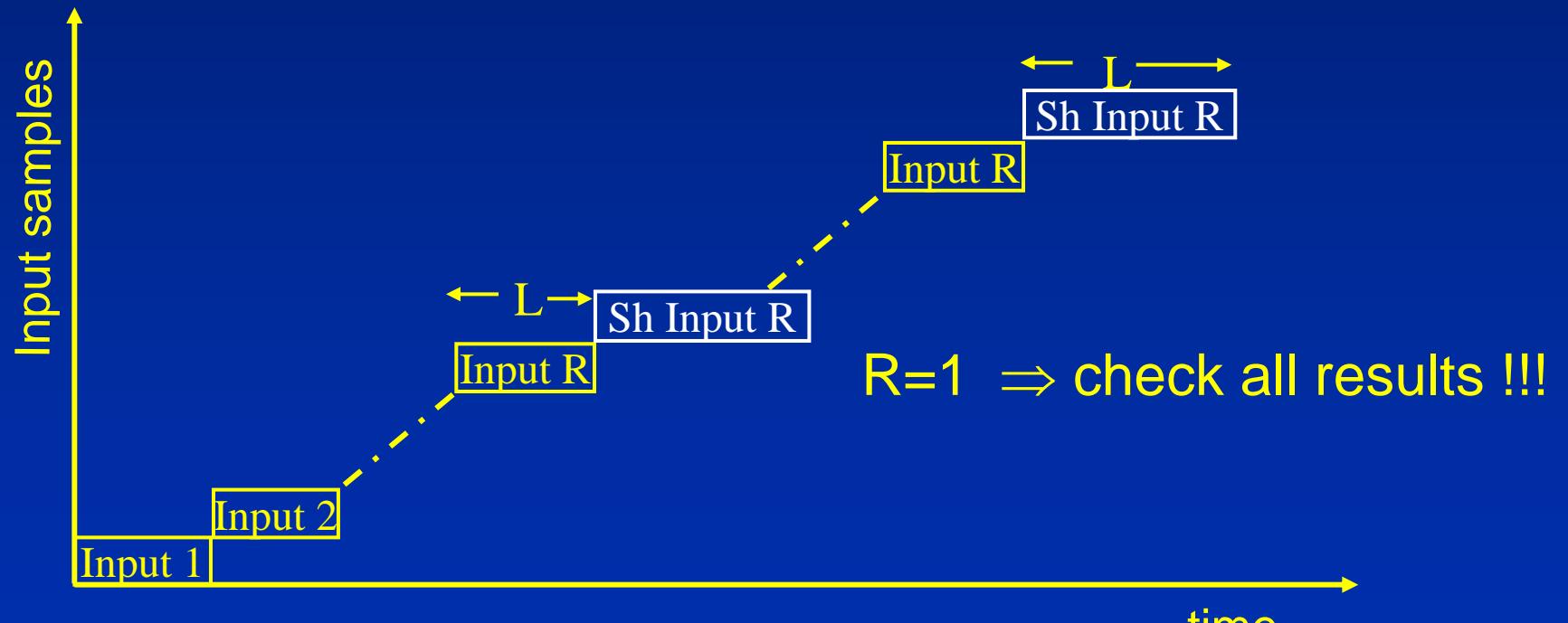


RT Level Data Diversity based CED



Checking Ratio (R)

$$\text{Checking Ratio} = \frac{\# \text{ of results computed}}{\# \text{ of results checked}}$$



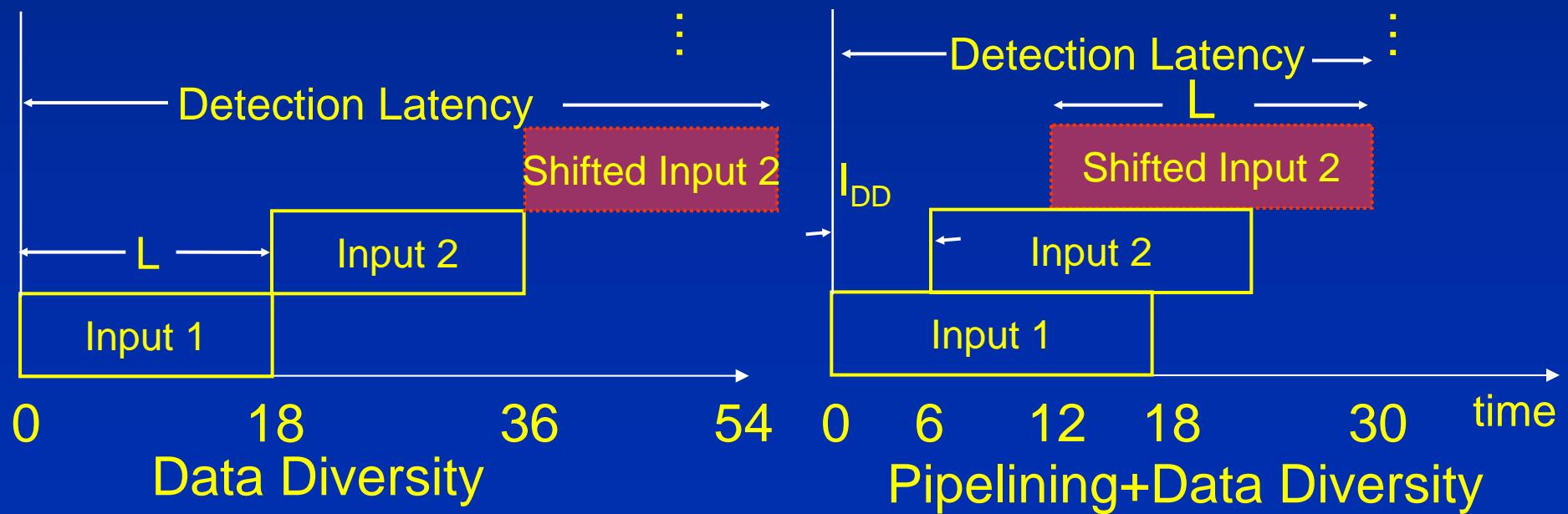
$L = \# \text{ of clock cycles per iteration}$

RT Level Data Diversity

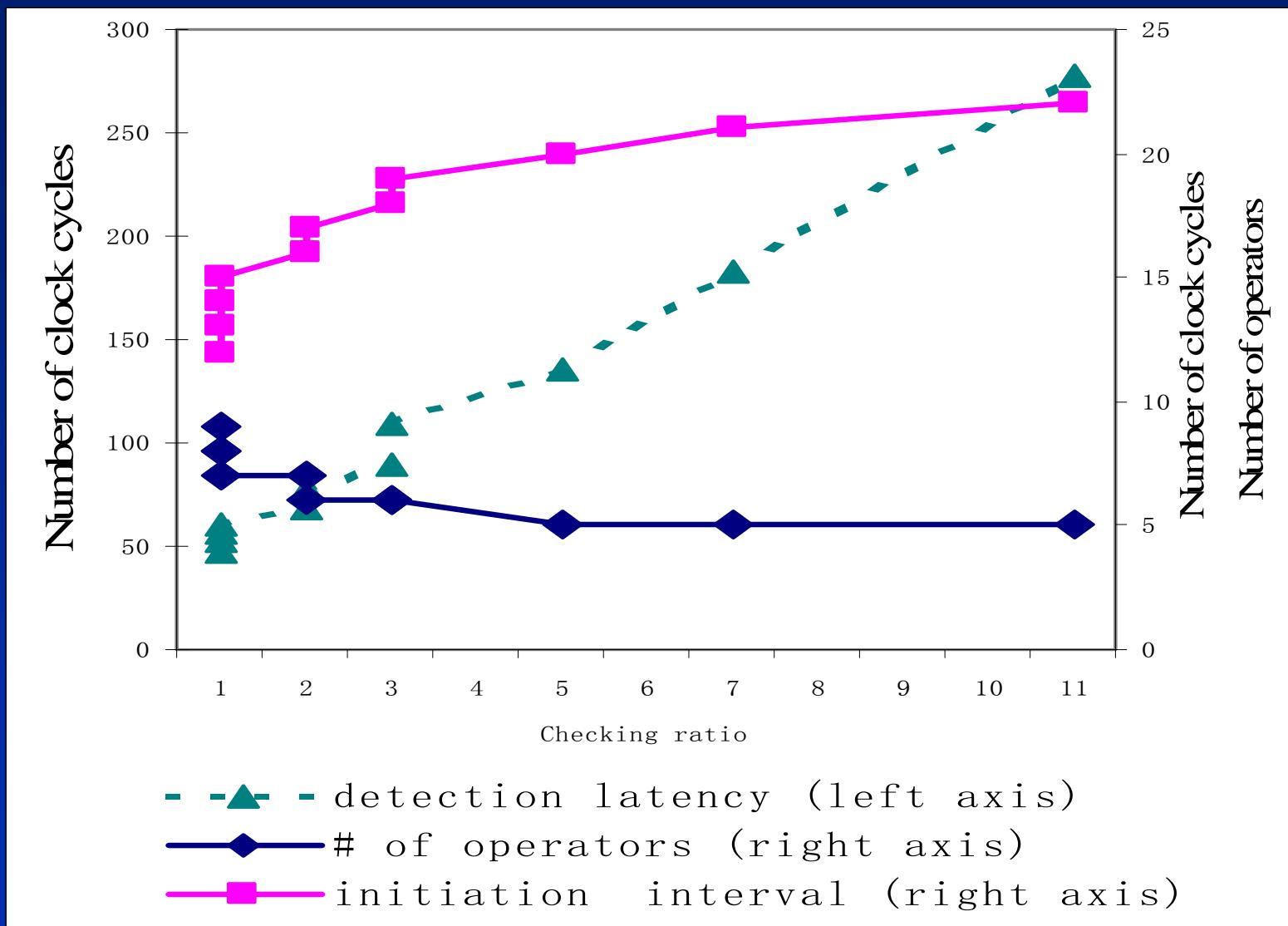
- Good points
 - ↳ Does not use fault tolerant logic operators
 - ↳ # of comparison(s) are reduced (checking operations at the RT Level)
 - ↳ Supports hardware overhead vs. performance penalty vs. error detection latency trade-offs
 - ↳ By increasing checking ratio, time overhead can be reduced
 - ↳ Compared to duplication, area overhead is reduced
- Bad points
 - ↳ Large detection latency, $(R+1) \times L$
 - ↳ Extra registers are required

Data Diversity+Pipelining

- Reduces Error Detection Latency
- If $L=18$, $R=2$
 - ↳ Detection Latency = 54 cycles for basic DD $(R+1) \times L$
 - ↳ Detection Latency = 30 cycles for pipelining+DD with initiation interval $I = 6$ $(R \times I_{DD}) + L$



RT Level Design Diversity Tradeoffs



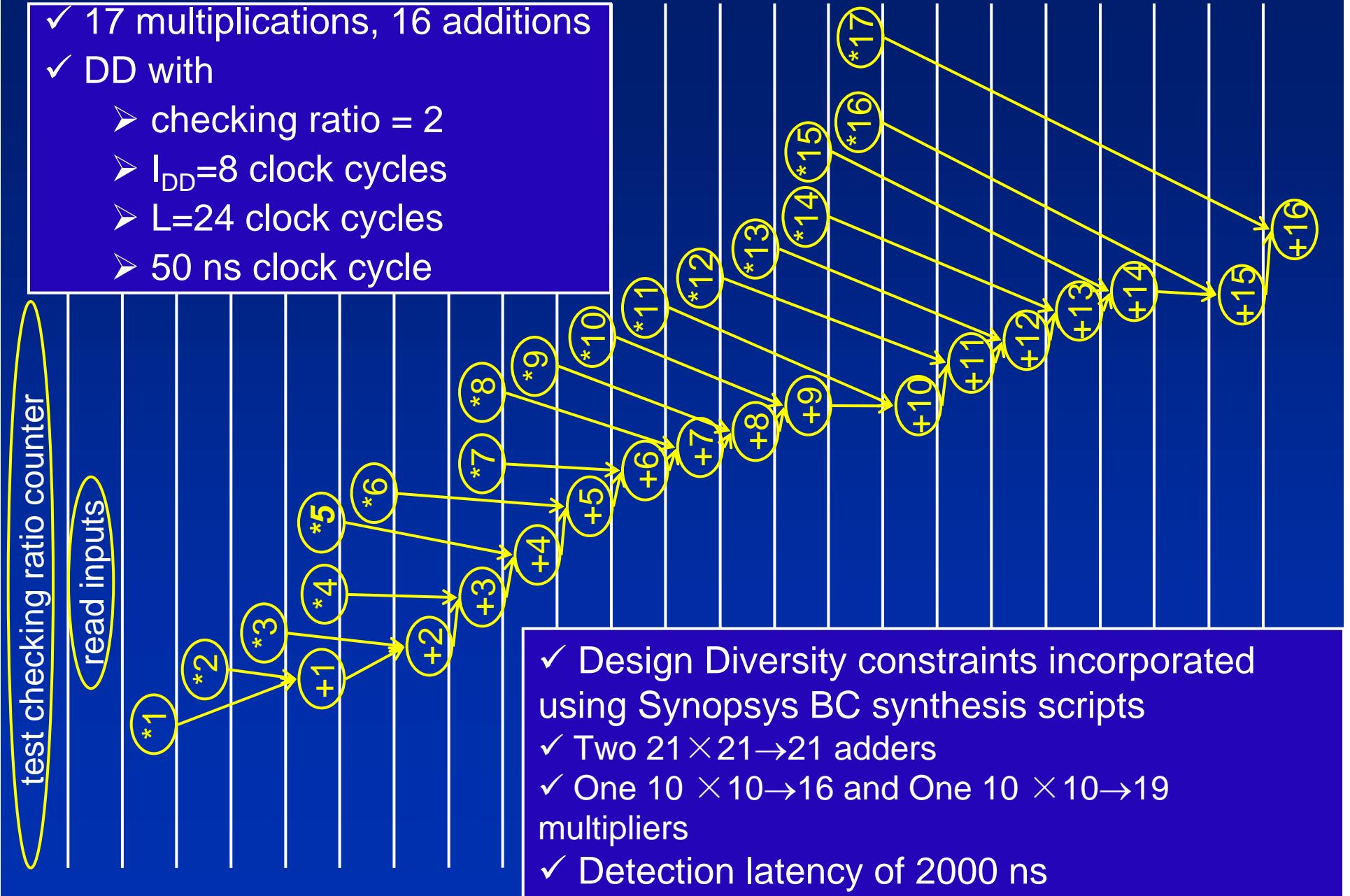
FIR Filter

50 ns clock	FIR $I=12, L=23$	Data Diversity-1 FIR $I_{DD}=6, R=1, L=24$	Data Diversity-2 FIR $I_{DD}=8, R=2, L=24$
Multipliers	$(8 \times 8 \rightarrow 14)$ $(9 \times 8 \rightarrow 17)$	$(10 \times 10 \rightarrow 16)$ $(10 \times 10 \rightarrow 17)$ $(10 \times 10 \rightarrow 19)$	$(10 \times 10 \rightarrow 16)$ $(10 \times 10 \rightarrow 19)$
Adders	2 ($19 \times 19 \rightarrow 19$)	3 ($21 \times 21 \rightarrow 21$)	2 ($21 \times 21 \rightarrow 21$)
Register bits	419	963	750
Combinational area (unit cells)	4051	6960 71.8%	5483 35.3%
Sequential area (unit cells)	4983	11506 130.9%	8635 73.3%
Total area (unit cells)	9034	18466 104.4%	14118 56.3%
Detection latency (ns)	-	$(6+24) \times 50 = 1500$	$(2 \times 8+24) \times 50 = 2000$

30.8% reduction in area at the expense of 33.3% increase in error detection latency.

FIR Filter Example - Schedule

- ✓ 17 multiplications, 16 additions
- ✓ DD with
 - checking ratio = 2
 - $I_{DD}=8$ clock cycles
 - $L=24$ clock cycles
 - 50 ns clock cycle

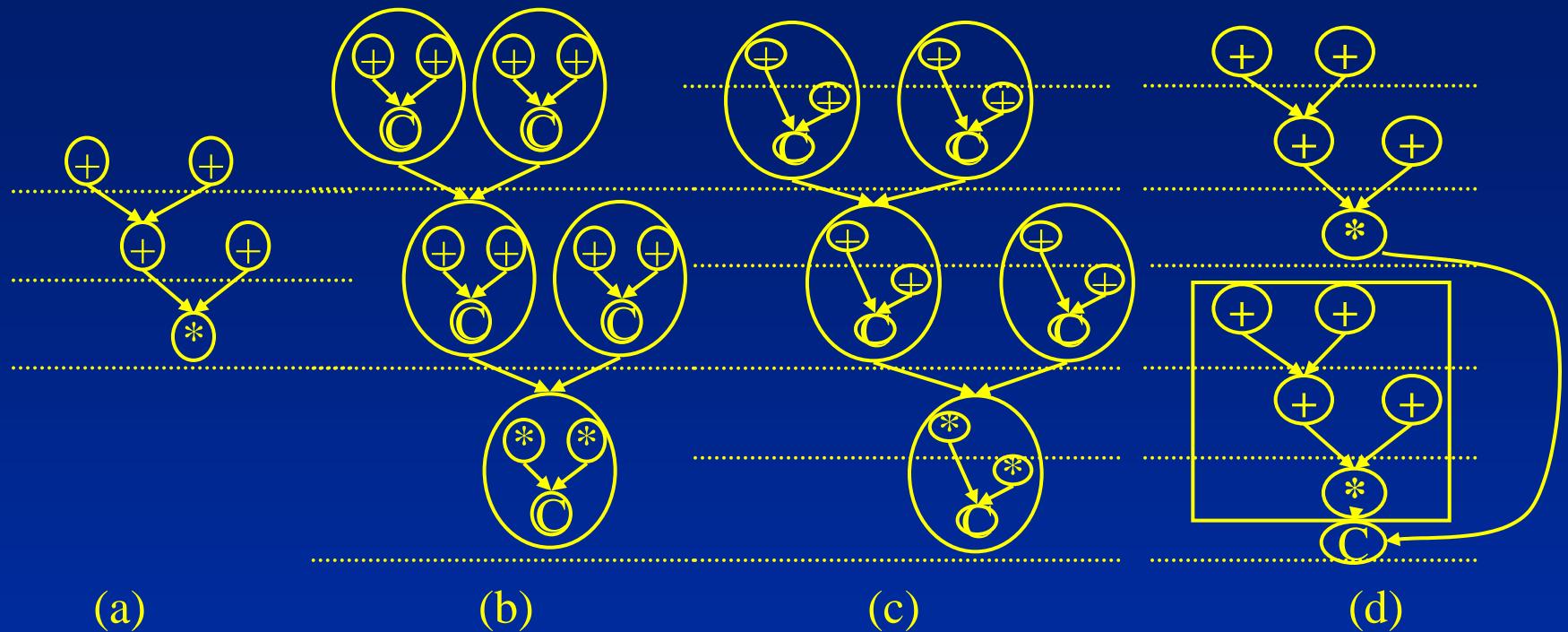


- ✓ Design Diversity constraints incorporated using Synopsys BC synthesis scripts
- ✓ Two $21 \times 21 \rightarrow 21$ adders
- ✓ One $10 \times 10 \rightarrow 16$ and One $10 \times 10 \rightarrow 19$ multipliers
- ✓ Detection latency of 2000 ns

CED capability of Data Diversity

- All RESO detectable SEL
- SEU detection capability varies with R (the checking ratio) and D (the # of data outputs that will be affected)
 - ↳ when $1 \leq R \leq D$, 100 % Logic RESO detectable faults
 - ↳ when $D < R$, $100 \times (D / R) \%$ Logic RESO detectable faults

RESO vs Data Diversity vs



(a) Example CDFG
Logic Level CED

(b) Duplication

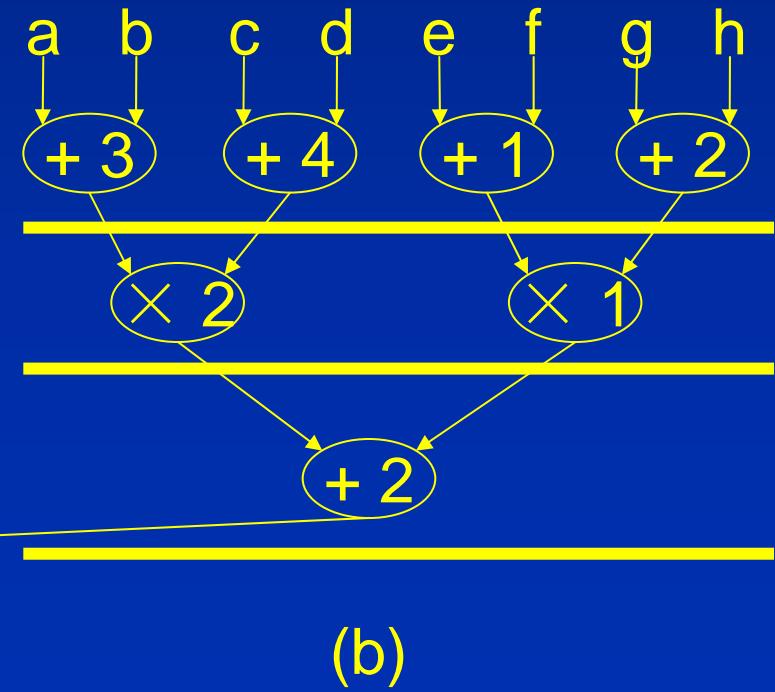
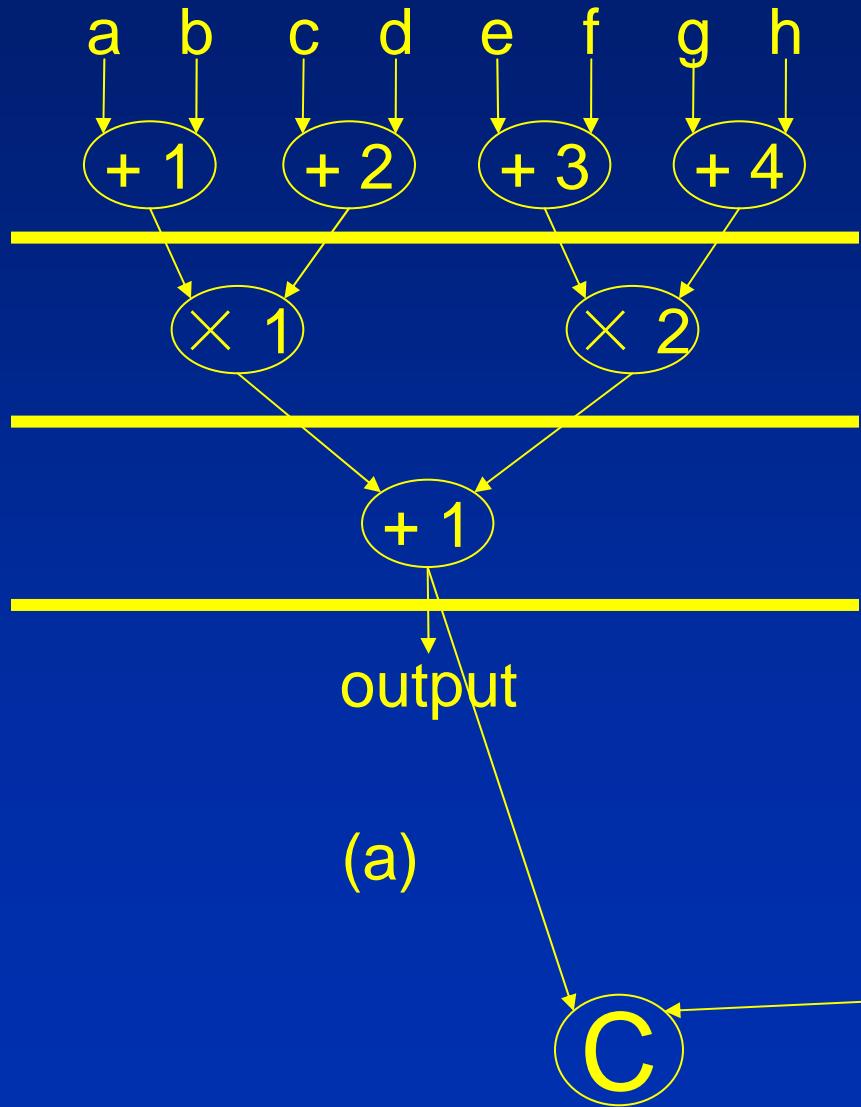
(c) RESO, RERO, REDWC etc..

(d) RT Level Time Redundancy based CED

RT Level Radiation Hardening

RT Level Allocation Diversity

RT Level Allocation Diversity



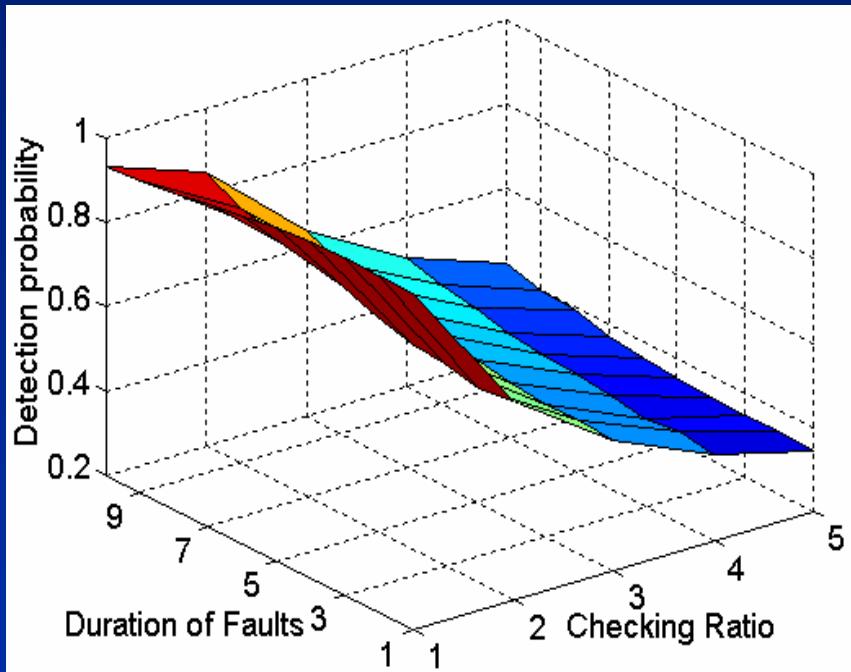
Faulty results due to a single stuck-at-1 fault in one of the modules

Faulty module	Possible faulty results from		Possible to miss a fault?
	Normal computation	Re-computation	
+3	$(a+b)(c+d)+(e+f+2^i)(g+h)$	$(a+b+2^i)(c+d)+(e+f)(g+h)$	No
+4	$(a+b)(c+d)+(e+f)(g+h+2^i)$	$(a+b)(c+d+2^i)+(e+f)(g+h)$	No
+1	$(a+b+2^i)(c+d)+(e+f)(g+h)$ $(a+b)(c+d)+(e+f)(g+h)+2^i$ $(a+b+2^i)(c+d)+(e+f)(g+h)+2^i$	$(a+b)(c+d)+(e+f+2^i)(g+h)$	No
+2	$(a+b)(c+d+2^i)+(e+f)(g+h)$	$(a+b)(c+d)+(e+f)(g+h+2^i)$ $(a+b)(c+d)+(e+f)(g+h)+2^i$ $(a+b)(c+d)+(e+f)(g+h+2^i)+2^i$	No
$\times 1$	$((a+b)(c+d)+2^i)+(e+f)(g+h)$	$(a+b)(c+d)+((e+f)(g+h)+2^i)$	Yes
$\times 2$	$(a+b)(c+d)+((e+f)(g+h)+2^i)$	$((a+b)(c+d)+2^i)+(e+f)(g+h)$	Yes

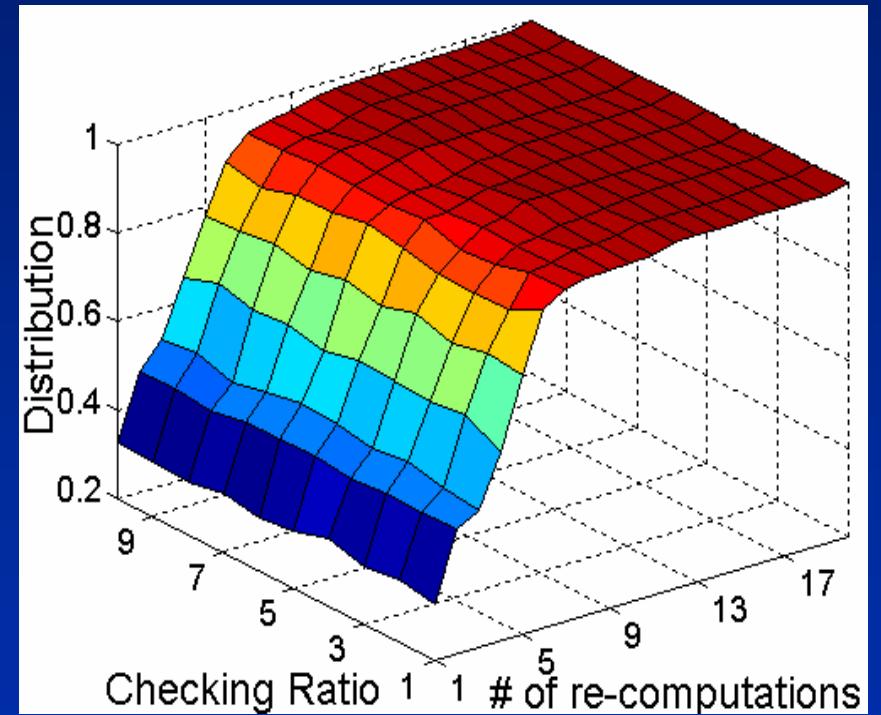
Windowed Filter

	Basic Design	Allocation diversity
Adders	4	4
Multipliers	4	4
Area (unit cell)	72293	80940
Area overhead	--	12%
Prob. of missing faults in adders	{1,1,1}	{0, 0, 0}
Prob. of missing faults in $\times 1$, $\times 2$	{1,1,1}	{0.11, 0.01, 0.02}
Prob. of missing faults in $\times 3$, $\times 4$	{1,1,1}	{0.27, 0.07, 0.11}

Windowed Filter: CED Capability



SEU tolerance



SEL tolerance

Concluding remarks

- Low area overhead and low time overhead CED
- Used Synopsys BC results (RT Level Synthesis Tool)
- Validated using simulated fault injection experiments
- Validation using real radiation sources (BNL)?