
Analog front ends for highly segmented detectors

Highlights from the 2003 specialist conferences

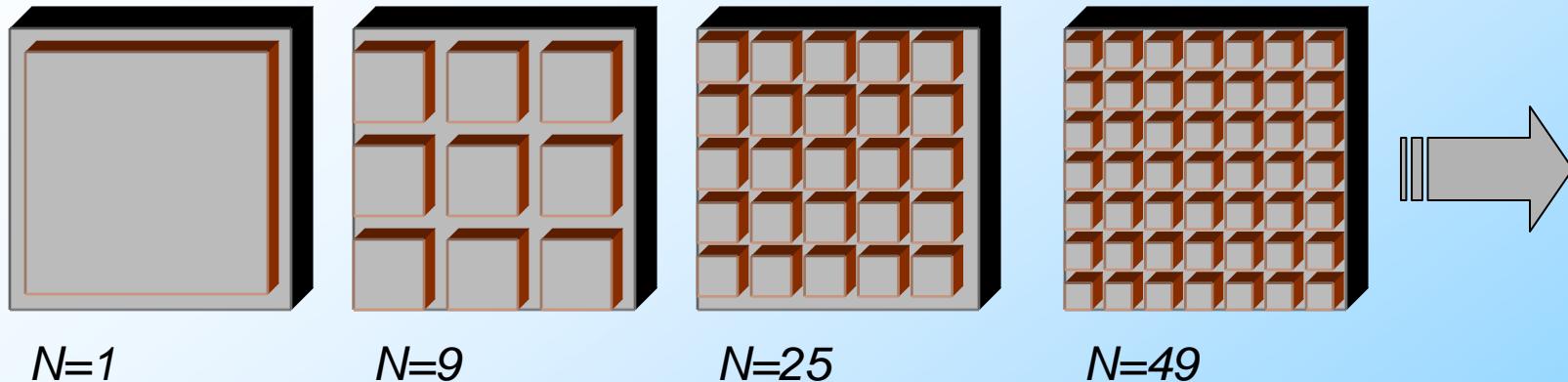
Paul O'Connor

Instrumentation Division Seminar

BNL

Dec. 17, 2003

Highly segmented detectors



Benefits:

- Position Resolution
 - pixel pitch $\sim 1/\sqrt{N}$
- Energy resolution:
noise \downarrow $\left\{ \begin{array}{l} - C_{DET} \sim 1/N \\ - I_{DARK} \sim 1/N \\ - \text{rate/pixel} \sim 1/N \\ (\text{pulse shaping time} \sim N) \\ - \text{signal confined to} \sim 1 \text{ pixel} \end{array} \right.$
- Faster charge collection
- “Small pixel” effect
 - improve energy resolution in semiconductor detectors with poor hole transport

Drawbacks:

- Electronics channel count
 - cost $\sim N$
 - power $\sim N$
- Interconnect density
 - density $\sim N$

Applications

- particle physics

- *tracking*
- *particle ID*

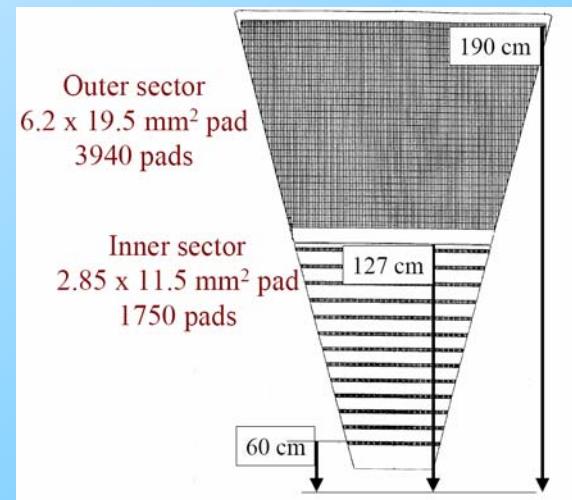
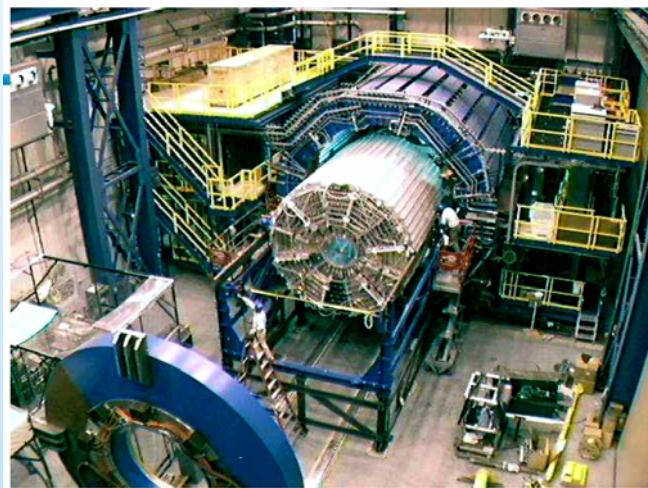
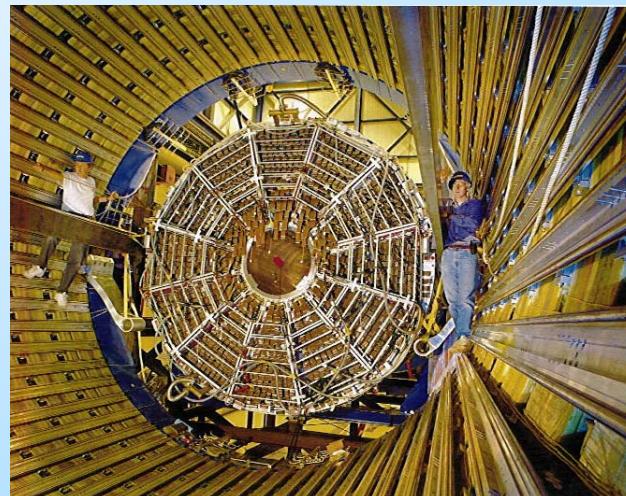
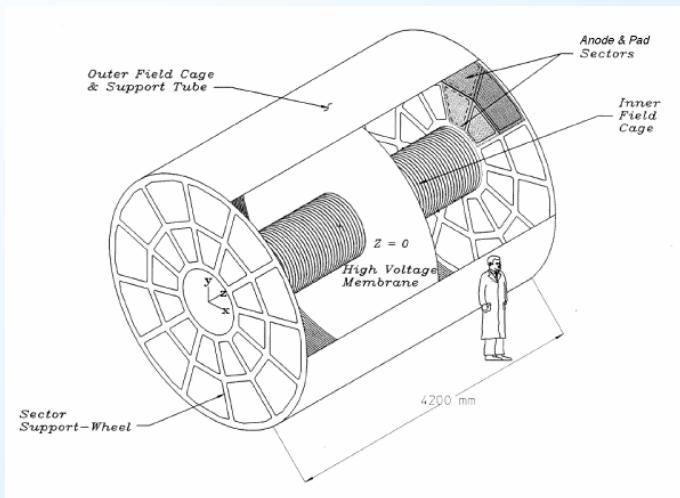
- medical and biological imaging

- *PET front ends*
- *nuclear medicine*
- *neutron scattering*
- *electron microscopy*

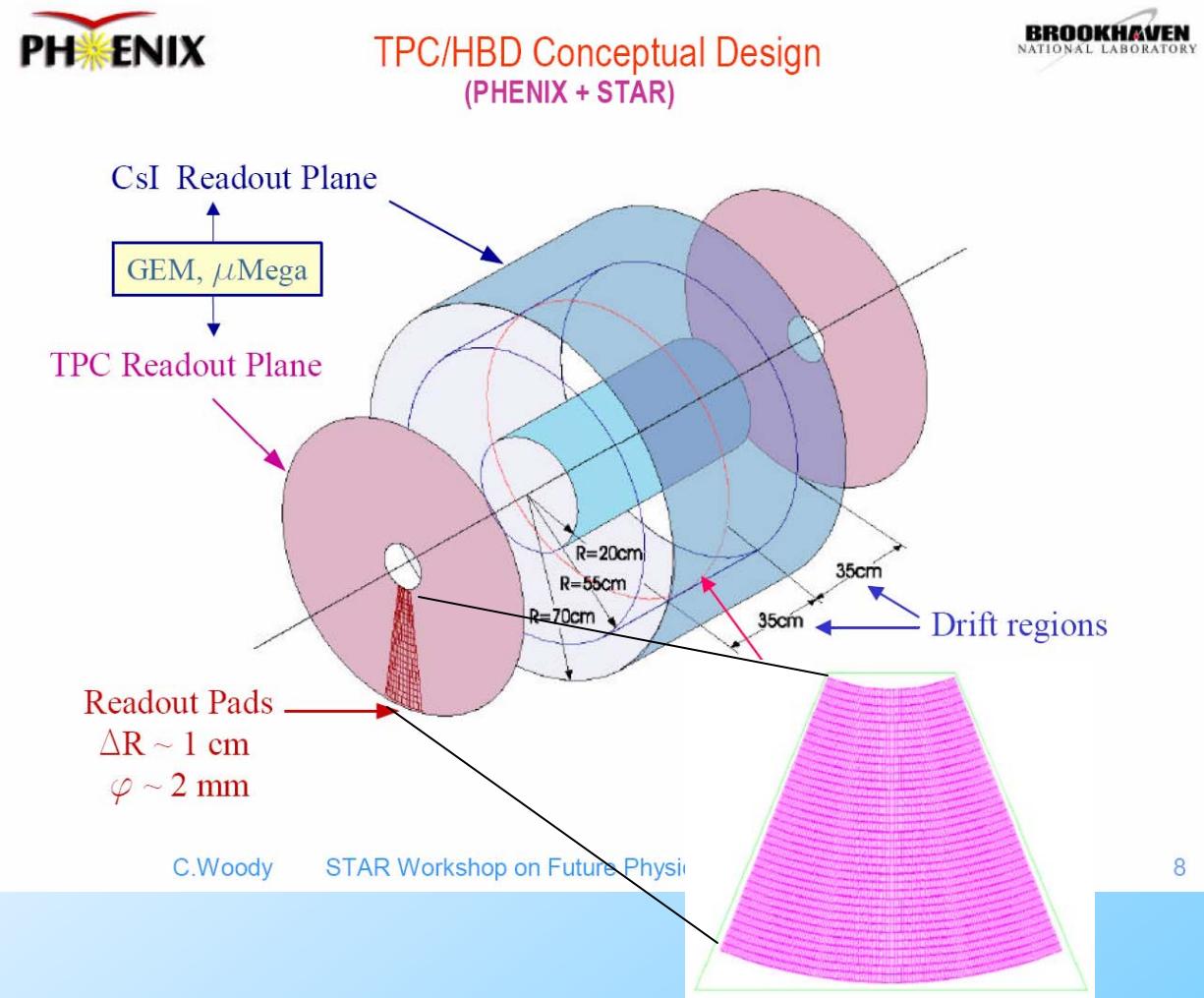
- synchrotron radiation studies

- *protein crystallography*
- *EXAFS*
- *X-ray microscopy*
- surveillance
- industrial inspection
- astrophysics
 - *gamma*
 - *X-ray*
 - *optical*

STAR Time Projection Chamber



TPC for the PHENIX experiment



8

Nuclear medicine

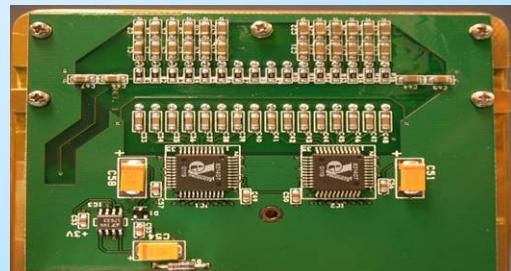
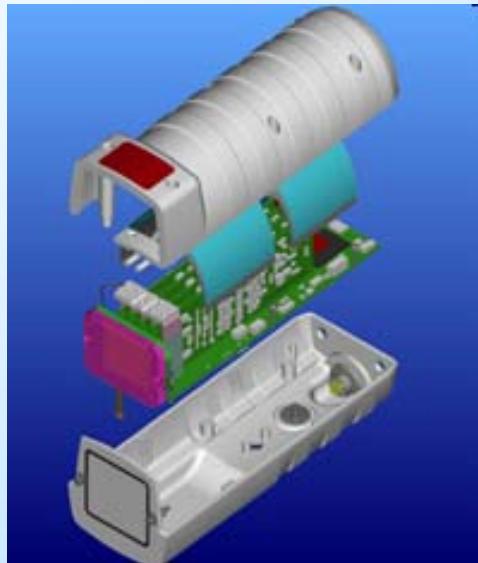
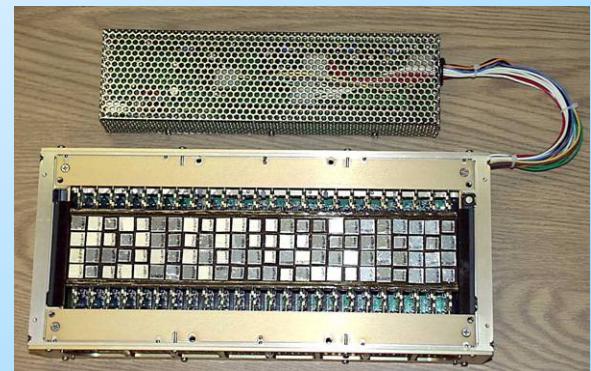
Intra-operative probes



Bone mineral densitometer

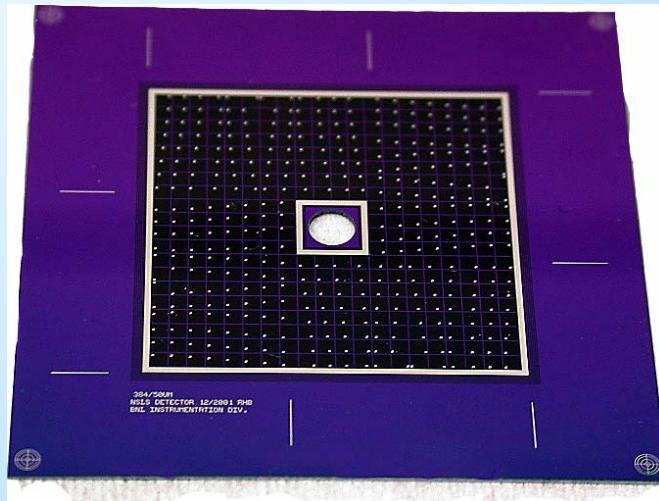
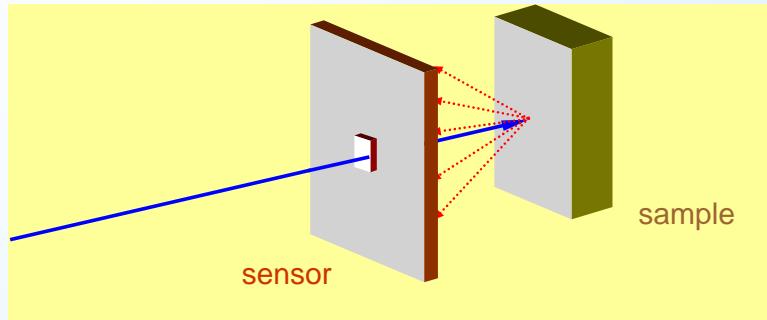


solid-state gamma camera



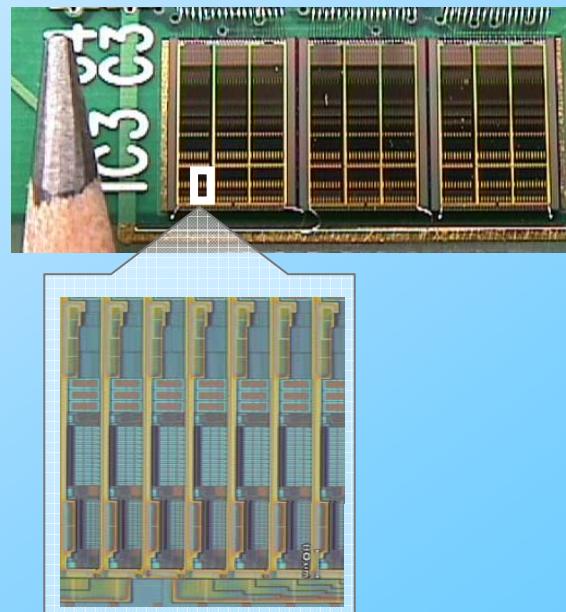
- 3072 pixels
 - 192 front-end ASICs
 - 1.3M events/second
 - average FWHM 3.8% at 122keV
-
- 16 pixels $3 \times 7 \times 3 \text{ mm}^3$
 - 2 front-end ASICs
 - DEXA (Dual Energy X-ray Absorptiometry)

Silicon sensor for EXAFS spectroscopy

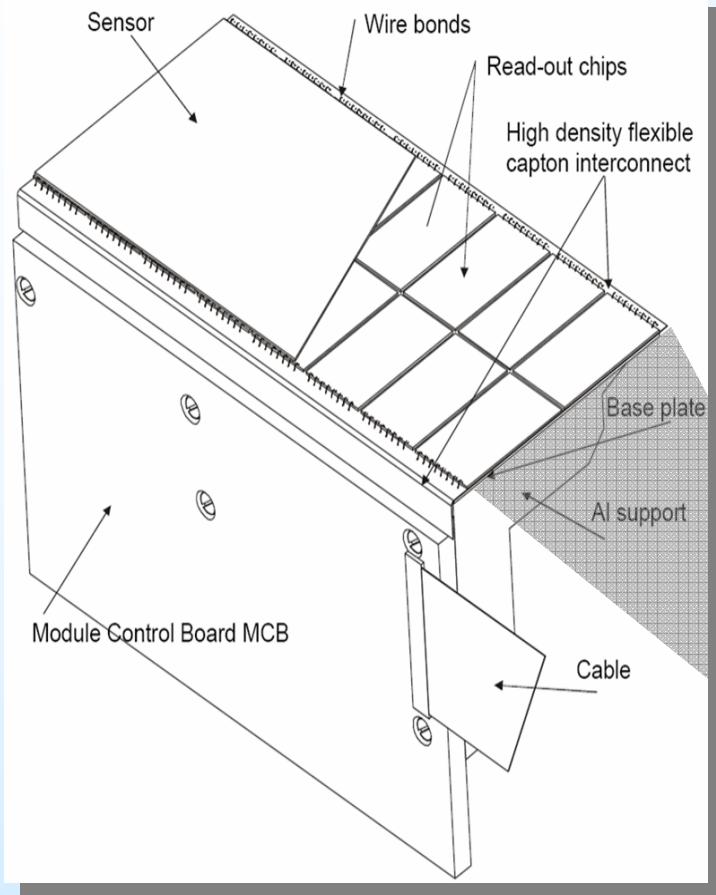


G. De Geronimo et al., Proc. PIXEL2002 International Workshop, Carmel, CA, 2002

- 384 pixels
- $1 \times 1 \times 0.25 \text{ mm}$ Si pad detector
- rate $> 10 \text{ MHz/cm}^2$
- 8.2 mW/chan
- FWHM $< 300\text{eV}$, noise $< 28 \text{ e}^-$
- preamps + digital integrated on-chip

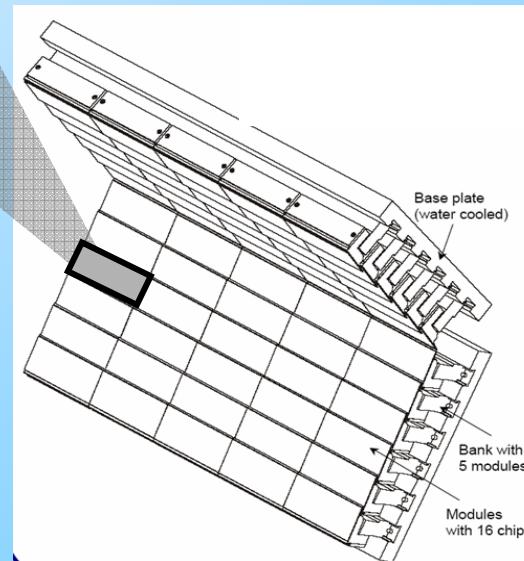


Protein crystallography detector

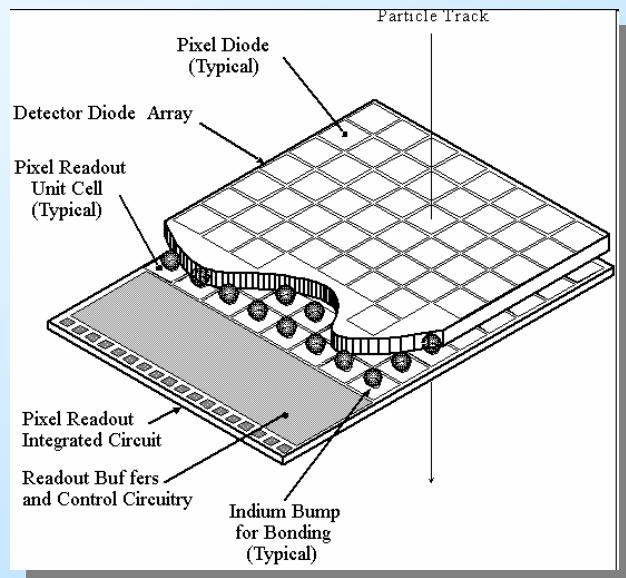
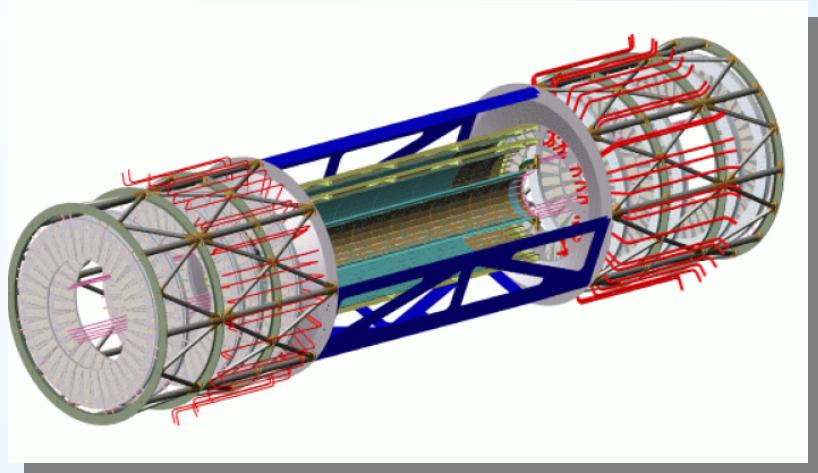


Ch. Brönnimann, SLS

- silicon hybrid pixel
- $200 \times 200 \mu\text{m}$
- 4 M total pixels
- 100 ns shaping
- $< 100 \text{ e}^-$ noise
- 0.16 m^2 total detector area
- 40 Mpix/s readout



ATLAS pixel detector



- size: 21.4 mm x 67.8 mm; 16 ICs
- 46080 PbSn-solder bumps; pitch: 50 μm
- 4 thin film metal layers: Ti:W/Cu - 3 μm ep.-Cu
- 5 dielectric layers: photo-BCB, 5 μm thick, 25 μm vias

- 10^8 hybrid pixels
- pixel size $\sim 400 \times 50 \mu\text{m}$
- 2 m² silicon
- 50 $\mu\text{W}/\text{pixel}$
- 1% X_0 per layer
- Noise, threshold dispersion $< 200 \text{ e}^-$
- 25 ns timing precision
- 50 Mrad , 10^{15} n/cm^2 radiation tolerance

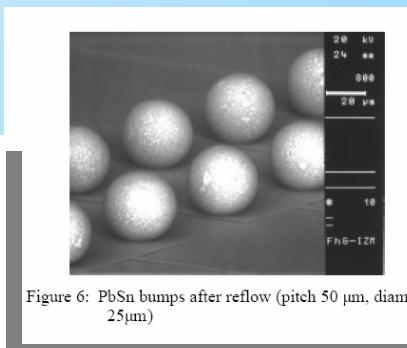
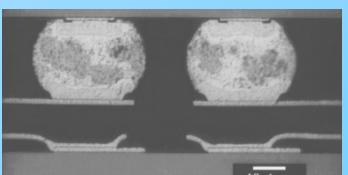
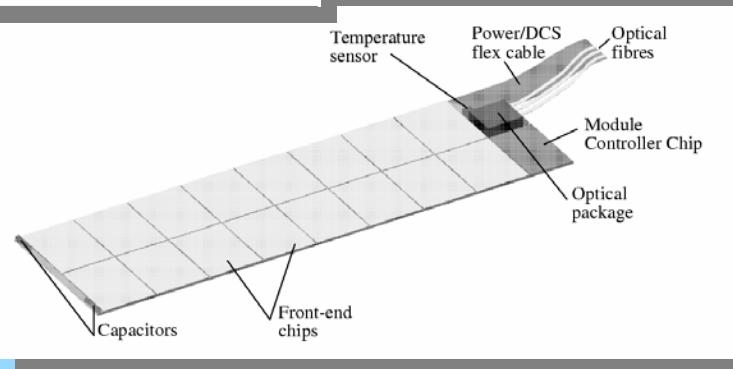
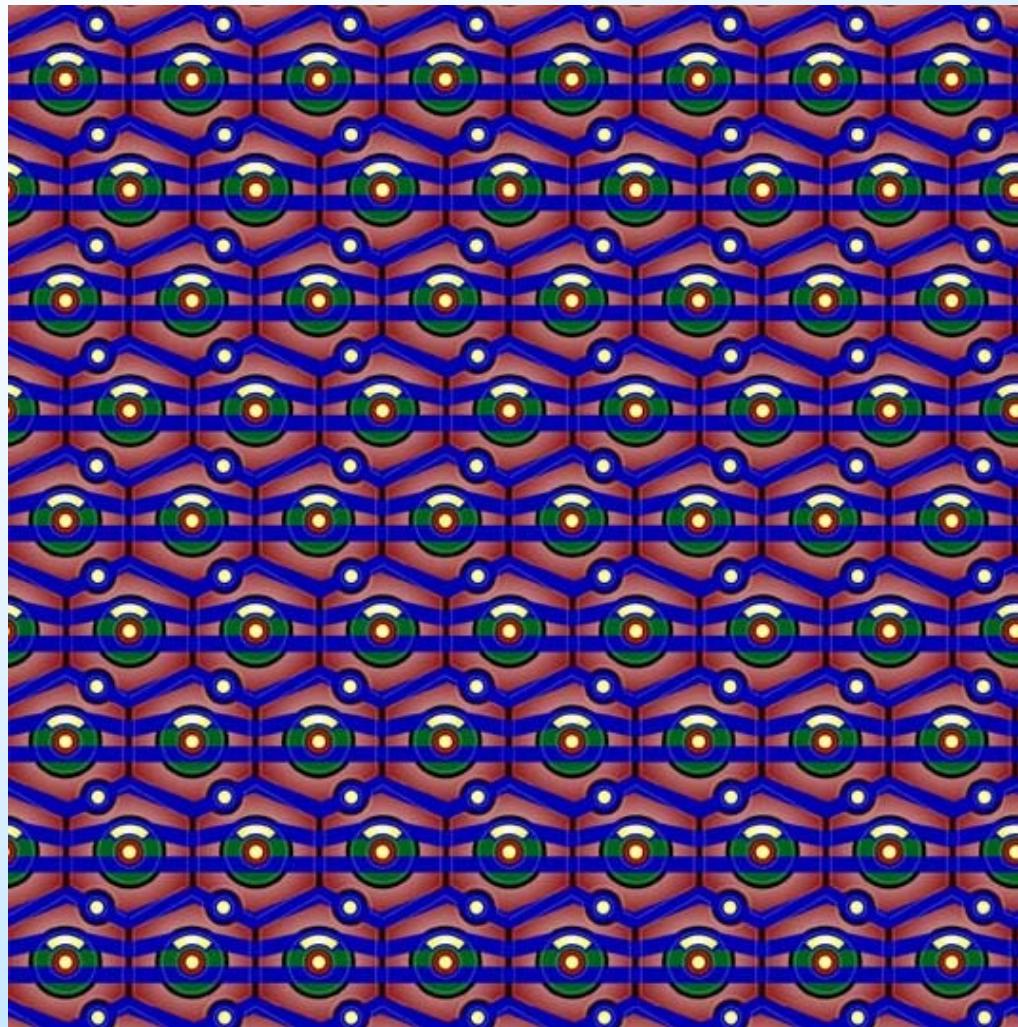


Figure 6: PbSn bumps after reflow (pitch 50 μm , diam. 25 μm)



K. Einsweiler, LBNL

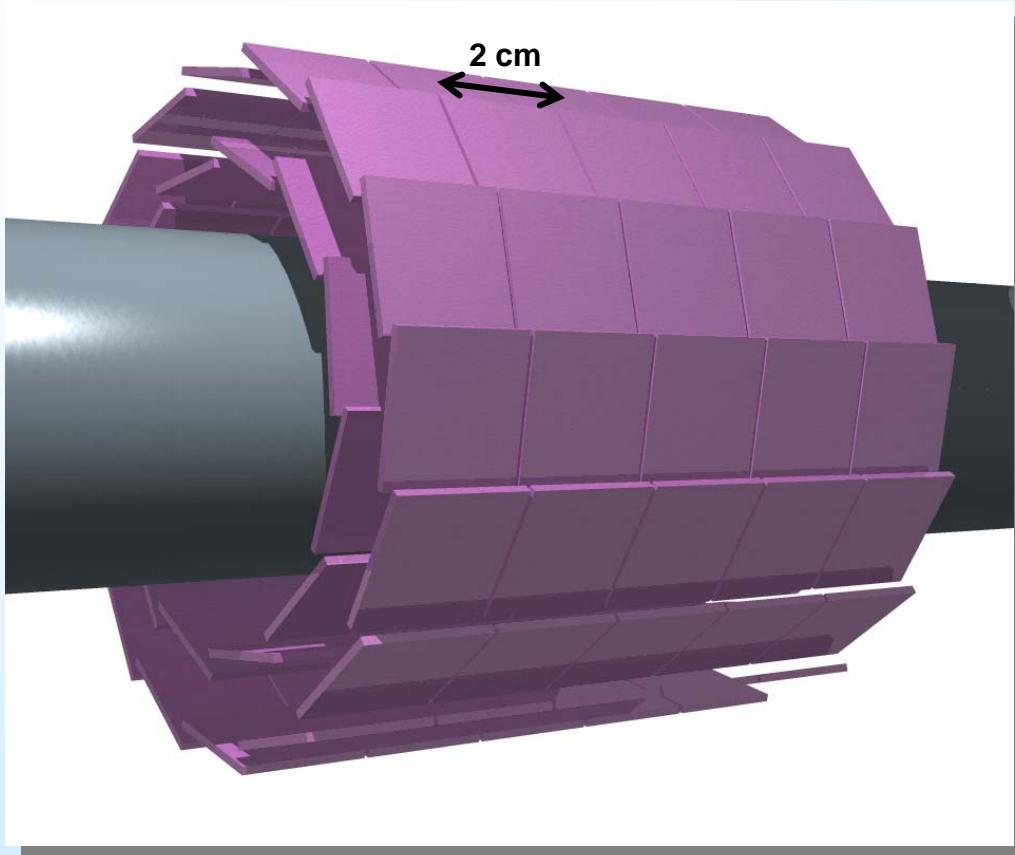
DEPFET array for XEUS X-ray satellite



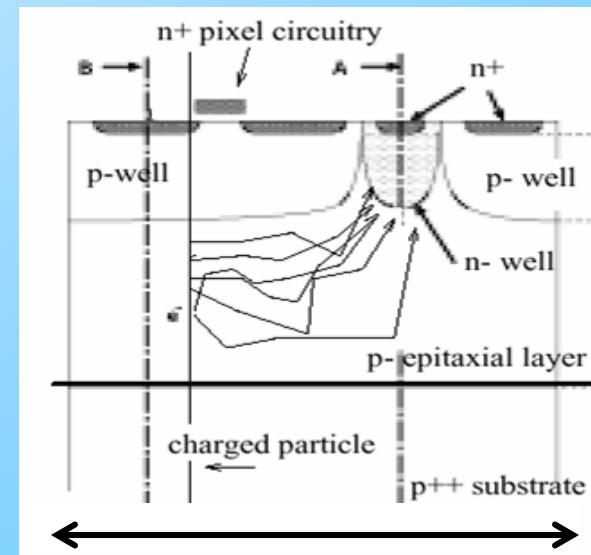
- active pixels on high resistivity silicon
- on-detector FET amplifier
- matrix readout
- energy resolution/ readout time tradeoff

L. Struder, MPI Munich
H. Wermes, Bonn

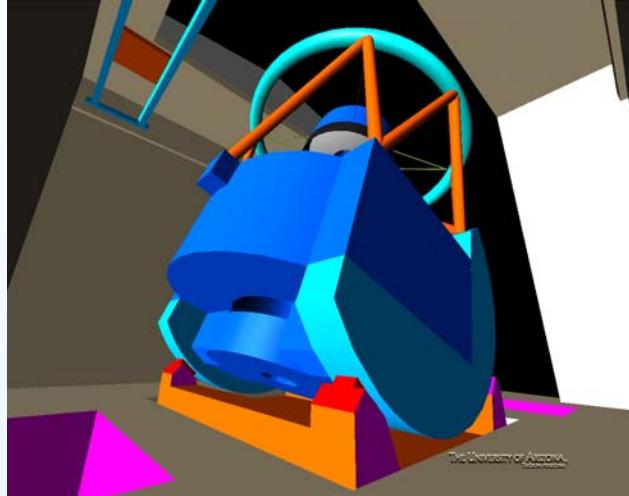
Vertex detector for STAR



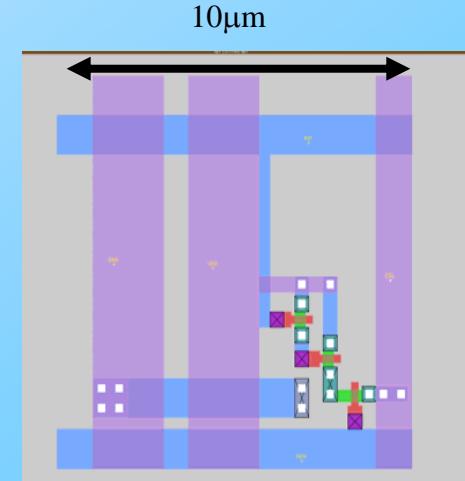
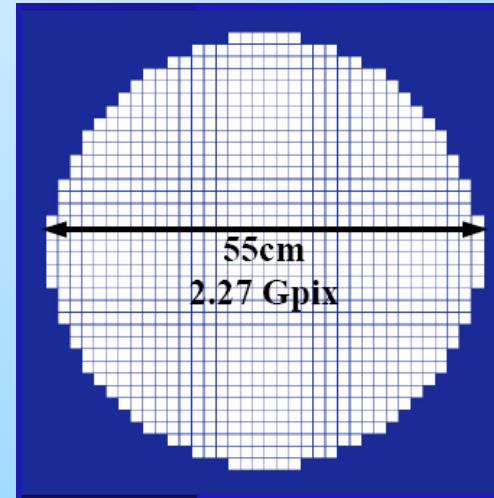
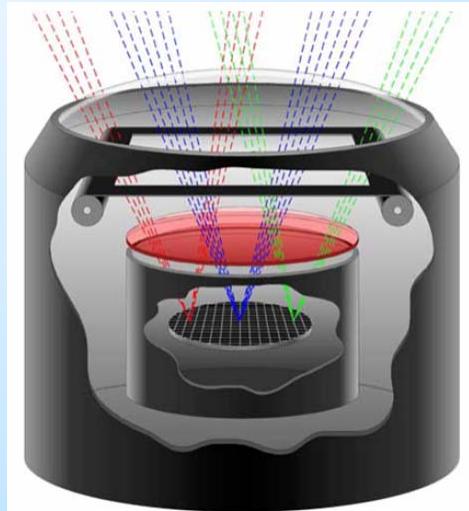
- monolithic active pixel sensor
- standard CMOS fabrication
- pixel size $\sim 20 \times 20 \mu\text{m}$
- 90 million pixels
- 40 μm thick chips



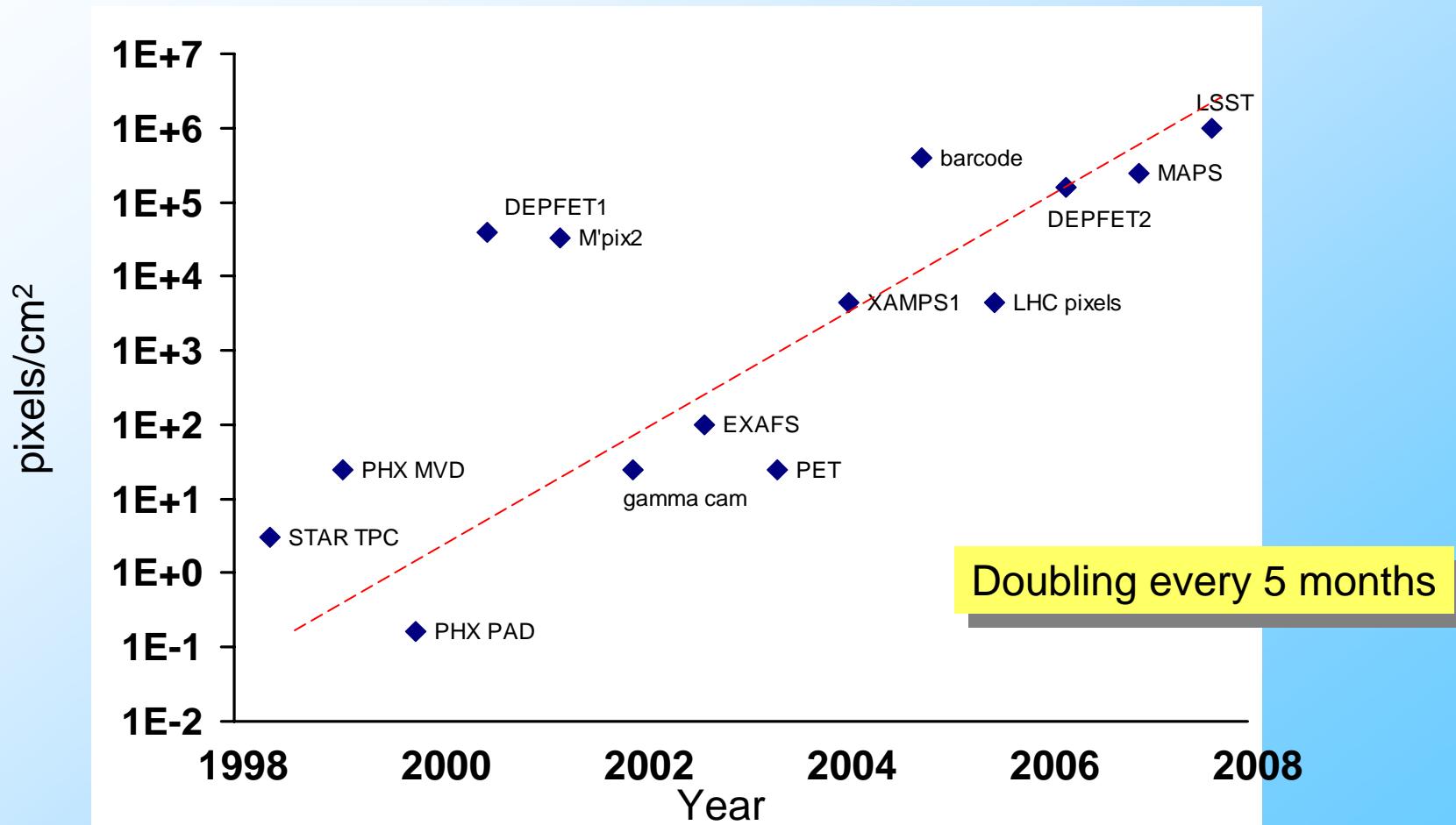
Large Synoptic Survey Telescope



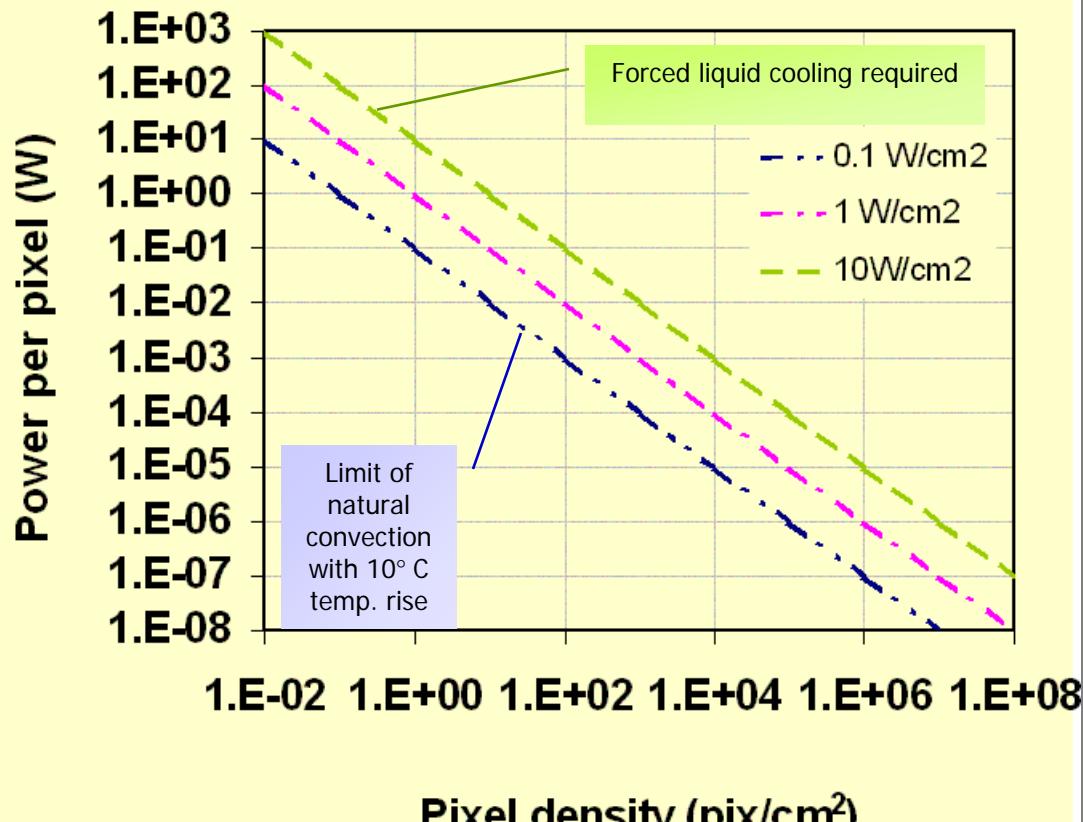
- 8.4 m primary mirror
- 55 cm, 3 Gpix focal plane
- hybrid pixel sensor, optical & NIR
- $10 \times 10 \times 100 \mu\text{m}$ pixels
- 5 e^- readout noise
- 1.5 Gp/s readout rate



Pixel density



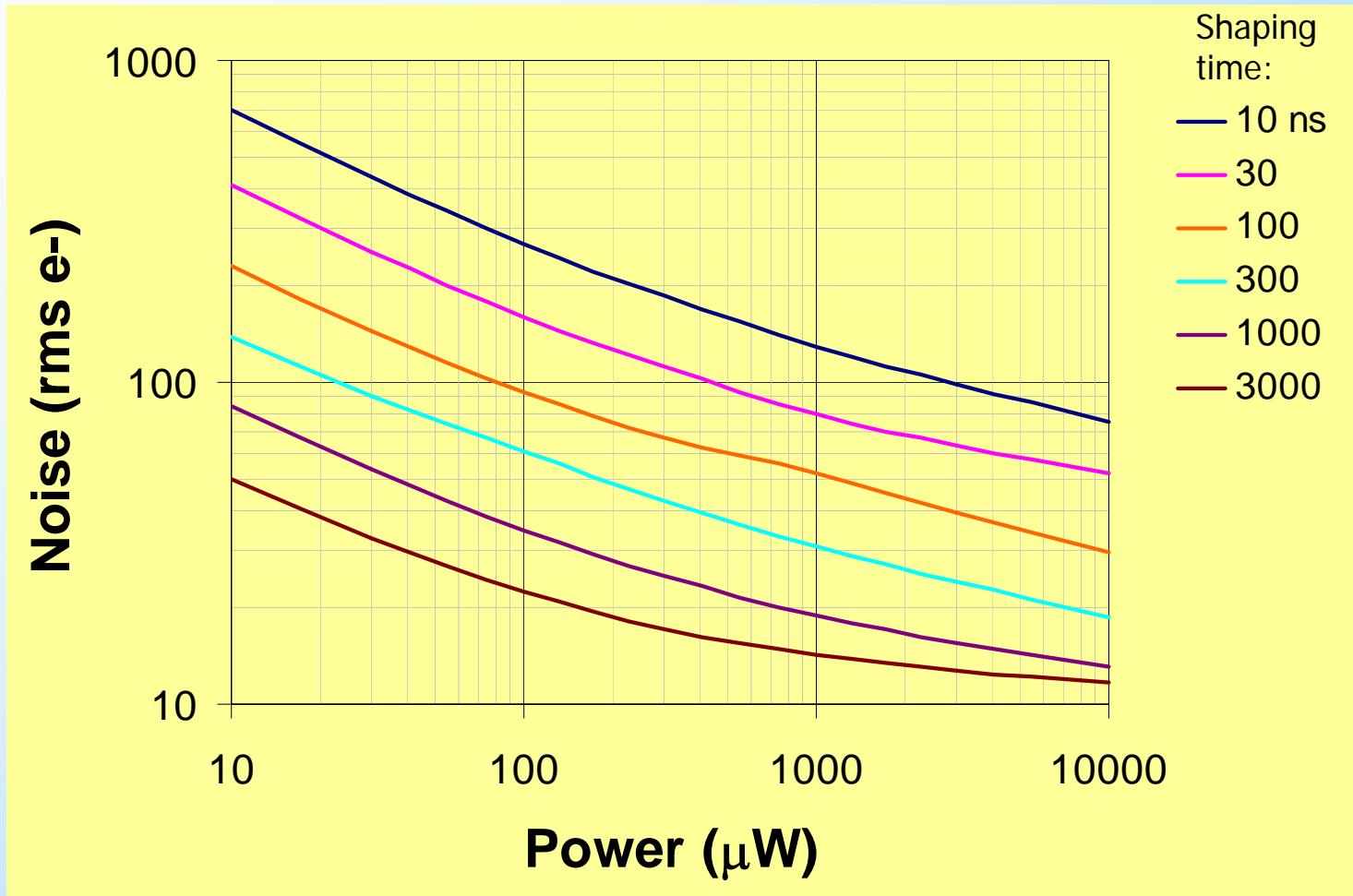
Power density



- On-detector power density is limited by cooling capability.
- Electronics for high-density detector must be extremely low power.

Optimized noise vs. power

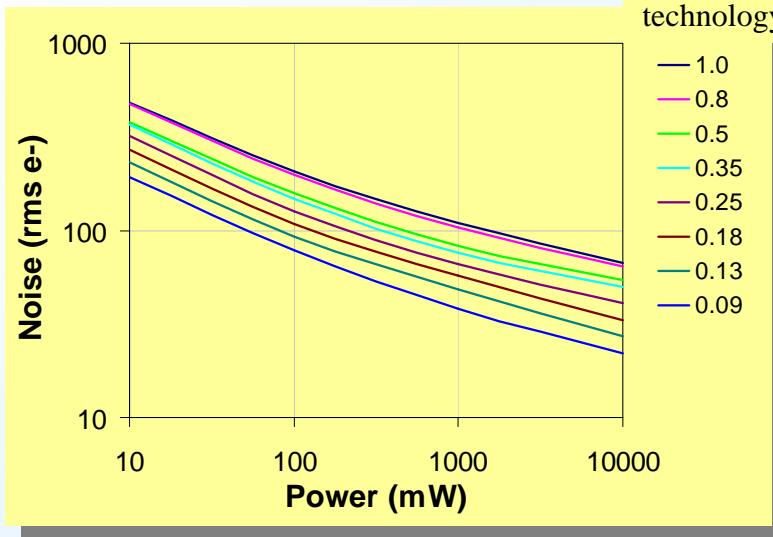
(N-MOSFET optimized at each power level and shaping time)



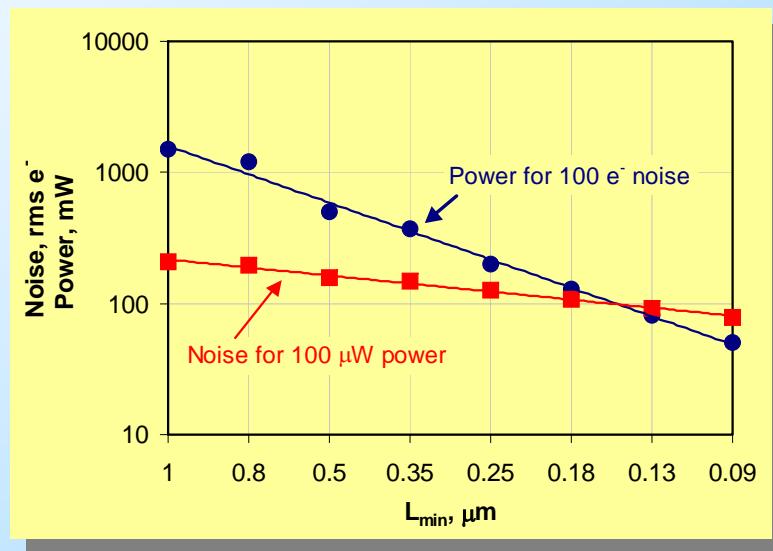
Note:
 $\left| \frac{d(\ln N)}{d(\ln P)} \right| \leq 0.4$

$C_d = 1\text{pF}$
0.25 μm CMOS

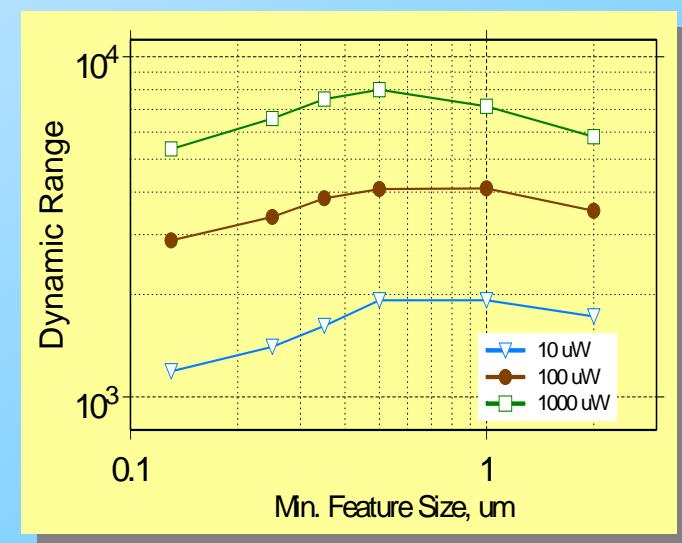
Scaling impact on the noise/power tradeoff



- Scaled technologies offer improved noise per unit of power, due to better g_m/C_{gs} ratio.
- More amplifier bandwidth per unit of power.
- Because of diminishing supply voltage, dynamic range may begin to decline with the 0.25 micron CMOS generation.



C_{det} 1pF
 t_s 50 ns

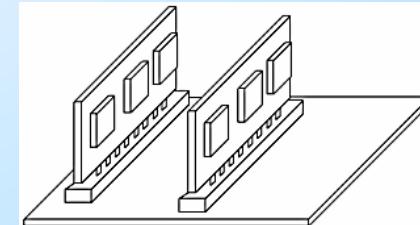


P O'Connor and G. De Geronimo
Prospects for charge sensitive amplifiers in scaled CMOS
NIM A480, 713 (Mar. 2002)

Detector – FE interconnect choices

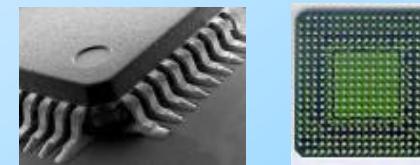
- **board-to-backplane**

- easy to test, repair
- large boards possible
- connector pins are failure points
- coarse pitch and high capacitance ($> 1\text{ pF}$)



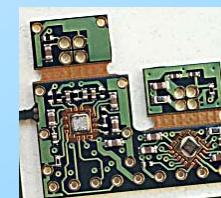
- **standard SMT package soldered to board (QFP or BGA)**

- easy to test, difficult to repair
- capacitance down to 0.2 pF for small packages
- board area limited by reflow oven capacity



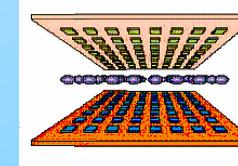
- **wirebonded chip-on-board**

- difficult to test, assemble, and repair
- board area limited by wirebonder
- fragile
- low capacitance (0.1 pF)



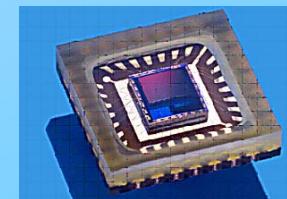
- **bump-bonded flip-chip**

- can match pixels with pitch from $\sim 30 - 1000 \mu\text{m}$
- difficult to test, assemble, and repair
- circuitry has to fit in same area as pixel



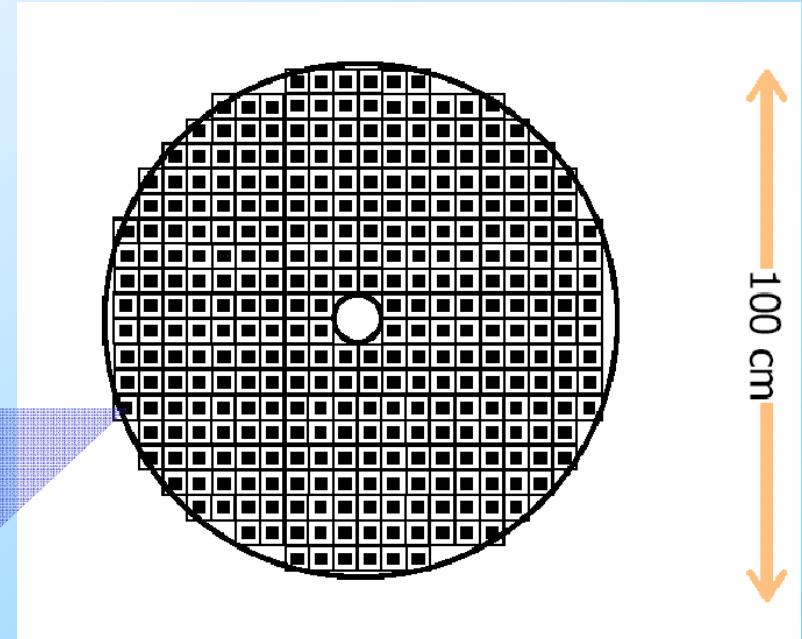
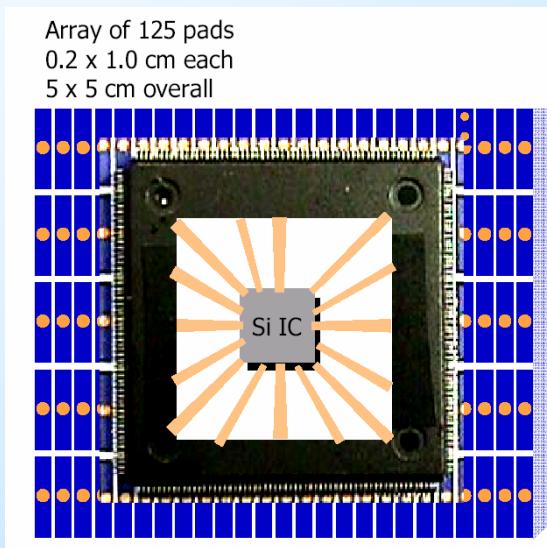
- **monolithic detector/electronics**

- interconnect is created as part of the detector fabrication process
- ultra-low capacitance (few fF)

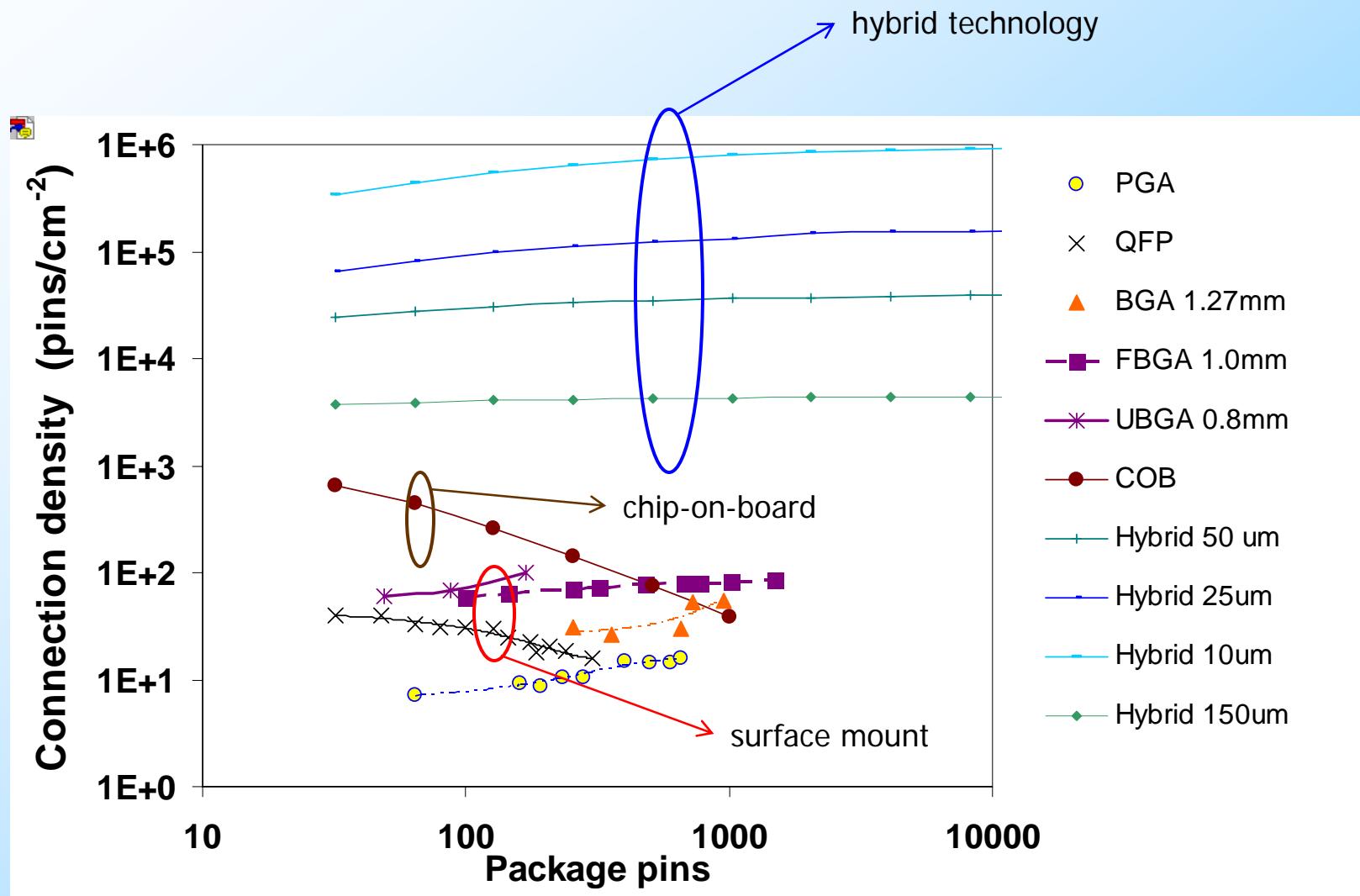


Packaging density example – PHENIX TPC

TPC readout plane with
readout IC's
~ 41,000 pads



Packaging density



**Vth INTERNATIONAL MEETING ON
FRONT END ELECTRONICS**

for High Energy, Nuclear, Medical, and Space Applications

**June 30th to July 3rd, 2003
Snowmass Village, Colorado**



FEE2003: David Frank, IBM

**CMOS Technology
for the Next 10 Years**

David J. Frank

IBM Watson Research Center
Yorktown Heights, NY 10598, U.S.A.

ITRS 2001 Roadmap Projections

Year	2001	2003	2005	2007	2010	2013	2016
DRAM ½ pitch (nm)	130	100	80	65	45	32	22
DRAM generation	512M	1G	2G	4G	8G	32G	64G
MPU transistors/chip	97M	153M	243M	388M	773M	1.55G	3.09G
Local clock (GHz)	1.7	3.1	6.2	6.7	11.5	19.3	28.8
Number wiring levels	8	8	10	10	10	11	11
Total wire length (km/cm²)	4.1	5.8	9.1	11.2	16.1	22.7	33.5
Interlayer eff. permittivity	3.3	3.3	2.8	2.5	2.1	1.9	1.8
High-perf. logic physical gate length (nm)	66	46	32	25	18	13	9
High-perf. logic EOT (nm)	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
High-perf. VDD (V)	1.2	1.0	0.9	0.7	0.6	0.5	0.4
High-perf. Power (W)	130	150	170	190	218	261	288
Low-power logic physical gate length (nm)	90	65	45	32	22	18	11
Low-power logic EOT (nm)	2.0-2.4	1.6-2.0	1.2-1.6	1.0-1.4	0.8-1.2	0.7-1.1	0.6-1.0
Low-power VDD (V)	1.2	1.1	1.0	0.9	0.8	0.7	0.6
Low-power Power (W)	2.4	2.8	3.2	3.5	3.0	3.0	3.0

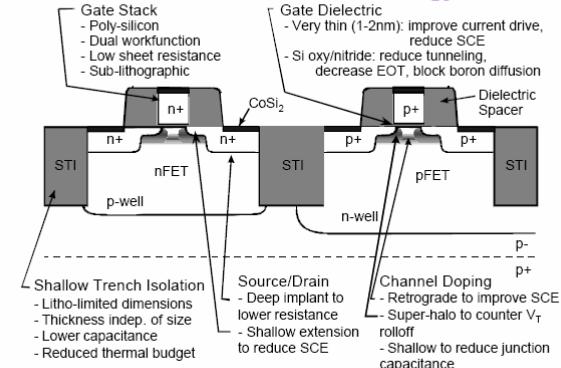
Industry agreed-upon targets for future technology.
Typically, everyone tries to beat these targets.

OUTLINE

1. CMOS Technology Overview
 - ITRS projections
2. Future Technology Directions
 - Metal gates
 - Strained Si
 - High-k gate dielectrics
 - Ultra-thin SOI
 - Double-gate FETs (FinFETs)
3. Scaling Limitations
 - Device tolerances
 - Power dissipation
4. Conclusions

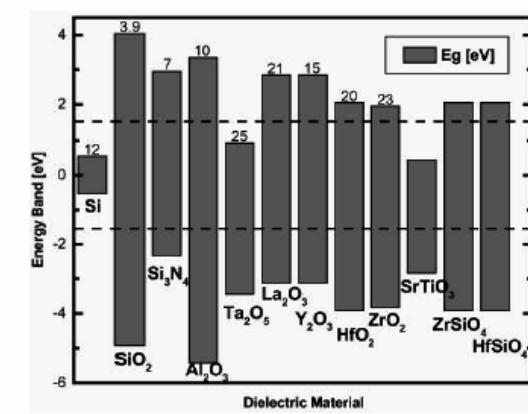
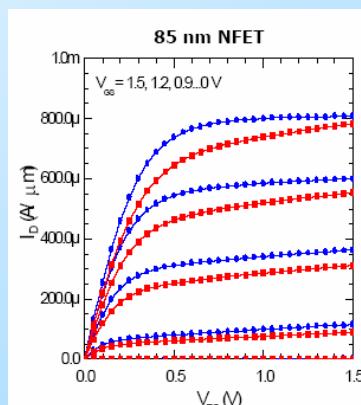
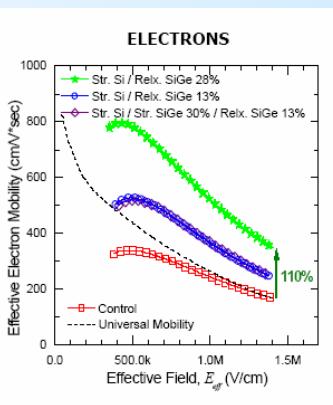
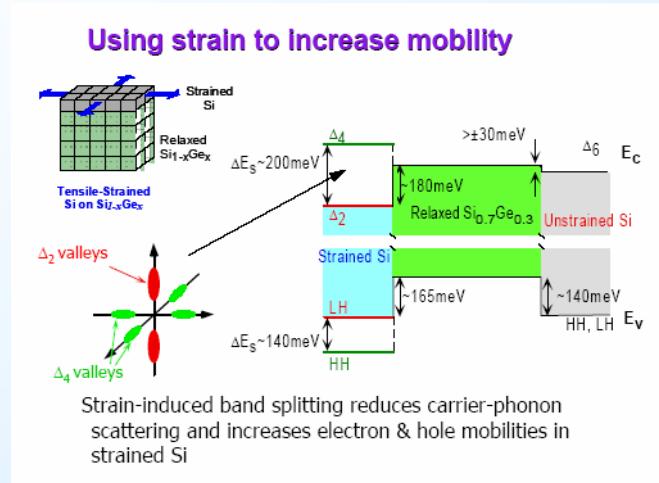
1. CMOS TECHNOLOGY OVERVIEW

State-of-the-art bulk CMOS technology

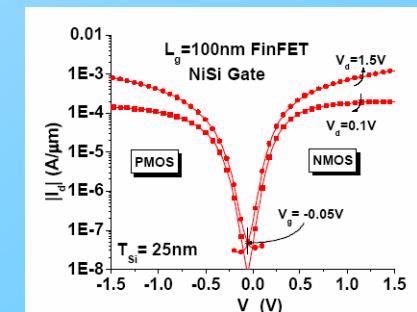
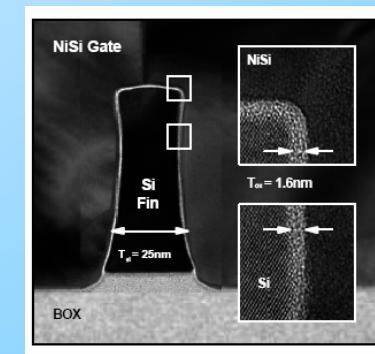
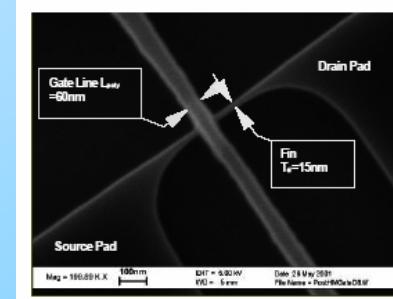
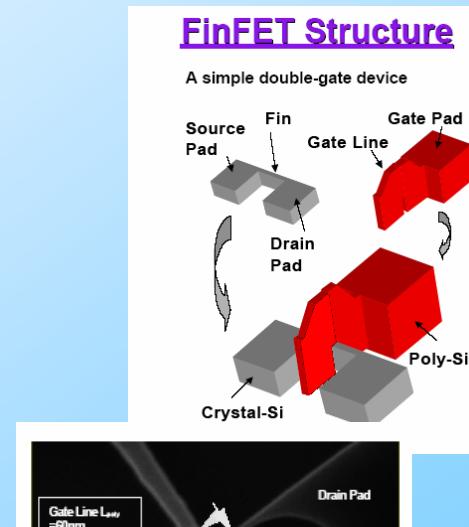
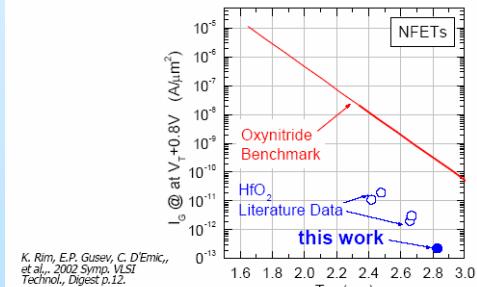


[H.-S. P. Wong, et al., Proc. IEEE, 87, p.537, 1999 and S.-F. Huang, et al., IEDM Tech. Dig., p.237, 2001.]

FEE2003: David Frank, IBM



Gate leakage reduction with HfO_2



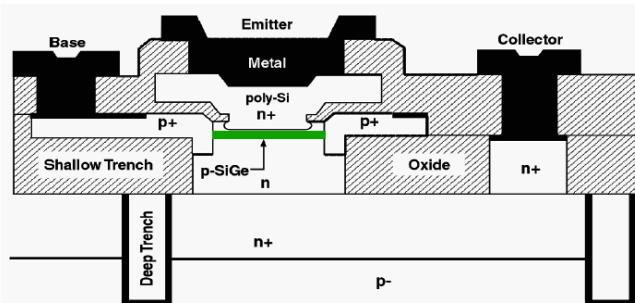
FEE2003: John Cressler, GA Tech

Assessing SiGe HBT Technology For Front-end Electronics Applications

John D. Cressler
 School of Electrical and Computer Engineering
 777 Atlantic Drive, N.W., Georgia Institute of Technology
 Atlanta, GA 30332-0250 USA
 cressler@ece.gatech.edu
 Tel (404) 894-5161 / FAX (404) 894-4641
 http://users.ece.gatech.edu/~cressler/



- Conventional Shallow and Deep Trench Isolation + CMOS BEOL
- Unconditionally Stable UHV/CVD SiGe Epitaxial Base
- 100% Si Fabrication Compatibility



SiGe BiCMOS Evolution

Georgia Institute
of Technology
 School of Electrical and Computer Engineering

- Best-of-Breed CMOS Comes Along for the Ride!
- Enables System-on-a-Chip Integration

Parameter	First	Second	Third
$W_{E,\text{eff}}$ (μm)	0.42	0.18	0.12
peak β	100	200	400
V_A (V)	65	120	> 150
BV_{CEO} (V)	3.3	2.5	1.7
BV_{CBO} (V)	10.5	7.5	5.5
peak f_T (GHz)	47	120	207
peak f_{max} (GHz)	65	100	285
min. NF_{min} (dB)	0.8	0.4	< 0.3

SiGe HBT



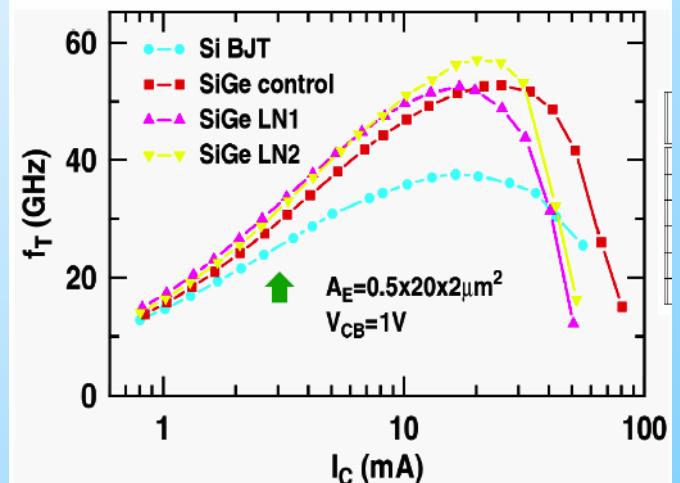
Parameter	First nFET	First pFET	Second nFET	Second pFET	Third nFET	Third pFET
L_{eff} (μm)	0.36	0.36	0.14	0.15	0.092	0.092
V_{DD} (V)	3.3	3.3	1.8	1.8	1.5	1.5
I_{ox} (nm)	7.8	7.8	4.2	4.2	2.2	2.2
$V_{T,lin}$ (mV)	580	-550	326	-415	250	-210
$I_{D,sat}$ ($\mu\text{A}/\mu\text{m}$)	468	231	600	243	500	210

Si CMOS



Note:
 not strained Si!
 not strained SiGe!

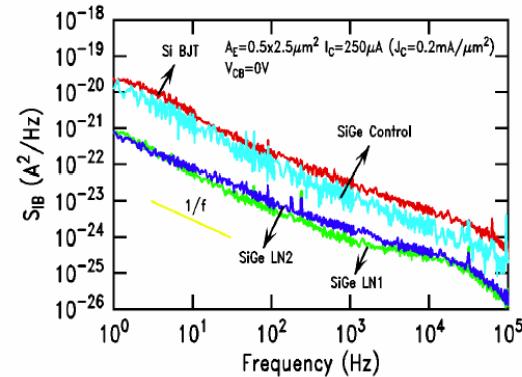
• Improved f_T at Low J_C



Low-Frequency Noise

Georgia Institute
of Technology
 School of Electrical and Computer Engineering

- Significant Improvement Over Si BJT at Fixed Bias Current
- Much Better Than CMOS or III-V

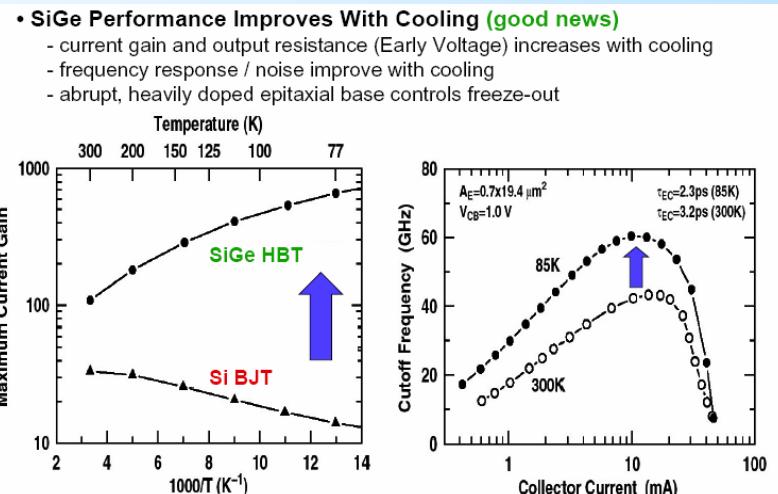
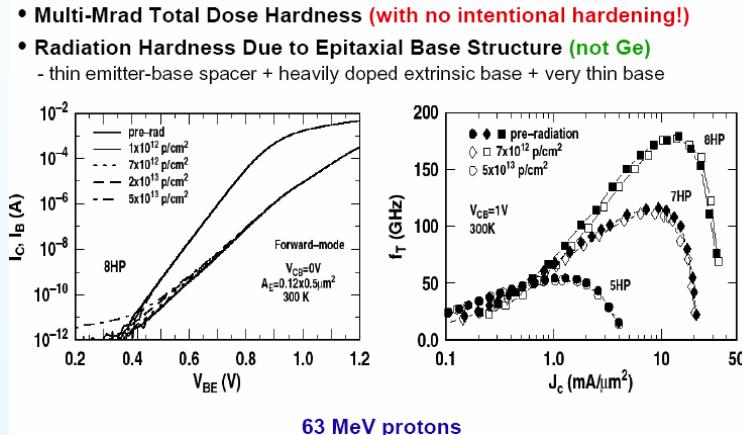


$$S_{I_B} = \frac{K_F}{A_E} \frac{I_C^2}{\beta^2}$$

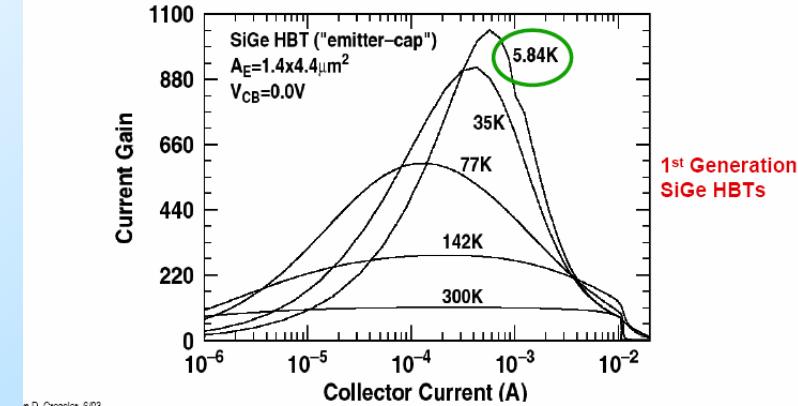
Sub-kHz
Corner Frequencies
Possible

FEE2003: John Cressler, GA Tech

Radiation Results



- SiGe Is Clearly Capable of Operation Down to the Helium-T Regime
 - base doping is above Mott transition – minimal base freeze-out
 - more work needed to flesh out the HeT design/operation space



Summary



SiGe HBT BiCMOS Technology:

- The SiGe HBT is the First Practical Bandgap Engineered Device in Si
- SiGe Combines III-V Device Performance at Si Cost (and CMOS for SoC)
- Compared to an Identically Constructed Si BJT, SiGe HBTs Offer Better:
 - $\beta + V_A + \beta V_A + f_T + f_{max} + 1/f + NF_{min}$
- There Is Still Room for Lots of Performance Improvement ($f_T > 300$ GHz)

Radiation Effects:

- Total Dose Hardness to Multi-Mrad Levels Without Hardening!
- No EDLRS; No Bias Effects; Minimal Displacement Effects
- Analog and RF Circuits Not Degraded By Total Dose Exposure
- SEU Is Clearly a Concern, But Mitigation Steps Appear Promising

Operation at Cryogenic Temperatures:

- Device Properties Improve Down to 77K!
- Operation at Helium Temperatures Is Feasible

→ SiGe Technology is Here to Stay!
→ Great Potential For Front-end Electronics!

John D. Cressler, FEE03

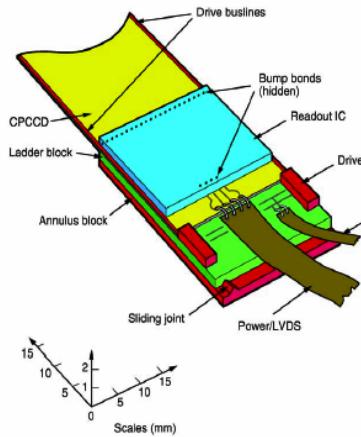
FEE2003: Marcus French, RAL



Read-out electronics for
a Linear Collider CCD
Vertex Detector

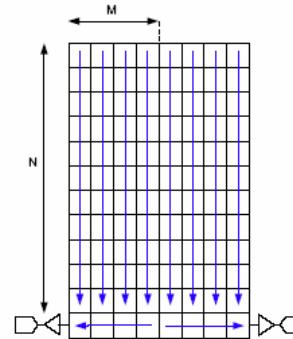
Microelectronics Group

Column Parallel Read-out (CPR) IC

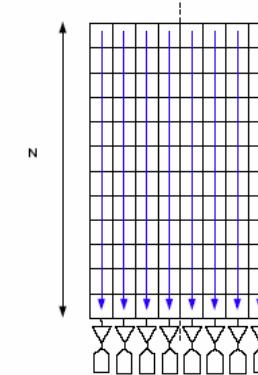


- Electronics only at the ends of the ladders;
- Bump-bonded assembly between thinned CPCCD and readout chip;
- Readout chip does all the data processing:
 - ◆ Amplifier and ADC for each CCD column
 - ◆ Hit cluster finding
 - ◆ Data sparsification
 - ◆ Memory and I/O interface
- CPCCD is driven with high frequency, low voltage clocks (~50MHz, ~2V);
- Low inductance layout for clock delivery.

Column Parallel CCD structure



Conventional CCD:
outputs at corners

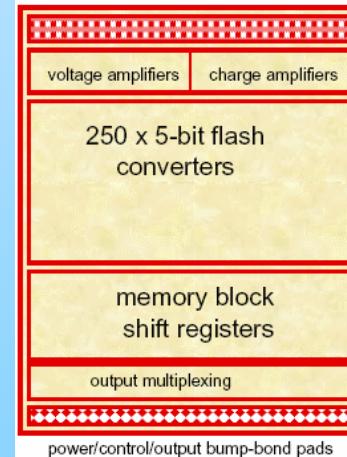


Column Parallel CCD:
outputs along one side

$$\text{Readout time} = N \times M / \text{Clock Freq}$$

$$\text{Readout time} = N / \text{Clock Freq}$$

input bump-bond pads



In CPR-1:

- Voltage amplifiers – for source follower outputs from the CPCCD
- Charge amplifiers – for the direct connections to the CPCCD output nodes
- Amplifier gain in both cases: 100 mV for 2000 e- signal
- Noise below 100 e- RMS (simulated)

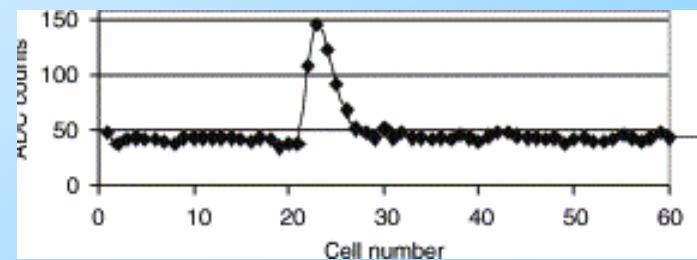
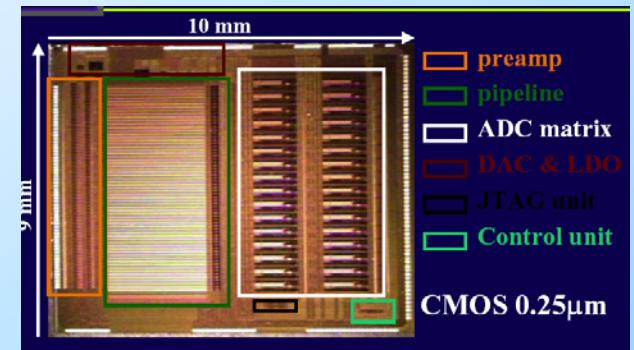
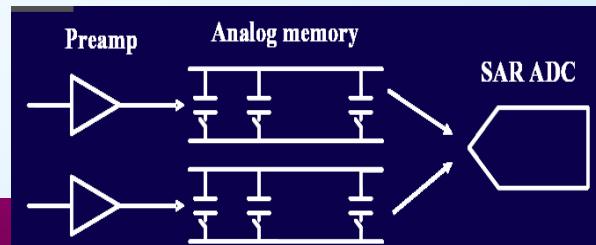
Direct connection and charge amplifier have many advantages:

- Eliminate source followers in the CCD;
- Reduce total power to ≈ 1 mW/channel, no active components in the CCD;
- Programmable decay time constant (baseline restoration).

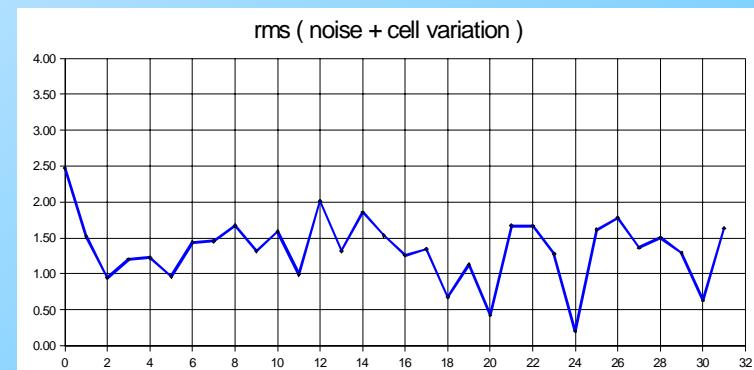
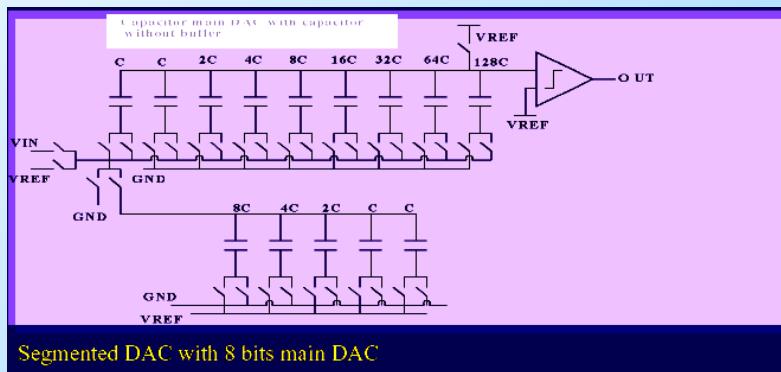
FEE2003: A. Rivetti, INFN Torino

A 64-channel Mixed-Signal ASIC for the Read-Out of Silicon Drift Detectors

- Gain : 26 counts/fC (36 mV/fC)
- Noise : 2 counts (480 e⁻)
- ADC resolution : 9.3 bit @ 2 MS/s, 8.1 bit @ 4 MS/s
- Non-linearity : < 0.9%
- Power consumption/ch : 4 mW (acq.) – 10 mW (conv.)
- Chip size : 7x6 mm²
- Technology : CMOS 0.25 μ m
- less than 10% noise degradation at 30 Mrads



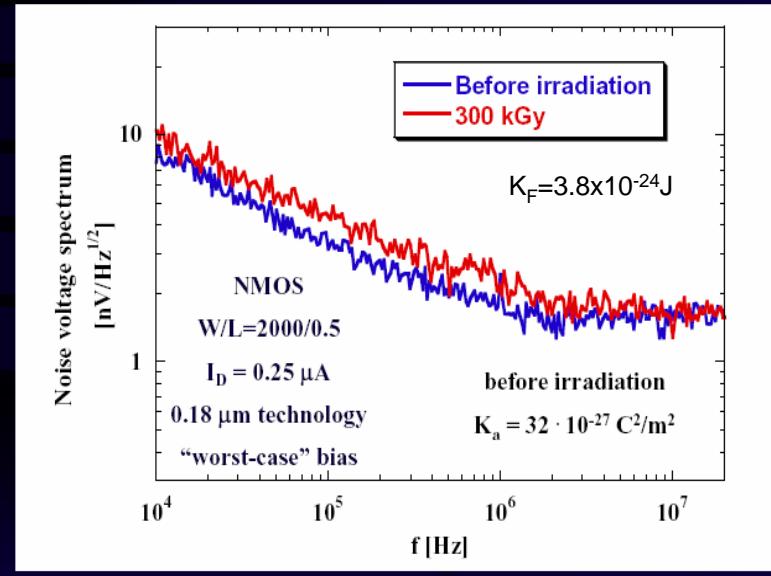
Also discussed by G. Mazza at
NSS
(paper N18-4)



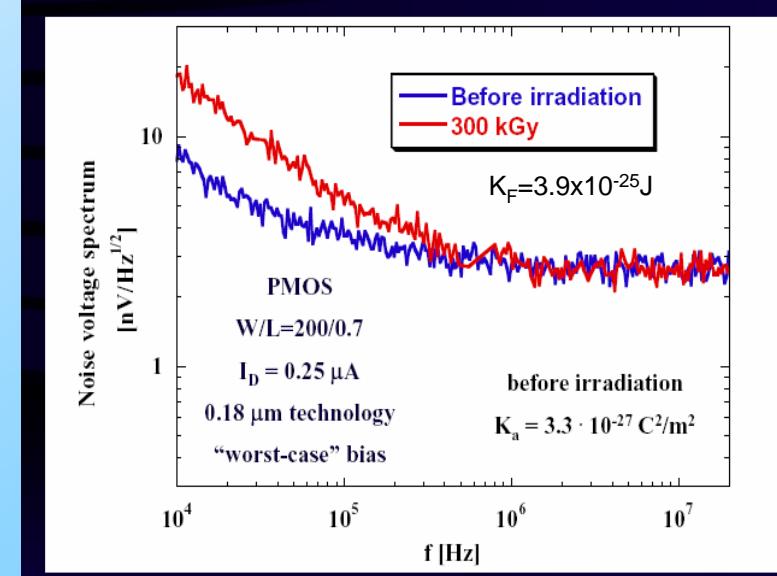
RMS noise+analogue cell variation 2 counts
(2.73mV - 460 e⁻)

Ionizing Radiation Effects on the Analog Parameters of a 0.18 μ m CMOS Technology

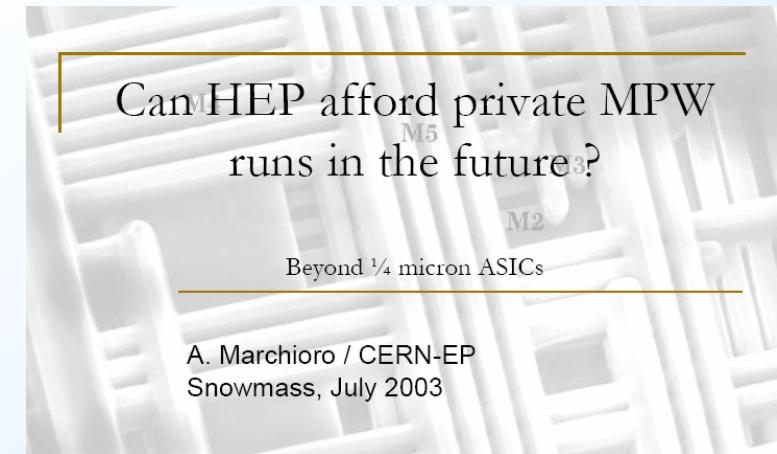
Noise voltage spectrum: NMOS



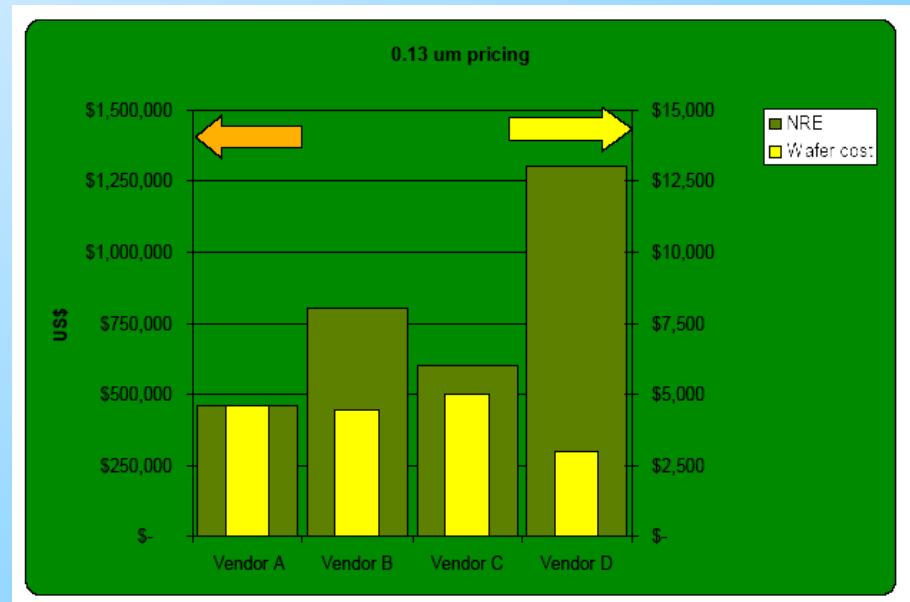
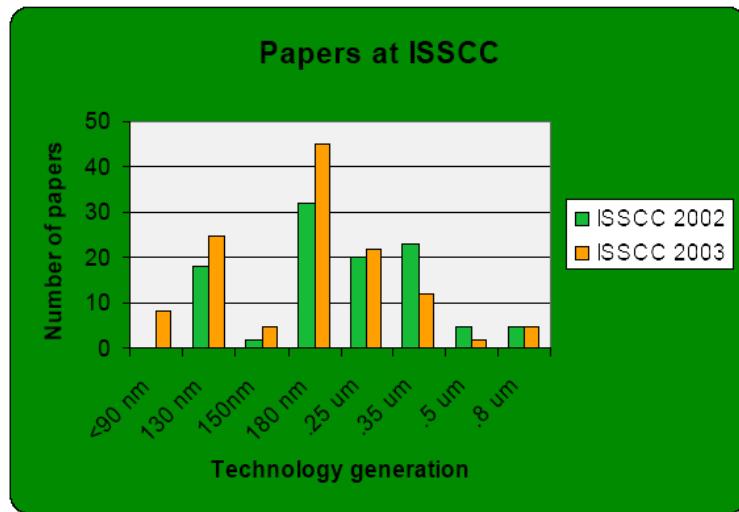
Noise voltage spectrum: PMOS



FEE2003: A. Marchioro, CERN

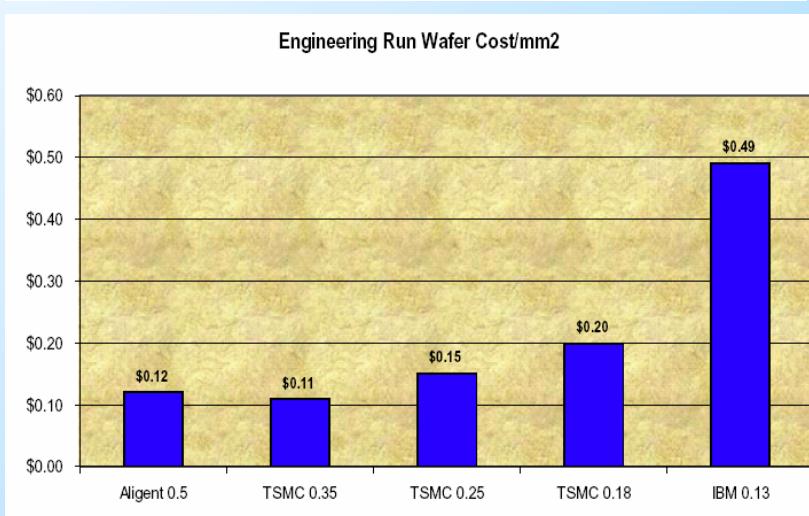
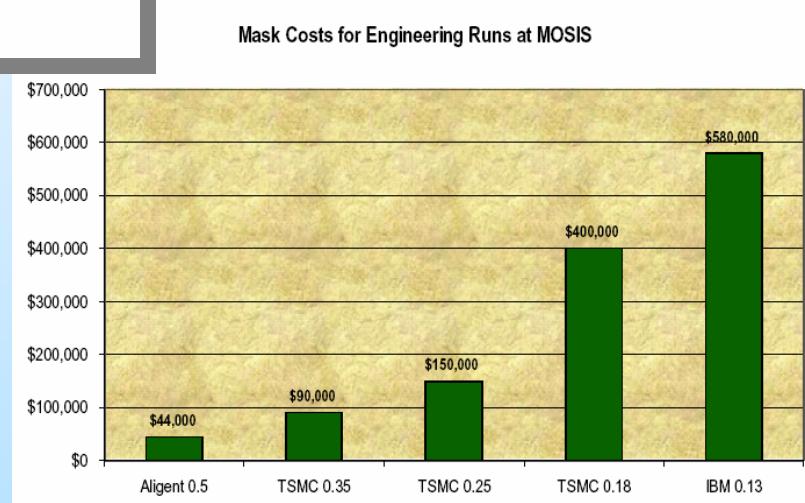
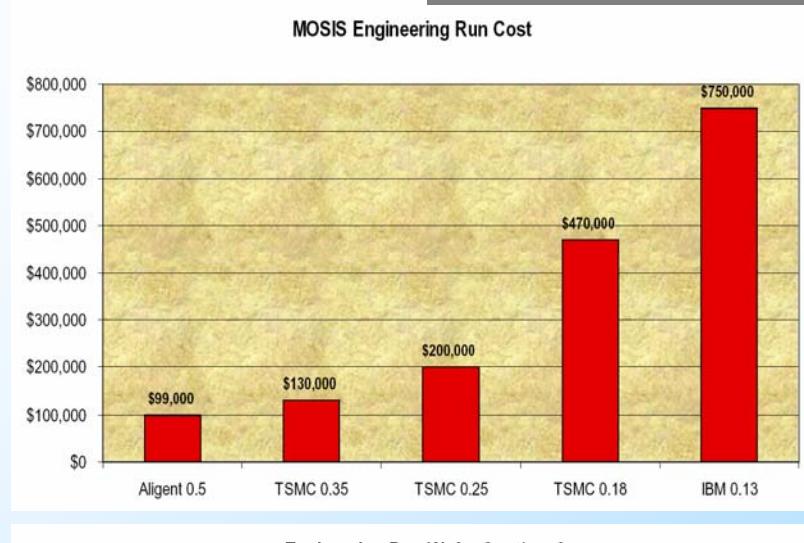


Where is industry going



FEE2003: R. Yarema, Fermilab

ASIC Fabrication Trends and Costs



Processes

- Increased mask cost is significant.
- Increased cost per square mm is offset by higher layout density.
- According to MOSIS the 0.25 μm and 0.18 μm processes are expected to be available as engineering runs for the next 5 years.
- According to MOSIS, mask cost does not decrease much over process lifetime.

“TRDs for the 3rd millennium”

II Workshop on advanced Transition Radiation Detectors for accelerator and space applications

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Bari, Italy, September 4-7, 2003

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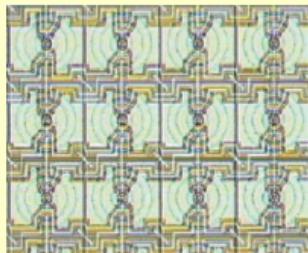
TRD2003: N. Rando, ESA

Space Science applications of cryogenic detectors



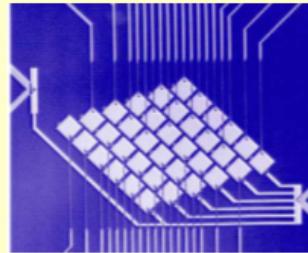
XEUS main instruments

Large field-of-view
imaging spectrometer:
Semiconductor based
(e.g. DEPFET array)



70 x 70 mm²
0.1 - 30 keV
50 eV FWHM @ 1 keV
75 μm position resolution
70 μs timing resolution
QE > 90% for E > 280 eV
 $T_{op} = 280$ K

High energy resolution
imaging spectrometers:
Cryogenic (STJ-based
and/or bolometer array)



7 x 7 mm²
0.05 - 7 keV, 0.5 - 15 keV
3 eV (goal 1 eV) @ 1 keV
150 μm position resolution
1 μs timing resolution
10 kHz/pixel
20-90 mK, 15-30 mK

D-SCI/A, Science Payloads &
Advanced Concepts Office



TRD 2003 – September 2003.

Detector type:	T_{op}	ΔE (fwhm)	Count rate.
TES(Mo-Cu)	80 mK	4 eV	< 1kHz
NTD - Bolometer	50 mK	5-7 eV	< 1 kHz
STJ (Ta-Al)	300 mK	10 eV	< 100 kHz
Magnetic Calorimeter.	35 mK	< 10 eV	< 1 kHz
SC granules.	100 - 1200 mK	NA	< 1kHz

@ 6 keV

XEUS will provide a major leap forward in capability:

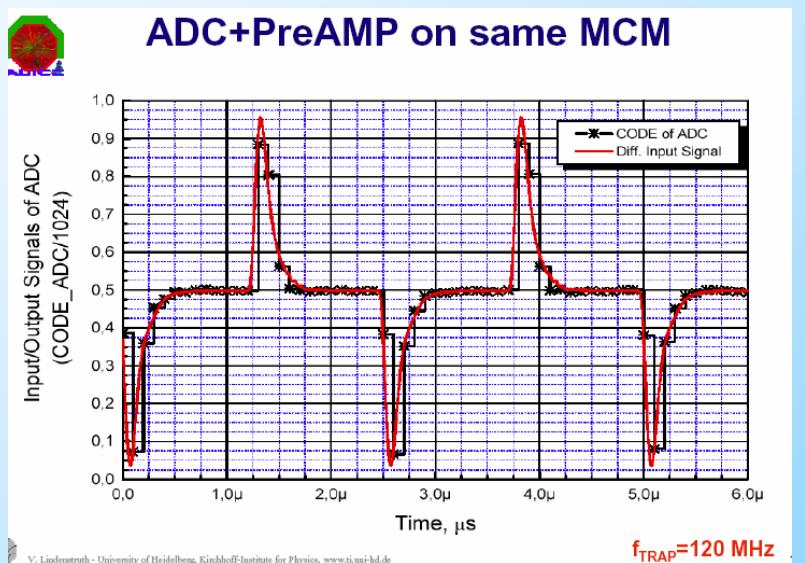
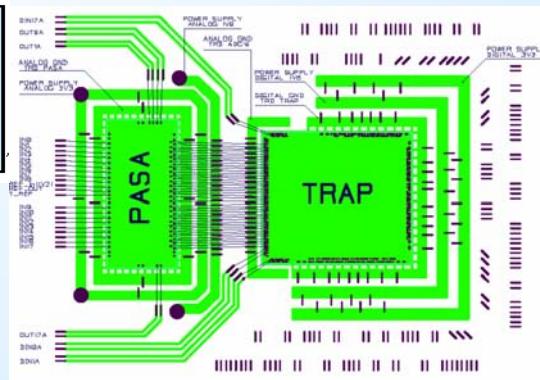
- 30 m² of collecting area (fully grown), 6 m² (zero growth) at 1 keV
- 3 m² at 8 keV and 1000 cm² at 20 keV
- Imaging resolution with a goal at 1 keV of 2" HEW (Half Energy Width)
- A limiting sensitivity of $4 \cdot 10^{-18}$ erg cm⁻² s⁻¹ – about 250 times deeper than XMM-Newton
- Spectral resolution with a goal of 1 eV at 1 keV (specification 2 eV)
- Broadband coverage between 0.05 and 30 keV
- A field of view of 5 arc minutes

- Growing importance of cryogenics in Space Science and remarkable technological progress over last 20 yr.
- Large number of future astrophysics / fundamental physics missions based on cryogenic instrumentation
- Key role played by cryogenic detector technology
- XEUS as study case and example of emerging trends.

FEE2003: V. Lindenstruth, KIP Heidelberg

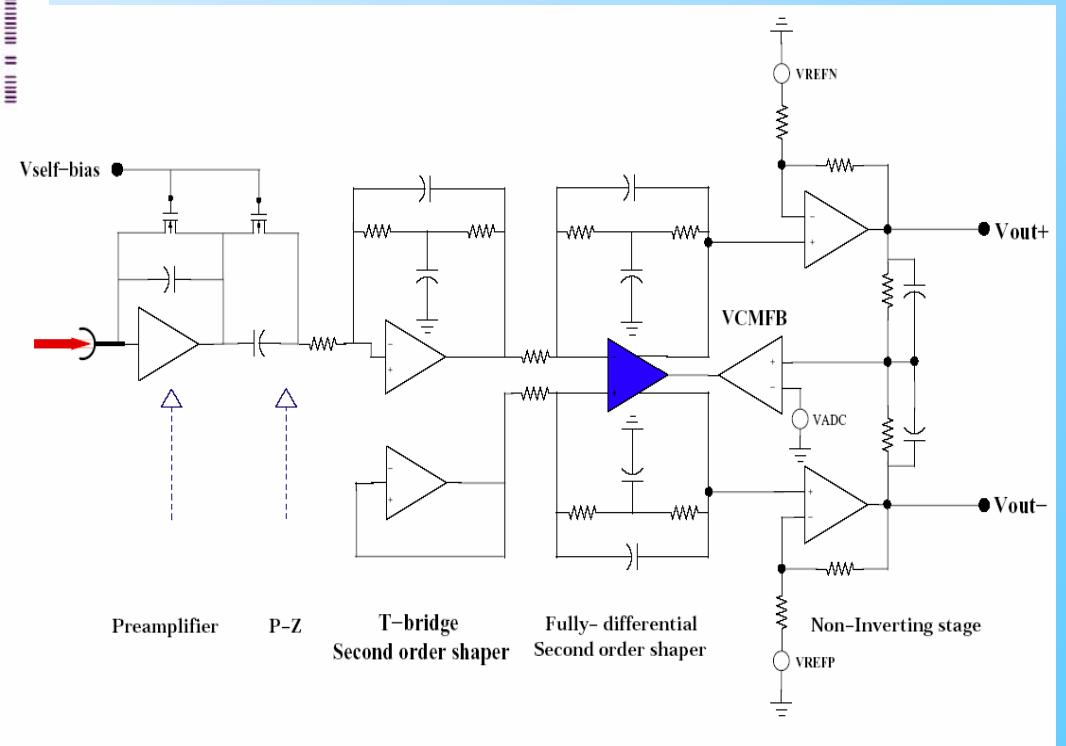
Fast on-detector integrated signal processing:
status and perspectives (Readout electronics
for the ALICE TRD)

- ◆ 1.2 million channels
- ◆ 1.425 million ADCs
- ◆ peak data rate: 17.8 TB/s
- ◆ 64224 MCMs
- ◆ computing time: 6 μ s

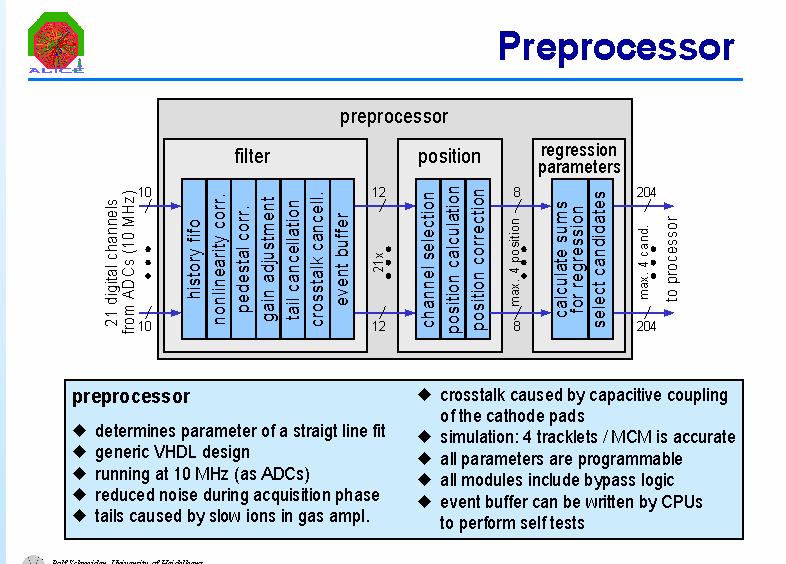
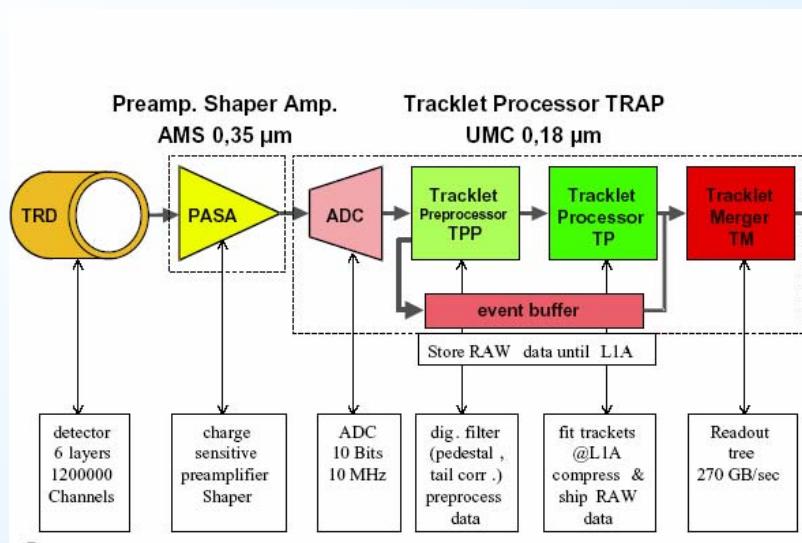


PASA:

- NMOS-input CS-preamp
- CR-RC⁴, 30 ns shaper
- ENC 210 + 25 e⁻/pF
- dynamic range 165 fC
- programmable test pulse generator
- differential output
- 11 mW/chan
- AMS 0.35 μ m CMOS
- 200 μ m channel pitch



FEE2003: V. Lindenstruth, KIP Heidelberg



TRAP:

- 240 MHz clock
- 21 10b cyclic ADCs (12 clock latency)
 - 10MSa/s, 7.5mW per ADC
 - 0.07 mm^2
- digital filter:
 - nonlinearity correction
 - dynamic pedestal subtraction
 - gain adjustment
 - programmable tail cancellation filter (2 exp.)
 - crosstalk suppression filter
- tracklet preprocessor
 - charge accumulator
 - cluster charge threshold
 - center-of-gravity calculation

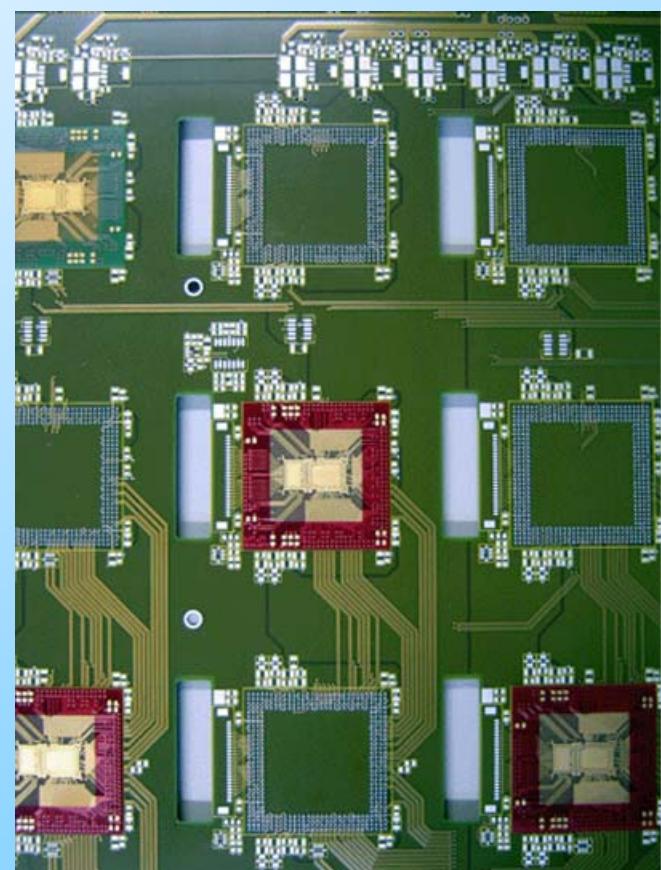
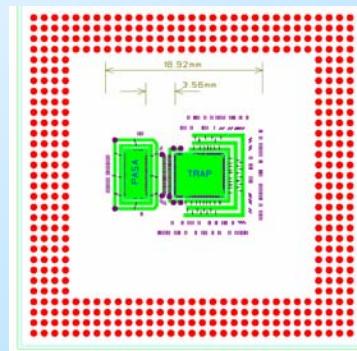
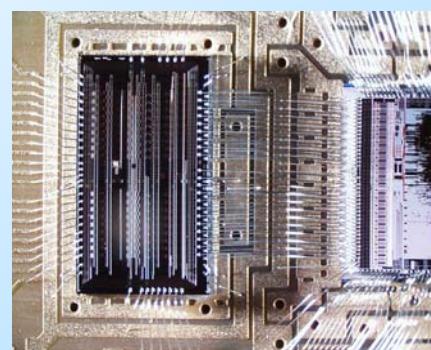
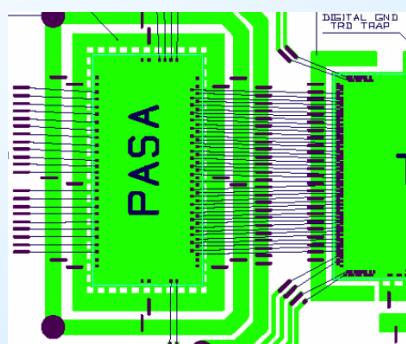
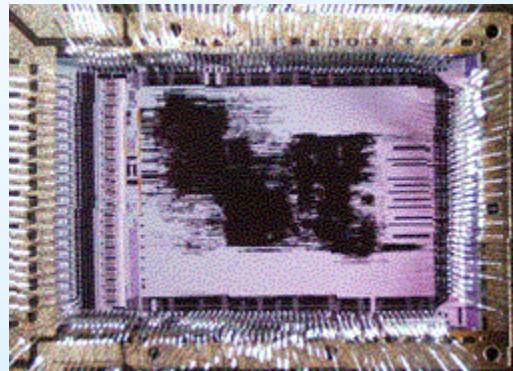
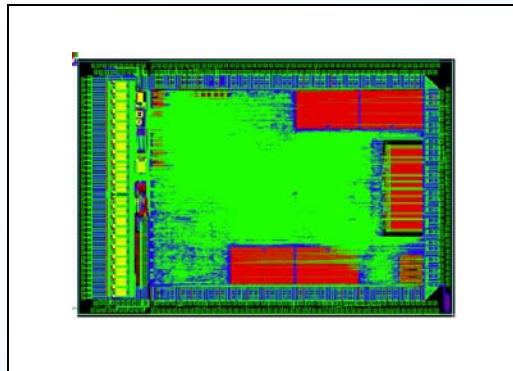
- event buffer for raw data

Processor

- quad RISC CPU
- shared data memory, separate instruction memory
- four RISC CPU's, 4kB quad-port SRAM
- fast 32b multiplier in ALU
- 4-tracklet candidate fitting
- data compression

- ~ 6M transistors
- UMC 0.18um CMOS

FEE2003: V. Lindenstruth, KIP Heidelberg





Nuclear Science Symposium
Medical Imaging Conference
13th International Workshop on Room-Temperature
Semiconductor X- and Gamma-Ray Detectors
Symposium on Nuclear Power Systems

October 19-25, 2003 • Doubletree Hotel -- Hayden Complex • Portland, Oregon, U.S.A.



- 4 multi-day conferences
- 1200 contributions (oral & poster)
- 7 workshops
- 7 short courses
- Industrial exhibit (40 companies)

NSS2003: M. Volpert, CEA-LETI, Grenoble

**ULTRA FINE PITCH HYBRIDIZATION OF
LARGE IMAGING DETECTORS**

M.Fendler, M.Volpert, F.Marion, L.Mathieu, J.-M. Debono, P.Castelein, C.Louis

CEA-DRT-LETI/DOPT - CEA/GRE
17,rue des Martyrs – 38054 GRENOBLE Cedex 9 - FRANCE

 CEA / LETI
Optronic Dept. / Infrared Labs.

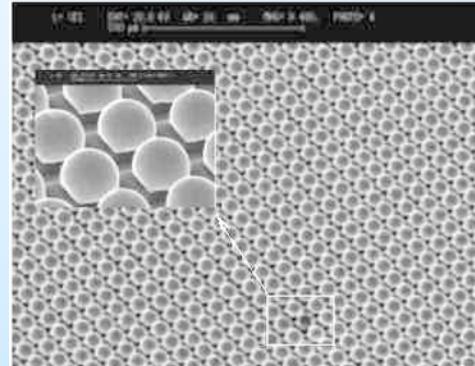
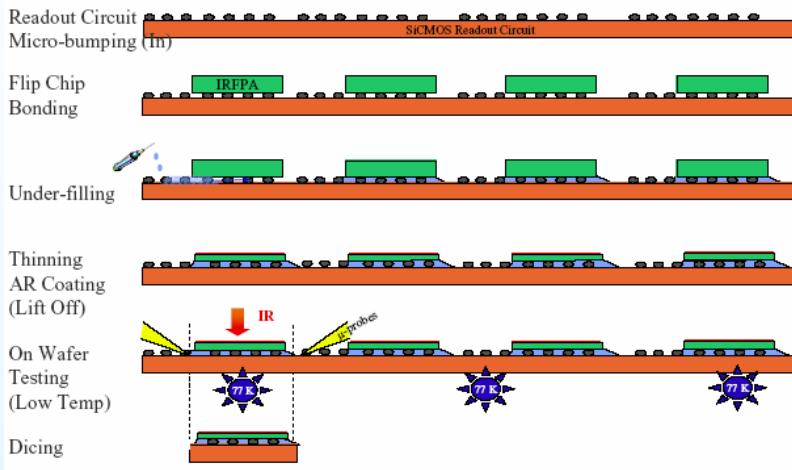
 Sofradir

leti Optronic Dept. / Infrared Labs (LIR) 1

NSS2003: M. Volpert, CEA-LETI, Grenoble

Hybridization Process

PROCESS FLOW CHART



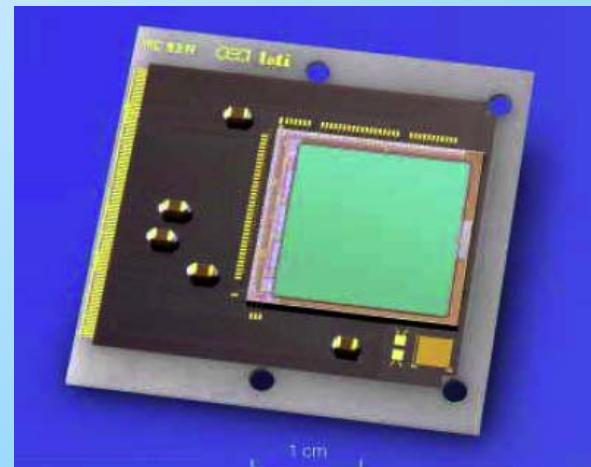
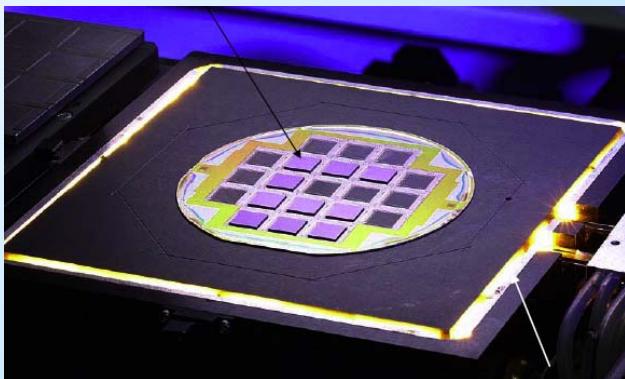
Wafer-scale hybridization
Indium bumps, 15um pitch,
underfill

Test before dicing

Ageing & temp cycling:

- 90°C, 15 days
- 1000 cycles, room temperature → 77K
- “11 out of 15 assemblies had 99.8% pixels operability”

Production 2005



NSS2003: C. Gillot, CEA-LETI, Grenoble

Assessment of advanced Anisotropic Conductive Films for Flip-Chip Interconnection based on Z-axis conductors

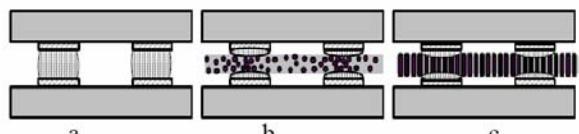
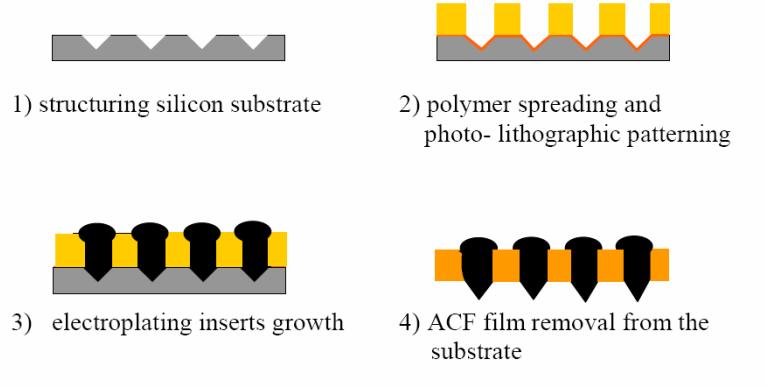
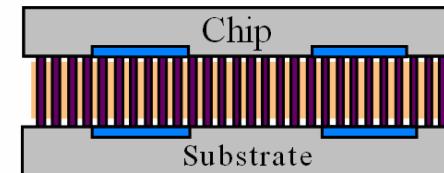


Figure 1 : Cross-section of Flip-Chip bonding a) micro-balls, b) ACF containing conductive particles and c) Z-axis ACF

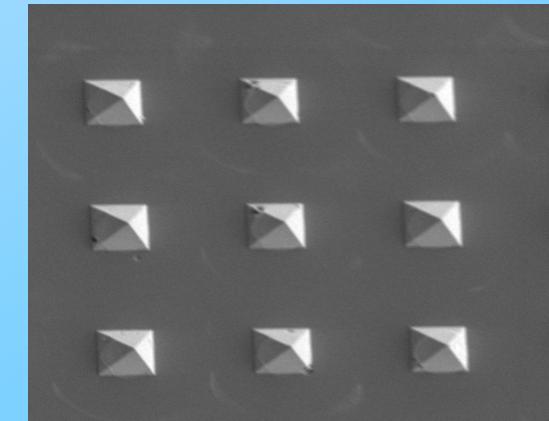
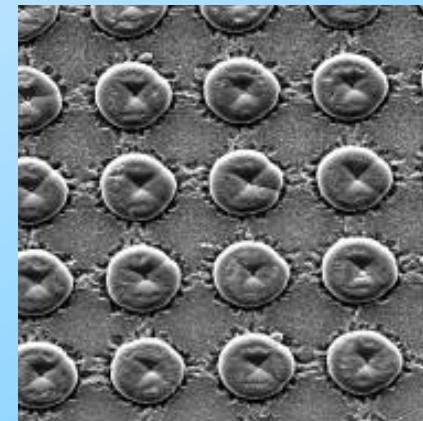
Advantages : lower temperature processing, no underfilling process, **no need of bumps on pads, pitch down to 20 µm, low contact resistance**



Flip-chip : Structured Z-axis ACF



LETI Z-axis ACF



NSS2003: C. Gillot, CEA-LETI, Grenoble

