

Overview:

The PHENIX TEC- Preamp/Shaper CMOS Integrated circuit is designed for the PHENIX tracking system. The tracking system of PHENIX is designed to locate all charged tracks of interest within their fiducial volume, measure the particle momenta, help in identifying which of the tracks are electrons, and contribute trigger information to the PHENIX detector.

The sub-detector namely the Time-Expansion Chamber (TEC), for which the monolithic circuit is designed for preforms both particle Identification and tracking functions in PHENIX. Through measurement of charged particles ionization losses (dE/dx), the detector allows separation of Electrons from Pions over a momentum range of 250 MeV/c to 3.0GeV/c.

The TEC front-end electronics consists of a preamplifier and a 70ns shaping amplifier chain, is implemented in the monolithic circuit. The parameters of the electronics are determined by the requirements of both TEC's dE/dx and TRD operations. A shaping time of 70ns is chosen so that the FADC clock runs at a fraction of the shaping time to assure good position resolution. The Shaping time is also appropriate for the Transition Radiation (TR) measurements, where the shaping time chosen will allow containment of the total signal from the TR X-Ray absorbed by the gas chamber. The output of the shaper is split into two, so that the FADC has sensitivity for both low dE/dx signals (0.2 - 0.3 KeV for Xe gas), and the Transition Radiation signals (3 - 10 KeV for Xe gas). The preamplifier-shaper electronics is designed for 70ns shaping time and a FWHM < 100ns. The ENC to be less than 1500 electrons (70ns, 30-40pF) to ensure Electron - Pion separation. The shaping function is unipolar, with a Semi-Gaussian impulse response

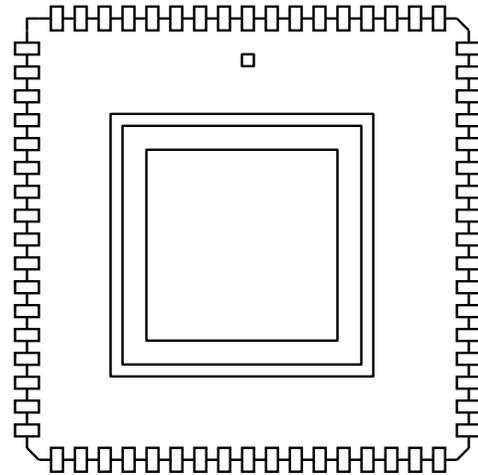
Features:

- ◆Multi-Channel (Eight).
- ◆Low and High gain outputs for TR and dE/dx .
- ◆Onchip Calibration capacitors for every channel.
- ◆Digitally programmable calibration mask.
- ◆Digitally programmable peaking time, 4 steps.
- ◆Digitally programmable gain, 8 steps.
- ◆Digitally programmable Tail cancellation, 8 steps.
- ◆Digitally programmable Channel masks.
- ◆All programmable bits implemented using serial interface logic, and chips can be daisy chained.
- ◆Low Power, 44mWatts /channel.

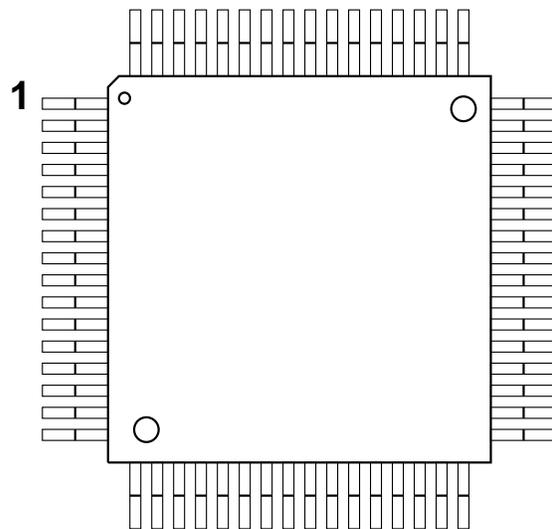
◆Size: 3.5mm x 5mm.

Package Description:

68-J-Leaded Ceramic:



64 PQFP:



Pin Description:

Pin descriptions for both the packages are showing in Table 1

Table 1: Pin Description

68 LDCC	64 PQFP	PIN
1	8	RET 4
2	9	IN 3
3	10	RET 3
4	11	IN 2
5	12	RET 2
6	13	IN 1
7	14	RET 1
8	15	IN 0
9	16	RET 0
10	18	VDD
11	19	OBIAS
12	20	VDDP1
13	21	VSSP1
14	22	GNDS1
15	23	DIN
16	24	VDDP1
17	25	LD
18		
19	26	CLK
20	27	MODE
21	28	DOUT
22	29	CALIB
23		
24	30	VSS
25	32	VSSS1
26	33	DE/DX 0
27	34	TR 0
28	35	DE/DX 1
29	36	TR 1
30	37	DE/DX 2
31	38	TR 2
32	39	DE/DX 3
33	40	TR 3
34	41	DE/DX 4
35	42	TR 4

Table 1: Pin Description

68 LDCC	64 PQFP	PIN
36	43	DE/DX 5
37	44	TR 5
38	45	DE/DX 6
39	46	TR 6
40	47	DE/DX 7
41	48	TR 7
42		
43		
44	50	VSSS2
45		
46		
47	52	DOUT
48		
49		
50	54	REF 2
51	55	REF 1
52	56	VB 2
53	57	VB 1
54	58	VDDS2
55	59	GNDS2
56	60	VSSP2
57	61	VDDP1
58	62	IBIAS
59	64	RBIAS
60		
61		
62	1	IN 7
63	2	RET 7
64	3	IN 6
65	4	RET 6
66	5	IN 5
67	6	RET 5
68	7	IN 4

N/C: 68 LDCC: 18,23,42,43,45,46,48,49,60,61

N/C: 64 PQFP: 17,31,49,51,53,63

Pin Details:
Analog Section:

IN [0:7]: Preamp Inputs channel 0 to channel 7.
RET [0:7]: Preamp Returns channel 0 to channel 7.

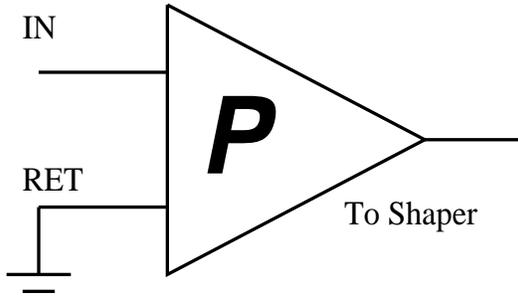


Fig 1. Preamplifier.

TR[0:7]: Transition Radiation output.
dE/dx[0:7]: Ionization energy loss output [x5].

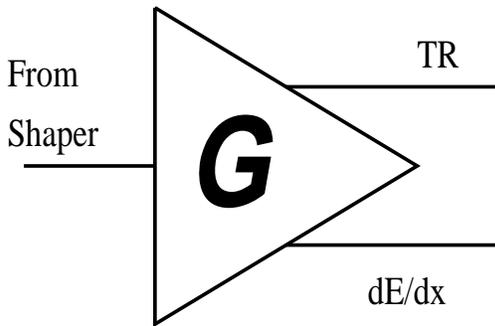


Fig 2. Output gain stage.

REF 1 and REF 2: DC offset correction control, if unused connected to GND. Should be decoupled.

CALIB: Calibration signal input.

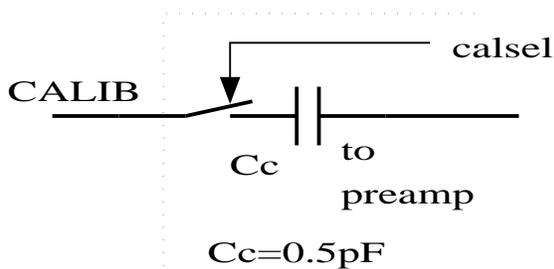


Fig 3. Calibration module.

The CALIB is the external signal applied to the chip for calibration, The Calibration capacitor used on chip is

0.5pF, and the calibration switch for each channel is selected using serial configuration.

IBIAS, RBIAS, OBIAS: Shaping stage Bias lines.
VB1 and VB2: Preamplifier Bias lines. These lines should be decoupled using 0.1uF ceramic chip capacitors close to the pins, as shown below.

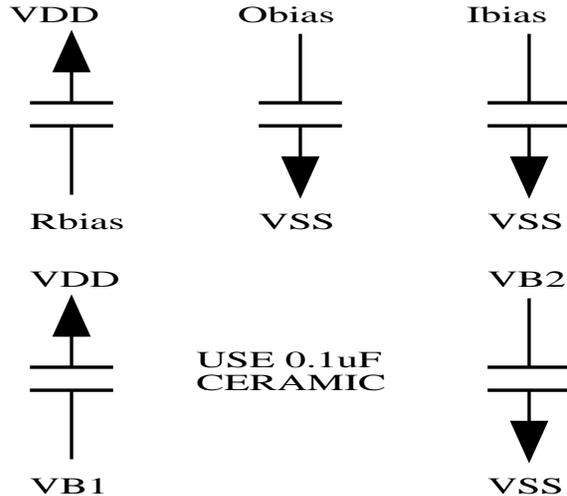


Fig 4. Bias line decoupling.

Digital Section:

- CLK:** Serial interface registers shift clock, (Negative edge triggered registers).
- DIN:** Serial interface Data input
- DOUT:** Serial interface Data output to daisy chain and readback. [4mA output driver].
- LD:** Parallel registers Load signal, (Negative edge triggered registers).
- MODE:** Serial interface function selector, Mode = 0; Default all channels enabled with calibration on and with default circuit parameters: Mode = 1; Serial interface enables, and data set it from download stream.

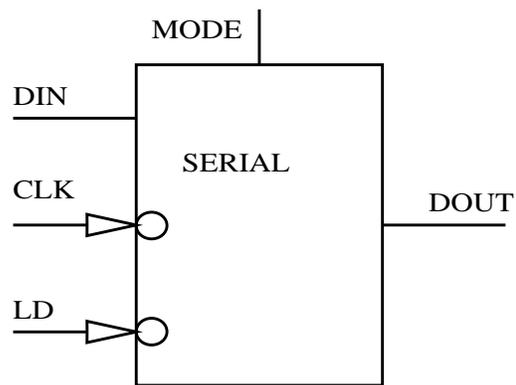


Fig 5. Serial Interface.

The mode line has a internal pull-down resistor of 8K to VSS.

Power Supply:

- VDD: ESD ring positive supply (+2.5V).
 - VSS: ESD ring negative supply (-2.5V).
 - VDDP1, VDDP2: Preamplifier positive supply (+2.5V)
 - VSSP1, VSSP2: Preamplifier negative supply (-2.5V).
 - VDDS1, VDDS2: Shaper positive supply (+2.5V).
 - VSSS1, VSSS2: Shaper negative supply (-2.5V).
 - GNDS1, GNDS2: Shaper ground (0V).
- Decoupling the supply pins are essential.

Serial Interface Module:

The serial interface module in the integrated circuit is used for setting circuit parameters of the preamp-shaper chain. The circuit parameters that are configured using the serial interface are 4 steps of Peaking time, 8 steps of ion tail cancellation and 8 steps of coarse gain adjustment.

The serial interface is also used to control two other functions namely the calibration and channel enable/disable mask. By default when at MODE=0 the IC is set to the following state.

- Shaping Time: TP1:TP0 = 01
- Ion Tail cancellation: TC2:TC1:TC0 = 011
- Gain: G2:G1:G0 = 101
- Calibration: channel 0 to 7: Enabled.
- Channel 0 to 7: Enabled.

The internal architecture of the serial interface is shown in figure 6.

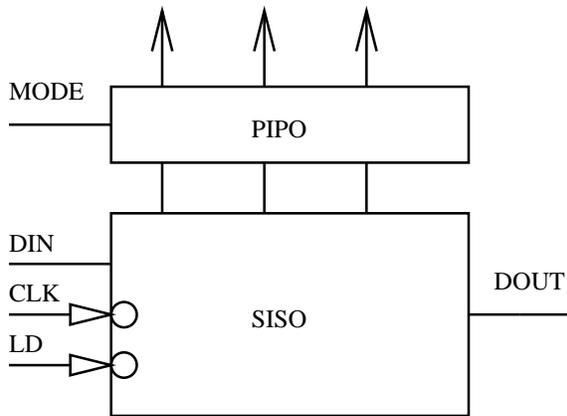


Fig 6. Internal architecture of the serial interface.

The serial interface is made up of a 24 bit, Serial-In-Serial-Out (SISO) shift register, another 24 bit Parallel-In-Parallel-Out (PIPO) latch, a output multiplexer for multiplexing serial data and default data using MODE control and a 1/2 cycle delay register.

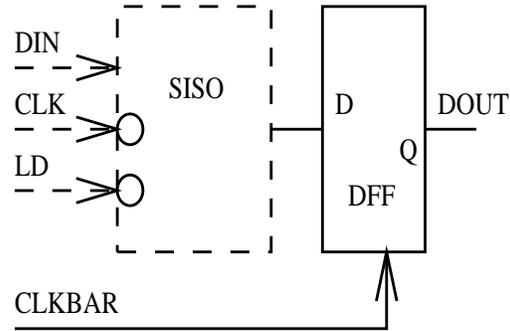


Fig 7. 1/2 cycle Delay cell.

The delay cell is necessary to preserve the data and clock timing offset, to ease the setup and hold conditions.

Serial control word:

The serial control word is 3 bytes long. The bit-wise information is shown in figure 8.

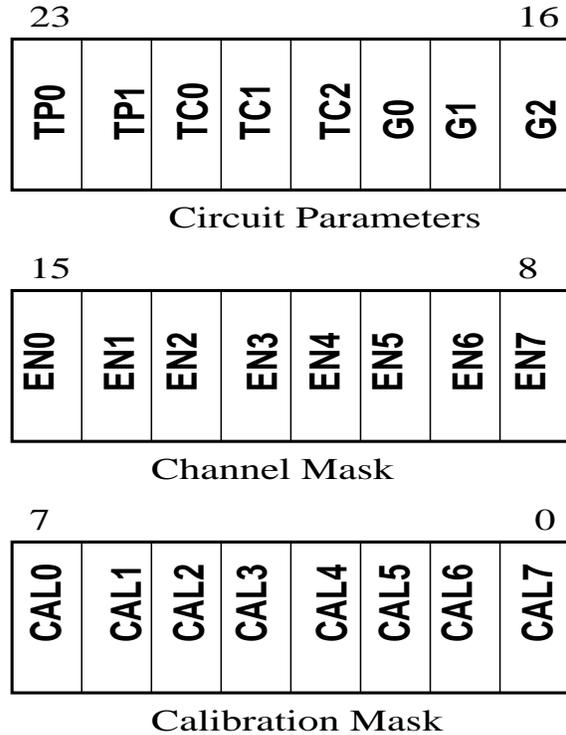


Fig 8. Serial Control word.

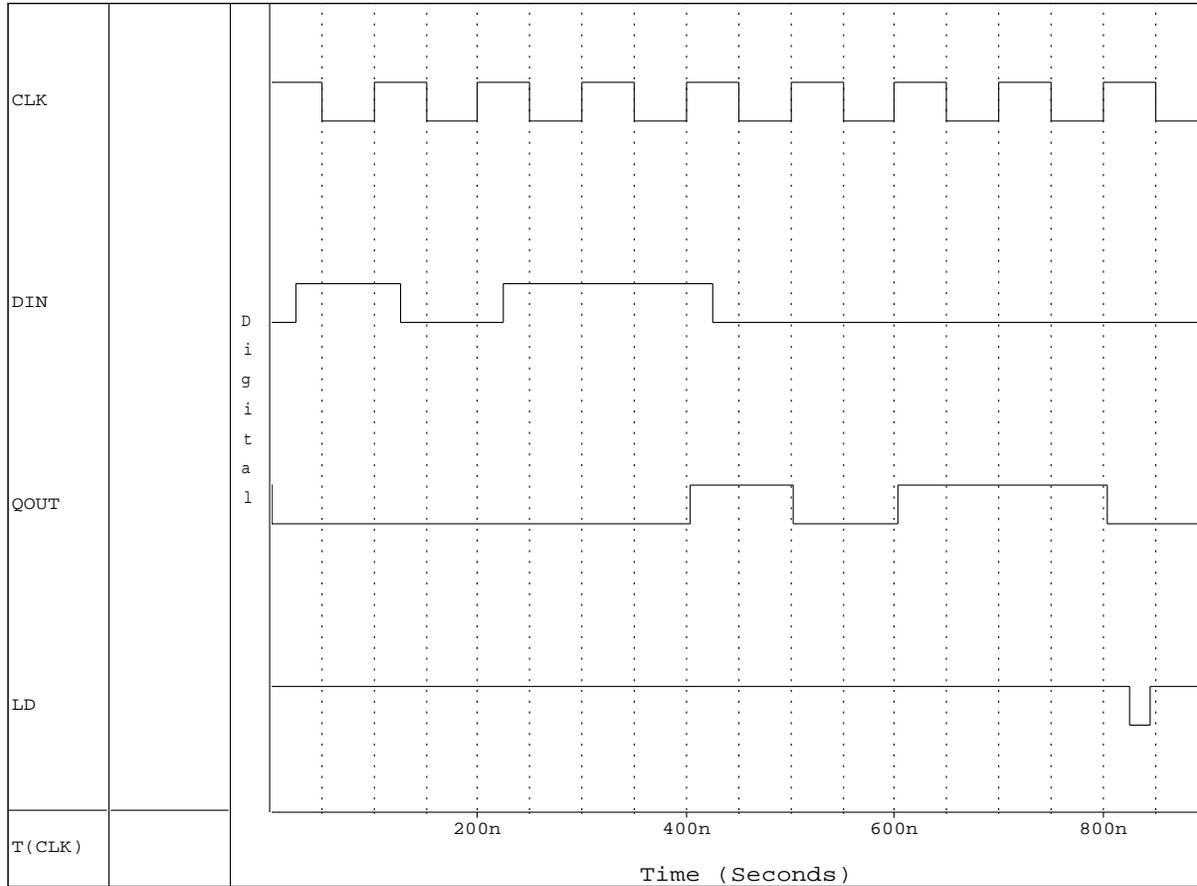


Fig. 9. Serial Interface Logic Diagram example.

The worst case timing condition taken from the SCMOS standard cell library for the D-Flip Flop used in the shift registers are shown in table 2.

Table 2: D-FF Timing

Parameter	Value
Setup time	3.56ns
Hold time	1.49ns
CLK pulse width	5.29ns

The inputs to the shift registers are buffered using Schmitt-trigger input pads. Noise immunity can even be further improved by adding non-inverting schmitt trigger inverter chain. A typical scheme is shown in figure 10, which consists of a RS-422 receiver to receive TTL signals and also for level translation to the compatible logic levels for the chip which is +2.5 (logic High) and -2.5 (logic Low)

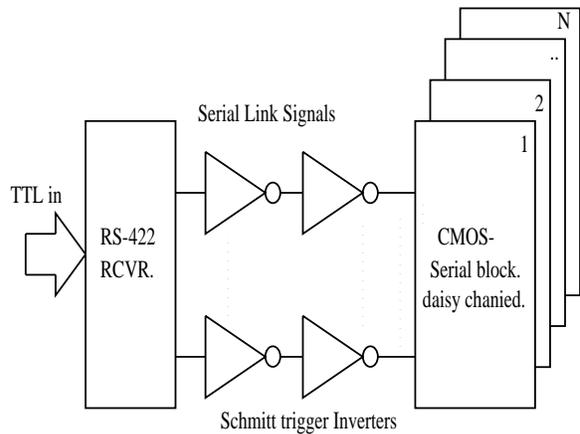


Fig 10. Typical Serial link scheme.

The data output of each TEC-PS can be daisy chained, and the output driver can drive upto 4mA of current. The logic conversion of TTL to custom level of $\pm 2.5V$ is done by the RS-422 receiver, running of $\pm 2.5V$.

Electrical Specifications:

Parameter		TYP	Note ^a
GAIN (mv/fC)	TR	4.3	Gain and Shaping time ranges for the dE/dx give below in mV/fC and nSecs respectively. Gain: 12 to 50 in 8 steps Shaping time: 60 to 120 in 4 steps
	dE/dx	21.3	
Shaping Time (nS)	TR	73.6	
	dE/dx	74.3	
Offset (mV)	TR	-3.63	
	dE/dx	-0.066	
ENC (r.m.s electrons) [Cdetector = 18pF]	TR	1697	
	dE/dx	1251	

a. There are 256 combinations of gain and shaping time due to Gain, Peaking and Tail cancellation settings only a few of the gain settings are listed here to show the gain range.

Power Supply:

Supply			Units
VDD	Voltage	+2.5	Volts
	Current	57	mA
VSS	Voltage	-2.5	Volts
	Current	52	mA
GROUND/RETURN	Current	5	mA

The power supply numbers above correspond to the multi-channel chip (8) and not a single channel. The electrical parameters were obtained under the following test conditions. Vdd = +2.5 V; Vss = -2.5V; REF1 = 0V; REF2 = 0V Each channel was tested by injecting a known charge, by applying a voltage step to the internal calibration capacitors, and the output was observed using a scope terminated at 50 Ω, The TR and dE/dx output was buffered using analog devices AD811, with a Gain = +1, operating from ±15V. The block diagram of the test setup is shown in figure 11.

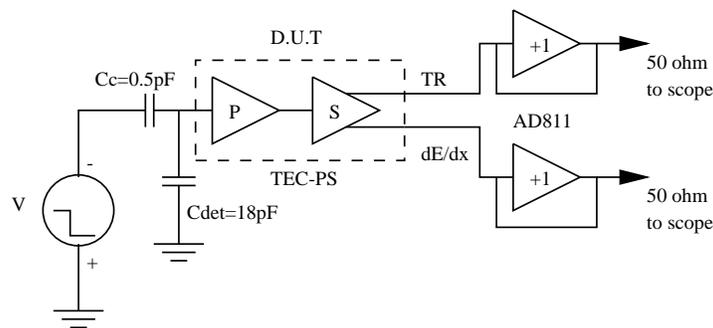


Fig 11. Test Setup for Electrical parameter measurement.

Figure 12, shows the two dE/dx and TR waveforms of a single TEC-PS channel injected with 100mV negative step into a 0.5pF injection capacitor,[charge of 50fC]. [Note the Vertical scale change].

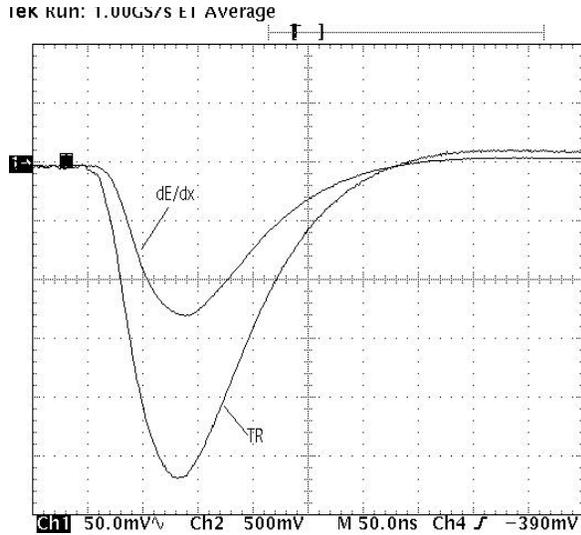


Fig 12. TR and dE/dx output waveform.

The CMOS can be tested for a first order working condition by monitoring the bias voltages, and the input bias condition of the pre-amplifier. Table 3 provides the bias voltages levels expected out of a functioning chip.

Table 3: Monitor outputs.

Node		Units
VB1	102	mV
VB2	-953	mV
RBIAS	-1.145	V
IBIAS	-1.136	V
OBIAS	-1.437	V
PREAMP-INPUT	1.187	V

The monitor output values are typical values.

Test Beam results:

Results obtained from the May 1996, Beam test at the AGS facility at BNL are shown in figures. 13 to 15. The TEC-PS was tested connected to one plane of the TEC in the AGS environment.

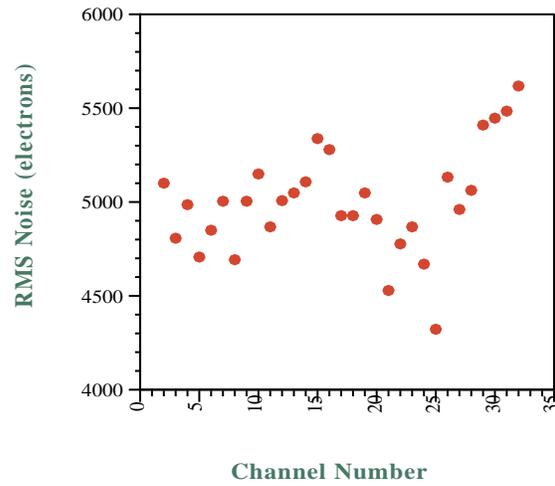


Fig 13. RMS noise in Chamber.

Figure 13, shows the total rms noise of the chamber and the CMOS electronics during.

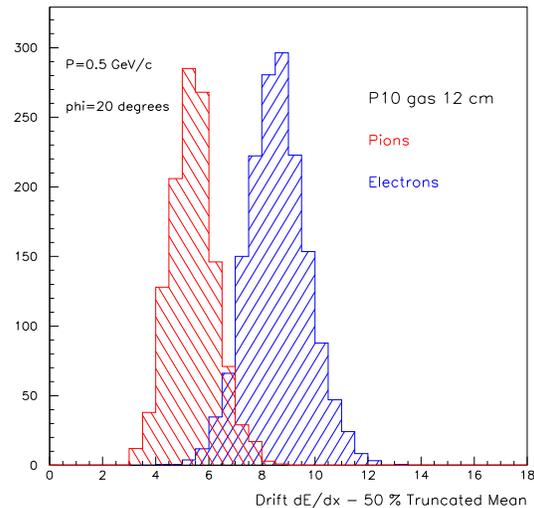


Fig 14. electrons-pions identification.

Electron and pions were identified using the Cherenkov and Lead Glass information. The dE/dx distribution was calculated by taking the average of the Nevis Fadc time bins eliminating the highest 50% of the FADC values.

Figure 15, pion efficiency figure: To evaluate the electron-pion separation we select a FADC value for which 90% of the electron are identified correctly and we calculate the "pion efficiency", the probability of mis-identifying a pion as an electron. A comparison of the

"pion efficiency" hybrid electronics and the CMOS preamp shaper shows that overall the CMOS electronics performs better than the hybrid although the noise was on the higher side. We think this difference could be due to the CMOS better tail cancellation characteristics.

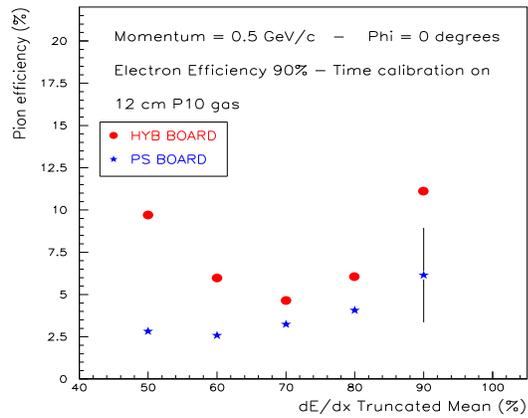


Fig 15. Pion efficiency of the TEC-PS.

Process specifications:

The CMOS preamp-shaper for the TEC is fabricated using Hewlett Packard's 1.2 micron Analog process with Poly-silicon resistors and linear capacitors, namely CMOS34/AMOSI.

TEC-PS Die:

TEC-PS

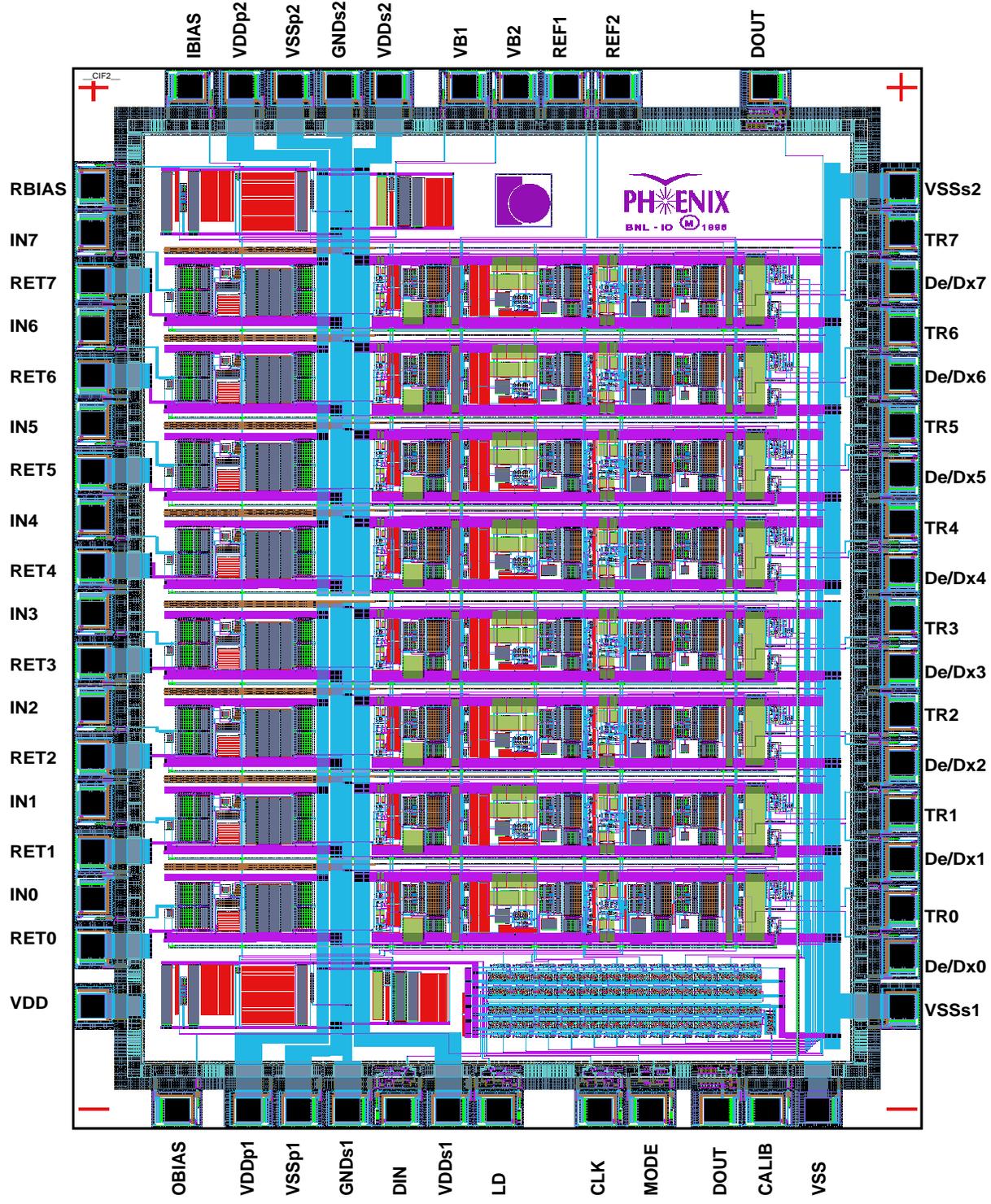


Fig 16. TEC-PS Bonding Diagram for 68 pin LDCC package.

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TEC-PS 64 pin PQFP Bonding Diagram:

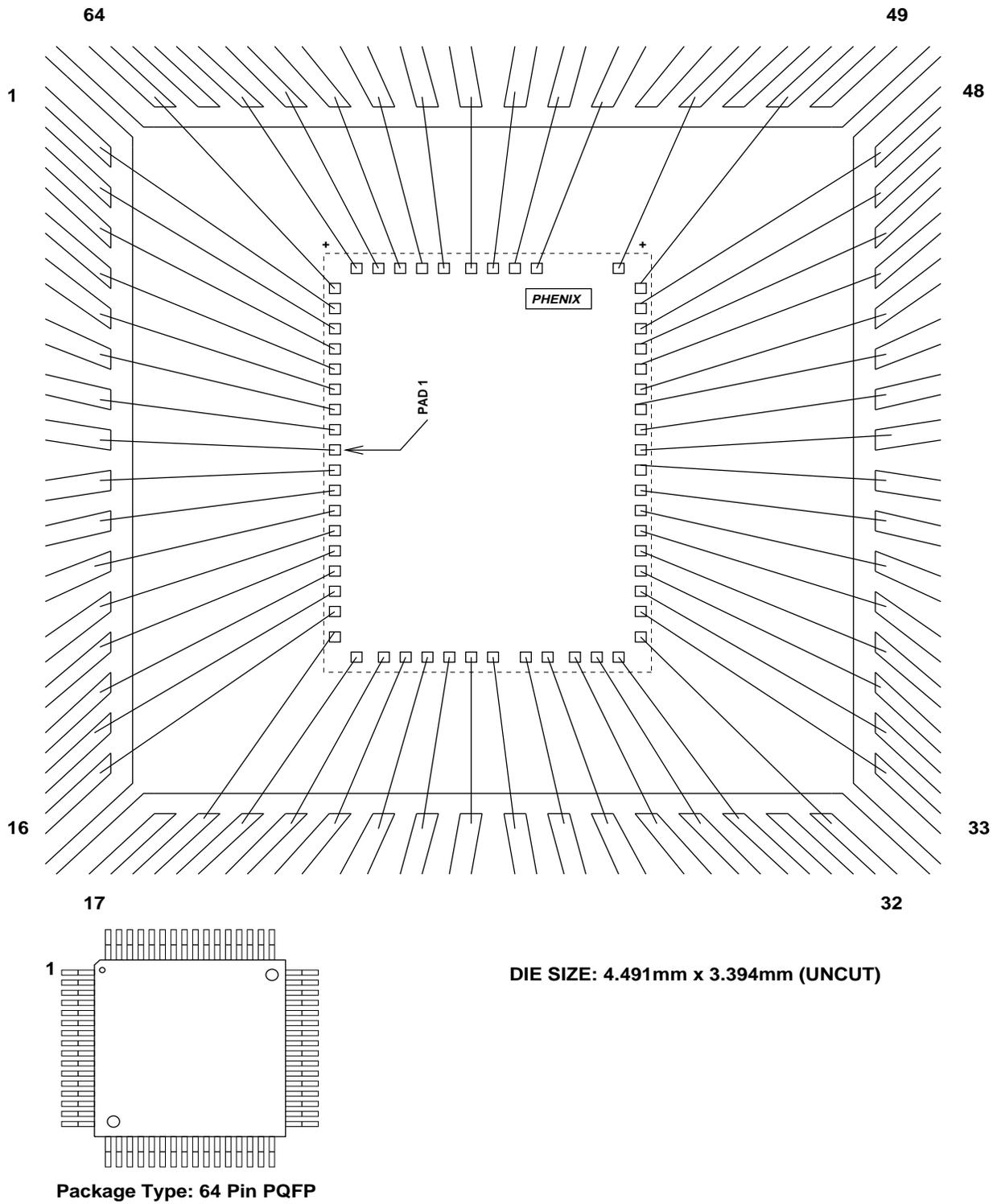
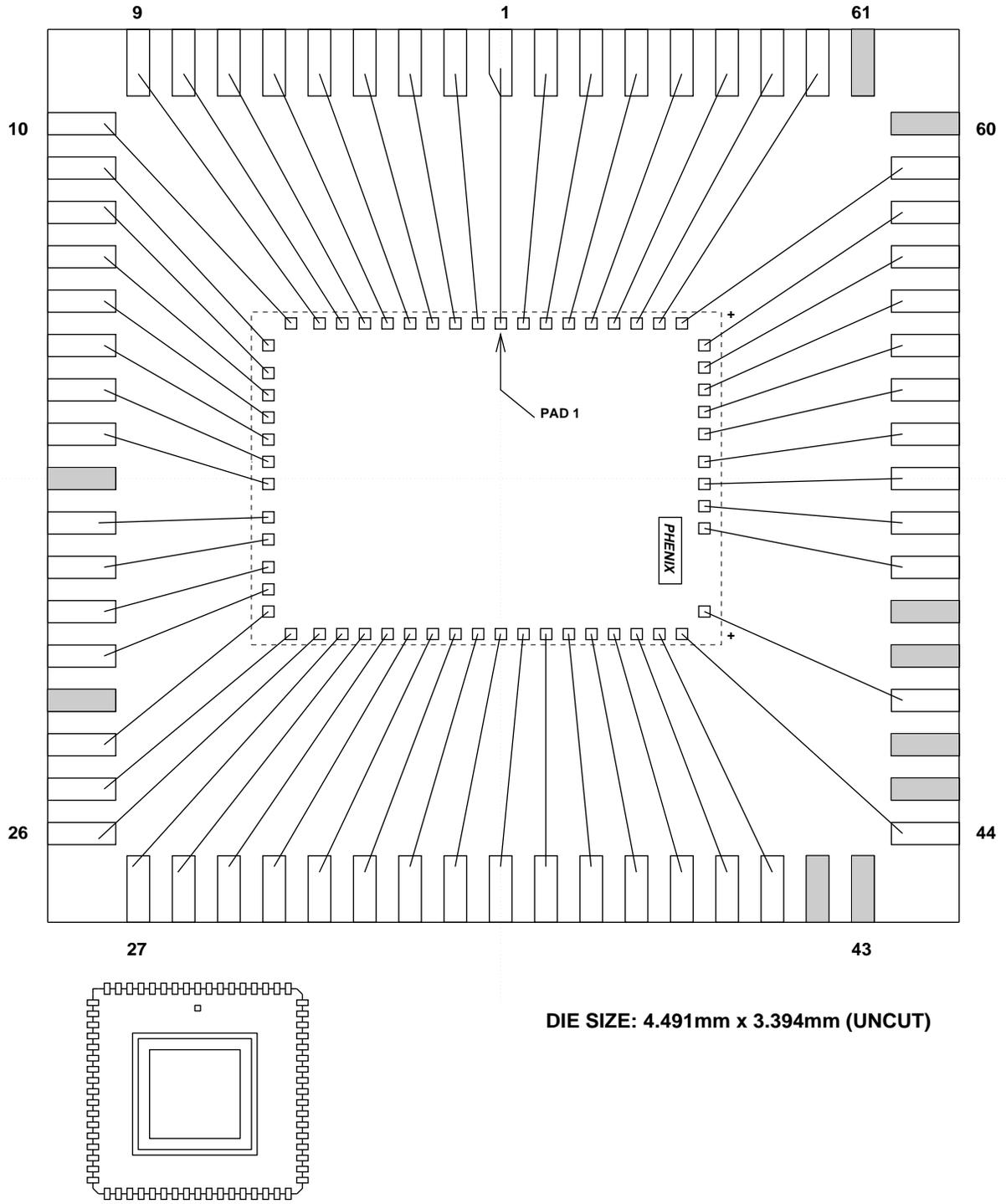


Fig 17. TEC-PS 64 Pin PQFP Bonding Diagram.

TEC-PS 68 pin LDCC Bonding Diagram:

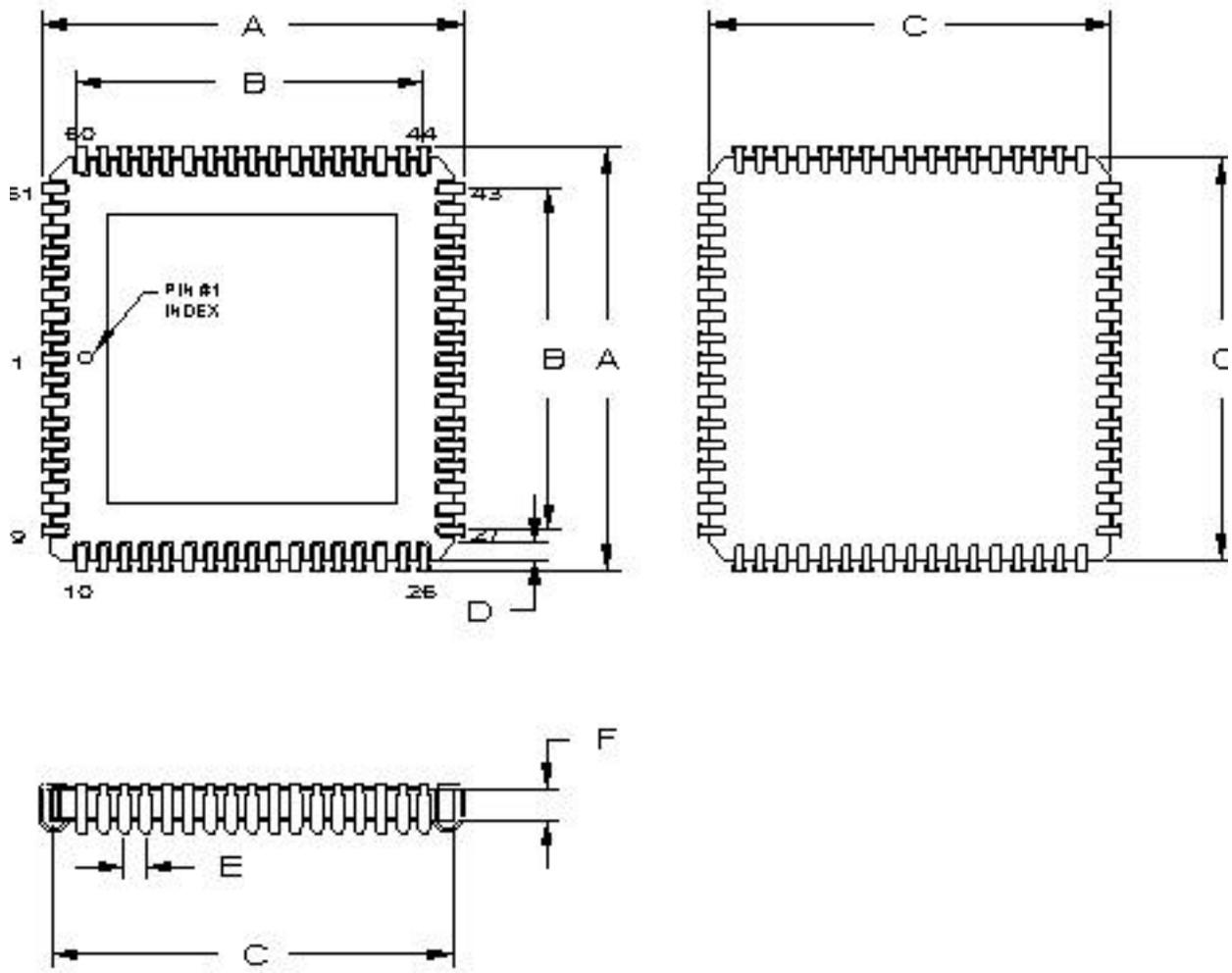
TEC-PS



Package Type: 68 J-LDCC, 0.400 SQ CAVITY

Fig 18. TEC-PS 68 pin LDCC Bonding Diagram.

68 Pin LDCC Package:



TEC-PS

DIM	in mm.
A	25.15
B	20.52
C	24.1
D	0.50
E	1.27
F	2.03

