

PHENIX
Time Expansion Chamber
Preamplifier-Shaper
Front End Printed Circuit Board
Instruction Handbook

IO-865

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PHENIX

Time Expansion Chamber Preamplifier-Shaper Front End Printed Circuit Board

Overview:

THE PHENIX TEC- PREAMPLIFIER/SHAPER (TECPS) Front End Printed Circuit Board (PCB) is designed for the PHENIX tracking system. The tracking system of PHENIX is designed to locate all charged tracks of interest within their fiducial volume, measure the particle momenta, help in identifying which of the tracks are electrons, and contribute trigger information to the PHENIX detector.

The sub-detector namely the Time-Expansion Chamber (TEC), for which the PCB is designed, performs both particle Identification and tracking functions in PHENIX. Through measurement of charged particles ionization losses (dE/dX).

The TEC front-end PCB employs a preamplifier and a 70ns shaping amplifier, which is implemented in a monolithic circuit. The TEC Front End PCB's primary function is charge conversion and signal shaping performed by the TECPS monolithic circuit. The shaped signals are then transmitted to the Front End Module (FEM) as fully differential signals. The PCB houses 128 line drivers using external Operational-Amplifiers (OPAMP). The PCB also houses calibration circuitry for the TECPS chips and voltage regulation for onboard electronics. Each TECPS PCB handles 32 anode wire inputs, and there are two signal outputs for each corresponding anode wire [TR and dE/dX]. Each of these 64 outputs are converted into Fully differential signals and carried over twisted pair cables to the FEM. These signals are then received using differential receivers and digitized using custom non-linear 5 bit flash analog to digital converters (TEC FADC¹) in the FEM.

Features:

- 32 Anode Signals/per board handling capacity.
- On-Board Precision Calibration circuitry.
- Fully Differential Line Drivers for output signals.
- On-Board Electro-Static-Discharge (ESD) protection circuitry on preamplifier inputs.
- Digitally Programmable Calibration masks.
- Digitally Programmable Channel Enable masks.
- Digitally Programmable Channel Gain [8 Steps].
- Digitally Programmable Peaking Time [4 Steps].
- Digitally Programmable Tail Cancellation [8 Steps] for adapting to different Gas mixtures.
- Local On-Board Voltage Regulators and power supply filters.
- Power Consumption : 262mWatts/Channel
- On-Board Re-Settable Fuses (PTC) on every power supply line.
- RS-422 Link for Serial Interface.

¹ Custom 5 Bit Non-Linear Flash ADC for PHENIX TEC, developed by Joseph Harder, Instrumentation Division, Brookhaven National Laboratory.

Time Expansion Chamber Pre-amplifier Shaper PCB:

Component side:

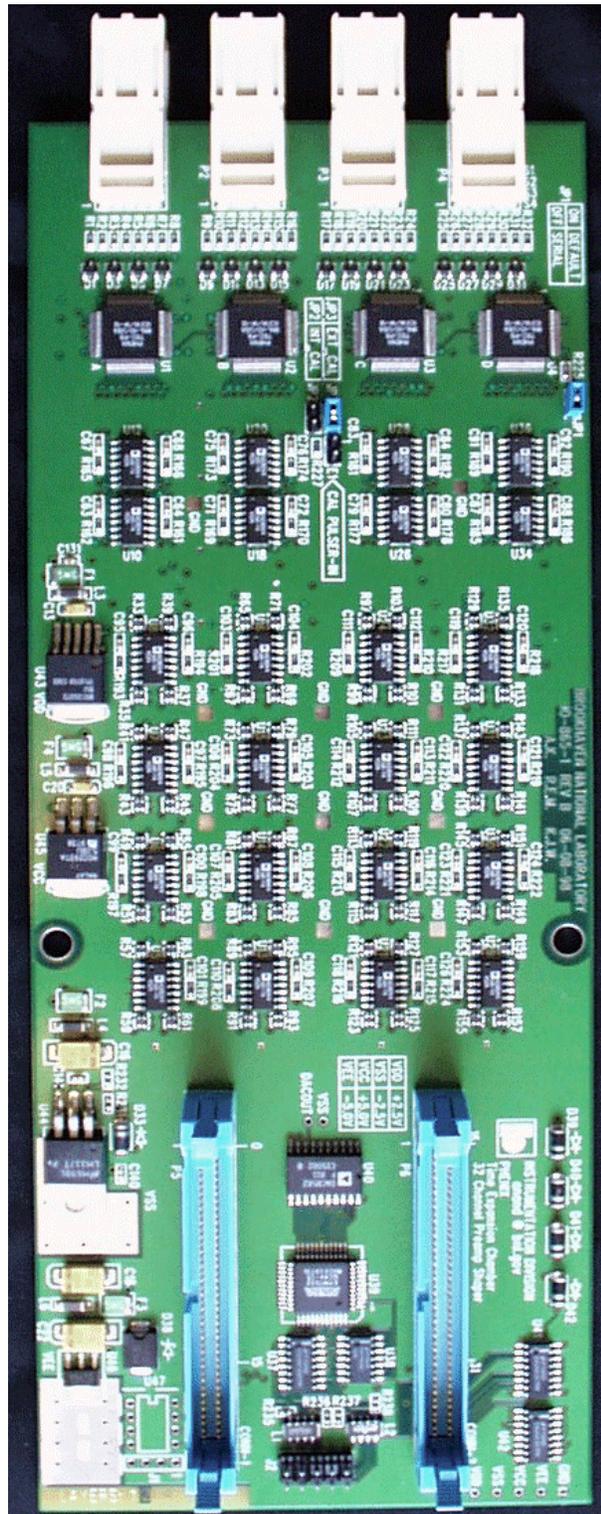


Figure 1. TECPS PCB Component side.

Solder side:

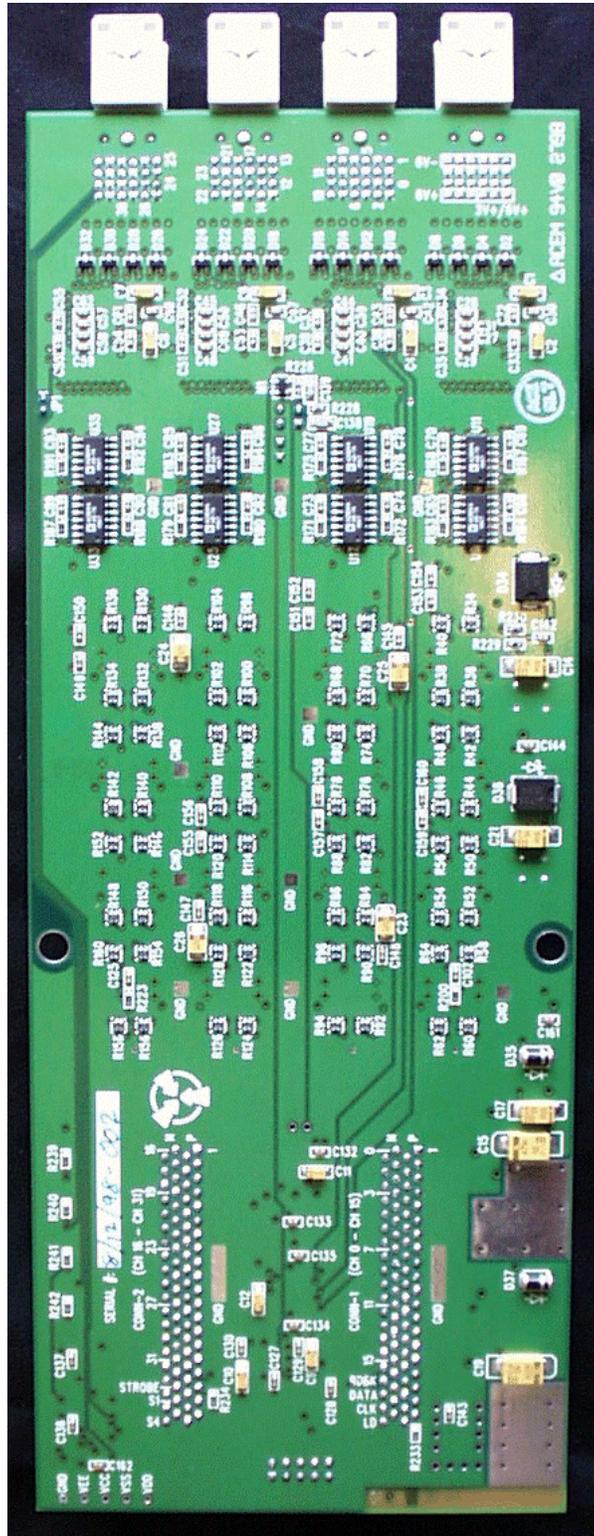


Figure 2. TECPS solder side.

Major Components of the TECPS PCB:

1. CMOS Pre-amplifier-Shaper:

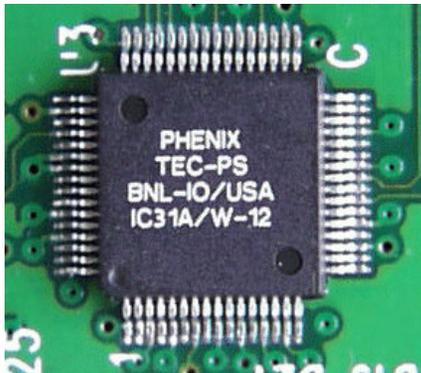


Figure 3. TECPS CMOS IC

The Time Expansion Chamber's Front-end electronics consists of a preamplifier and a 70ns shaping amplifier chain per channel, implemented as an Octal monolithic integrated circuit (IC). The output of the shaping stage is split into two outputs namely dE/dX and TR with a gain of x5 and x1 respectively. The IC has two modes of operation, Default mode and Serial mode. In the Default mode all 8 amplifiers are configured for a shaping time of 70ns, and dE/dX gain of 25mV/fC and TR gain of 5mV/fC and also the calibration and channel masks are set to enable. In the serial mode the IC is configured using a 3-wire serial interface. The TECPS is packaged using a 3-wire serial interface. The TECPS is packaged in a JEDEC 64 pin Quad Flat Pack (QFP) package. The TECPS chip can be identified by its marking as shown left in Figure3. The wafer identifier follows the IC31A marking. For further detailed information regarding this

integrated circuit refer to the document available at <http://www.inst.bnl.gov/~anand/phenix/>

Debugging TECPS IC:

- Check for proper voltages at TECPS IC's power pins, TECPS IC requires +2.5Volts, -2.5Volts and Ground for proper operation. For detailed information pertaining to pin numbers and its functions refer to the data sheet available at <http://www.inst.bnl.gov/~anand/phenix/>
- Check for Bias voltages at the following pins:

Pin No:	Bias Node	Typical
19	Obias	-1.43 Volts
64	Rbias	-1.14 Volts
62	Ibias	-1.13 Volts
57	VB1	100 mVolts
56	VB2	-953 mVolts

Table 1. Bias Voltages for TECPS IC.

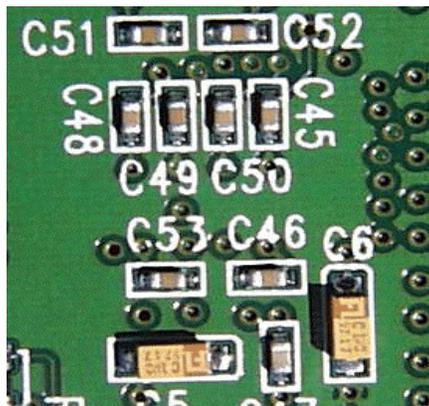


Figure 4 . Bias voltages probing .

Bias voltages are decoupled using multilayer ceramic chip capacitors and are easily accessible from the Solder side of the PCB. One of the regions underneath the TECPS on the solder side is shown in figure 4. All four TECPS IC have their Bias lines decoupled. Table 1 illustrates typical Bias voltages observed in a fully functioning TECPS IC.

- Check for Preamplifier Input Bias, this should be around +1.2 Volts.

Input Bias voltages of each preamplifier can be probed either at the pins of TECPS IC, but it is easier to probe them at the series resistor pads, in between the input connector and the IC. Figure 5 illustrates the location of these resistors corresponding to one of the four TECPS IC. All four of the TECPS IC's are laid out to have identical input and output routing, hence locating the remainder of the probe should be straight forward.

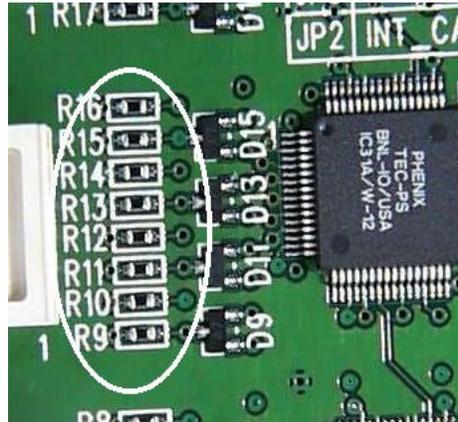


Figure 5. Preamplifier Input Bias.

2. Operational amplifiers – Line drivers:

Analog Devices Opamp AD8044 is used for the line driver stage. Two Opamp's are required for each TECPS output signals from the TECPS IC for achieving fully differential signals for driving the twisted pair cable of approximately 20 feet in length. There are 64 CMOS output signals [32 dE/dX and 32 TR] from four TECPS IC resulting in 128 Opamp's [32 Quad AD8044's].

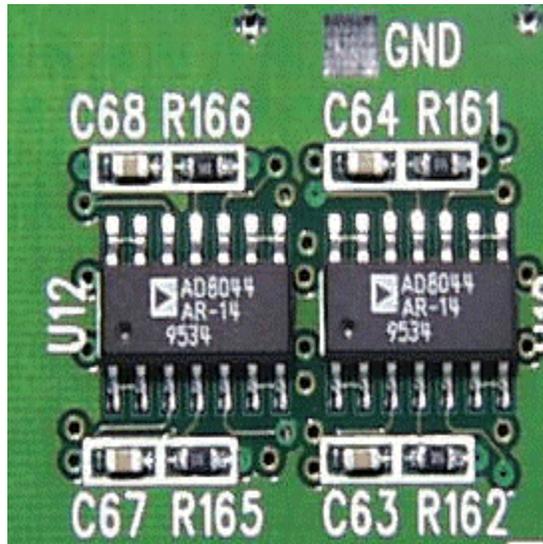


Figure 6. AD8044 Opamp.

The Opamp's are divided into to blocks namely Follower and Inverter. The Follower Opamp's are placed close to TECPS IC's on both side of the PCB in order to minimize the trace capacitance seen by the output stage of the TECPS. The output from the follower Opamp's form the positive signal of the fully differential pair. The Inverter Opamp's are in turn driven by the follower Opamp's, forming the negative signal of the fully differential pair.

Debugging the Line Drivers:

- Check for proper voltages at the power supply pins of the Quad opamp. AD8044 is operated out of +/- 5.0V. AD8044 being a Quad, both power supply pins are shared by 4 Opamp's. Each Quad opamp is isolated from the +5 and -5 volt supplies using a 51-ohm resistor. Taking the IR drop into consideration on these 51-ohm resistors the Voltages at the Opamp, power pins are pin 4 and pin 11 with +4.3 and -4.3 for +V and -V respectively.
- Check for the presence of signals at the Output terminal of the Opamp's. The output terminal of the AD8044 Opamp is conveniently located the 4 outer corners of the package, pin 1,7,8 and 14.

3. Voltage Regulators:

The TECPS PCB requires four different Voltages for its operation. These four voltages are obtained by locally regulating the unregulated power supplies (+6.0Volts and -6.0Volts).

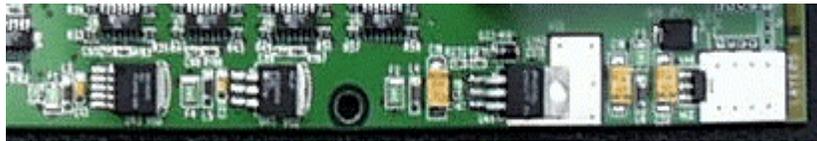


Figure 7 Local Voltage Regulators.

Figure 7 shows the four Local Voltage regulators in the PCB. Figure 6 shows the Voltages for the VDD, VSS, VCC and VEE. Normal operating voltages are marked on the PCB.

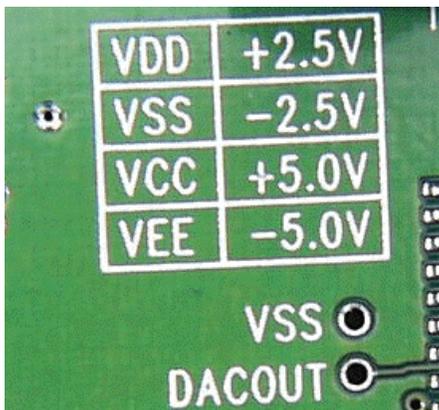


Figure 8. Voltages on the PCB.

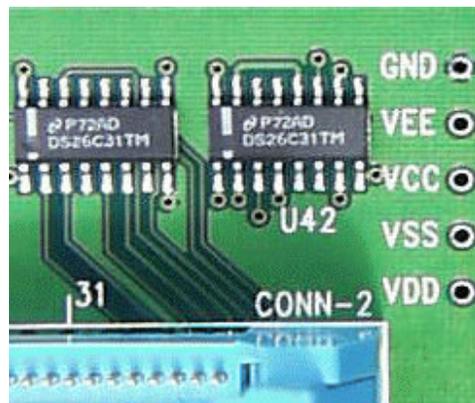


Figure 9. Voltage test points.

Figure 9 shows the test points for the four voltages shown in figure 8, For normal operation of the PCB the voltages measures at these points should be comparable to the voltages shown in figure 8.

IMPORTANT NOTE:

Ground pads are provided for attaching the scope probe or multi-meter probe to the PCB. These pads are clearly indicated using the letters "GND". Use only these pads as your ground return for your test instruments. Figure 10 shows these ground pads circled. Figure 11 shows a region where a big piece of copper is inviting one to attach the ground return of the instrument while it is not a ground, this region is clearly marked as "NOT GND".

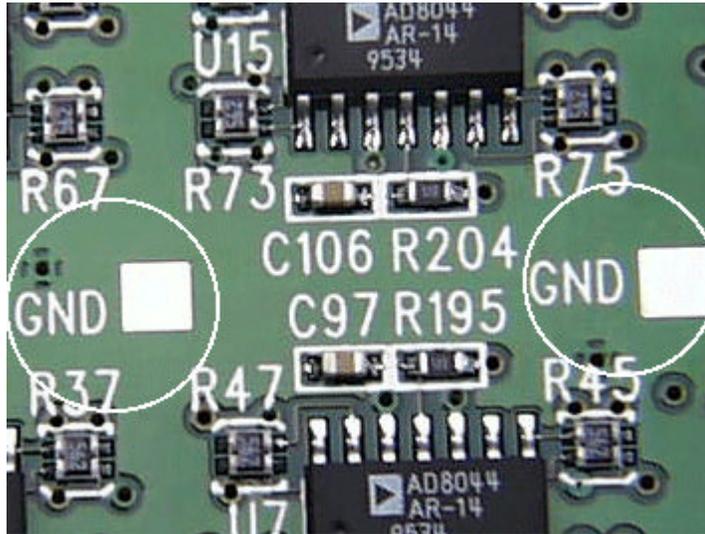


Figure 10. Ground pads.

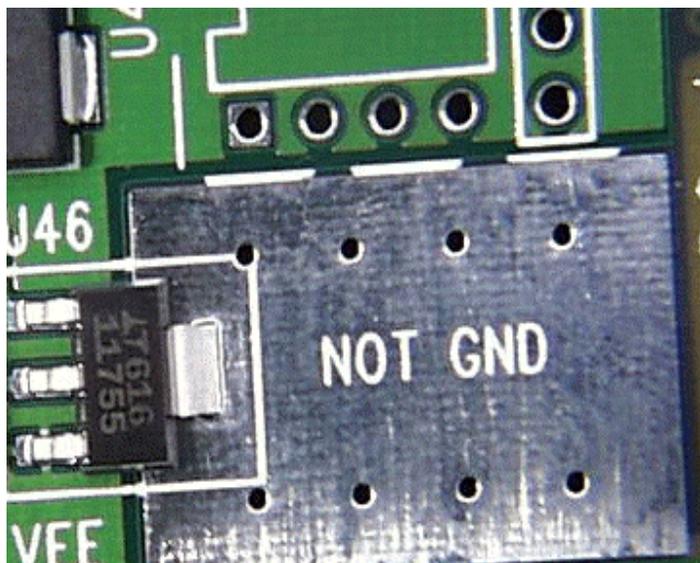


Figure 11. Do NOT use this as Ground.

4. Calibration DAC:

Analog Devices DAC8562, A 12 Bit Parallel D2A converter is used as the Reference source for the calibration circuit. This DAC is set using the serial stream downloaded to the Programmable Logic Device (PLD) on board the PCB. The DAC value set can be measured at the test point marked DACOUT near the DAC as shown in figure 12. This reference voltage is measured with respect to VSS and not GND. For convenience, a VSS pad is also provided nearby.

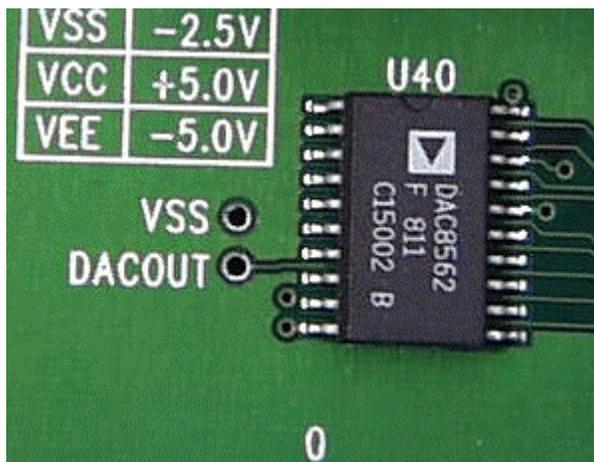


Figure 12. DAC and DACOUT.

5. RS-422 Serial Link Interface:

The Serial link interface consists of CMOS RS-422 receivers for Data, Clock and Load signals and a Programmable logic device (PLD) for converting a part of the serial stream into parallel bits for use by the calibration DAC. The PLD use in an ALTERA EPM 7032 device. The PLD also acts as a buffer for the three signals mentioned above, these buffered signals are used to configure the configuration of the TECPS IC when in serial mode. Figure 13 shows the RS-422 receivers along with the PLD and DAC.

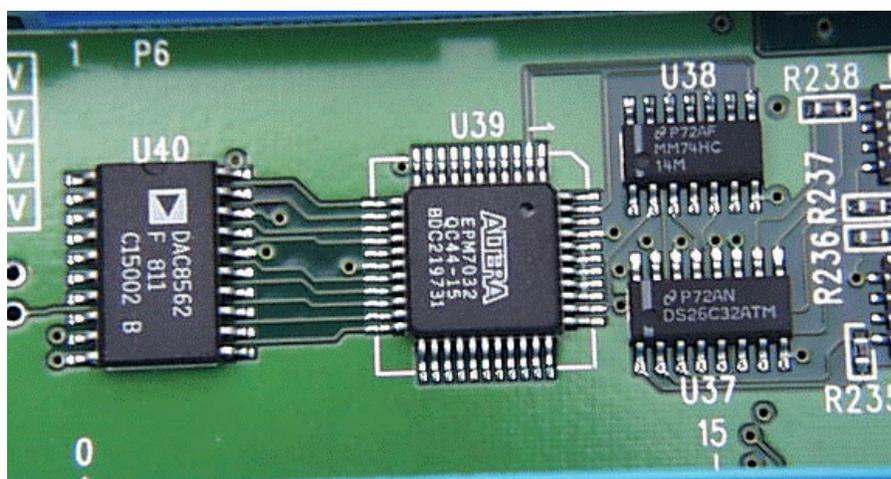


Figure 13. RS-422 Serial link interface.

6. Electro Static Discharge Protection:

Inputs of the TECPS IC are protected against Electro Static Discharges resulting from sparking of the anode wires in the chamber. The ESD circuitry consists of a series resistor in between the anode wire and the preamplifier input and two pull-up and pull-down diodes. Figure 14 shows the ESD protection circuitry on the TECPS PCB. The diodes are mounted on both sides of the PCB.

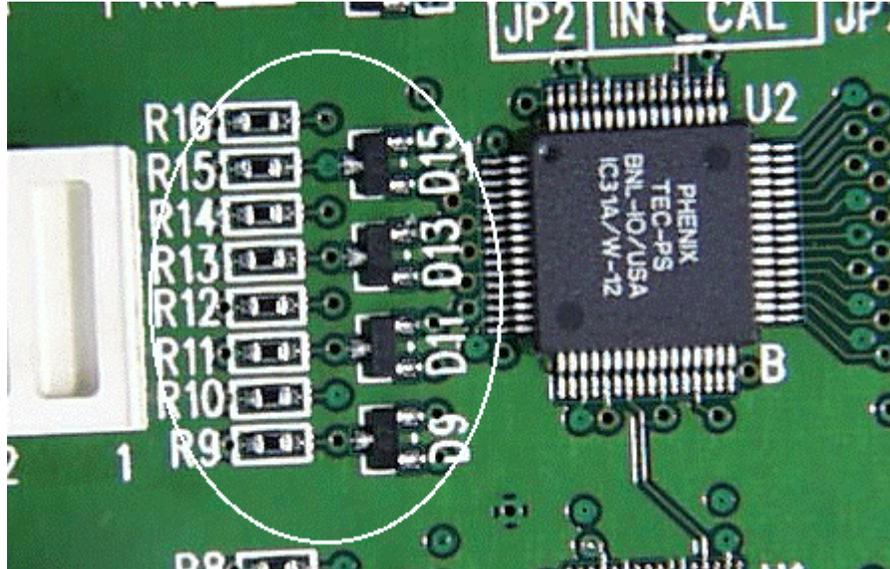


Figure 14. ESD Protection.

7. FUSE:

All unregulated power supply lines have fuses to protect the electronics in the PCB from short circuits in the circuitry of the TECPS PCB. The fuses used are Poly Resettable fuses [Positive Temperature Co-efficient (PTC) devices] manufactured by Raychem. Figure 15 shows one of the poly resettable fuse. Once tripped these fuses can only be reset by powering off the PCB.

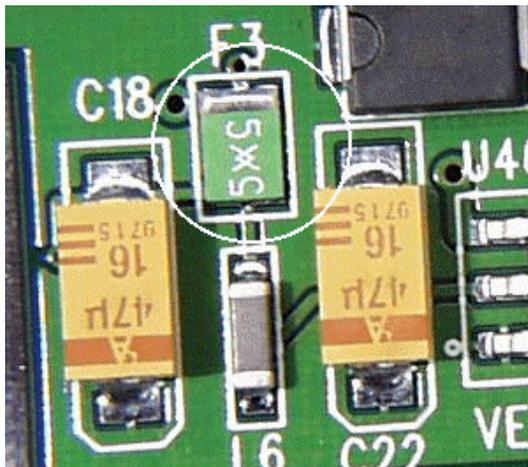


Figure 15. Poly resettable Fuse

8. Input Connectors:

Four Zpack connectors are used on the TECPS PCB for interfacing with the chamber. One of the connectors is completely dedicated to power supply. The geographical address of the TECPS board is carried through this connector. Figure 16 shows the four input connectors for anode signals, power and geographical address bits.

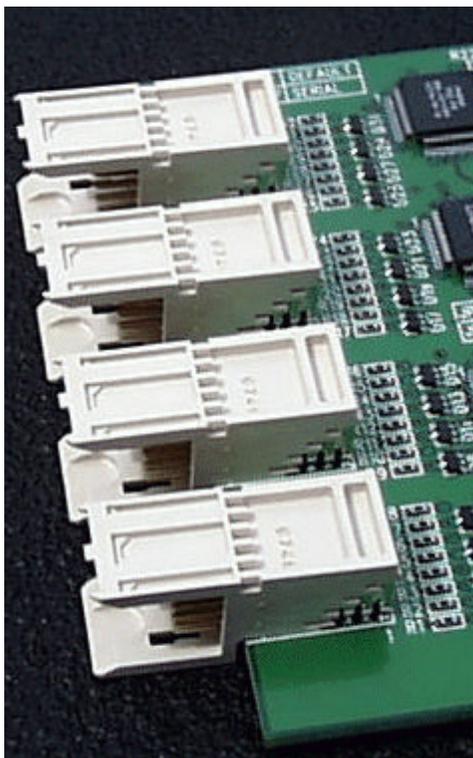


Figure 16. Zpack input connectors.

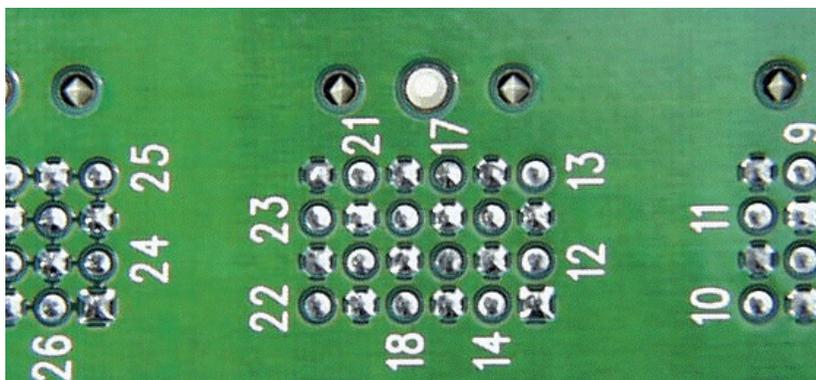


Figure 17. Anode signal pins.

On the solder side of the PCB, the anode signal pins are identified by their corresponding channel number on the TECPS board as shown in figure 17. The pins that are not numbered are the ground pins.

The unregulated power supply can be probed at one of the input connectors that can be easily identified by markings as shown in figure 18.

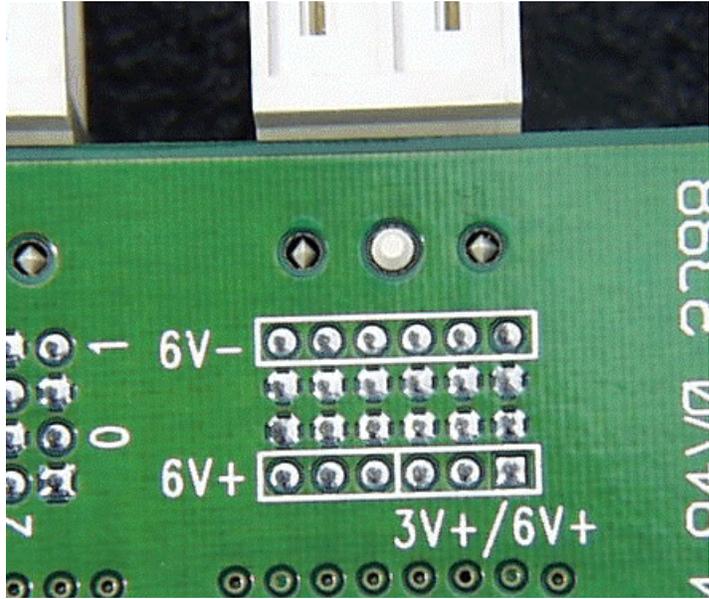


Figure 18. Input power pins.

9. Output Connectors:

Two High-Density IDC connectors are used for the 64 fully differential signals, also the same connectors are used for the RS-422 signals for the TECPS serial registers and the TECPS PCB geographical address bits. The two output connectors are shown in figure 19.

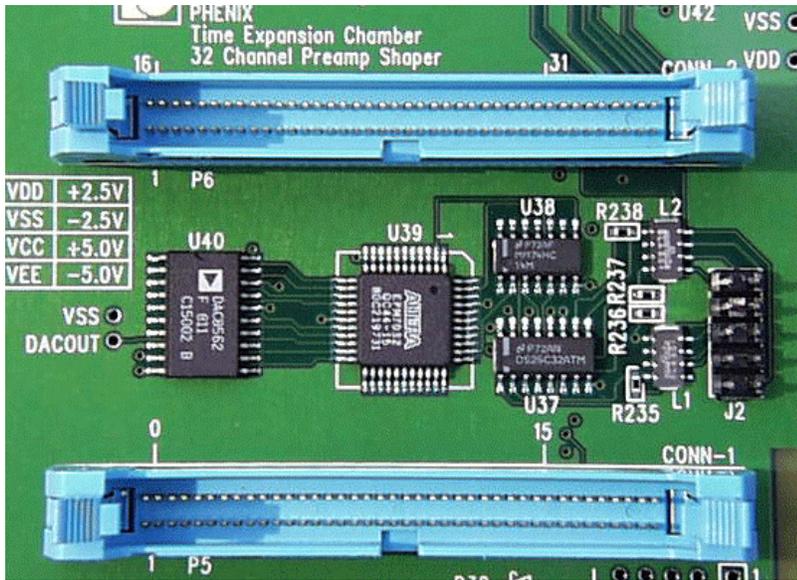


Figure 19. Output Connectors.

On the solder side certain pins are identified for ease in debugging as shown in figure 20. “P” indicates the positive sense of the fully differential signal (output of the Gain = +1 stage) and “N” indicates the negative sense of the fully differential signal (output of the Gain = -1 stage). Since the TECPS output signal is negative going, the signal observed at “P” pins are still negative going (+1 multiplier) and the signal observer at “N” pins are positive going (-1 multiplier).

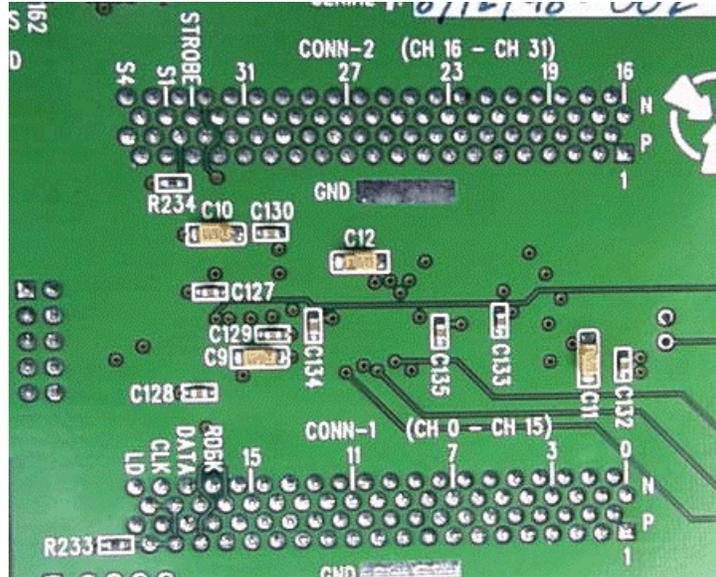


Figure 20. Markings on the output connector.

10. Calibration Jumpers:

Jumpers are provided to facilitate the board to be tested either with an external pulser or using the internal calibration circuitry. Two jumpers JP2 and JP3 can be see in figure 21. In order to use the external calibration pulse, jumper JP3 is installed and JP2 is removed. For using the internal calibration circuitry, jumper JP3 is removed and JP2 is installed. During installation of the TECPS PCB’s on the chamber make sure only jumper JP2 is present. This is the desired option in the system for the internal calibration circuitry.

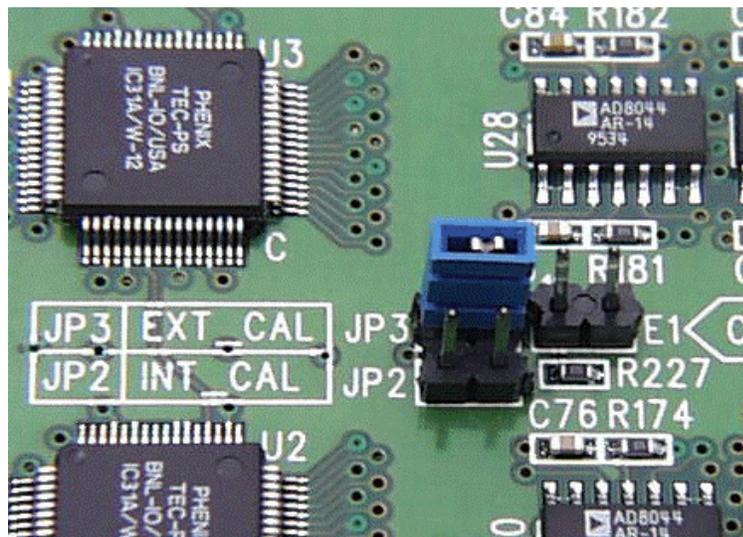


Figure 21. Calibration jumpers.

11. Mode selection Jumpers:

The TECPS IC has two modes of operation namely Serial mode and Default mode. In the serial mode, the parameters of the TECPS IC (like Gain, Peaking time, Tail cancellation, Calibration mask and channel enable mask) can be set to user defined values using the RS-422 serial link. In the Default mode, the TECPS IC is in a defined state necessary for normal operation. This default mode is also handy to test the PCB's on the test bench. This default/serial mode is controlled using the Jumper JP1 for default operation. This jumper has to be present as shown in figure 22, this is also the state in which it will be installed in the chamber

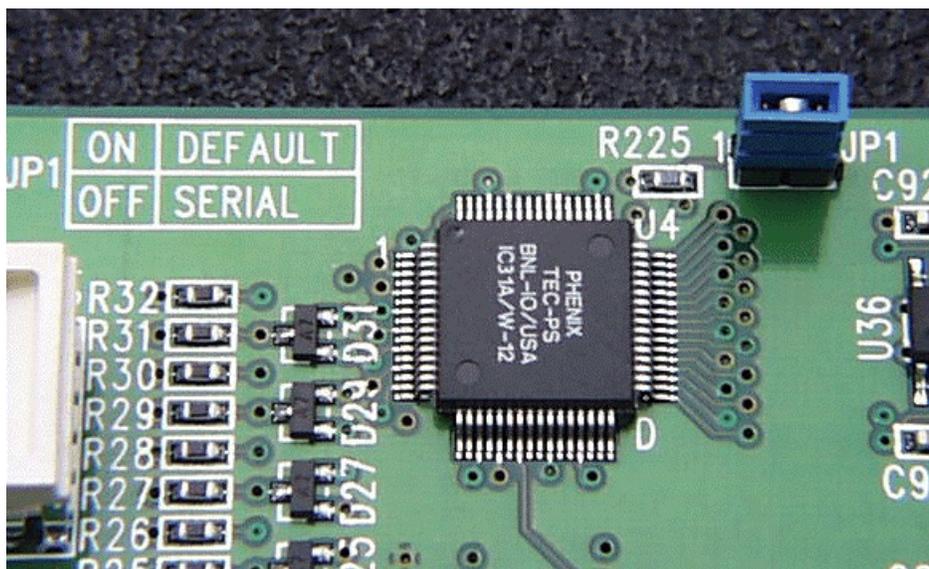


Figure 22. Default/Serial mode jumper.

Testing of the TECPS Board.

Equipment's required:

- Dual tracking power supply (+6V/-6V) with at least 800mA current/output.
- Digital Volt Meter.
- Pulser for Voltage step input for calibration [BNL/Instrumentation part number: IO-391]
- Analog or Digital oscilloscope.
- Test Jig. [See figure 23].
- BNC – to – 2 pin header cable [Meritec part number: 941339].
- Receiver board [BNL/Instrumentation part number IO-848].
- 80 conductor Output cable.

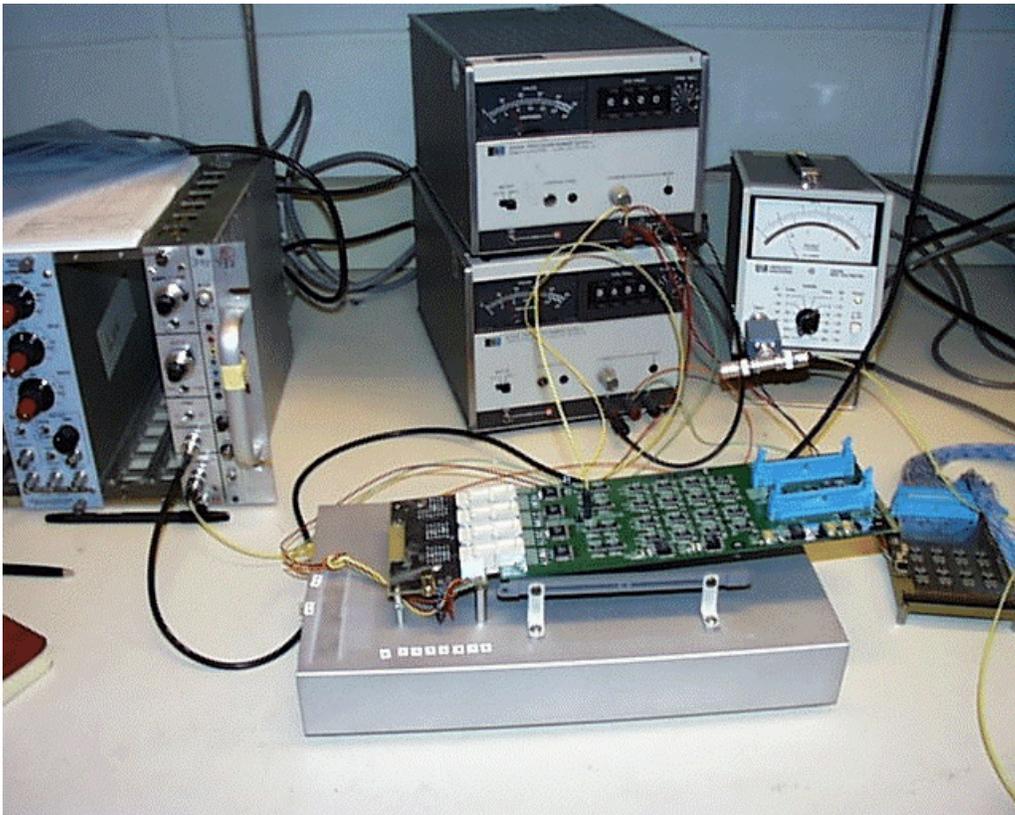


Figure 23. Test bench setup.

The TECPS PCB under test is mounted to the test fixture and the default mode is set using jumper JP1 as shown in figure 22. The calibration jumper is set to EXT_CAL (Jumper JP3) and the calibration pulse of 100mV (Frequency = 1 to 5 KHz) is fed to the PCB using the Meritec cable at header E1. Figure 24 shows the calibration connector connected to the header and the jumper JP3 set accordingly. Note the Pin 1 marking on the calibration connector.

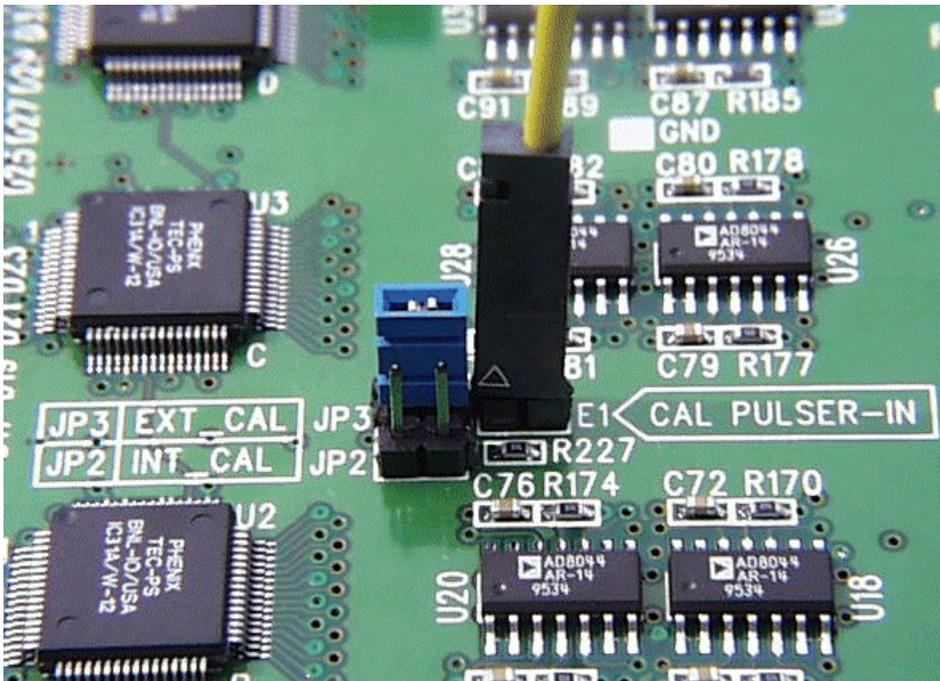


Figure 24. External calibration pulse input.

The output of the TECPS board can be observed using an oscilloscope and monitoring the output nodes of the receiver board.

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