

PHENIX

Time Expansion Chamber Preamplifier-Shaper Front End Electronics Specifications

1. Overview:

The PHENIX TEC- Preamp/Shaper CMOS Integrated circuit is designed for the PHENIX tracking system. The tracking system of PHENIX is designed to locate all charged tracks of interest within their fiducial volume, measure the particle momenta, help in identifying which of the tracks are electrons, and contribute trigger information to the PHENIX detector.

The sub-detector namely the Time-Expansion Chamber (TEC), for which the monolithic circuit is designed for performing both particle Identification and tracking functions in PHENIX. Through measurement of charged particles ionization losses (dE/dX), the detector allows separation of Electrons from Pions over a momentum range of 250 MeV/c to 3.0GeV/c.

The TEC front-end electronics consists of a preamplifier and a 70ns shaping amplifier chain, which is implemented in the monolithic circuit. The parameters of the electronics are determined by the requirements of both TEC's dE/dX and TRD operations. A shaping time of 70ns is chosen so that the FADC clock runs at a fraction of the shaping time to assure good position resolution. The Shaping time is also appropriate for the Transition Radiation (TR) measurements, where the shaping time chosen will allow containment of the total signal from the TR x-ray absorbed by the gas chamber. The output of the shaper is split into two, so that the FADC has sensitivity for both low dE/dX signals (0.2 - 0.3 KeV for Xe gas), and the Transition Radiation signals (3 - 10 Kev for Xe gas). The preamplifier-shaper electronics is designed for 70ns shaping time and a FWHM < 100ns. The ENC to be less than 1500 electrons (70ns, 30-40pF) to ensure Electron - Pion separation. The shaping function is unipolar, with a Semi-Gaussian impulse response.

The TEC Preamplifier Shaper Front End Electronics board's primary function is charge conversion and signal shaping performed by the TECPS monolithic circuit and Fully differential cable drivers performed using external operational-amplifiers. The Board also performs calibration function for the TECPS chips and voltage regulation for onboard electronics. Each TECPS front end board handles 32 anode wire inputs, and there are two signal outputs for each corresponding anode wire [TR and dE/dX]. Each of this 64 outputs are converted into Fully differential outputs leaving the board to the FEM which houses the FADC's.

2. Interface to the TEC Anode board:

- The TECPS board is interfaced to the TEC Anode board using AMP Z-PACK 2mm Future Bus connectors. The Z-PACK connector is shown in Figure 1.

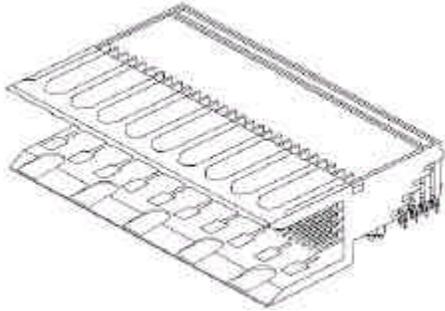


Figure 1

- Four 24 Pin connectors per TECPS board.
- Right angled male Z-PACK connectors.
- Connectors are mounted on the bottom side of the printed circuit board.

3. Protection circuitry for TEC PS CMOS IC:

TECPS have internal ESD structures on all of its I/O pins and also the preamp inputs have external ESD protection diodes.

4. Power and Grounding:

- Unregulated Power Supply feed from the Anode boards, through the Z-PACK connectors. The following unregulated supplies are required from the Anode board for local regulation.
 1. +6.0 Volts [minimum] for +5.0 Volts and +2.5 Volts regulation.
 2. -6.0 Volts [minimum] for -5.0 Volts and -2.5 Volts regulation.
 3. Power Supply Ground and Preamp/Shaper Returns.

Note: Above indicated voltages are voltages at the input of the regulator. The individual(s) designing the power distribution should deliver the above indicated voltages after taking into account for IR drop on the distribution lines.

- Power supply for the TEC-PS board electronic components are regulated locally on every board. The following regulated voltages are available on the TEC-PS board along with Ground.
 1. +2.5 Volts.
 2. -2.5 Volts.
 3. +5.0 Volts.
 4. -5.0 Volts.
- All Ground pins on the TECPS board components are returned to a single ground net. Which is a solid ground plane. This Ground is the same ground as the chamber.

5. Power Consumption:

TEC-PS:

Current consumption per TEC-PS chip:

$I_{V_{dd}}$: 57 mA	$I_{V_{ss}}$: -52 mA	I_{gnd}	: -5 mA
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Current consumption per TEC-PS board consisting of 4 TEC PS chips:

$I_{V_{dd}}$: 228 mA	$I_{V_{ss}}$: -208 mA	I_{gnd}	: -20 mA
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Line Drivers:

Total Opamp quiescent current per board : 384 mA [128 Opamp's @ 3.0 mA each]

The Transmission Line is a 112 ohm system, with 56 ohm back termination's.

$I_{V_{cc}}$: 384 mA	$I_{V_{ee}}$: -384 mA
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6. Power Regulation and Current distribution in the TECPS board:

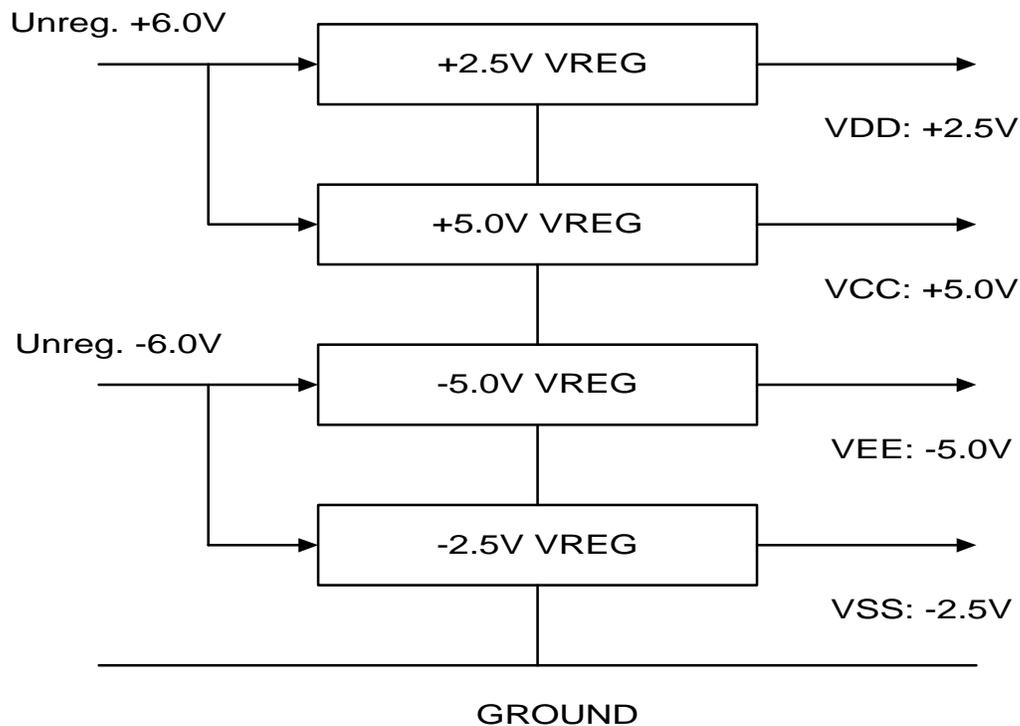


Figure 2

Figure 2 illustrates the power supply regulation scheme implemented on the TECPS board.

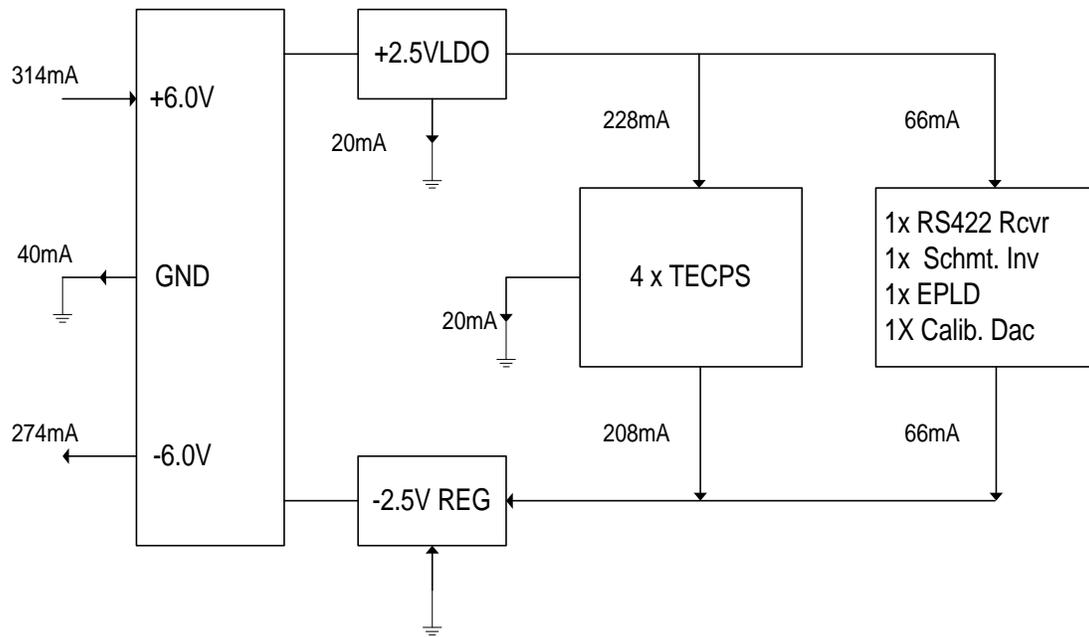


Figure 3

Figure 3 illustrates the current distribution among the components sharing the VDD and VSS power.

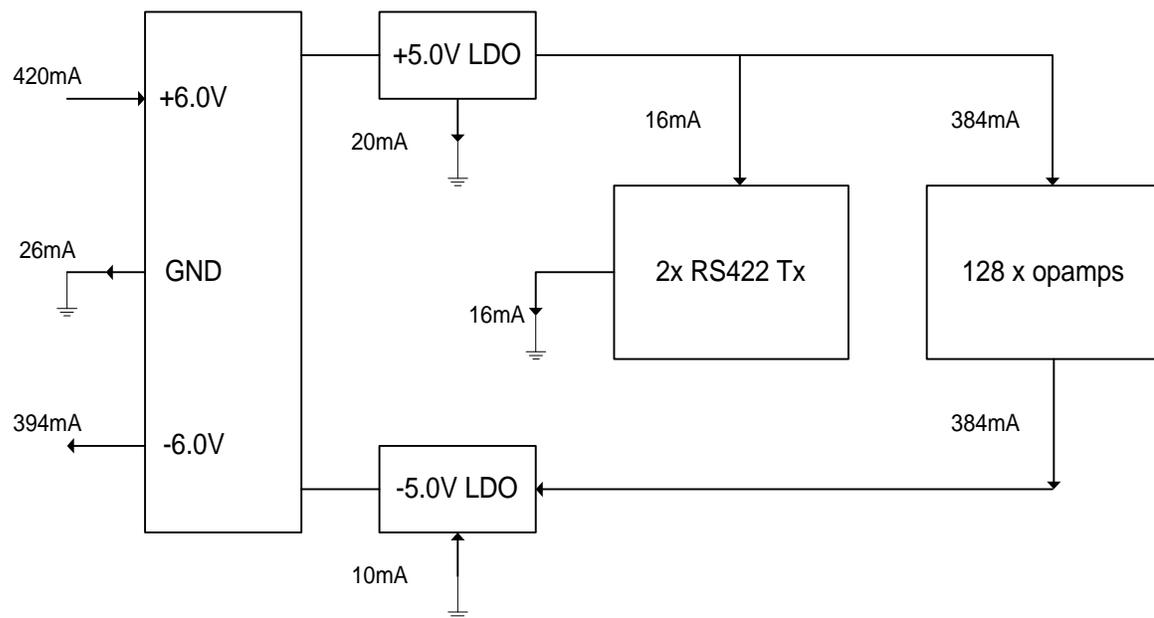


Figure 4

Figure 4 illustrates the current distribution among the components sharing the VCC and VEE power.

Supply	Power (current)
+6.0V	4.40 W (734mA)
-6.0V	4.00 W (668mA)

Table 1

Power dissipation for the TECPS board is given in table 1.

Total Power dissipation/Board [32 channels]	8.40 Watts
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7. Power Supply reversal and short circuit protection:

The following methods are implemented in the TEC PS board to protect the local regulators.

- Positive regulators are protected against input supply reversal by their internal protection.
- Negative regulators are protected against input supply reversal by reverse biased power diodes at their inputs.
- Regulator outputs have Schottky diodes in shunt to ease startup and also for short circuit protection., with the exception of the -VSS regulator which only has a power diode in shunt.
- TECPS power circuitry is protected using poly resettable fuses on every unregulated supply inputs on every board.

8. Geographical Addressing and Connector Identification for TEC-PS Boards:

- Geographical Addressing from each PS board on every TEC plane:
 - ◆ 15 boards/plane requiring 4 ID bits.
 - ◆ ID bits are routed into the PS board through the Anode Interface Z-PACK connectors.
 - ◆ Logic Levels of ID bits from the Anode Board:

+6.0 Volts :	“ONE”
0 Volts :	“ZERO”

ID Bits are one-diode voltage dropped before the interface circuits.
 - ◆ ID bits are level translated into RS-422 Signals and transmitted to the FEM through the output connectors.
 - ◆ Connector Identification is transmitted as a 1bit RS-422 Signal on each output connector.

9. Mechanical specifications of the TEC-PS Board:

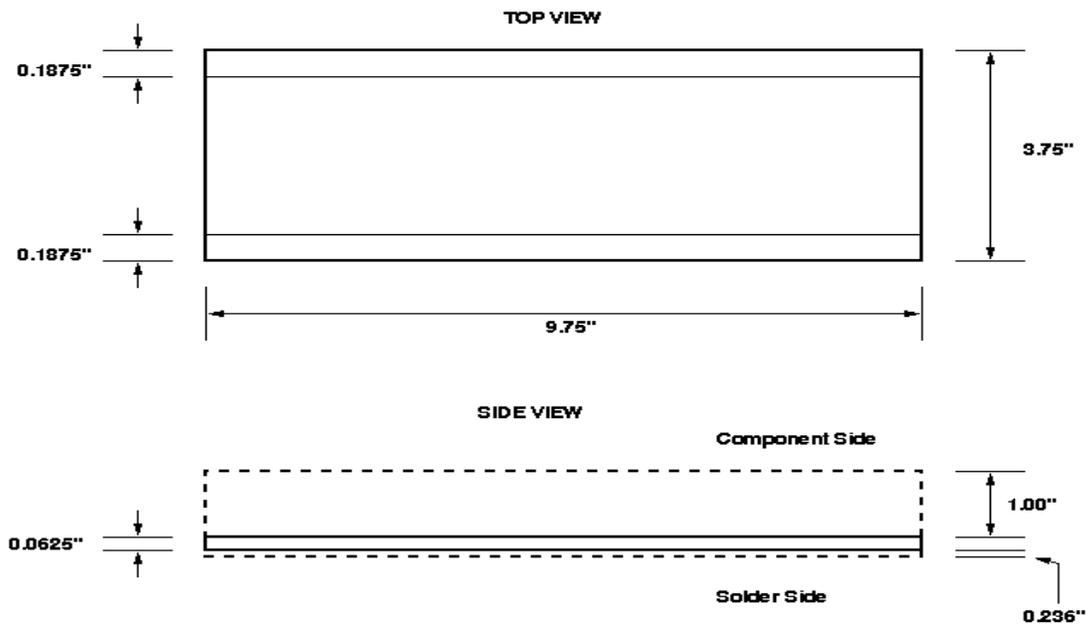


Figure 5

- ◆ Mechanical dimension and board clearances of the TEC-PS board.

Board width	: 3.75"	maximum
Board edge to component clearance	: 0.1875"	minimum
Board thickness	: 0.0625"	maximum
Board length	: 9.75"	
Component height on the solder side	: 0.236"	maximum
Component height on the component side	: 1.00"	

10. Interface to the FEM Board:

a. Preamp-Shaper:

- 32 Preamp-Shaper Channels per TEC PS board.
 1. 32 dE/dX outputs.
 2. 32 TR outputs.
- Fully Differential output Line drivers for TR and dE/dX signals to the FEM.
- TEC-PS to TEC-FEM interface using Amphenol 0.025" Twist 'N' Flat planar cable, 40 twisted pairs.
- Amphenol 0.025" High-Density connectors for output cable interface.
 - ◆ Amphenol's Cable mount High density IDC sockets.
 - ◆ Amphenol's Board mounted High density straight IDC headers

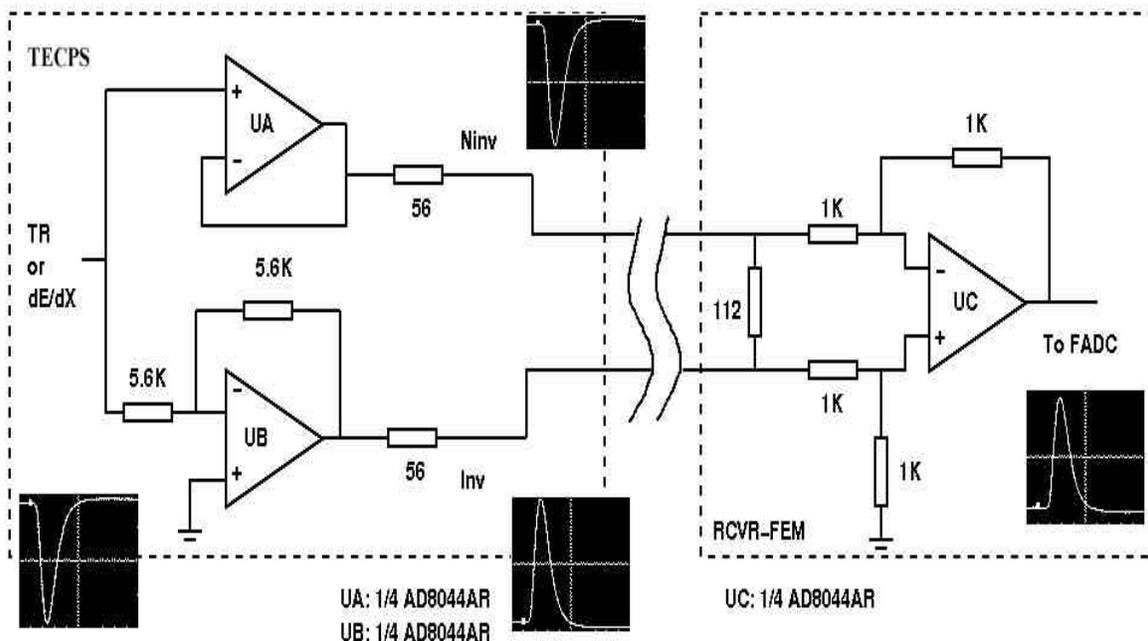


Figure 6

Ninv and Inv nodes correspond to XX_P and XX_N nodes on the system, where XX is either dE/dX or TR.

- Output connectors are mounted on the bottom side of the TEC-PS board and should be within the maximum clearance allowed (1.00”).
- b. Control, Calibration, Read-back and Monitoring:**
 - TEC-PS configuration [Gain, Calibration mask and Channel Mask] are set using the serial stream downloaded from the FEM.
 - ◆ All control lines given below are fully differential using RS-422 protocol.
 1. Serial Data Input.
 2. Serial Clock.
 3. Serial Data Load.
 4. Serial Data Output [Read-back].
 - Onboard Calibration circuit.
 - ◆ On Board DAC and switching circuitry for Preamp/Shaper Calibration.
 - ◆ Maximum Calibration charge : 200fC.
 - ◆ Calibration Strobe signal from the FEM as differential RS-422 signal.

- ◆ The DAC is programmed from the FEM using the same serial stream used for configuring the TEC-PS Integrated circuits.

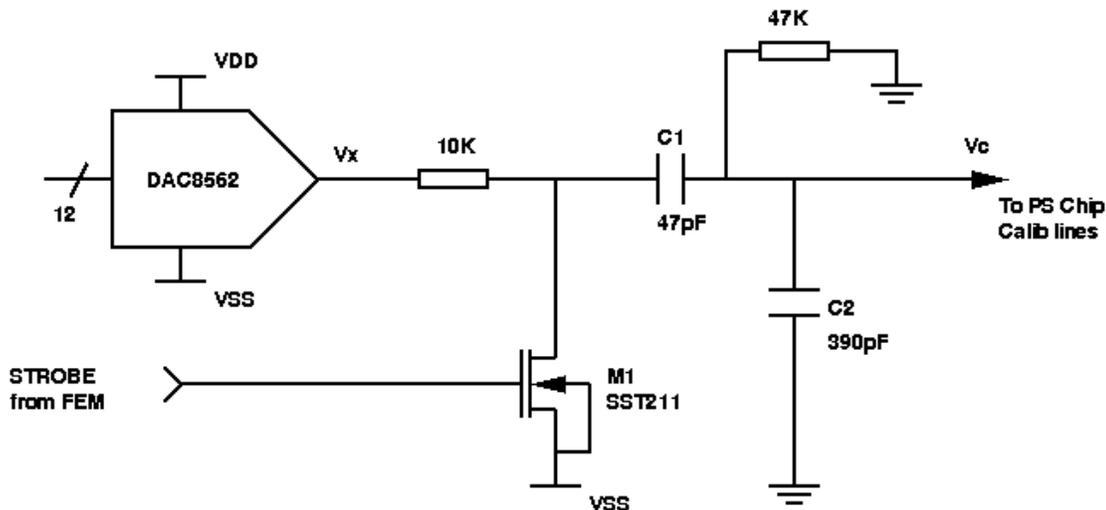


Figure 7

The DAC used for calibration is a 12 bit DAC, with 1mV/bit resolution and Vout max of 4095mv. The calibration pulse for the TEC PS is obtained by switching the DAC output Vout_dac and VSS(-2.5), using a mosfet (SST211), with its control (gate) form the FEM. The capacitive divider C1 and C2 attenuates the switched voltage by a factor of 10, yielding ΔV , which is used as the Calibration pulse for the Preamp-Shaper chips. The attenuation is done after the switch, in order to reduce the charge injection by the mosfet also by the same factor of 10.

$$\begin{aligned}\Delta V &= V_{dac} (Z_2/(Z_1+Z_2)) \\ &= V_{dac} (1/C_2)/((1/C_2) + (1/C_1)) \\ &= 0.107V_{dac}\end{aligned}$$

It should be noted that, the DAC is powered of the VDD and VSS which are +2.5V and -2.5V respectively. This is due to the fact that the CMOS chips are on the powered of the same supply and no level translation need to be undertaken in the serial stream in order to daisy chain the serial devices. Since, the charge injected $Q = \Delta V * C_{inj}$, and ΔV is given as $V_{dac} = V_{dac_set} - V_{low_ref}$, and V_{low_ref} is not 0 [Ground], it is -2.5 [VSS] V_{dac} is offset by a value of -2.5, [Setting 1V on the DAC, actually delivers -1.5]. This DAC output is toggled between the V_{low_ref} and V_{dac_set} , giving the ΔV required.

- Onboard PLD is used for converting part of the serial stream [12 bits] to parallel data for the DAC. The PLD is a feed through for the entire serial stream which consists of data to configure 4 TEC-PS integrated circuits.
- No ground connection to exist between the FEM and the TEC-PS boards. All control and data signal [Calibration strobe, Serial and Analog] are differential, Analog signal output to the FEM are fully differential. The serial link, calibration strobe and address bits are fully differential using RS-422 protocol.

- Two 40 Pair cables for output and control signals to and from the FEM and TEC-PS board.
 - ◆ dE/dX and TR signals interleaved on two output connectors. [32 preamp shaper signal pairs on each connector].
- Input connector for pulsing the TEC-PS integrated circuits for diagnostics purposes, bypassing the onboard calibration circuitry. [A 2 pin SIP header is sufficient].
- Input connector for diagnosing the serial link. [This connector is separate from the output connector].

11. Serial Link Specifications:

- Data is latched into the shift register flip-flops on the falling edge of the clock.
- Total number of bits per TEC-Preamp-Shaper Integrated circuit:

1. Control:

◆ Peaking Time	:	2	bits
◆ Tail Cancellation	:	3	bits
◆ Gain	:	3	bits

2. Calibration : 8 bits

3. Channel Mask : 8 bits

Total : 24 bits

- Total number of bits per TEC-Preamp Shaper Board:

◆ DAC	:	12	bits
◆ TEC-PS (4 x 24 bits)	:	96	bits
Total	:	108	bits

- Serial Protocol:

1. The entire serial stream (108 bits) are shifted in, on the negative edge of the serial clock.
2. A falling edge on the LOAD line latches the serially shifted data onto the configuration registers of the TEC-PS integrated circuits and the output bits of the PLD for the DAC.
3. The data-out of each chip in the chain is delayed by ½clock cycle to avoid any flip-flop setup violations.

The entire Serial stream for the TEC-PS board is as shown in Figure 8.

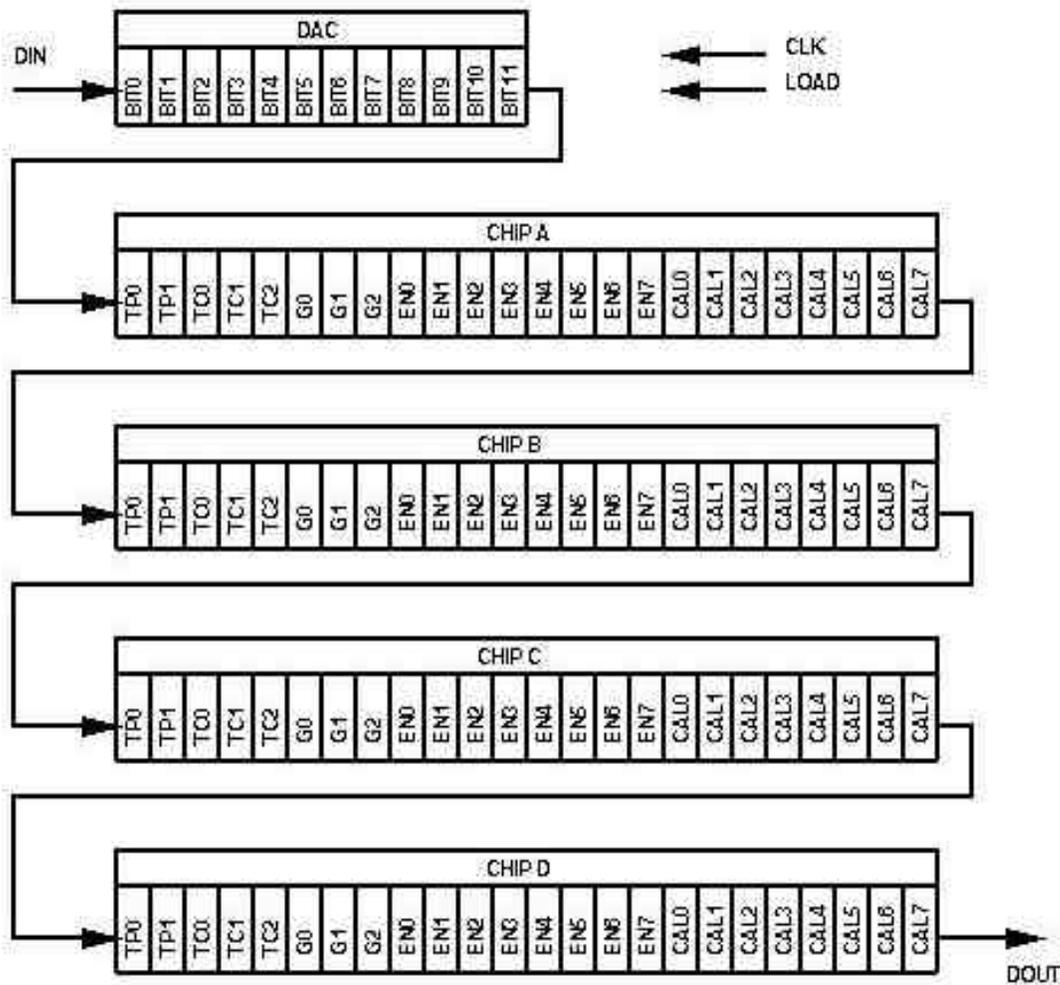


Figure 8

Figure 8, shows the DAC is on the serial link, In the system only the bits required for the DAC are on the serial stream residing in the PLD.

12. Thermal Management:

- The Packages chosen for the Local Power regulators does not impose the need for any additional heat sinks for the regulators for any power dissipation considerations and thermal runaway of the regulators.

13. TEC-PS Printed Circuit Board Assembly and Connector details:

- Input Connector Pin count:

1. Anode wire inputs	:	32	
2. Ground [Preamplifier Returns + Power Ground]	:	48	
3. Power +3.0 Volts	:	3	
4. Power +6.0 Volts	:	3	
5. Power -6.0 Volts	:	6	
6. ID Bits [Geographical Addressing Bits]	:	4	
	Total Used	:	96
	Used/Total	:	96/96

- Output Connector Pin count [in pairs]:

1. dE/dX outputs	:	32	
2. TR outputs	:	32	
3. Serial Download	:	3	
4. Serial Read back	:	1	
5. Calibration Strobe	:	1	
6. ID Bits [Geographical Addressing Bits]	:	4	
7. Connector ID bit	:	2 (1 per connector)	
8. TEC-PS board Serial status	:	2	
	Total Used	:	77

Unused pins are pulled up and down to VCC and VEE respectively with 47K ohm resistor.

	Used/Total	:	80/80
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- Input Connector Pin assignments for the TEC-PS board:

The TEC-PS board is designed right side up and is inverted and interfaced to the TEC anode boards. This requires extensive mapping of the pins from the Anode board to the TEC-PS board. The figure and the pin numbers give below are for the right side up [Good only for layout needs and Test bench]. Only on inverting and interfacing it to the anode boards, the pins and the signal correspond to the correct mapping.

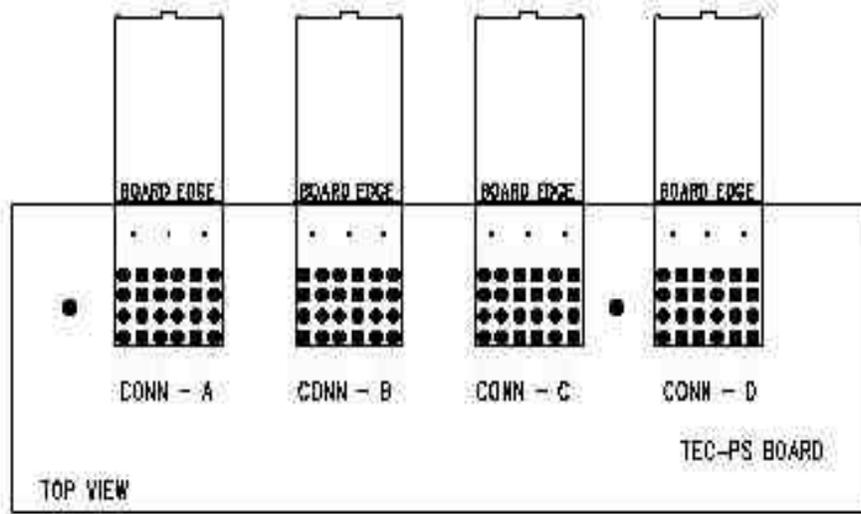


Figure 9

Figure 9 illustrates the 4 Z-Pack connectors on the TEC-PS board along with the naming convention.

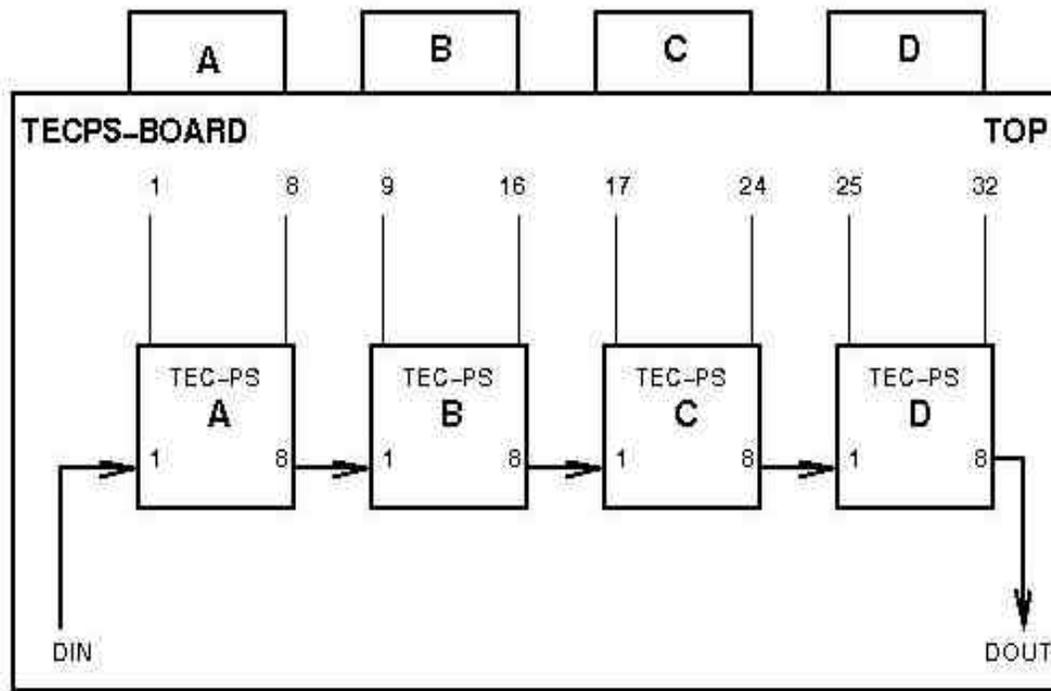


Figure 10

Figure 10, depicts how the layout designed and the test bench engineer interprets the TECPS board. The channels are numbered from left to right as Anode 0 to Anode 31.

The TECPS board layout is approached in the following manner, since the TECPS board has to be interfaced to the TEC-Anode board flipped. Since the CAD tools work on the top-down topology, the board is designed as if its 180 degrees flipped. Figure 10 and 11 illustrates this method.

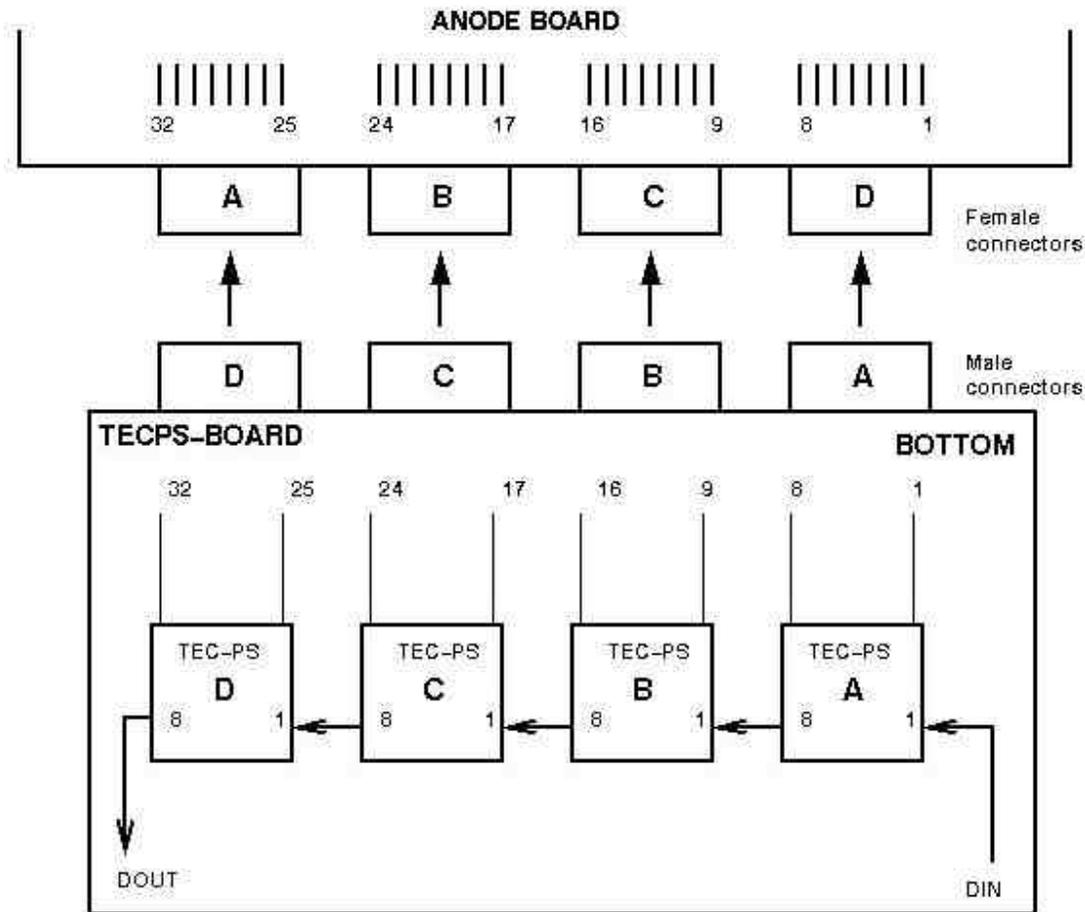


Figure 11

Figure 11 illustrates how the assembled TECPS board will be flipped and mated with the TEC anode interface board. The figure corresponds to looking through the TECPS printed circuit board and the components are on the bottom side.

- Input Connector Pin assignment:
 - ◆ Anode Signal assignments

Anode	Chip ID	Connector ID	Pin Number
0	A	B	2
1	A	B	4
2	A	B	5
3	A	B	7
4	A	B	10
5	A	B	12
6	A	B	13
7	A	B	15
8	B	B	18
9	B	B	20
10	B	B	21
11	B	B	23
12	B	C	2
13	B	C	4
14	B	C	5
15	B	C	7
16	C	C	10
17	C	C	12
18	C	C	13
19	C	C	15
20	C	C	18
21	C	C	20
22	C	C	21
23	C	C	23
24	D	D	2
25	D	D	4
26	D	D	5
27	D	D	7
28	D	D	10
29	D	D	12
30	D	D	13
31	D	D	15

Table 2

- ◆ Ground pin assignment:

Connector ID	Pin number
A	2,3,6,7,10,11,14,15,18,19,22 and 23
B	1,3,6,8,11,14,16,17,19,22 and 24
C	1,3,6,8,11,14,16,17,19,22 and 24
D	1,3,6,8,11,14,16,17,18,19 and 20

Table 3

◆ Unregulated power supply pin assignment:

Connector ID	Unregulated Supply	Pin number
A	+6.0 Volts	13,17 and 21
A	-6.0 Volts	4,8,12,16,20 and 24
A	+6.0 Volts (see note 1)	1,5 and 9

Table 4

◆ Geographical address bits pin assignment:¹

ID Bit	Connector ID	Pin number
S1	D	24
S2	D	23
S3	D	22
S4	D	21

Table 5

• Serial link diagnostic connector pin assignment:

The serial link diagnostic connector is a standard 0.100” center 8 pin header.

Signal	Pin number
Rdbk_P	1
Rdbk_N	2
DATA_P	3
DATA_N	4
CLK_P	5
CLK_N	6
LD_P	7
LD_N	8
STROBE_P	9
STROBE_N	10

Table 6

This connector is necessary to test serial capability of the TEC PS boards on the test bench, in the absence of the FEM.

¹ This +6.0 Volts corresponds to the previous +3.0Volts connection.

- Output connector pin assignment:

Signal	Pin number	Signal	Pin number
dE/dX_P 0	1	dE/dX_N 0	2
TR_P 0	3	TR_N 0	4
dE/dX_P 1	5	dE/dX_N 1	6
TR_P 1	7	TR_N 1	8
dE/dX_P 2	9	dE/dX_N 2	10
TR_P 2	11	TR_N 2	12
dE/dX_P 3	13	dE/dX_N 3	14
TR_P 3	15	TR_N 3	16
dE/dX_P 4	17	dE/dX_N 4	18
TR_P 4	19	TR_N 4	20
dE/dX_P 5	21	dE/dX_N 5	22
TR_P 5	23	TR_N 5	24
dE/dX_P 6	25	dE/dX_N 6	26
TR_P 6	27	TR_N 6	28
dE/dX_P 7	29	dE/dX_N 7	30
TR_P 7	31	TR_N 7	32
dE/dX_P 8	33	dE/dX_N 8	34
TR_P 8	35	TR_N 8	36
dE/dX_P 9	37	dE/dX_N 9	38
TR_P 9	39	TR_N 9	40
dE/dX_P 10	41	dE/dX_N 10	43
TR_P 10	43	TR_N 10	44
dE/dX_P 11	45	dE/dX_N 11	46
TR_P 11	47	TR_N 11	48
dE/dX_P 12	49	dE/dX_N 12	50
TR_P 12	51	TR_N 12	52
dE/dX_P 13	53	dE/dX_N 13	54
TR_P 13	55	TR_N 13	56
dE/dX_P 14	57	dE/dX_N 14	58
TR_P 14	59	TR_N 14	60
dE/dX_P 15	61	dE/dX_N 15	62
TR_P 15	63	TR_N 15	64
CONN1_P	65	CONN1_N	66
Rdbk_P	67	Rdbk_N	68
MODE_P	69	MODE_N	70
DATA_P	71	DATA_N	72
V+Dummy	73	V+Dummy	74
CLK_P	75	CLK_N	76
V+Dummy	77	V+Dummy	78
LD_P	79	LD_N	80

Table 7

Signal	Pin number	Signal	Pin number
dE/dX_P 16	1	dE/dX_N 16	2
TR_P 16	3	TR_N 16	4
dE/dX_P 17	5	dE/dX_N 17	6
TR_P 17	7	TR_N 17	8
dE/dX_P 18	9	dE/dX_N 18	10
TR_P 18	11	TR_N 18	12
dE/dX_P 19	13	dE/dX_N 19	14
TR_P 19	15	TR_N 19	16
dE/dX_P 20	17	dE/dX_N 20	18
TR_P 20	19	TR_N 20	20
dE/dX_P 21	21	dE/dX_N 21	22
TR_P 21	23	TR_N 21	24
dE/dX_P 22	25	dE/dX_N 22	26
TR_P 22	27	TR_N 22	28
dE/dX_P 23	29	dE/dX_N 23	30
TR_P 23	31	TR_N 23	32
dE/dX_P 24	33	dE/dX_N 24	34
TR_P 24	35	TR_N 24	36
dE/dX_P 25	37	dE/dX_N 25	38
TR_P 25	39	TR_N 25	40
dE/dX_P 26	41	dE/dX_N 26	43
TR_P 26	43	TR_N 26	44
dE/dX_P 27	45	dE/dX_N 27	46
TR_P 27	47	TR_N 27	48
dE/dX_P 28	49	dE/dX_N 28	50
TR_P 28	51	TR_N 28	52
dE/dX_P 29	53	dE/dX_N 29	54
TR_P 29	55	TR_N 29	56
dE/dX_P 30	57	dE/dX_N 30	58
TR_P 30	59	TR_N 30	60
dE/dX_P 31	61	dE/dX_N 31	62
TR_P 31	63	TR_N 31	64
CONN2_P	65	CONN2_N	66
MODE_P	67	MODE_N	68
Strobe_P	69	Strobe_N	70
V-Dummy	71	V-Dummy	72
S1_P	73	S1_N	74
S2_P	75	S2_N	76
S3_P	77	S3_N	78
S4_P	79	S4_N	80

Table 8

dE/dX_P and TR_P denote non-inverted signals and dE/dX_N and TR_N denote inverted signals. Table 7 describes connector #1 and Table 8 describes connector #2.

14. TEC PS printed circuit board:

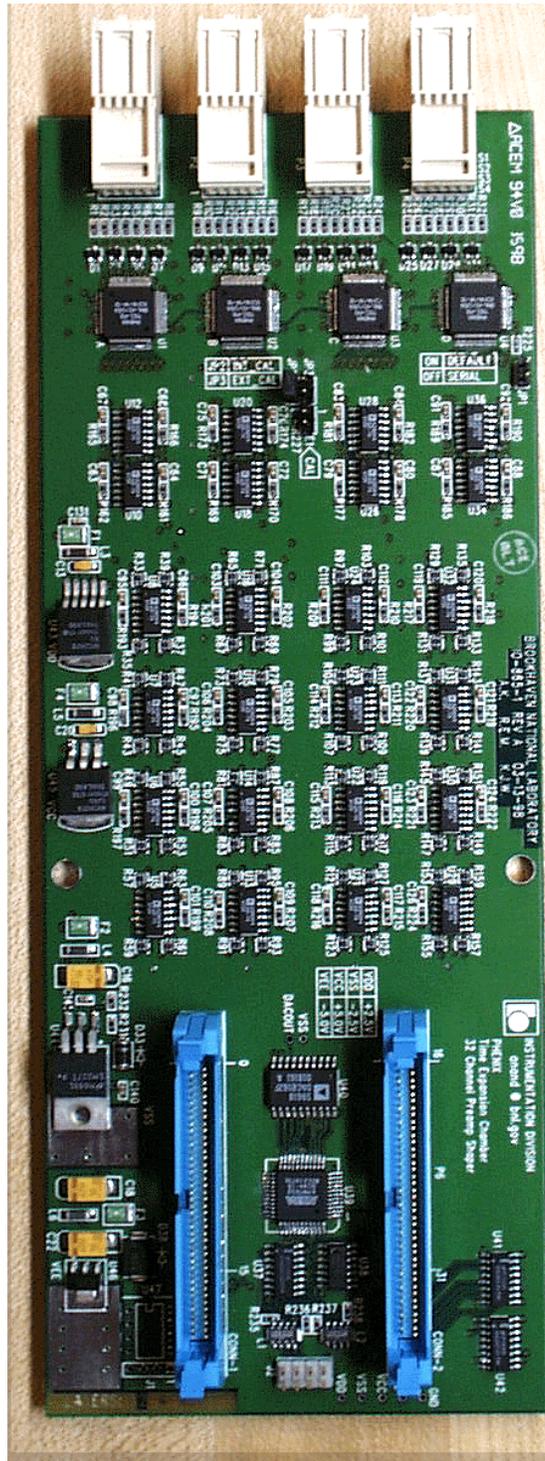


Figure 12

The information furnished in this documents is believed to be accurate and reliable. The author reserves the right to change circuitry and specifications, maintaining the functionality of the system at any time without prior notice. The author guarantees that at the date of publication,(which is shown on the lower right hand corner of every page in this document) the information is current and up to date. However the reader is encouraged to check for any updates on this document at the following URL, <http://alvin.inst.bnl.gov/~anand/phenix>

Revision History:

06/29/1998: GND pin assignment table (Table 3) corrected – A. Franz