Proposed Test System to study SEU and Loss of Lock For the HP G-Link Giga-Bit Optical Link

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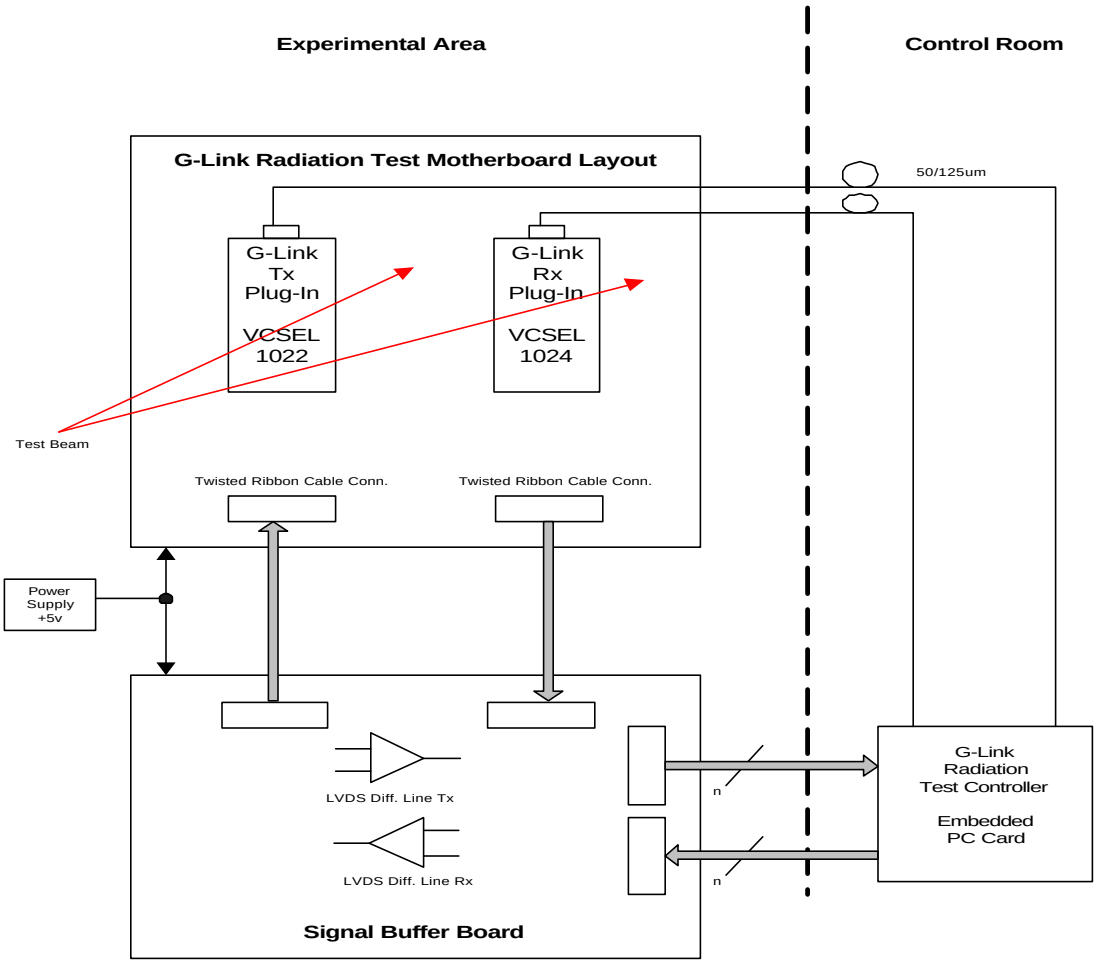
Introduction

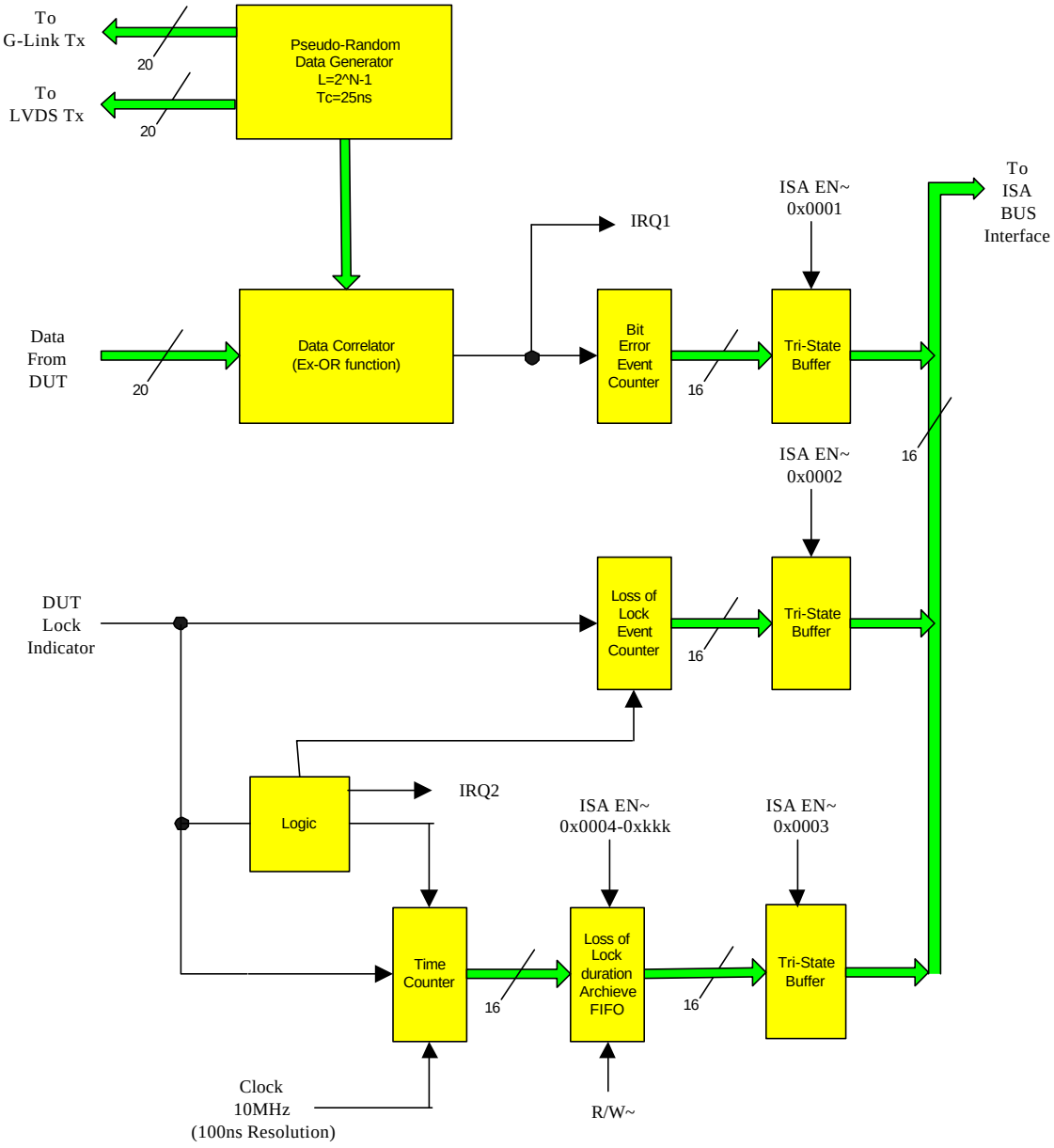
Based on the discussions that took place at our last phone meeting I put together a few diagrams illustrating a possible approach to evaluating the G-Link optical link under radiation. Fig. 1 illustrates the general approach. A PC based board would be designed that included a single FPGA to generate and check data for bit errors. The card would also include an optical transceiver along with a serializer and deserializer. Bit errors and loss of lock occurrences would be monitored as well as the time duration of each loss of lock. Errors would initiate an interrupt. The computer would then record the error event into a file as well as on a computer screen. A simple command shell or a Visual Basic routine would be all that is required. The ISA interface has already been developed.



G-Link Radiation Study Test Setup

Fig. 1

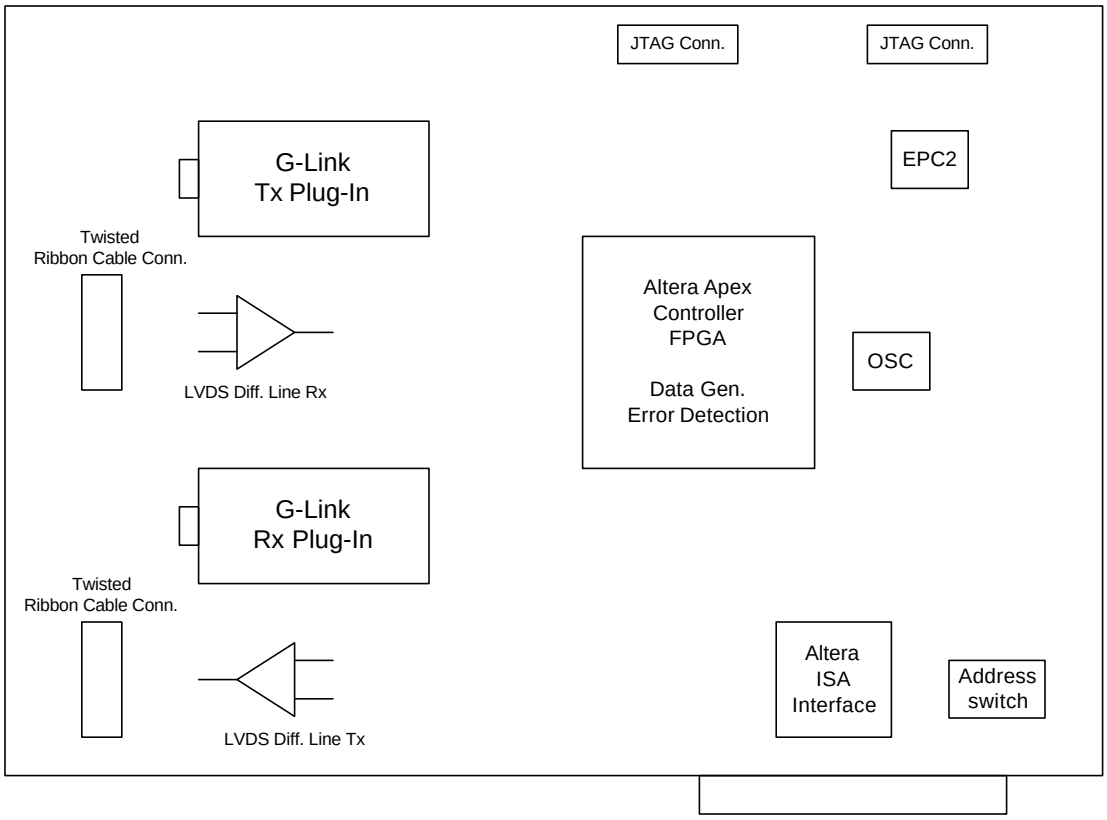
A functional block diagram of the G-Link radiation test controller is shown in Figure 2.



G-Link Radiation Test Controller Functional Block Diagram

Fig. 2

Figure 3 illustrates a possible layout for the PC based board.



G-Link Radiation Test Controller

Fig. 3

Test Method

A possible test method would be to generate a pseudo-random code, transmit the code to the DUT, and then correlate the data received to the data transmitted. The data correlation would be an exclusive-or function. Errors could be logged as individual bit errors and if necessary multiple bit errors. When loss of lock occurs the event would trigger an interrupt as well as a counter to measure the time of the event. The time resolution of the counter would be 100ns (10MHz). This number is based on the minimal G-Link recovery time of 128 frames (1.6us) running in the double frame mode at 80MHz. Previous results [1] show a mean down time of 300us and a maximum down time of 500us. Implementing a 14-bit counter would be adequate to record the duration of the loss-of-lock event.

Additionally automated current monitoring may be desirable for device latchup. It may be possible to current sense individual devices.

It should be noted that the tests performed in [1] did not check the data field for errors. Only the error flag generated by the G-Link was monitored for link bit errors. This flag only checks the 4-bit control word for

errors that would represent an illegal control word. Also the demultiplexing chip was dismissed as a source of errors based on the fact that it was a standard ATLAS component.

Possible Problems and Concerns

To run the link in the double frame mode would require a demultiplexing chip. At 80MHz the chip should be located on the G-Link plug in board. This raises the issue of uncertainty due to exposure to radiation.

The optical transceiver would be in close proximity the HP serializer or deserializer. This again raises an uncertainty issue due to exposure. We may be able to dismiss this based on previous results showing the Methode VCSEL as a radiation tolerant device. LAr has selected the Methode VCSEL over the HP5305 based on previous testing.

Possible difficulties may arise from the timing of the received test data to the reference data.

Data integrity of the generated source data transmitted to the DUT over a significantly long channel.

Knowledge of the beam test area must be know to devise a scheme to study the effects of the angle of beam incidence on the DUT.

REFERENCES

[1] M-L. Andrieux, B.Dinkespiler, G. Evans, L.Gallin-Martel, J.Lundqvist, O. Martin, *M.Pearce*, R.Stroynowski, J.Ye, " Development Of Radiation Tolerant Gb/s Optical Links for The Front-End Readout of the Atlas Liquid Argon Calorimeter".