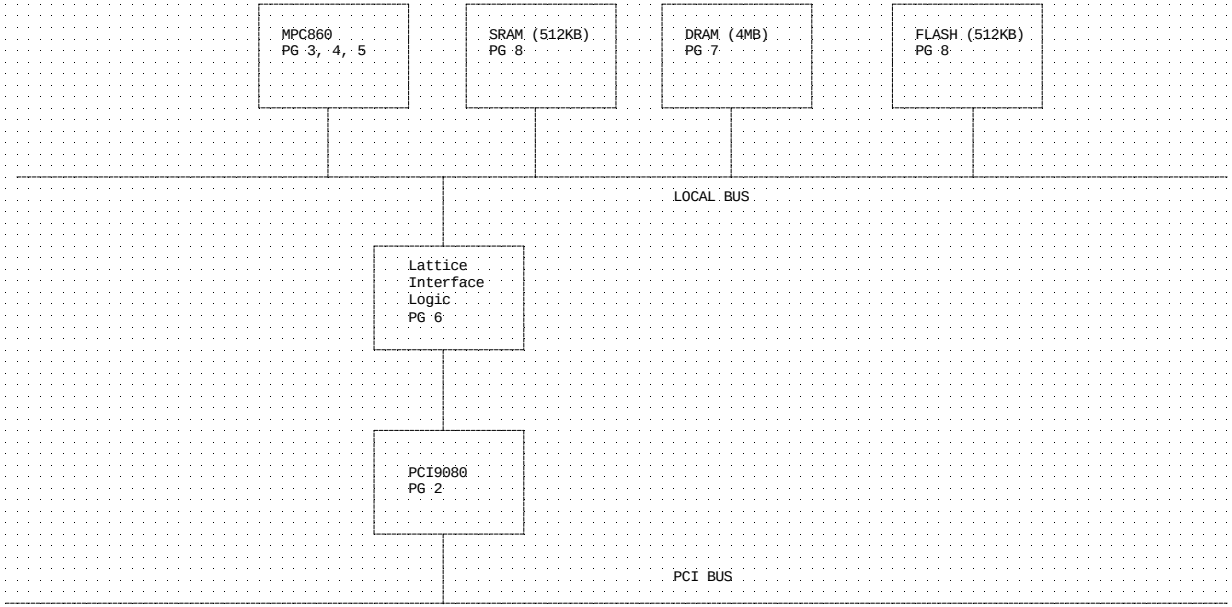
PCI9080RDK-860 BLOCK DIAGRAM

ECN HISTORY

ECN NUMBER	DATE	APPROVAL
PCI9080RDK-860 Rev 1.0	7/23/97	
PCI9080RDK-860 Rev 2.0	12/5/97	
PCI9080RDK-860 Rev 2.0	02/01/98	



This reference design has been developed and tested by Vitana Corp.

Vitana Corporation
Tel: 613-740-4445
Email: rdk@vitana.com
Web: www.vitana.com

PLX TECHNOLOGY, MOUNTAIN VIEW, CA
PCI9080-860 RDK

Block Diagram

H. W. Leahy	Size: Custom	CAGE Code	DWG NO: 9080860	Rev: 2.0
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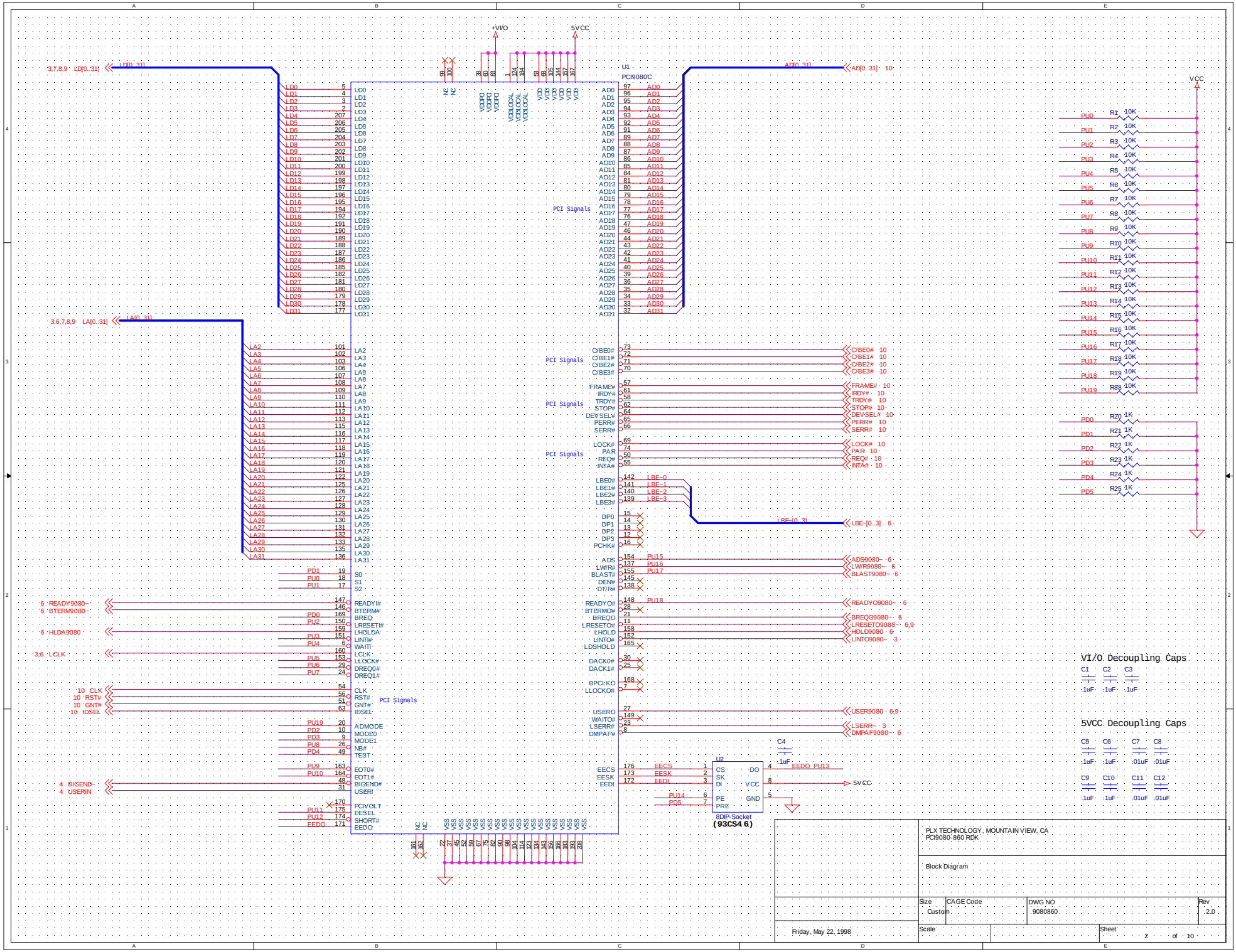
U1
PCI9080C
+VIO
5VCC
VCC
PCI Signals
LD[0..31]
LA[0..31]
AD[0..31]
LBE[0..3]
U2
CS
SK
DI
PE
PRE
DO
VCC
GND
8DIP-Socket
(93CS46)
VI/O Decoupling Caps
5VCC Decoupling Caps
PLX TECHNOLOGY, MOUNTAIN VIEW, CA
PCI9080-860 RDK
Block Diagram
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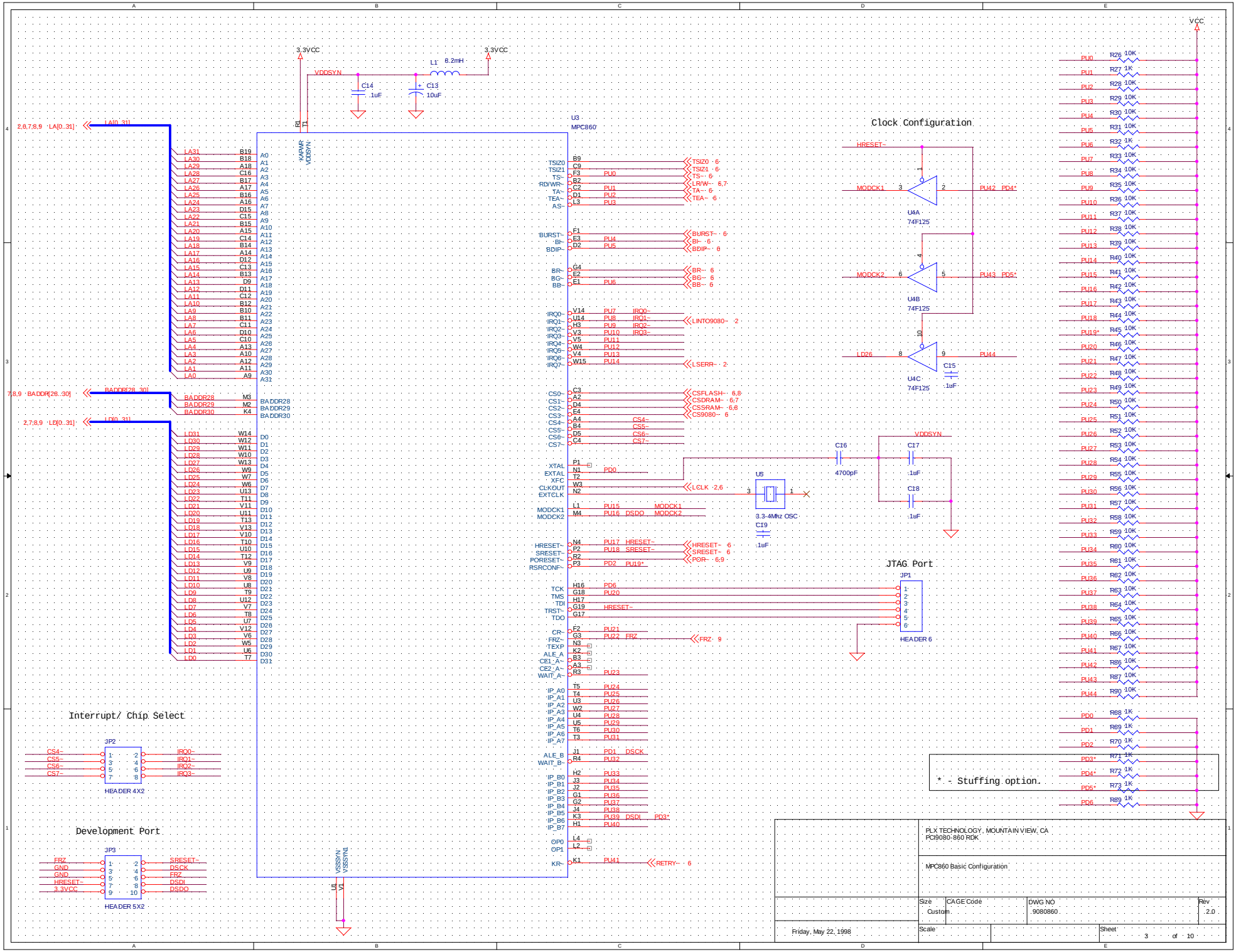
3.3VCC
VDDSYN
L1 8.2mH
C14 .1uF
C13 10uF
U3
MPC860
Clock Configuration
U4A 74F125
U4B 74F125
U4C 74F125
C15 .1uF
C16 4700pF
C17 .1uF
C18 .1uF
C19 .1uF
U5
3.3-4Mhz OSC
JTAG Port
JP1
HEADER 6
Interrupt/ Chip Select
JP2
HEADER 4X2
Development Port
JP3
HEADER 5X2
VCC
VSSSYN
VSSSYN1
* Stuffing option.
PLX TECHNOLOGY, MOUNTAIN VIEW, CA
PCI9080-860 RDK
MPC860 Basic Configuration
Size Custom
CAGE Code
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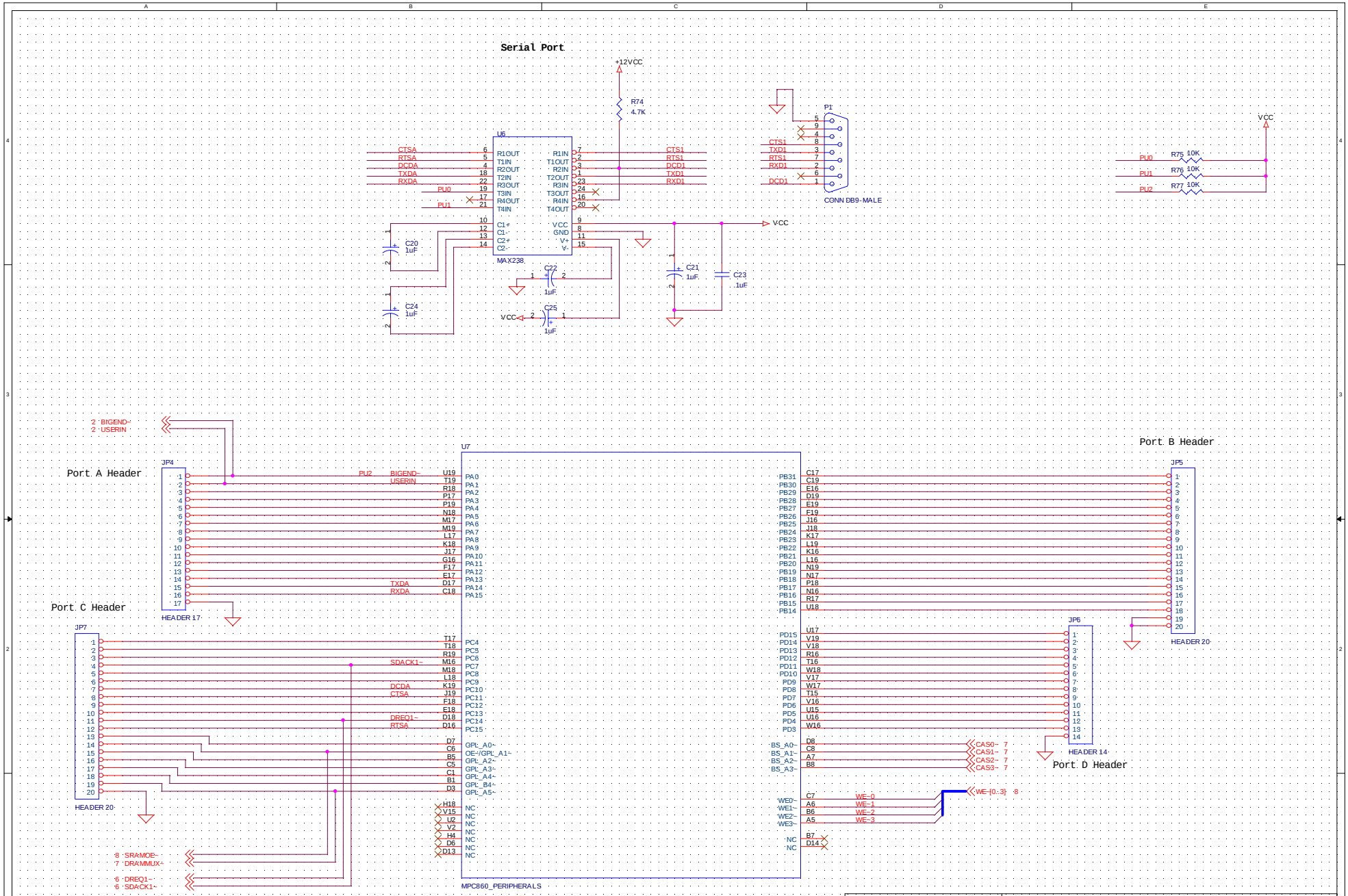
Serial Port
+12VCC
R74
4.7K
U6
MAX238
R1OUT
T1IN
R2OUT
T2IN
R3OUT
T3IN
R4OUT
T4IN
R1IN
T1OUT
R2IN
T2OUT
R3IN
T3OUT
R4IN
T4OUT
C1+
C1-
C2+
C2-
VCC
GND
V+
V-
CTSA
RTSA
DCDA
TXDA
RXDA
PU0
PU1
CTS1
RTS1
DCD1
TXD1
RXD1
C20
1uF
C21
1uF
C22
1uF
C23
1uF
C24
1uF
C25
1uF
P1
CONN DB9-MALE
R75 10K
R76 10K
R77 10K
PU2
Port A Header
JP4
HEADER 17
2 BIGEND~
2 USERIN
BIGEND~
USERIN
TXDA
RXDA
Port C Header
JP7
HEADER 20
SDACK1~
DCDA
CTSA
DREQ1~
RTSA
8 SRAMOE~
7 DRAMMUX
6 DREQ1~
6 SDACK1~
U7
MPC860_PERIPHERALS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
GPL_A0~
OE~/GPL_A1~
GPL_A2~
GPL_A3~
GPL_A4~
GPL_B4~
GPL_A5~
NC
WE0~
WE1~
WE2~
WE3~
PB31
PB30
PB29
PB28
PB27
PB26
PB25
PB24
PB23
PB22
PB21
PB20
PB19
PB18
PB17
PB16
PB15
PB14
PD15
PD14
PD13
PD12
PD11
PD10
PD9
PD8
PD7
PD6
PD5
PD4
PD3
BS_A0~
BS_A1~
BS_A2~
BS_A3~
CAS0~
CAS1~
CAS2~
CAS3~
WE=0
WE=1
WE=2
WE=3
WE=[0:3]
Port B Header
JP5
HEADER 20
Port D Header
JP6
HEADER 14
Note:
Serial Port 1 uses SCC1
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PCI9080-860 RDK
MPC860 Peripherals
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Custom
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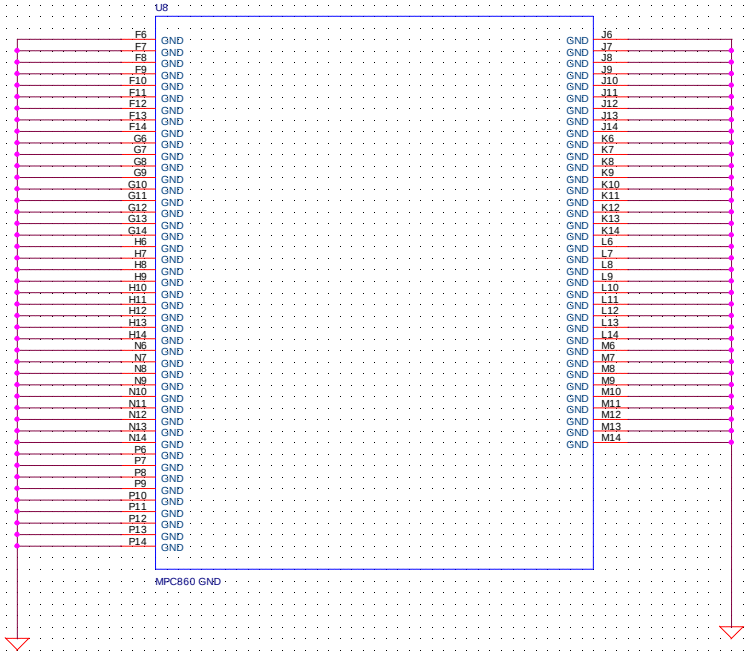
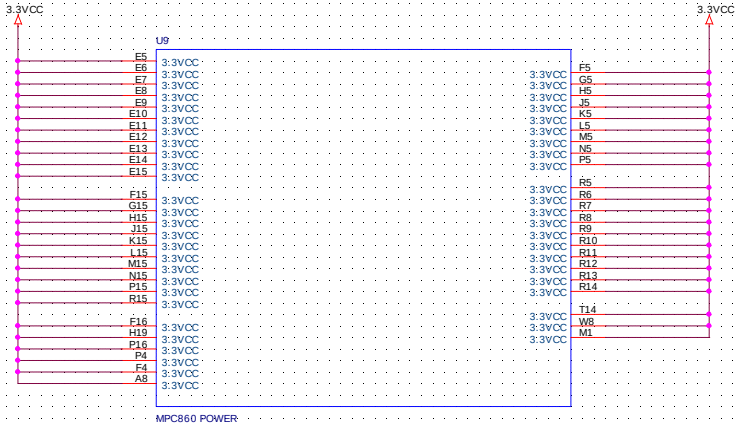
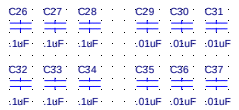




MPC860 Decoupling Caps



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	MPC860 Power & Ground			
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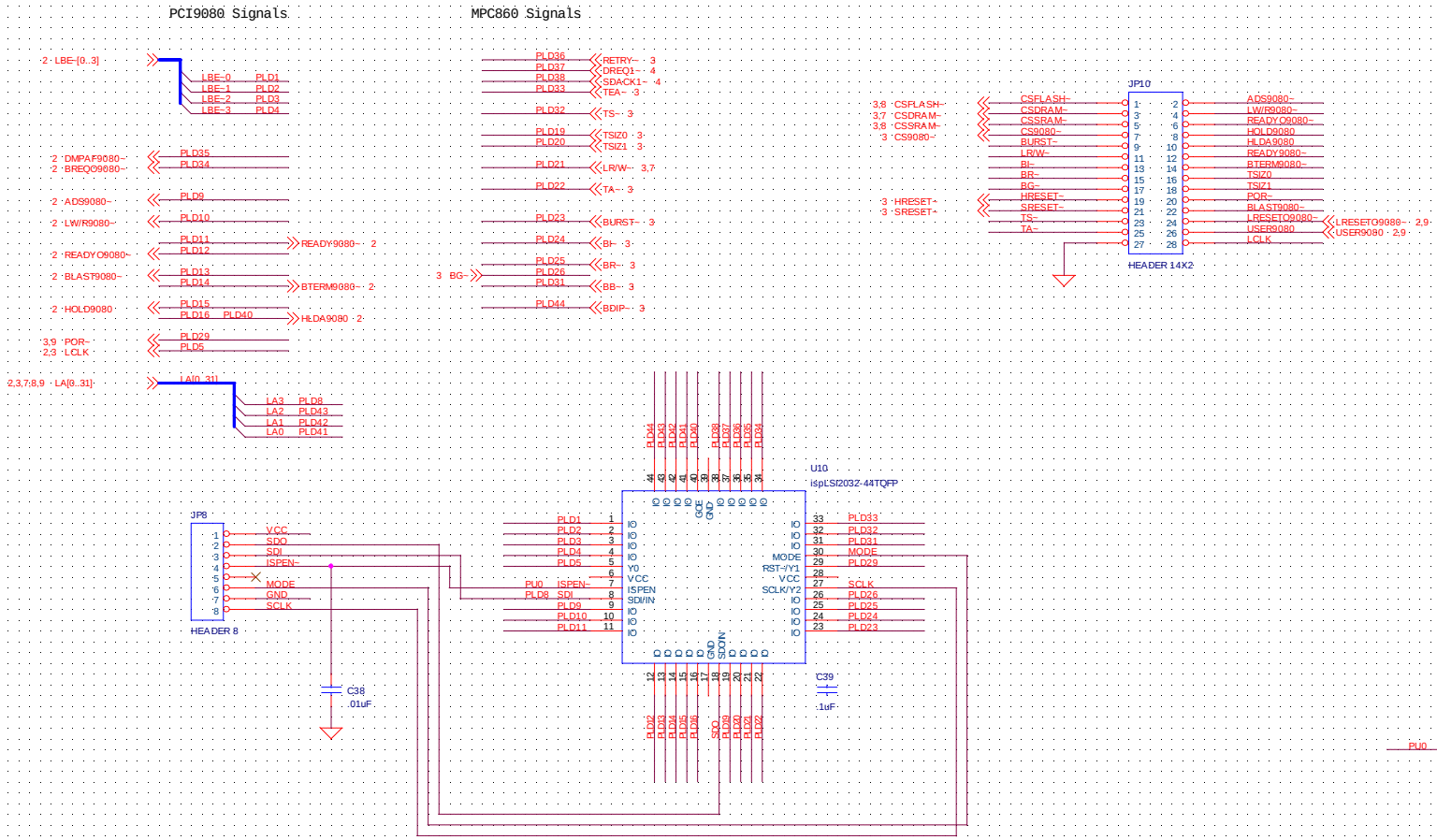

Note:
Bring the following pins on U10 to external vias:
33,34,35,36,37,38,41,42,43,44

* - Stuffing Option

	PLX TECHNOLOGY, MOUNTAIN VIEW, CA PCI9080-860 RDK			
	MPC860 Interface			
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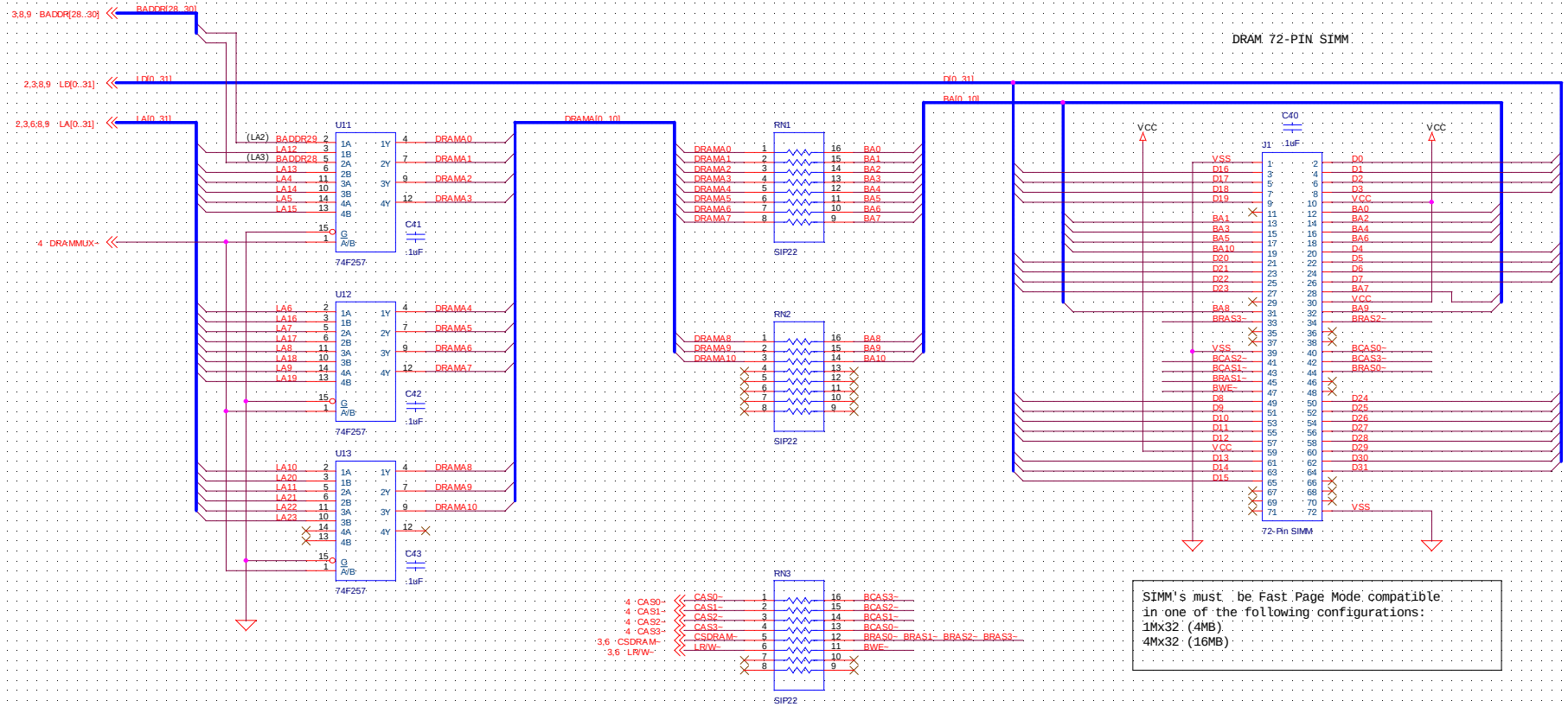

SIMM's must be Fast Page Mode compatible
in one of the following configurations:
1Mx32 (4MB)
4Mx32 (16MB)

PLX TECHNOLOGY, MOUNTAIN VIEW, CA PCI9080-860 RDK			
DRAM			
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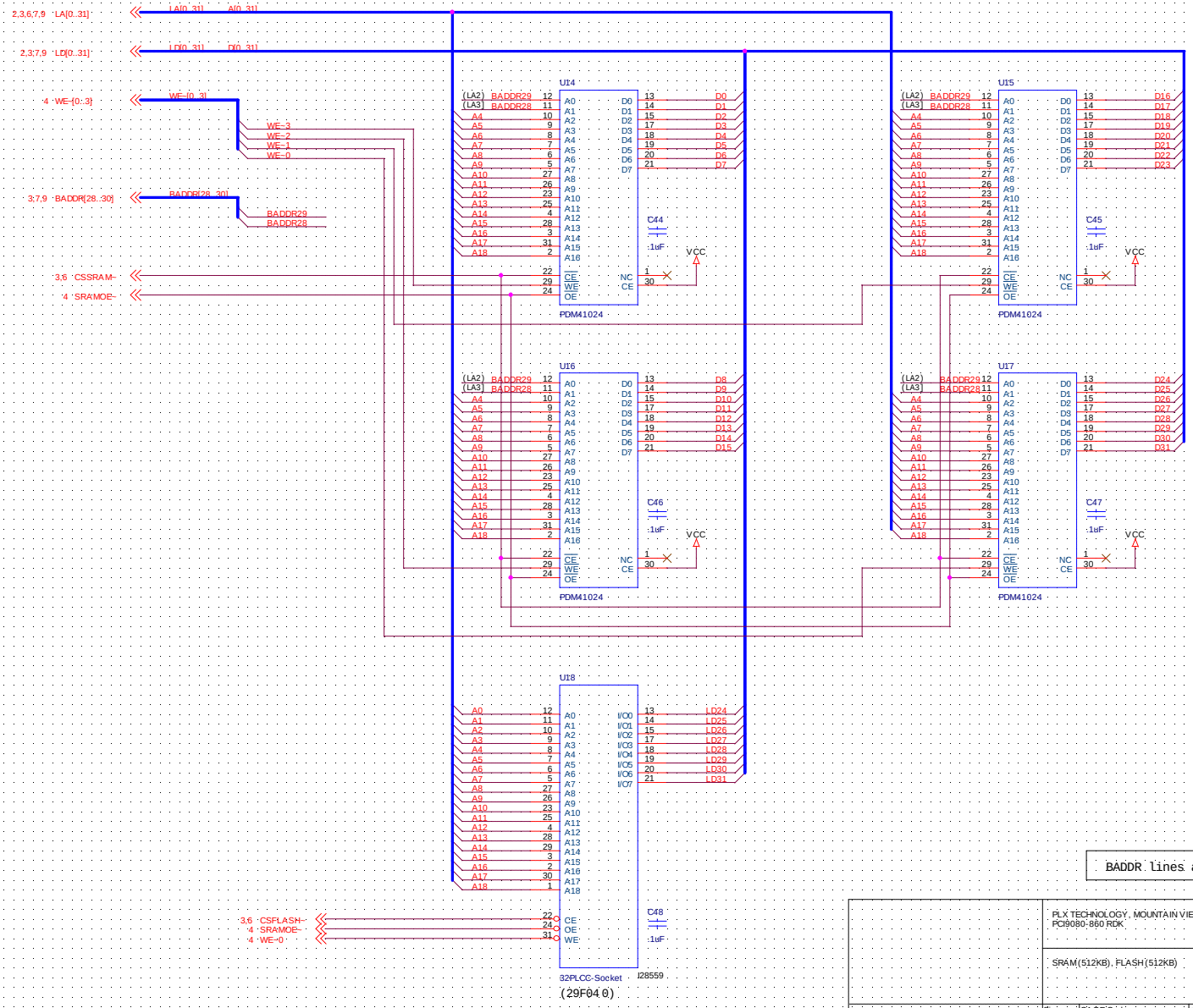

BADDR lines are used to support bursting

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PCI9080-860 RDK

SRAM(512KB), FLASH(512KB)

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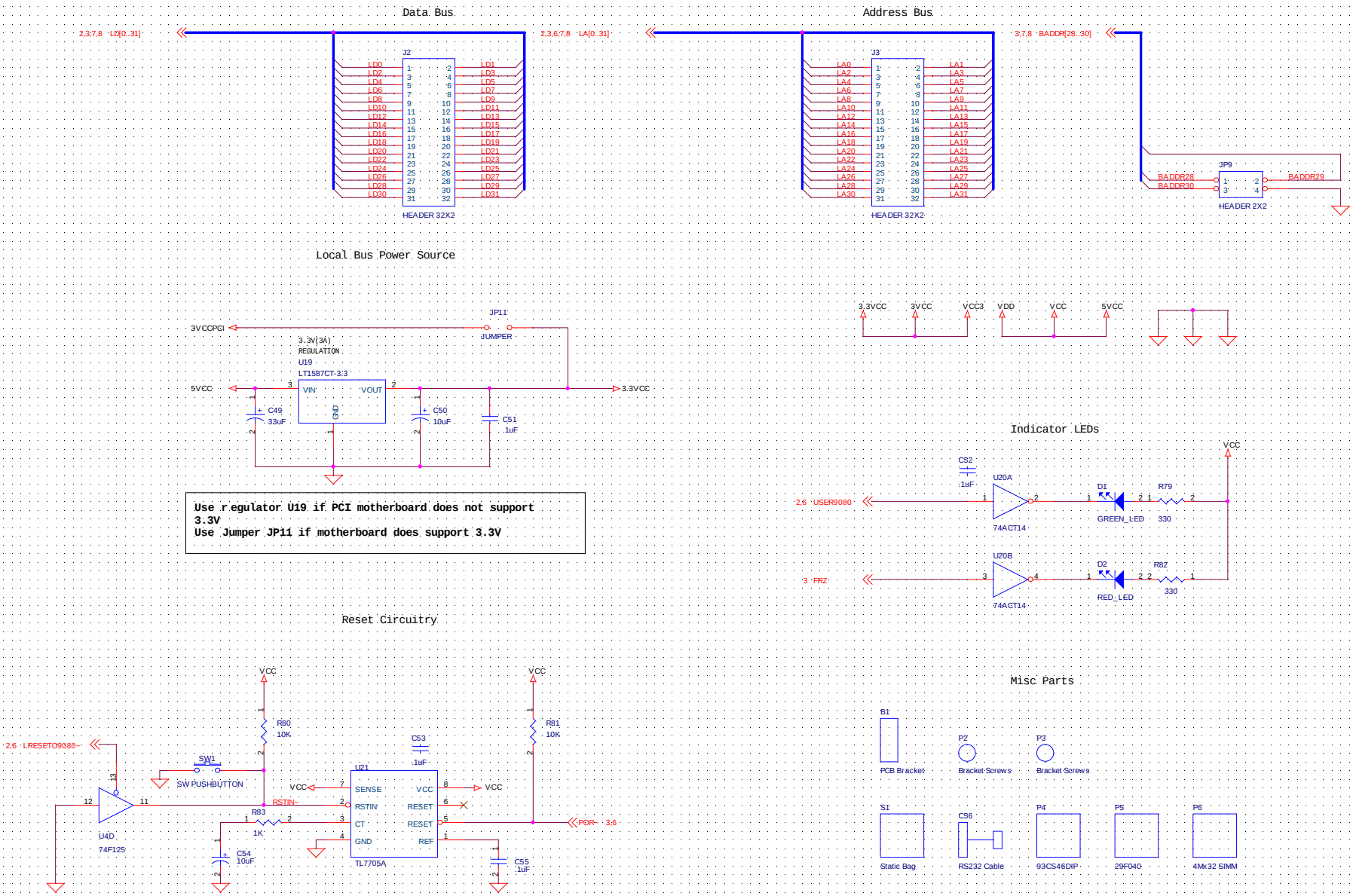

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PCI9080-860 RDK

Reset

Size	CAGE Code	DWG NO	Rev
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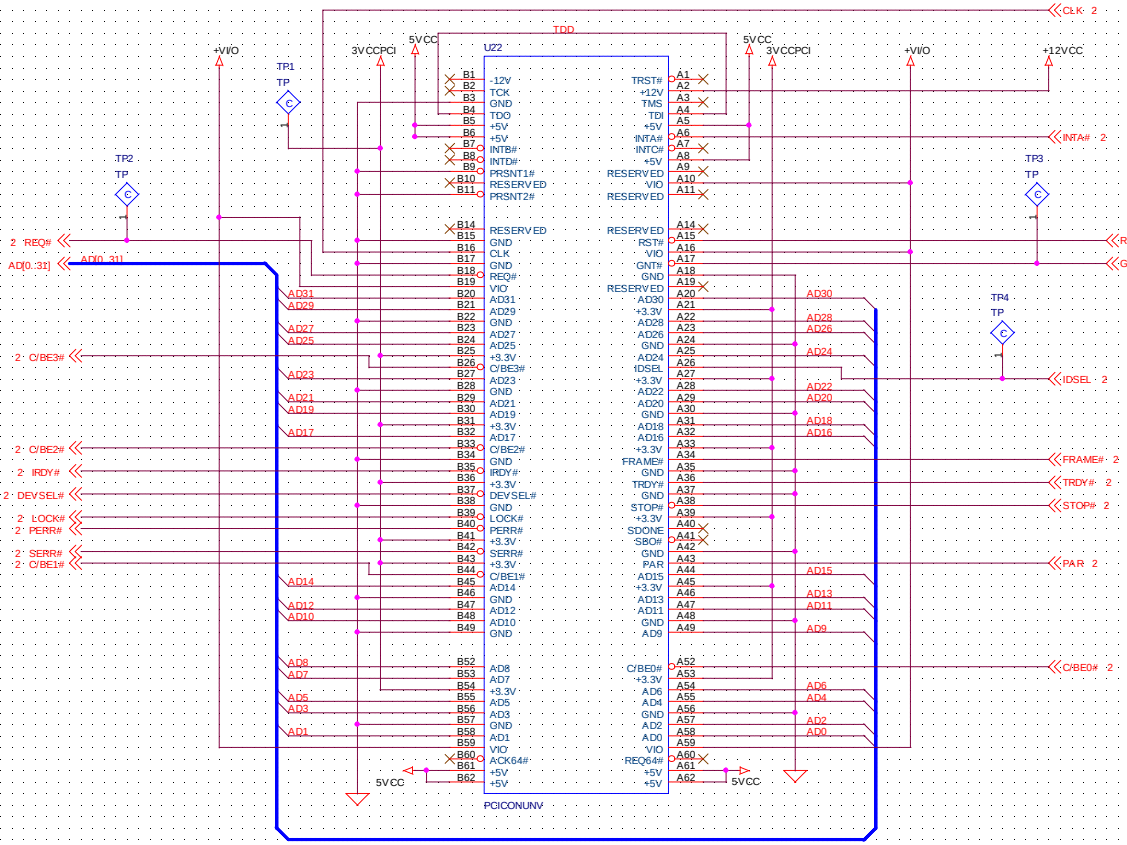
PCI Edge Connector



Note:
This connector is keyed for both 3.3V and 5V PCI I/O

PLX TECHNOLOGY, MOUNTAIN VIEW, CA PCI9080-860 RDK			
PCI Edge Connector			
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