

PLX PCI SDK

Software Development Kit

Version 2.1

Revision 1

User's Manual

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1. Introduction

1.1 About This Manual

The PLX family of 32bit I/O accelerator chips connect the PCI bus to Intel, Power PC processors and other processors. They provide full Intelligent I/O (I₂O) compatibility. The PCI Software Development Kit (PCI SDK) provides a powerful I/O Platform Application Programmer's Interface (IOP API), and Windows software that are used to control PLX devices. We are confident that through the use of the PCI SDK, your PLX designs will be brought to market faster and more efficiently.

This manual provides information about the functionality of the PCI SDK. Customers have the choice of using the PCI SDK with any PLX Reference Design Kit (RDK), or a generic device that uses a PLX chip. Users should consult this manual when installing the PCI SDK and for general information.

1.2 PCI SDK Features

The PCI SDK includes the following features:

- A feature based IOP API, with support for a variety of PLX PCI chips;
- Board Support Package (BSP) that allows customization of the PCI SDK;
- A Back-End Monitor application used for debugging;
- IOP DMA Resource Manager that supports three modes of operation;
- A PCI API and device drivers compatible with Windows NT/98; and,
- PLXMon 98, a Windows Graphical User Interface (GUI) application used to configure and modify PLX PCI devices.

1.3 Where To Go From Here

The following is a brief summary of the chapters to help guide your reading of this manual:

Chapter 2, Getting Started, discusses how to start using the PCI SDK and some of the applications provided.

Chapter 3, PCI SDK Software Architecture Overview, describes the layout of the PCI SDK software.

Chapter 3, section 3.4, IOP Software Architecture, provides a brief explanation of the IOP software, specifically the Board Support Package (BSP), the IOP API, and the Back-End Monitors (BEM).

Chapter 3, section 3.5, Host Win32 Software Architecture, provides a brief explanation of the Win32 software, specifically the PCI API and the device driver.



1.4 Other PCI SDK Manuals

The PCI SDK includes the following manuals which users should consult for design details:

- PCI SDK Programmer's Reference Manual: This manual covers all software design issues regarding the device drivers, API and user applications.
- PLXMon 98 User's Manual: This manual describes the usage of the PLXMon 98 application.

1.5 Conventions

Please note that when software samples are provided the following notations are used:

- *italics* are used to represent variables, function names, and program names;
- `courier` is used to represent source code given as examples.

1.5.1 Windows Programming Conventions

Some designers may not be familiar with Windows programming conventions. Therefore, a few conventions have been noted below:

- *PU32 data* is analogous to *U32 *data* or *unsigned long *data*; and
- *IN* and *OUT* are used to distinguish between parameters that are being passed into API functions and parameters that are being returned by API functions.

1.6 Terminology

All references to Windows NT assume Windows NT 4.0 or higher and may be denoted as WinNT.

All references to Windows98 may be denoted as Win98.

Win32 references are used throughout this manual to mean any application that is compatible with the Windows 32-bit environment.

All references to IOP (I/O Platform) throughout this manual denote the RDK board and all references to IOP software denote the software running on the RDK board.

All references to FLASH should be replaced with EPROM for users of the PCI 9080RDK-SH3 and PCI 9080RDK-RC32364 Reference Design Kits.

1.7 Development Tools Needed

Development tools needed for the PCI SDK that are not supplied include:

- Win32 Applications: Microsoft Visual C++ 5.0, with Microsoft Developer Studio;
- Win32 Applications: Microsoft Platform Software Development Kit (SDK);
- Windows NT 4.0 Drivers: Microsoft Windows NT 4.0 Device Driver Kit (DDK);
- Windows98 Drivers: Microsoft Windows98 Device Driver Kit (DDK);
- PCI 9080RDK-860, CompactPCI and PCI 9054RDK-860 IOP Software: Diab Data, Inc. Compiler and Linker for the MPC860, version 4.0b;



- PCI 9080RDK-401B IOP Software: IBM High C/C++ PowerPC Cross-Compiler, version 1.0 (7/31/96); and IBM 401 EVB Software Support Package, version 1.6.4 (4/1/97).
- PCI 9080RDK-RC32364 IOP Software: IDT/c Cross Compiler System Version 5.5/7.0 GNU Developer's Kit.
- PCI 9080RDK-SH3 IOP Software: Cygnus GNU compiler: gcc version 2.7-96q3a

Note: The versions above indicate the versions that were used during development of the PCI SDK software.

1.8 Customer Support

Prior to contacting PLX customer support, please ensure that you are situated close to the computer that has the PCI SDK installed and have the following information:

1. Model number of the PLX PCI RDK (if any);
2. PLX PCI SDK version (if any);
3. Host Operating System and version;
4. Description of your intended design:
 - PLX chip used
 - Microprocessor
 - Local Operating System and version (if any)
 - I/O
5. Description of your problem; and
6. Steps to recreate the problem.

You may contact PLX customer support at:

Address: PLX Technology, Inc.
Attn. Technical Support
390 Potrero Avenue
Sunnyvale, CA 94086

Phone: 408-774-9060
Fax: 408-774-2169
Web: <http://www.plxtech.com>

You may send email to one of the following addresses:

west-apps@plxtech.com
mid-apps@plxtech.com
east-apps@plxtech.com
euro-apps@plxtech.com
asia-apps@plxtech.com

2. Getting Started

2.1 PCI SDK Installation

2.1.1 Unpacking

The PCI SDK comes complete with the following items (see Figure 2-1):

- PCI SDK User's Manual (this document);
- PCI SDK Programmer's Reference Manual;
- PLXMon 98 User's Manual; and
- PCI SDK CD-ROM.

Please take the time now to verify that your PCI SDK is complete. If not, please contact Customer Support.

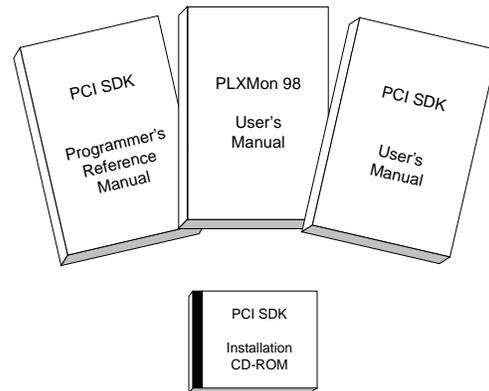


Figure 2-1 Components of the PCI SDK

2.1.2 Minimum System Requirements

Minimum host system requirements for the PCI SDK are as follows:

- Windows NT 4.0 with Service Pack 3, or Windows98;
- 32MB RAM (when used with only one PLX PCI RDK. Additional memory may be required if more than one PLX PCI RDK are in the system);
- 20MB hard drive space; and,
- 1 RS 232 serial port.

2.1.3 Development Requirements

The PCI SDK development environment is either the Window NT 4.0 or Windows98 operating systems.

The PCI API was developed using Microsoft Developer Studio, supplied with Microsoft Visual C++ 5.0 and the Microsoft Platform Software Development Kit.

The WinNT device drivers were developed using the Microsoft Windows NT DDK, version 4.0 and Microsoft Visual C++ 5.0.

The Win32 Driver Model (WDM) device drivers were developed using the Microsoft Windows98 DDK and Microsoft Visual C++ 5.0.



2.1.4 Software Installation

2.1.4.1 Windows NT Installation Procedures

To install the PCI SDK Support Software, complete the following:

Note: All previous PCI SDK versions located on the computer must be removed before installing a PCI SDK update. Refer to section 2.1.4.3 for more details.

1. Insert the CD-ROM into the appropriate CD-ROM drive.
2. Run “D:\Install.exe” either by typing it at a command prompt or by choosing the Run option of the Start Menu (where “D:” is the drive letter for the CD-ROM Drive).
3. This will launch the Install Wizard application that will ask you to select the PLX RDK that you are using. The appropriate PCI SDK version will then be installed.
4. Reboot the computer.

Note: For proper WinNT installation, the PCI SDK should be installed by a user with “administrator” user rights.

The default installation directory may be changed from default path (C:\Plx\PciSdk211) to any drive and path that is desired. This document uses “<INSTALLPATH>” to denote the installation directory.

This completes the PCI SDK software installation.

2.1.4.1.1 Windows NT Device Driver Installation

Unlike the Win98 installation wizard the Windows NT installation wizard takes care of the device driver installation.

2.1.4.2 Windows98 Installation Procedures

The installation of the PCI SDK software onto a Win98 system requires two steps: Install the PCI SDK files, and, then install the Win98 device drivers. The following two sections describe how to completely install the PCI SDK Support Software for Win98.

2.1.4.2.1 Windows98 Software Installation

To install the PCI SDK software, complete the following:

Note: All previous PCI SDK versions located on the computer must be removed before installing a PCI SDK update. Refer to section 2.1.4.3 for more details.

1. Ensure no PLX RDK boards are installed in your computer.
2. Insert the CD-ROM into the appropriate CD-ROM drive.
2. Run “D:\Install.exe” either by typing it at a command prompt or by choosing the Run option of the Start Menu (where “D:” is the drive letter for the CD-ROM Drive). The interactive installation program will install all files.
3. This will launch the Install Wizard application that will ask you to select the PLX RDK that you are using. The appropriate PCI SDK version will then be installed.

The default installation directory may be changed from default path (C:\Plx\PciSdk211) to any drive and path that is desired. This document uses “<INSTALLPATH>” to denote the installation directory.

This completes the PCI SDK software installation. Proceed to the next section to install the Win98 device driver.

2.1.4.2.2 Windows98 Device Driver Installation

A device driver is necessary for the PCI SDK software to communicate to the PLX RDK board. PCI SDK applications cannot communicate with any RDK board through the PCI interface without a PCI SDK device driver installed. The installation script used to install the PCI SDK can not entirely install the PCI SDK. To install the device driver in Win98, complete the following:

1. After installing the PCI SDK successfully (see the previous section), shutdown the computer.
2. Insert a PLX RDK board into a free PCI slot.
3. Reboot the computer. Windows98 should first detect the new hardware device with a “New Hardware Found” message box. Acknowledge this message box.
4. Windows98 displays the “Add New Hardware” Wizard. Windows98 displays the following message: “This wizard searches for new drivers for:” with the corresponding board name following it. If you are using a PLX RDK board proceed to step 5. If you are using a custom engineering board with a PLX device then proceed to step 10.

Driver Installation for PLX Engineering Boards:

5. Click on the “Next” button. Once Windows98 has completed its search the following prompt is displayed: “What do you want Windows to do?” At the prompt select “Search for the best driver for your device”. This is the default option. Click on “Next” to continue.
6. The installation wizard asks “Windows will search [...] in any of the following selected locations.” Check none of the items in the list and click on “Next” to continue.
7. The device driver is ready to be installed when the installation wizard displays the following message: “Windows is now ready to install the best driver for this device.” Click on “Next” to continue.
8. The device driver installation is complete when Windows98 displays the following message: “Windows has finished installing the software that your new hardware device requires”.
9. Click on “Finish” to complete the Win 98 device driver installation.

Driver Installation for Custom Engineering Boards with PLX devices:

10. The installation wizard will detect your custom device as a “PCI Bridge”. Click on the “Next” button and then choose the option “Display a list of all the drivers in a specific location.” Click “Next”.
11. Select “Other Devices”. Click “Next”.
12. Now select the column that says “PLX Technology, Inc.” and choose “Unknown PCI 9054 board” if using a PCI 9054 device. Otherwise choose “Unknown PCI 9080 board” if using a PCI 9080 device. The install wizard will warn you that this device driver is not specific for your device. Ignore this warning by choosing “Yes”. Click “Next”.



13. Click “Finish” to complete the Win 98 device driver installation.

Note: If you change the PLX RDK board from one slot to another, Windows98 will treat it as a “New Hardware” and will display the same dialog.

Once the Win98 device driver installation is complete it is ready to run without having to reboot the system.

2.1.4.3 Uninstalling All Previous Versions Of The PCI SDK Software

Prior to installing a new version of the PCI SDK, you should first uninstall all older versions. There is interaction between PCI and IOP software modules and it is important not to mix releases. To remove all PCI SDK Software, including device drivers, complete the following:

1. Stop all PLX applications;
2. Open the Windows Control Panel;
3. Double click on the Add/Remove Programs icon in the Control Panel window;
4. Choose the PCI SDK package from the item list; and
5. Click the Add/Remove... button.

Note: This only removes the files that were originally installed by the PCI SDK installation program. For proper removal in WinNT, the PCI SDK should be removed by a user with “administrator” user rights.

This completes the PCI SDK software removal.

2.1.4.4 PCI SDK v2.1 Compatibility

Due to interaction between host and IOP software components it is very important that PCI SDK releases are the same on both sides (i.e. If the host software is from PCI SDK v2.1 then the IOP software should also be from PCI SDK v2.1). If you have recently purchased a PLX RDK then it will already contain the correct IOP software preprogrammed, so you need not concern yourself with this section. However, if you have purchased the PCI SDK as an upgrade and intend to use it with an earlier PLX RDK board you will need to upgrade the RDK board’s FLASH with a current version. This is necessary to ensure that nothing unpredictable occurs due to incompatibilities with modules.

Although it is important to have your host and IOP software from the same release, the IOP API and PCI API are compatible with PCI SDK v2.0 and higher. PLX has developed an API model that is portable and will continue to support this model in future releases. The previous paragraph is necessary because some PLXMon 98 features rely on a communication protocol with the IOP BSP and the protocol has improved in each release. The IOP API and PCI API are fully compatible between releases.

User’s who are upgrading their PCI SDK and intend to use it with an earlier PLX RDK board should follow the steps below.

To upgrade your FLASH image follow the steps below:

- User’s of the PCI 9054RDK-860 may use PLXMon 98, as described in the PLXMon 98 User Manual, to download the “helloworld” sample to the PCI 9054RDK-860. The image should be programmed at FLASH offset 0x00000.

- User's of the CompactPCI 9054RDK-860 may use PLXMon 98, as described in the PLXMon 98 User Manual, to download the "helloworld" sample to the CompactPCI 9054RDK-860. The image should be programmed at FLASH offset 0x00000.
- User's of the PCI 9080RDK-401B may use PLXMon 98, as described in the PLXMon 98 User Manual, to download the "helloworld" sample to the PCI 9080RDK-401B. The image should be programmed at FLASH offset 0x60000.
- User's of the PCI 9080RDK-860 must use a device programmer to reprogram the FLASH with the "helloworld" sample application. The image should be programmed at FLASH offset 0x00000.
- User's of the PCI 9080RDK-SH3 must use a device programmer to reprogram the EPROM with the "helloworld" sample application. The image should be programmed at EPROM offset 0x00000.
- User's of the PCI 9080RDK-RC32364 must use a device programmer to reprogram the EPROM with the "helloworld" sample application. The image should be programmed at EPROM offset 0x00000.

2.1.4.5 Troubleshooting

You may experience difficulties when using the PCI SDK with Windows NT with low memory and multiple PLX RDK boards. If you notice that one of your RDK boards is not being assigned the proper memory resources by the PCI BIOS (e.g. no address provided to the Local Space 0 address) it is most likely due to a common memory problem with WinNT. It is recommended that users increase the amount of available system pages in their System Registry by following the steps below;

1. From a command prompt type: regedt32. This will bring up the Registry Editor window. (This editor looks similar to the Windows Explorer application.)
2. Select the HKEY_LOCAL_MACHINE on Local Machine window from within the Registry Editor.
3. Open the SYSTEM folder.
4. From the SYSTEM folder, open the CurrentControlSet folder.
5. From the CurrentControlSet folder, open the Control folder.
6. From the Control folder, open the Session Manager folder.
7. From the Session Manager folder, open the Memory Management folder.
8. From the Memory Management folder, change the value of the SystemPages key from 0x0 to 0x13880.

If problems persist, please contact Customer Support.

2.1.4.5.1 Driver Interrupt Sharing

The PCI SDK device drivers have interrupt sharing enabled. This allows PLX devices to share the same interrupt line as other devices. However, in order to share interrupts with non-PLX devices the device driver for the non-PLX device must also support sharing. Because many device drivers do not support interrupt sharing the PCI SDK can only be guaranteed to function properly with other PLX devices.



If a PCI SDK device driver will not start, a possible cause is the computer's BIOS is assigning an interrupt to the PLX device that is already being used by a device that doesn't support interrupt sharing. A possible work around for this condition is to manually configure the BIOS to assign a free interrupt to the PLX device.

2.2 Understanding The PCI SDK

2.2.1 IOP Software

2.2.1.1 Introduction

The PCI SDK includes several samples of IOP applications. Their purpose is to demonstrate how designers can interact with the PLX chip from IOP software. The IOP applications are user-interactive and require PLXMon 98 with a serial cable link.

The IOP applications are designed specifically to run on a PLX RDK board. However, the IOP applications can be used as a good starting point for designers using their own hardware device.

2.2.1.2 IOP Applications

The PCI SDK contains several sample applications. By default all PLX RDK boards contain the "helloworld" application preprogrammed in FLASH memory. This application blinks an LED and prints "Hello World" from the serial port. Complete source code for this application is provided in the PCI SDK. Please refer to the PLXMon 98 User's Manual for more information on how to communicate to the PLX RDK boards IOP applications.

2.2.1.2.1 MiniRom Application

MiniRom is included in the PCI SDK to provide a good starting point for users who have an untested hardware device and for this reason, it is limited in features and functionality. It provides bare minimum boot up code for most boards. This application configures the microprocessor, the PLX chip, and proceeds to blink the LED that is connected to one of the PLX chip's USER pins. To use the MiniRom application, you should program the binary image into the FLASH using a FLASH chip programmer. Once the FLASH is programmed, reboot the board and if the LED blinks then the MiniRom application configured the board properly. If this test is successful, the FLASH can be reprogrammed with the PCI SDK PLXRom image (supplied with the PCI SDK).

Note: This ROM application is provided as a bare bones ROM application useful for confirming the functionality of new boards. It does not contain any PCI SDK features that are described in any PCI SDK manual.

2.2.2 Windows Based Host Software

2.2.3 Introduction

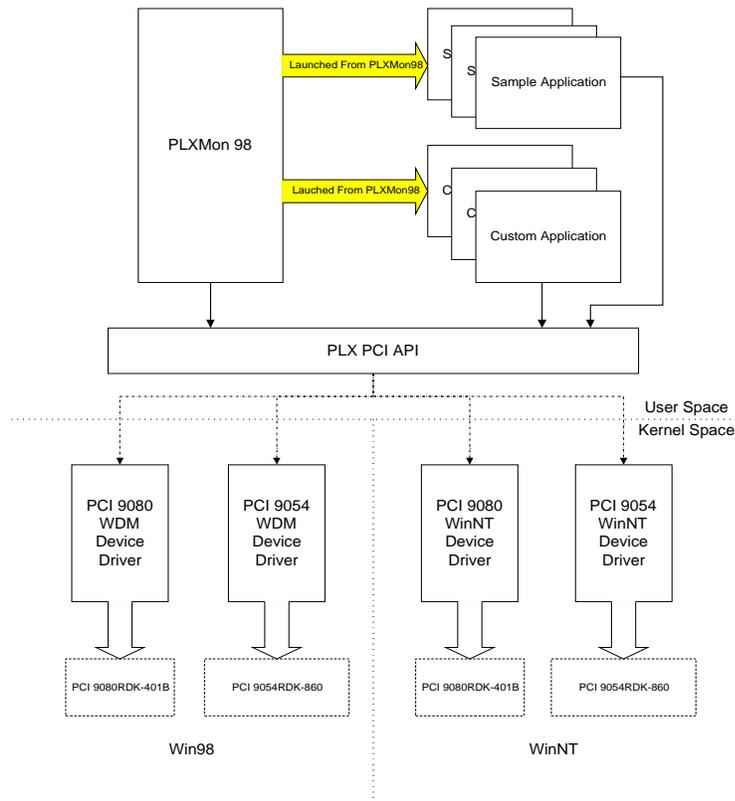


Figure 2-2 Windows Host software Layout for PCI SDK v2.1

The PCI SDK contains four distinct device drivers, an API, and a Windows monitor application (see Figure 2-2). They are as follows:

- Two PLX WinNT Device Drivers supporting the PCI 9080 and the PCI 9054;
- Two PLX WDM Win98 Device Drivers supporting the PCI 9080 and the PCI 9054 ;
- PCI API, a powerful API compatible with all PLX devices and PLX device drivers; and
- PLXMon 98, a Graphical User Interface (GUI) application that can be used to monitor and modify PLX chip registers. It can also download software to a PLX RDK board, and communicate to the software running on the RDK board.

All Win32 executables included in the PCI SDK are located in the “<INSTALLPATH>\bin” directory. Furthermore, this path is added to the environment variables when the PCI SDK is installed.

For more information on PLXMon 98, please refer to the PLXMon 98 User's Manual.

2.2.3.1 Windows NT Device Drivers

The PCI SDK includes Windows NT device drivers for each PLX device. All device drivers are located in the <WINDOWS SYSTEM DIR>\system32\drivers directory. The naming convention used for the device drivers is: `Pci<DEVICETYPE>.sys`. For example, the device driver for the PCI 9080 device is named `Pci9080.sys`.

2.2.3.1.1 Starting And Stopping

There may be times when you will need to restart the Windows NT device driver. For instance, you must restart the device driver after changing the supported device list.

To restart the Windows NT device driver you should use the Windows NT Control Panel. The Control Panel contains a utility called 'Devices' that allows you to start and stop the device driver (see Figure 2-3).

Note: Before stopping the device driver, all PCI SDK applications should be closed.

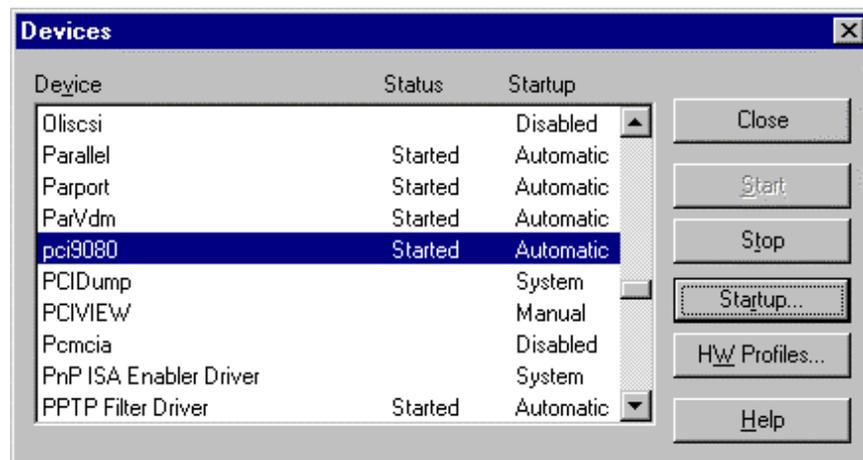


Figure 2-3 The Devices Utility Window.

By default, the device driver is configured to startup automatically at Windows NT boot time. You may configure the device driver to start manually by selecting the 'Startup...' button. However, no PCI SDK applications will function without the device driver being started.

You may also use the PCI SDK applet DriverWizard to restart the device drivers. Consult Section 2.2.3.1.4 for more details.

2.2.3.1.2 Event Logging

The Windows NT Device Driver has the capability to record errors into the Windows NT Event Viewer. When trouble shooting problems with the device driver it is recommended that the event viewer be used.

Events can be viewed by selecting an event item. Figure 2-4 shows an example of the event

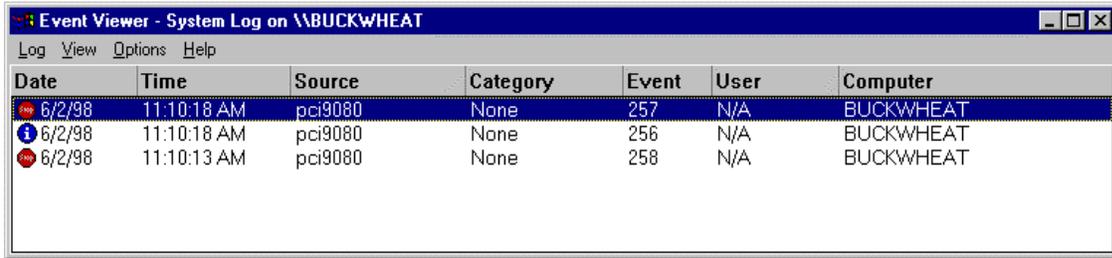


Figure 2-4 The Event Viewer Window.

viewer and Figure 2-5 shows details of an event.

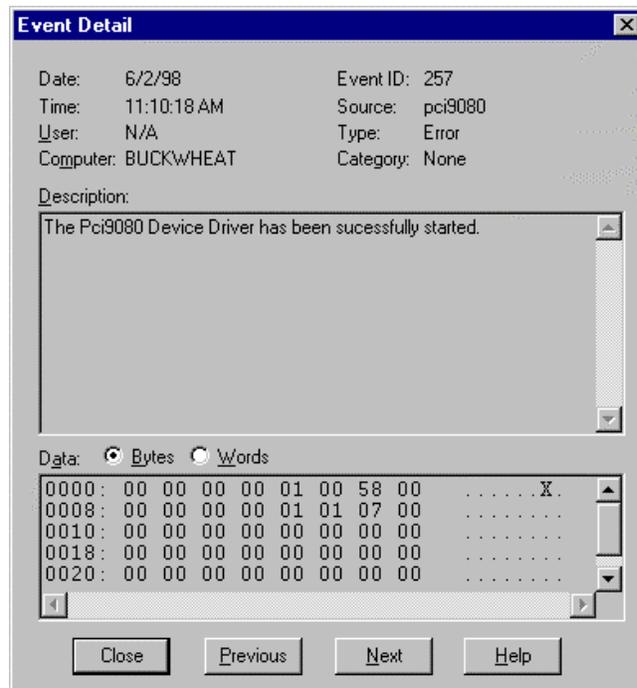


Figure 2-5 The Event Detail Window

2.2.3.1.3 Registry Configuration

Every Windows NT device driver requires an entry in the registry editor. The registry editor contains information required by the operating system as well as information required by the device driver. The name in the registry will be the same as the driver name. For instance, the `pci9080.sys` device driver has a `pci9080` registry item as shown in Figure 2.6. All device drivers are located under the `LocalMachine\System\CurrentControlSet\Services` tree.

The figures below show the required registry settings for the PCI SDK device drivers.

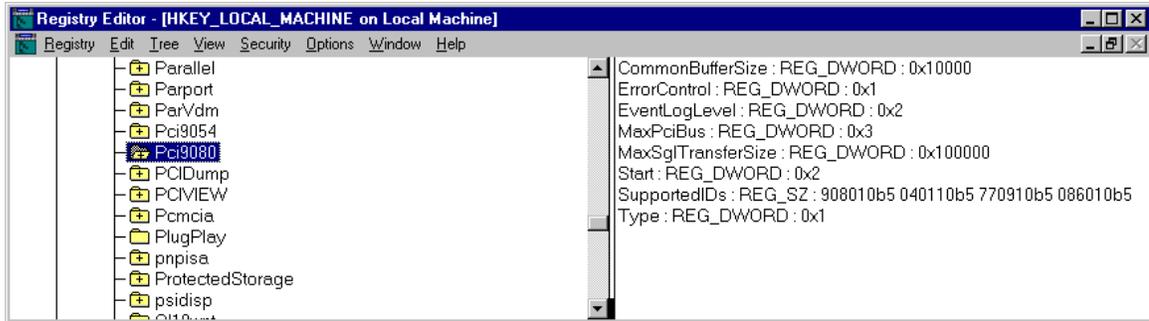


Figure 2-6 Registry Information for PCI 9080 Driver

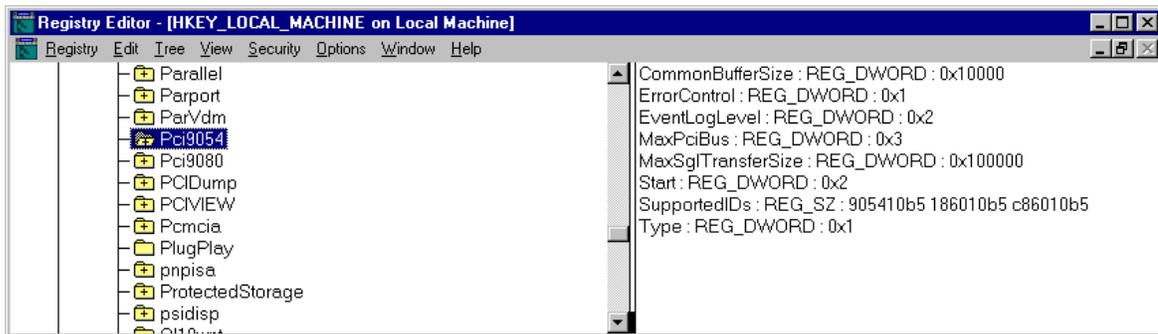


Figure 2-7 Registry Information for PCI 9054 Driver

Note: The registry editor should only be modified by advanced users with administrative rights. It is recommended that you do not change any values contained in the registry.

The registry values for the device driver are:

- *CommonBufferSize:* This value sets the size of the user buffer (PlxMon98 hbuf). By default it is set to 64KB. *Warning: The device driver will try to allocate the size requested but if it can not due to a lack of system resources, it will decrement the size until it can allocate a buffer. You should use the PlxPciCommonBufferGet() API function to determine the actual buffer size.*
- *ErrorControl:* This value is required by the operating system and should not be modified.

- *EventLogLevel*: This value sets the event logging mode in the device drivers. If this value is 0 then events will not be logged. If this value is 1 then high severity events will be logged. If this value is 2 then all events will be logged.
- *MaxPciBus*: This value sets the highest PCI bus that the device driver will scan for PLX devices. By default it is set to 0x3.
- *MaxSglTransferSize*: This value sets the size of an internal buffer that is required for SGL and Shuttle DMA transfers. It should not be modified.
- *Start*: This value is required by the operating system and should not be modified.
- *SupportedIDs*: This value contains the Vendor Ids and Device Ids for the PLX devices that the driver supports. Users should use the PCI SDK applet DriverWizard to indirectly modify this field.
- *Type*: This value is required by the operating system and should not be modified.

2.2.3.1.4 Driver Configuration

Before using the device driver with a custom engineering board, the driver must first be configured with the appropriate Vendor ID and Device ID. PLXMon 98 has a hot-link to a PCI SDK utility called the Device Driver Wizard. This utility should be used to add or remove engineering board IDs to the appropriate device driver. It also lets you enable or disable the desired PLX device driver.

Note: If you are not using the PCI 9054 or PCI 9080 device driver you should disable it by using this utility. You must either restart your computer or restart the device driver before the settings take effect.

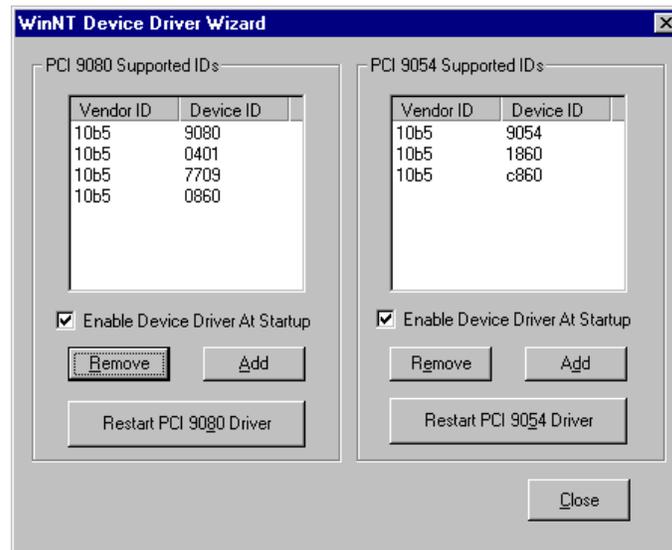


Figure 2-8 The PCI SDK Device Driver Wizard



2.2.3.2 Windows98 Device Drivers

The PCI SDK includes Windows98 device drivers for each PLX device. All device drivers are located in the <WINDOWS SYSTEM DIR>\system directory. The naming convention used for the device drivers is: Pci<DEVICETYPE>.sys. For example, the device driver for the PCI 9080 device is named Pci9080.sys.

2.2.3.2.1 Starting And Stopping

Unlike Windows NT drivers, Windows98 device drivers are started and stopped as needed by the operating system. The PLX device drivers are started when Windows98 detects a device that needs it. If, at a later time, the device is removed (by hitting the “Remove” button for a device from the Device Manager window), the device driver will be stopped unless there was another device that needs it.

There is no applet that controls the starting or stopping of a device driver.

2.2.3.2.2 Event Logging

Event logging is not accessible on Windows98.

2.2.3.2.3 Registry Configuration

Every Windows98 device driver requires an entry into the registry. The registry contains information required by the operating system as well as information required by the device driver. All device drivers are located using the registry editor under the:

HKEY_LOCAL_MACHINE\System\CurrentControlSet\Services\Class\Unknown\000X tree, where 000X is the driver number within the “Unknown” class of drivers. The PLX device driver can be found within the Unknown class by looking at the NTMPDriver value of each key, which should describe the driver name (pci9080.sys or pci9054.sys, depending on the PLX chip in use).

Note: *The registry editor should only be modified by advanced users. It is recommended that you do not change any values contained in the registry.*

2.2.3.2.4 Known Problems With The Windows98 Device Drivers.

Windows98 is not a mature operating system like Windows NT and it contains a few features that do not yet perform as expected. The following list contains some known features that affect the operation of the PCI SDK.

Scatter-Gather And Shuttle DMA

The Win98 device driver can periodically fail to transfer huge Scatter-Gather and Shuttle DMA data buffers. This affects the following PCI API functions: *PlxDmaSglTransfer()* and *PlxDmaShuttleTransfer()*. It is recommended that all data buffers used in the DMA transfers do not exceed 1 MB in size.

Changing Device Slot Numbers

If the RDK board is removed and placed into another PCI slot, Windows98 will consider the board as a “New Hardware device” and will show the “Add New Hardware Wizard”. You must

then repeat the Win98 device driver installation procedure (see section 2.1.4.2.2 for information on installing Win98 device drivers).

Using Power Management Features Of The PCI 9054

Windows98 Power Management support was not complete when the PCI SDK was released. Therefore, the method recommended by Microsoft to change the power level of a device does not work as described in the Microsoft documentation. To overcome this problem two possible methods can be used:

1. Change the PCI 9054 power level using a different method than the one recommended by Microsoft. The intended behavior can be obtained however this could cause problems in future releases of Windows98.
2. Leave the device driver sections as is, in hopes that Microsoft will correct the problem in future releases of Windows98.

The PCI SDK uses the first option in order to maintain Power Management capabilities.

2.3 Using The PCI SDK With A New Board

The following steps can be used as a guide on how to use the PCI SDK with a new board.

1. Program the desired Vendor and Device IDs into the configuration EEPROM.
2. If using Windows NT, you will need to the new Vendor and Device IDs to the Supported Device List. To add support for new IDs, use the Device Driver Wizard utility (see section 2.2.3.1.4).
3. If using Windows98, you will need to consult section 2.1.4.2.2 to register the new device with the Windows98 device drivers.
4. Edit the MiniRom application as necessary to support the new engineering board.
5. Program the board's FLASH with the modified MiniRom application binary image file.
6. PLXMon 98 can now access the engineering board's configuration EEPROM. Using PLXMon 98's EEPROM Configuration window, customize the EEPROM settings for the new engineering board and reboot the system for the changes to take effect.
7. Try accessing IOP memory by using the Direct Slave memory accesses to the engineering board.

When the following steps have been performed and are working properly, modify the IOP Board Support Package (BSP) module to begin porting the PCI SDK to the new engineering board. Consult the PCI SDK Programmer's Manual for more information on porting the PCI SDK to new engineering boards.

2.4 Using PCI SDK API Libraries With Other Operating Systems And Compilers

This version of the PCI SDK contains IOP API and PCI API libraries which are compiled to work with Windows operating systems (Windows NT and Windows98) and with the microprocessor of your RDK. By contacting PLX Customer Support, you can create new libraries to work with other operating systems and other compilers not supported by this SDK. Most libraries should be



recompilable without any errors. However with some compilers, compiler warnings or errors may arise. The following list can be used to determine some causes of warning or errors:

- Ensure that the IOP base data types for S8, U8, S16... are typecasted to the appropriate data types for the compiler used;
- If the embedded operating system/compiler supports 64 bit code ensure that the appropriate 64 bit data type is used for S64 and U64 data types; and,
- Some embedded operating systems/compiler may not provide functions that are needed by the PCI SDK. It may be necessary to recreate the operation of these functions or redirect these functions to similar functions provided by the operating system/compiler.

2.5 RTOS Support

If you are interested in developing a driver for a RTOS (Real Time Operating System), then you can use almost all of the IOP API library functions from this version of the PCI SDK. The IOP API library supplies a library of functions that can be called from within a RTOS. The RTOS code needs to call the `PlxInitApi()` function to initialize the PLX API. This completes the integration of the IOP API with your RTOS.

3. PCI SDK Software Architecture Overview

3.1 Assumptions

This section discusses some assumptions made in the design of the PCI SDK.

3.1.1 PCI SDK Assumptions

The assumptions for the PCI SDK are as follows:

- Mailbox register 0, 1, 6 and 7 are reserved for communication between PLXMon 98 and the IOP software when downloading applications.
- After starting the host device drivers, mailbox register 0 will contain the address of the PCI common buffer, and mailbox register 4 will contain the size of the buffer.

3.1.2 IOP API And IOP Software Assumptions

The assumptions for the IOP API and the IOP software are as follows:

- For the Back-End Monitor to function properly the IOP board must have one available serial port, configurable by the Board Support Package software;
- The data received by the serial port must be retrieved in a timely manner in order to eliminate any lost data;
- The initialization of the PLX chip is done by the IOP software only;
- The data expected by the application will not contain any data that could be interpreted by the Back-End Monitor as a command if they are linked in with the application;
- All IOP applications must be reentrant, cyclic and relinquish the processor periodically to avoid starvation of the Back-End Monitor (cooperative or non-preemptive multitasking);
- When an application is downloaded to the IOP RAM memory the IOP BSP must execute the *CheckPciDownloadToRam()* and the *CheckSerialDownloadToRam()* functions at microprocessor reset;
- The *BlinkLed()* function assumes that the LED is connected to the PLX chip's USERo pin; and,
- Supplied IOP Libraries are compiled for Big Endian processors only and contain no support for 64 bit processors or compilers. However, the source code does support Little Endian processors but it must be recompiled for that purpose. Please send an email to software@plxtech.com if you require support for Little Endian processors.

3.1.3 PCI API And Win32 Software Assumptions

The assumptions for the PCI API and the Win32 software are as follows:

- All Win32 applications supplied with the PCI SDK will provide full functionality to all PLX registered devices; and,



- The doorbell interrupts, QUERY_EEPROM_TYPE, DOORBELL_KERNEL_RESET, FLASH_READ, and FLASH_WRITE are reserved for PCI SDK purposes.

3.2 Overview

The PCI SDK is separated into two distinct sets of software, the IOP software that runs on the RDK board and the PCI software that runs on the Windows host system (as shown in Figure 3-1). Each API contains distinct function calls that emphasize the features of the PLX chip. Some function calls look and react similarly in both API's but may have different parameter lists.

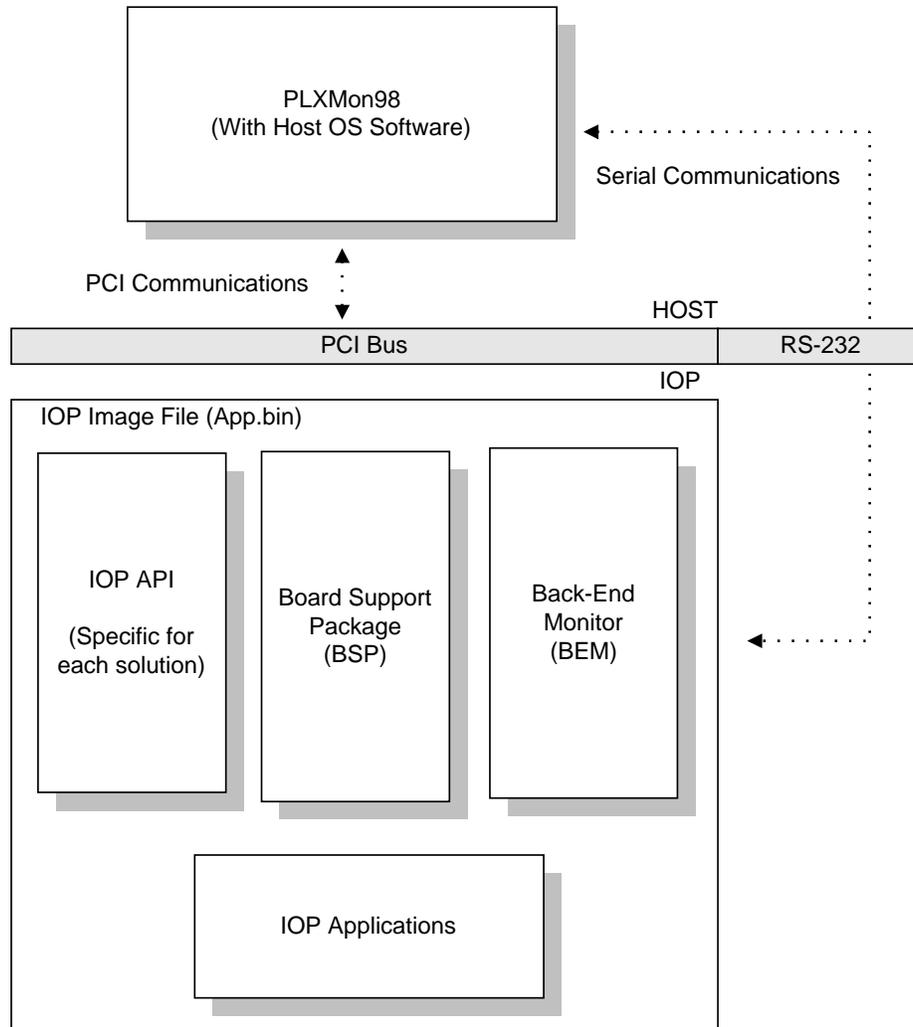


Figure 3-1 The PCI SDK Software Architecture

The IOP software contains three modules (excluding the IOP application), the IOP API library, the Board Support Package (BSP) and the Back-End Monitor (BEM). The IOP API is designed specifically for each PLX chip or for a combination of PLX chips on one RDK board. The IOP API can be customized to run on any RDK board by modifying the Board Support Package. IOP debugging can be performed with PLXMon 98 by including the Back-End Monitor into the IOP application.

The PCI software can be separated into two different packages, the Serial Communication package and the PCI Bus Communication package (see Chapter 3.5). The Serial Communication package accesses the information from the board using messages sent through the serial port of the board. This communication method requires having the Back-End Monitor included into the IOP application running on the desired RDK board.

The PCI Communication package consists of two modules, being the PCI API Dynamic Link Library (DLL) and the Windows Device Driver. PCI applications make calls to the PCI API DLL where they are translated into the appropriate device driver calls. The device driver performs the requested action and provides a response, where appropriate, to the PCI API DLL. The status of the API call is passed back to the calling application.

3.3 Software Architecture

The PCI SDK software architecture is shown in Figure 3-1. The SDK software is divided into five major components:

- PLXMon 98: this module includes the Host PCI API and device driver for PCI Bus communications, and the PLXMon 98 Communications module for serial communications to the Back-End Monitor;
- IOP API Library: this library contains the code that performs the API functions and accesses the PLX chip. There are two IOP APIs for each PCI device: Release and Debug. Both libraries are the same except the release version eliminates many of the parameter validation steps that are performed in the debug version, and hence performance is increased when using the release version of the API. All debug libraries contain a 'd' suffix in their name (E.G. api860d.a). Release libraries do not contain the 'd' suffix in their name (E.G. api860.a).
- BSP Module: this module contains all board specific code, including the IOP bus memory map, the board and microprocessor initialization routines and the interrupt service routine for the PLX chip;
- Back-End Monitor: this module provides a monitor for debugging IOP applications which supports PLXMon 98 through the serial port; and,
- IOP Applications: this module contains the main application for the RDK board and the IOP.

3.4 IOP Software Architecture

The IOP software architecture is separated into four modules, being:

- The Board Support Package (BSP);
- The IOP API library;
- The Back-End Monitor (BEM); and,
- The IOP application software.

The PCI SDK software architecture is shown in Figure 3-2.

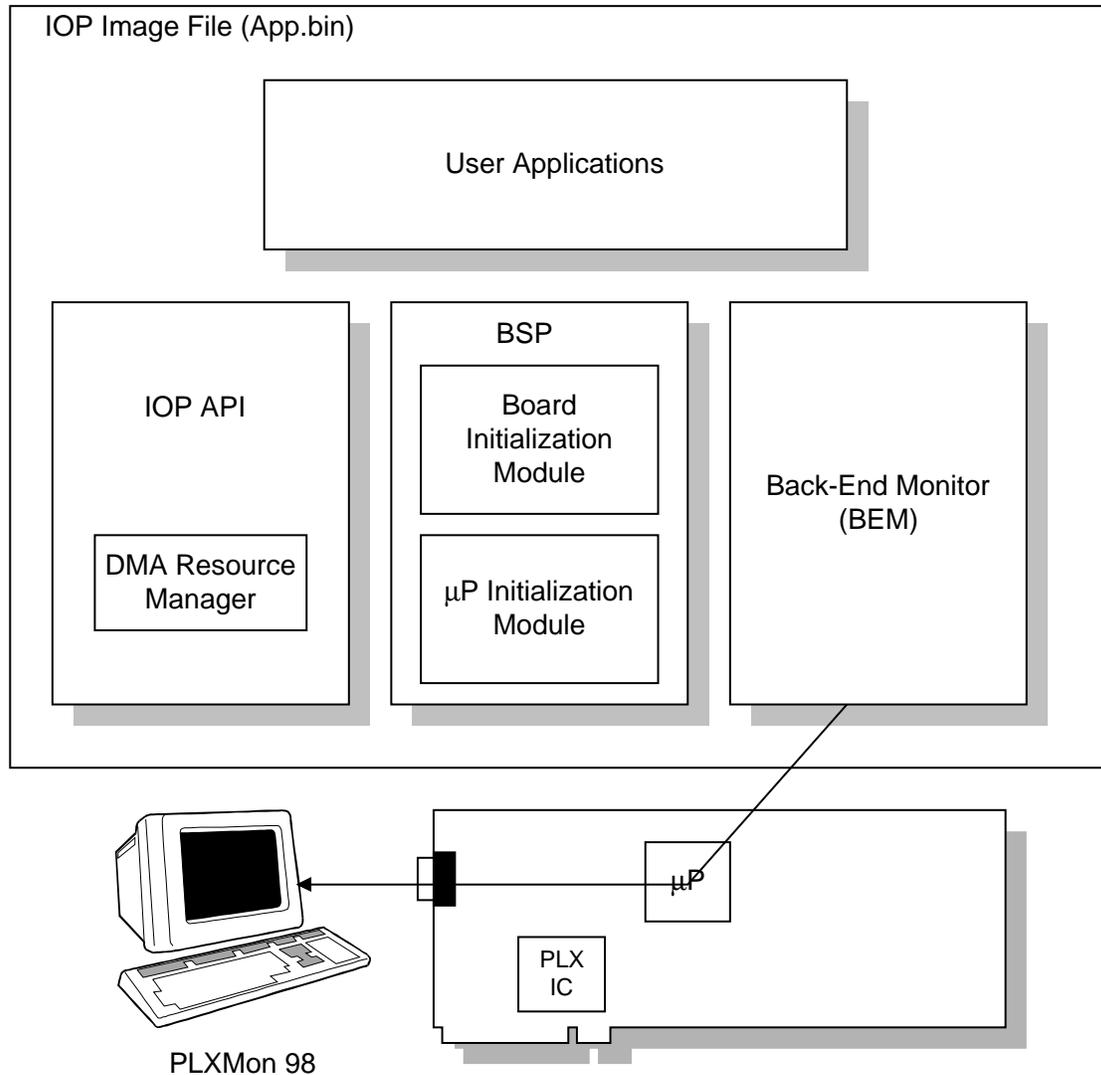


Figure 3-2 The IOP Software Architecture

3.4.1 Board Support Package (BSP)

The Board Support Package (BSP) contains all the information needed by the IOP API that is specific to the board. This module provides the necessary entry points needed to port the PCI SDK to new platforms. The BSP is composed of two main sub-modules, being:

- The Microprocessor Initialization module; and,
- The Board Initialization module.

Note: Prior to porting the PCI SDK to new boards an understanding of the BSP and its functionality should be acquired.

3.4.1.1 Microprocessor Initialization Module

The microprocessor initialization module contains all the necessary information about the microprocessor required by the IOP API. Some of the information contained within this module are the microprocessor boot code, the main default interrupt service routine (ISR) for the PCI SDK and the default PLX chip interrupt trigger support functions.

3.4.1.1.1 Microprocessor Boot Code

When the board is powered up, the microprocessor starts executing the boot code. This code initializes the microprocessor, configures the memory controller, copies data and code (if necessary for performance reasons) from the boot FLASH to RAM memory and brings the microprocessor to a ready state. The sequence of events is as follows:

1. The board is powered on.
2. The microprocessor begins at the reset address where it immediately jumps to the boot code.
3. The boot code configures the memory controller.
4. The data section and the code section (if necessary) of the boot application is copied to RAM memory.
5. The exception vector table is initialized.
6. Any other microprocessor specific initialization is done, such as configuring the endian registers, configuring the clock (if internal clocks are available), setting up any peripheral units internal to the microprocessor.
7. Once the microprocessor is initialized and is ready to run, the boot code jumps to the board initialization routine (see section 3.4.1.2).

Note: The MiniRom application included in the PCI SDK provides a good starting point for users who have untested engineering boards. The application is limited in features and functionality and should be the basis for porting the PCI SDK to new engineering boards (see section 3.4.5.2 for more information).

3.4.1.1.2 Interrupt Service Routine

The interrupt service routine (ISR) provided in the BSP controls all interrupts generated by any PLX chip. The ISR is divided into one main routine with one function to service each interrupt trigger on the chip. When an interrupt is generated, the main ISR determines the interrupt trigger and calls the appropriate interrupt trigger service routine to service the interrupt.

This method allows modification of individual interrupt trigger service routines or modification of the main interrupt service routine to customize the handling of interrupts for each application.

3.4.1.2 Board Initialization Module

The Board Initialization module contains information on the features of the board and the board initialization routine. Some of the information it provides includes the memory map of the IOP bus, specifically where the following devices are located in memory:

- SRAM address and range;
- DRAM address and range;



- SDRAM address and range;
- PLX chip Register Base address;
- UART ports (Control/Status, Data);
- Flash Memory address and range;
- Direct Master Memory Remap address and range;
- Direct Master I/O Remap address and range; and,
- Boot address.

The PCI SDK needs to know the endianness for each memory region. If the IOP bus is less than 32 bits wide, the PCI SDK needs to know how the IOP bus is connected to the PLX chip (specifically which bytes and byte lanes are used by the IOP bus).

The Back-End Monitor needs to know about the UART. The necessary UART ISRs and serial communication functions are included in this module.

3.4.1.2.1 Board Initialization Routine

The board initialization routine contains the necessary API functions to configure and initialize the PLX chip, the IOP API library, the Back-End Monitor and any other device on the RDK board. This function is called from the microprocessor initialization routine (the microprocessor boot code, see section 3.4.1.1.1) at start up. The board initialization sequence is as follows:

1. Initialize the PLX chip. A list of IOP API initialization functions is provided with each of its parameters set to the PLX chip's default values (set by calling the *PlxInitApi()* function).
2. Change the default values for the parameters as necessary before calling the respective IOP API initialization function.
3. Set the Local Init Status bit when the PLX chip is initialized (this asserts the NB# pin low). This bit allows the PCI BIOS to access the PLX chip. Once the PCI BIOS has assigned the appropriate values to the PLX chip's configuration registers, the PLX chip is completely initialized and is ready to run.
4. Initialize the different debugging levels of the Back-End Monitor with the necessary board specific information.
5. Initialize any other peripheral on the board.
6. Connect the ISRs to the appropriate interrupt lines of the microprocessor.
7. Initialize the application, if necessary, once all devices on the RDK board have been initialized and are operational.
8. Jump to the main application routine.

3.4.1.3 The Main() And AppMain() Functions

The BSP Library contains the *main()* function for any application using the PCI SDK. This function controls the operation of the IOP API. The function starts by initializing the microprocessor and its peripherals, the PLX chip (when there is no EEPROM connected to it), the UART chip, and the Back-End Monitor (when in use). The function proceeds to test the available memory on board and begins the main application section.

The main application section consists of a loop that allows execution of several tasks on a round-robin priority scheme. Each task is allowed as much time as it needs to run (non-preemptive and no priority levels). This loop runs without interruption in a cyclic fashion and therefore all the tasks must eventually return (tasks must be reentrant).

The Back-End Monitor can be used to filter the stream of data, supplied by the UART Services functions, to help in debugging new applications. The UART Services functions receive a stream of data from the RS-232 port on the RDK board and buffer it. This stream can be received by any task requiring data from the serial port.

The Back-End Monitor, *BemL1()*, does simple debugging. This monitor task is used with PLXMon 98's serial debugger support turned on. The *BemL1()* monitor task only accepts three commands, read and write to an IOP memory location, and a board reset command.

With the stream of data received from the serial port (see Figure 3-3), the *BemL1()* task receives and parses through it, searching for commands. When *BemL1()* finds a command that it recognizes, the monitor removes the command from the stream, reacts accordingly to the command and returns a response when appropriate. Once the stream of data has been completely parsed and all *BemL1()* commands have been removed from it the filtered stream is made available to the next task wishing data from the serial port. The filtered data stream is received by the application, *AppMain()*.

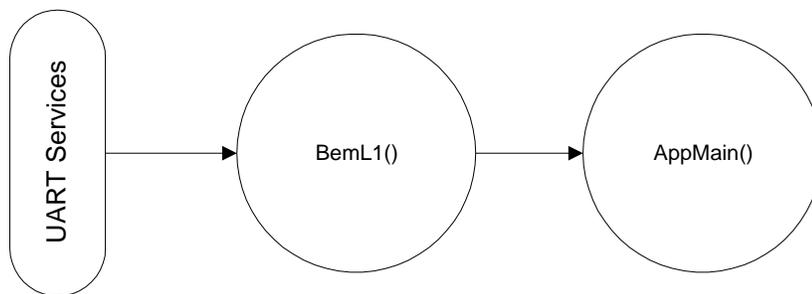


Figure 3-3 The Data Stream Flow Diagram.

The filtering of the data stream can be bypassed by a task at any point in time by calling the UART Services functions. An example of this feature is when a task starts an application download to memory. The application binary file being downloaded may contain data that looks similar to a command for the *BemL1()* task. If the *BemL1()* task is retrieving the data from the UART Services functions then some information about the application will be lost. Therefore, while the task downloads an application, it calls directly *PlxGetChars()* to retrieve the unfiltered data from the UART chip until the application is completely downloaded. Once the download is complete, the task returns control to the BSP Module's main loop to allow other tasks to run.

This feature should be used with caution however because it directly affects the operation of the other tasks dependant on the data stream coming from the serial port. When an application requests unfiltered data the task calls *PlxGetChars()* function and this function returns an unfiltered data stream. This task should not return to the main loop (within the BSP Module) to continue processing of debug commands until all the necessary unfiltered data has been received by the application. By doing this the Back-End Monitor task will not scan through the data and remove command data from the stream that was not intended to be a command for the debug monitors.



3.4.2 IOP API Library

The IOP API library contains the code for all the documented API functions. This code is standard for all IOP applications and is independent of the board configuration. The code directly calls the PLX chip (no intermediary functions).

There are two IOP APIs for each PCI device: Release and Debug. Both libraries are the same except the release version eliminates many of the parameter validation steps that are performed in the debug version, and hence performance is increased when using the release version of the API. All debug libraries contain a 'd' suffix in their name (E.G. api860d.a). Release libraries do not contain the 'd' suffix in their name (E.G. api860.a).

Note: Each PLX chip has its own IOP API library specifically designed to complement its features. To implement more than one PLX chip on one board, a new library must be created. This library would combine the features of each chip and have new functions to accent the features achieved by grouping the PLX chips.

3.4.2.1 DMA Resource Manager

The IOP API supports three different DMA (Direct Memory Access) transfer types and manages the DMA resources. The supported DMA transfer types are:

- Scatter-Gather DMA: Transfers data using Scatter-Gather Lists (SGL) and can transfer several blocks of data at a time (formally called chaining DMA);
- Block DMA: Transfers data one block at a time; and,
- Shuttle DMA: a circular Scatter-Gather DMA transfer.

The Scatter-Gather DMA transfer is most commonly used of all DMA transfers. This method supports DMA transfers where either the source or destination memory locations are not contiguous (this is common with most operating system memory allocation) the best. By grouping multiple DMA transfer requests, the IOP application is interrupted less often providing improved performance.

The Block DMA transfer is used primarily for single DMA transfers and where the number of transfer requests is small.

The Shuttle DMA Transfer is best used when the data transfers are repetitive (where the source and destination locations remain relatively constant but the transfer direction may switch or the transfer size is different).

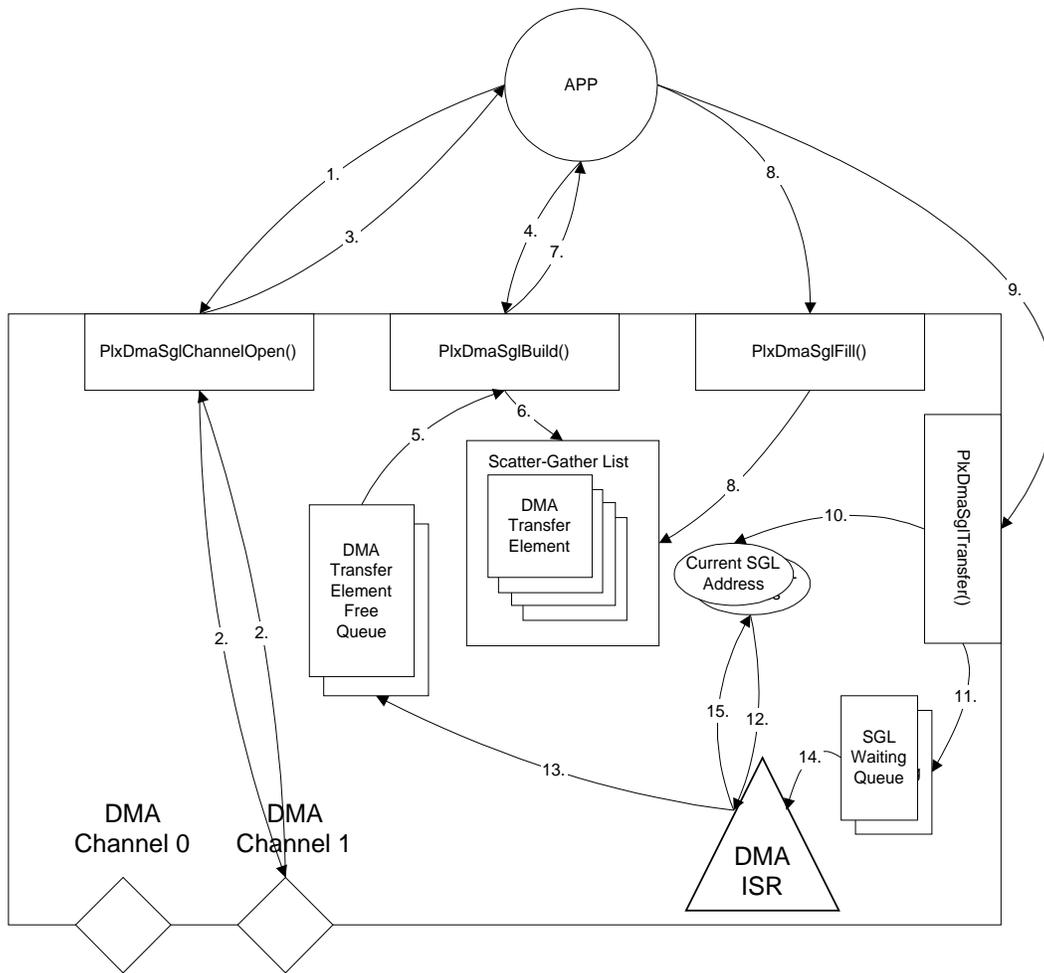


Figure 3-4 Scatter-Gather DMA Flow Diagram

Scatter-Gather DMA Transfers

In Scatter-Gather DMA transfers (see Figure 3-4), a SGL DMA channel is opened (steps 1-2). With a successful return (step 3), a Scatter-Gather List (SGL) is acquired from the DMA resource manager (steps 4-6) by calling `PlxDmaSglBuild()` and a handle to a list of DMA transfer element addresses is returned (step 7). The DMA transfer elements are programmed with the appropriate source and destination data addresses, the transfer size and the DMA transfer descriptors by calling `PlxDmaSglFill()` (step 8). The SGL is passed to the `PlxDmaSglTransfer()` function (step 9). If there is not a SGL currently executing on the DMA channel, this function programs the list address into the DMA descriptor register for the opened DMA channel and also into the Current SGL Address buffer (one buffer for each DMA channel), and the DMA transfer is started (step 10). If there is a SGL executing then this function places the SGL address into the SGL Waiting Queue (one queue for each DMA channel) (step 11). When the SGL currently executing is completed the ISR reads the Current SGL Address buffer (step 12) and frees the DMA transfer elements for this SGL to the DMA Transfer Element Free Queue (one queue for each DMA channel) (step 13). The ISR then removes all the current SGL entries in the SGL Waiting Queue and joins them together (step 14). The new SGL address is placed into the Current SGL Address buffer and it is placed and started on the DMA Channel (step 15).

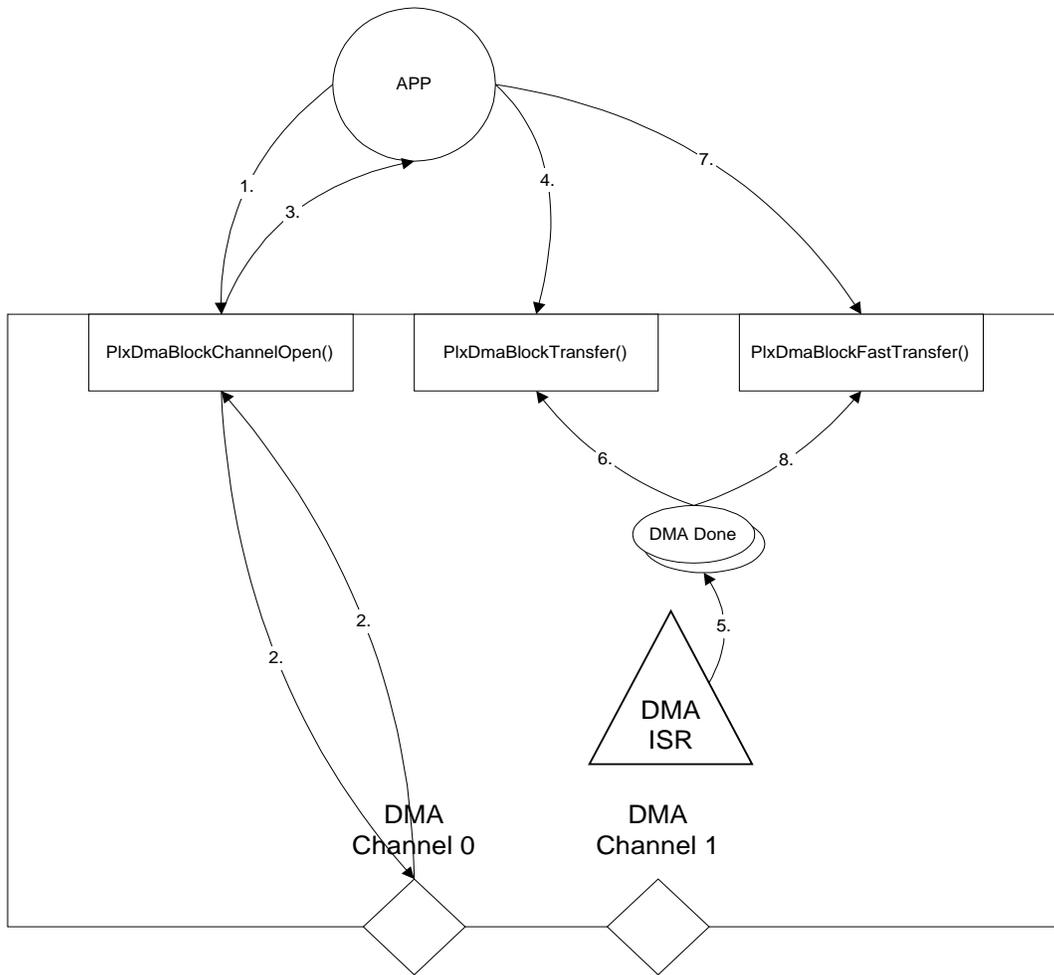


Figure 3-5 Block DMA Transfer Flow Diagram

Block DMA Transfers

In Block DMA transfers (see Figure 3-5), a Block DMA channel is opened (steps 1-2). With a successful return (step 3), the `PlxDmaBlockTransfer()` function is called with the appropriate source and destination data addresses, the transfer size and the DMA transfer descriptor (step 4). This function checks the status of the DMA channel to determine if there is a transfer in progress by checking the DMA Done flag. If there is a transfer in progress then the function returns the “In Progress” error code. Otherwise the DMA data is programmed into the DMA registers for the DMA channel and the transfer is started. When the transfer is completed, the ISR will set the DMA Done flag (step 5). If the `PlxDmaBlockTransfer()` function is set to not return immediately then this function polls the DMA Done flag (step 6) and when the flag is set the function will return. The `PlxDmaBlockTransferRestart()` function is used to quickly restart a Block DMA transfer that was pre-programmed with the `PlxDmaBlockTransfer()` function (step 7). The only parameter needed is the transfer size. All other DMA information is reused from the previous transfer. This function also supplies an immediate return feature where, when the parameter is set to FALSE, the function polls the DMA Done flag (step 8) until it is set then returns.

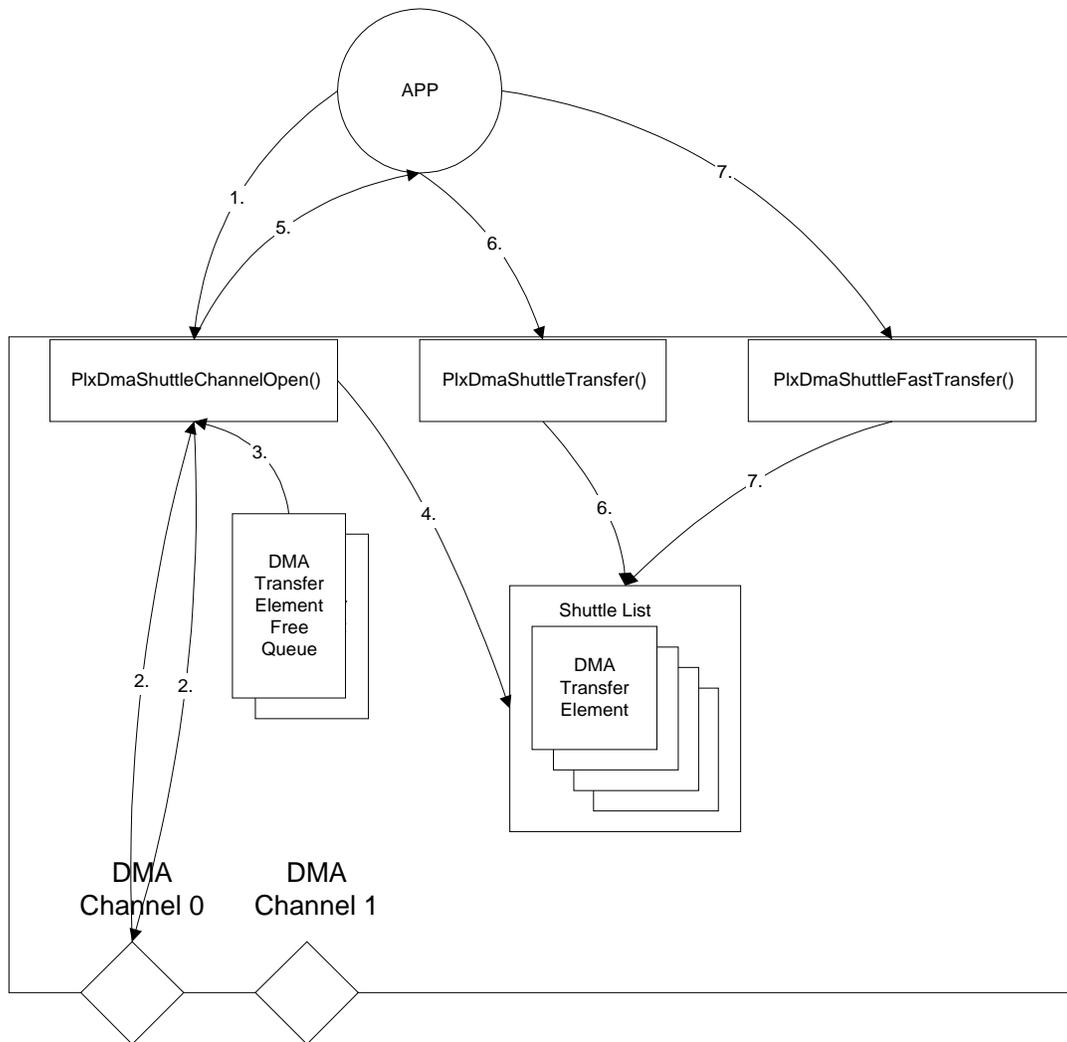


Figure 3-6 The Shuttle DMA Flow Diagram

Shuttle DMA Transfers

In Shuttle DMA transfers (see Figure 3-6), a Shuttle DMA Engine is started by opening a Shuttle DMA channel (steps 1-2). A number of DMA transfer elements are acquired from the DMA resource manager (step 3). The DMA transfer elements are linked to create a Shuttle List (step 4). This Shuttle List is placed on the opened DMA channel and is started thereby starting the Shuttle DMA Engine. A list of the DMA transfer element addresses is returned to the application (step 5). From this point, each DMA transfer element of the Shuttle List can be treated as a unique DMA channel. To start a transfer, the *PldmaShuttleTransfer()* function is called with the appropriate source and destination data addresses, the transfer size and the DMA transfer descriptors (step 6). This function checks the status of the Shuttle DMA channel to determine if there is a transfer in progress by checking the transfer size for the given DMA transfer element. If there is a transfer in progress then the function returns the “In Progress” error code. Otherwise the DMA data is programmed into the DMA transfer element provided by the application and the transfer is started. When the transfer is completed the PLX chip (through the PLX DMA Descriptor Write Back Feature) sets the transfer size for the completed DMA transfer element to zero. If the



PlxDmaShuttleTransfer() function is set for blocking then this function will poll the DMA transfer element's transfer size and when the size is set to zero the function will return. The *PlxDmaShuttleTransferRestart()* function is used to quickly restart a Block DMA transfer that was pre-programmed with the *PlxDmaShuttleTransfer()* function (step 7). The only parameter needed is the transfer size. All other DMA information is reused from the previous transfer. This function also supplies a blocking feature where it polls the DMA transfer element's transfer size until it is set to zero.

3.4.3 Back-End Monitor

The Back-End Monitor (BEM) provides features that help in the debugging of IOP applications. The monitor supports PLXMon 98 serial command passing to the IOP application from the serial port of the RDK board. This monitor only supports three commands, reading and writing to IOP memory locations (these commands support different data sizes) and reset the IOP software. These commands provide a generic interface for any application. PLXMon 98 uses this monitor to retrieve data from the IOP. In normal operation, this monitor accesses the UART Services functions to get a stream of data that has been received by the UART chip. The monitor extracts commands (that the monitor recognizes) from the data stream, performs the necessary action and provides a response when appropriate. This monitor provides the filtered data stream to the next task requiring serial data in the daisy chain.

There are times when a task may not want other tasks to extract data (or commands) from the data stream. Accessing the UART support functions directly can do this. A task wishing to receive raw data, bypasses the previous task in the daisy chain and calls *PlxGetChars()* to retrieve an unfiltered data stream. If a task chooses to access the unfiltered data stream it should take all the data necessary to perform the action and, only once the action is complete, return control back to the main routine (contained within the BSP).

The next application in the daisy chain, if required, retrieves the filtered data stream from the BEM monitor. The application can do whatever it needs to do with the data. The application can choose to provide a filtered stream of data from what is left over from its parsing of the data stream so that the data stream can be passed down to the next task in the chain.

3.4.3.1 Back-End Monitor Serial Protocol

The Back-End Monitor (BEM) can recognize three different commands coming from PlxMon98: reset the IOP microprocessor; read a memory location and write to a memory location. They all use a serial protocol that is discussed in the following sections.

Some commands use parameters. Parameters listed are normally necessary for the command except when a parameter is within square braces ('[' and ']'). These parameters are optional to the command.

Parameters listed with the vertical bar ('|') indicate that "one or the other" parameter must be provided, but not both.

Carriage returns are noted as <ENTER>.

Note that all commands should be lowercase. The Back-End Monitor does not recognize uppercase commands except in hexadecimal value parameters.

3.4.3.1.1 Reset IOP Microprocessor Command

Syntax:

~plx!

Response from the BEM:

No response

3.4.3.1.2 IOP Memory Read Command

Syntax:

~plxr[b|w|l|d] address<ENTER>

Parameter	Description
address	Address of the memory location to read. The address must be a hexadecimal number such as f0000.

Response from the BEM:

~plx value<ENTER>

Parameter	Description
value	Value read at the selected memory location. The format is a hexadecimal number preceded by "0x", such as "0x7fff".

Description:

This command reads an 8 bit byte (b), a 16 bit word (w), a 32 bit double word (d) or a 64 bits long double word (l) at the specified address and returns the value read.

3.4.3.1.3 IOP Memory Write Command

Syntax:

~plxw[b|w|d|l] address value<ENTER>

Parameter	Description
address	Address of the memory location to write to. The format must be a hexadecimal number such as "f0000".
value	Value to write at the memory location. The format of the value must be a hexadecimal number such as "905410b5".

Response from the BEM:

No response

Description:

This command writes an 8 bit byte (b), a 16 bit word (w), a 32 bit double word (d) or a 64 bit long double word (l) at the specified address.



3.4.4 Methods For Debugging IOP Applications

The PCI SDK supports two methods for debugging IOP applications, being:

- Win32 Debugging: Using PLXMon 98. This method assumes that there is no IOP application running on the RDK board. With newer RDK boards, this method provides the preliminary debugging and validation of new RDK boards.
- PLXMon 98 with the BEM: With the BEM linked into the IOP application, PLXMon 98 can communicate to the RDK board through the PC's COM port to the serial port on the RDK board. PLXMon 98 can be setup to communicate to the RDK board or IOP application using either the serial port or the PCI bus.

3.4.4.1 Operation Of The Back-End Monitor In A System

This section describes how the BEM can be used on an RDK board and how it affects system performance.

The Back-End Monitor combinations are as follows:

1. *AppMain()* only: the IOP application is running without any BEM tasks; and,
2. *BemL1()* and *AppMain()*: the IOP application is running with BEM debugger.

Method 1: This method is used once the application has been fully tested and is working properly. There is no monitor tasks running so this method provides the best performance for the application. PLXMon 98 can be used to debug the application if the RDK board is inserted into a free slot in the host system's PCI Bus and PLXMon 98's PCI Communication is turned on.

Method 2: PLXMon 98 is used to debug the application through the serial port. IOP application performance will be affected using this method because the BEM monitor is processing commands and copy data to and from different memory buffers. There is a possibility of lost data destined for the IOP application. If IOP application data matches BEM commands, the monitor will remove them from the serial data stream. When the IOP application requires data that could be captured by the monitor, the IOP application should access the UART Services module directly, bypassing the monitor (done by calling *PlxGetChars()*).

3.4.5 IOP Applications

All IOP applications are connected to the IOP API, the BSP and the Back-End Monitor to create the binary image. This image is then programmed into FLASH memory, or downloaded to RAM memory and executed.

All IOP applications have an *AppMain()* function which is the main application function. The *main()* function is kept within the BSP module. This limitation is imposed on all applications because of how the Back-End Monitor (BEM) is implemented. The BEM needs to run periodically to operate properly. Since there can only be one execution thread running at one time, a cyclic thread is created using the *main()* function. This thread loops forever calling the BEM and then the main application function sequentially (cooperative multitasking or non-preemptive multitasking). The *AppMain()* function should be cyclic in nature and should return control periodically back to the *main()* function.

3.4.5.1 IOP Memory And IOP Applications

IOP applications running in ROM or in RAM use memory in different ways. When an IOP application is running in ROM the application contains all the modules it needs, such as the Back-End Monitor. A ROM application contains:

- The main IOP application module;
- The IOP API;
- The BSP module; and,
- The Back-End Monitor (debug version of ROM application).

Figure 3-7 shows how the ROM application uses memory.

IOP RAM applications are built differently from IOP ROM applications. The IOP RAM applications look very similar to IOP ROM applications from a source code point of view but they differ when the IOP RAM application is linked to the libraries. IOP RAM type applications borrow the Back-End Monitor from the resident IOP ROM application. The size of IOP RAM applications is normally smaller because a lot of the code used by the IOP RAM application resides in the IOP ROM application. Therefore the IOP ROM application on the RDK board must have the modules needed for the IOP RAM application and the IOP ROM application must provide the links to those modules. The BSP provided with the PCI SDK contains the links for IOP RAM based applications.

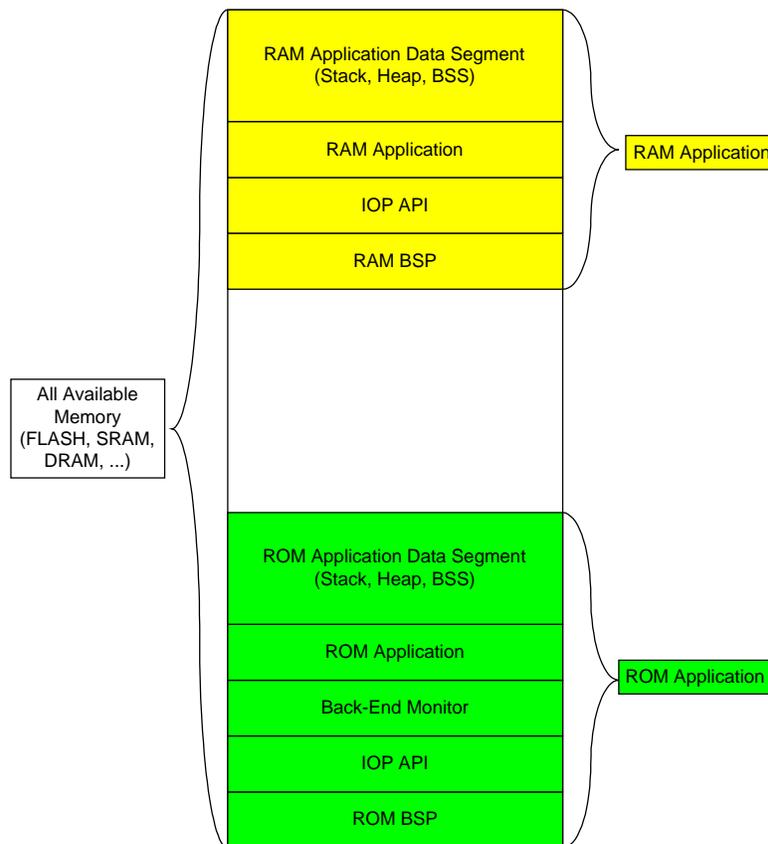


Figure 3-7 IOP Memory Diagram



3.4.5.2 MiniRom Application

MiniRom is included in the PCI SDK to provide a good starting point for users who have an untested engineering board and for this reason, it is limited in features and functionality. It provides bare minimum boot up code for most engineering boards. This application configures the microprocessor, the PLX chip, and proceeds to blink the LED that is connected to one of the PLX chip's USER pins. To use the MiniRom application, program the binary image into the FLASH using a FLASH chip programmer. Once the FLASH is programmed reboot the engineering board, and if the LED blinks then the MiniRom application configured the engineering board properly. If this test is successful, the FLASH can be reprogrammed with the PCI SDK HelloWorld image (supplied with the PCI SDK).

Note: This IOP ROM application is provided as a bare bones IOP ROM application useful for confirming the functionality of new engineering boards. It does not contain any PCI SDK features that are described in any PCI SDK manual.

3.4.6 Porting The PCI SDK To New Platforms

All information needed to port the PCI SDK to new platforms is contained within the BSP module. Some of the information contained within the BSP includes:

- The memory map of the IOP bus;
- The microprocessor boot code;
- The PLX chip interrupt service routine;
- The UART interrupt service routine;
- The board initialization routine; and,
- The board and/or application specific controls for the IOP API and the Back-End Monitor.

The IOP API and the Back-End Monitor need to know where certain devices are located on the IOP bus, such as the PLX chip, DRAM, SRAM and the UART. These values need to be updated when creating an application for new boards.

When the microprocessor is changed on a board, the microprocessor boot code must be modified to support the new microprocessor. This boot code is provided within the BSP module.

Most interrupt service routines are customized to the application. To customize the PCI ISR for an application, either modify the interrupt trigger service routines or modify the main ISR.

The Back-End Monitor relies on the UART ISR to send and receive data from the serial port. Modify the UART ISR to support the UART on the board.

To initialize the PLX chip modify the parameters for the IOP API initialization functions contained within the board initialization routine.

Within the BSP, there is some control parameters for the IOP API and the Back-End Monitor that can be modified to improve performance of the PCI SDK. These parameters are platform and application dependent and can affect the operation of the application differently on different systems.

3.4.7 Support For Multiple PLX chips On One Board

Each PLX chip has its own IOP API library. When two or more chips are present on one engineering board, a new IOP API library must be created. This library will contain the normal API functions (defined in this document) and some new or modified functions that represent new features made available by combining the features of the multiple chips. Some multiple chip libraries will be available (for the more popular implementations), however it will be up to the designer to create his/her own library for multi-chip combinations not currently supported.

3.5 Host Win32 Software Architecture

This section describes the Win32 software provided in the PCI SDK.

3.5.1 PLXMon 98

PLXMon 98 can communicate with PCI devices via two different paths (see Figure 3-8):

- Direct Serial Communications;
- Host API/Device Driver Interface.

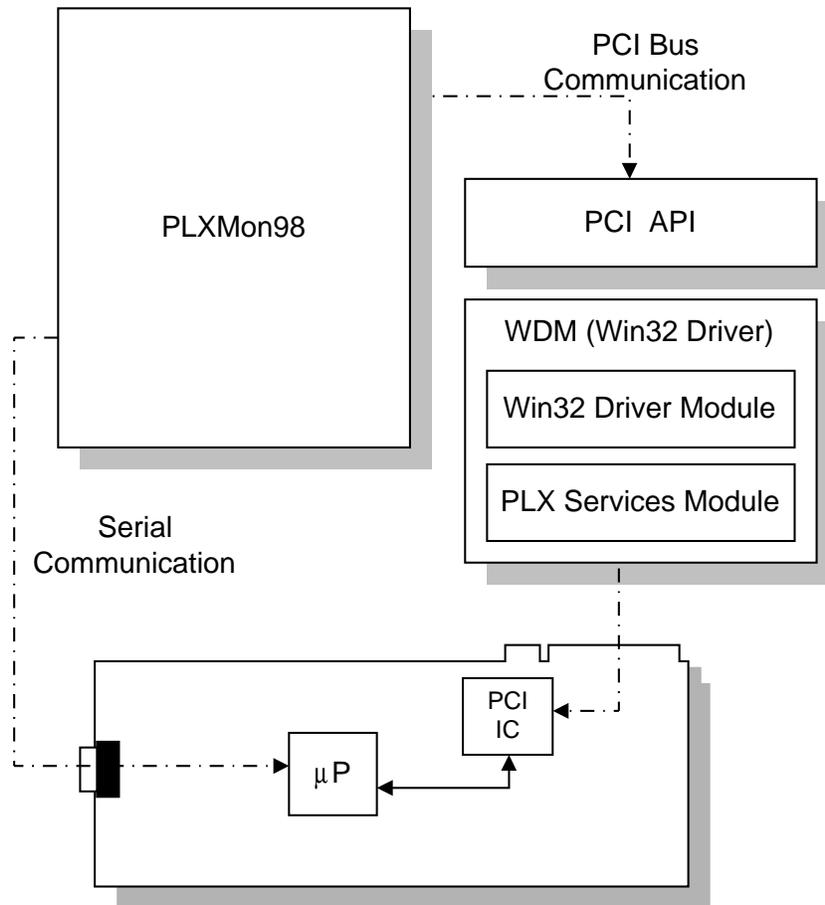


Figure 3-8 The Host Software Architecture



3.5.1.1 Serial Communication

This method of communicating with a PLX RDK board is mainly used for debugging purposes. While a custom host Win32 device driver is being created, it is helpful to be able to read and write values directly to and from the RDK board.

If PLXMon 98 is set to serial mode, it calls functions that reside in the PLXMon 98 Communications Module. It is the responsibility of the PLXMon 98 Communications Module code to convert the valid PLXMon 98 commands into a serial data stream. The protocol used in passing the data is based on an ASCII translation scheme (for more information on the serial protocol, see section 3.4.3.1). This stream of data is sent to the IOP application. The Win32 operating system provides a device driver to control the serial port. The Win32 SDK provides services to access this device driver.

When the data arrives, the RDK board's microprocessor must have a means of handling the incoming data. The Back-End Monitor contains functions that are hooked via an interrupt, so when data does arrive, they are called (when the UART generates an interrupt) to retrieve the data from the UART. The Back-End Monitor decodes the command and data, and acts on the command and returns a reply. If the data received by the Back-End Monitor is not a command the data is queued for the IOP application.

3.5.1.2 PCI API/Device Driver Communication

PCI Bus Communication is performed using the PCI API DLL and the Win32 device driver supplied with the PCI SDK.

3.5.1.2.1 PCI API Library

The PCI API consists of a library of functions, from which multiple PCI RDK boards can be accessed and used. The PCI API provides API function groups, which manage the features of each PLX chip. Groups such as DMA access, direct data transfers, and interrupt handling contain functions that can be universal to any PCI RDK board.

The PLXMon 98 application makes extensive use of the PCI API functions. For the most part, the PCI API's purpose is to translate application functions calls and send them to the appropriate device driver. The only functionality present in the PCI API is to manage the various device drivers. This includes opening, closing and searching for devices that are present on the PCI bus.

3.5.1.2.2 Win32 Device Driver

The device driver's role in the system is to store device data within the kernel and to execute the commands given to it from the PCI API. The device driver can be used as a framework to create custom software for managing PCI devices as well.

The Win32 Driver Model (WDM) is a new platform for developing device drivers on the Windows98/NT 5.0 operating systems. It is very similar in device driver architecture to that of Windows NT 4.0 and allows the creation of one device driver that can be used for both operating systems without any porting or modifications.

The architecture of the device driver is designed to reduce the time needed to create a new device driver for customer boards that contain a PLX device. By modifying the source code provided for the device driver, a new custom device driver can be created in minimal time.

3.5.2 Win32 Applications And The PCI SDK

All Win32 applications connect to and use the PCI API DLL. The Win32 application can communicate to any PCI device with a PLX chip by using the PCI API DLL. Each Win32 application can be created like any other Windows application. For more information on creating a Win32 application using the PCI API DLL, see the PCI SDK Programmer's Manual.

3.5.3 Win32 Device Driver Overview

This section describes the overall layout and concept of a PLX device driver. To accommodate the need for one common PCI API as well as to reduce development time for device driver design for new engineering boards, the following device driver model was created.

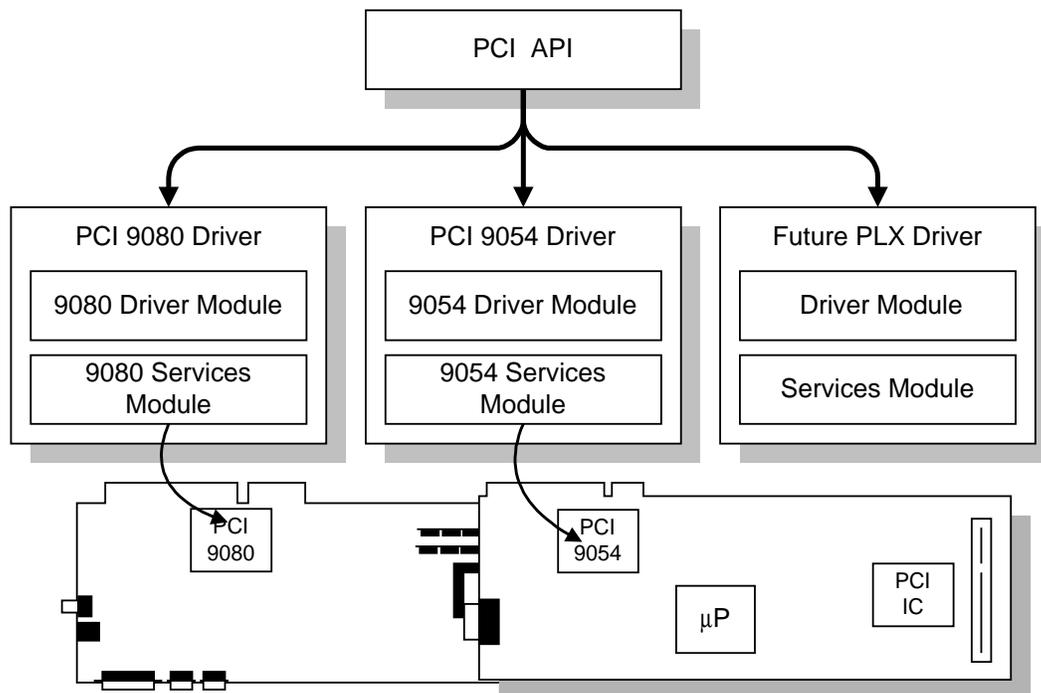


Figure 3-9 The PLX Device Driver Layout

One device driver handles each type of PLX chip, as seen in Figure 3-9. Each device driver communicates with the PCI API on a one-to-one basis; there is no device driver inter-communication. If a new device driver is developed and added to the system, it can be integrated simply by installing it into the Win32 operating system. If more than one PLX chip is present on an engineering board, the device driver can only see the one that is directly connected to the primary PCI bus. All PCI API functions will access this PLX chip only.

3.5.3.1 PLX Chip Device Driver Module

This module provides the management of the PCI RDK boards in Windows NT/98. This management includes storing device specific information, processing PCI API and system messages, handling interrupts, and allocating resources for each RDK board. Some non-PLX specific functionality is handled in this module, such as reading from and writing to PCI configuration registers.



3.5.3.2 PLX Chip Services Module

This module has access to the entire register set of the PLX chip, and thus is in charge of providing the functionality for the device driver.

3.5.4 Creating A New Driver

This section briefly covers how a new device driver can be created using the existing device driver as a template. When a new PLX chip Services Module, which provides the real functionality for the device driver, is updated to support a new PLX chip, the old PLX chip Services Module is replaced. The new PLX chip Services Module would reflect the new register set of the PLX chip and would support the existing PCI API by accessing the appropriate registers on the new PLX chip based on the PCI API function requested.

The PLX chip Device Driver Module would need little modification to create a new PCI device driver. If new API functions are created, the handling of those functions would force the modification this module to support the new functions.

3.5.5 Device Driver Features

The Win32 device driver supports the sharing of interrupts between many PLX RDK boards. The device driver uses one interrupt line on the PCI bus that all PLX RDK boards share to interrupt the host PC. The interrupt service routine determines which board caused the interrupt and services that board's interrupt.

The device driver supports event logging into the system log file. When the device driver determines an error in operation, it updates the system event log file with the appropriate information concerning the cause of the error. This log file can be used to debug the device driver when the device driver is started at boot time. This file contains the reasons why the device driver was not loaded and started.

Appendix A. RDK Software Quick Reference

The information below should be used as a guide to the PCI SDK software requirements for each PLX RDK board.

PCI 9054RDK-860:

The table below describes the memory requirements of the PCI SDK for the PCI 9054RDK-860.

Item	PCI 9054RDK-860
SDRAM Address	0x0000 0000 -> 0x01FF FFFF (32MB)
FLASH Type	AT49LV040(default as shipped) AM29F040 also supported in software
FLASH Address	0xFFFF0 0000 -> 0xFFFF7 FFFF (512KB)
FLASH Image Base Address	0x0000 0000
Memory space used by ROM code	0x0000 0000 -> 0x0003 FFFF
Memory space used by RAM code (PCI SDK Samples)	0x0004 0000 -> 0x0007 FFFF
Direct Master to PCI memory space Address	0x4000 0000 -> 0x40FF FFFF (16MB)
Direct Master to PCI IO space Address	0x5000 0000 -> 0x50FF FFFF (16MB)
PCI 9054 Register Address	0x3000 0000 -> 0x3000 01FF
Memory space recommend for user's use.	0x0008 0000 -> 0x01FF FFFF (31.5MB)

User's who have upgraded the PCI SDK and intend to use it with an existing PLX RDK, must first reprogram the configuration EEPROM connected to the PLX chip. Skipping this step can cause unpredictable behavior of the PCI SDK. If you have purchased the PCI SDK with a PLX RDK then there is no need to upgrade the EEPROM because it was programmed at the factory before shipping. The following diagram shows the default settings for the RDK.

Displaying 93CS56 EEPROM values

PCI Configuration Registers

Device ID (00h)	1860	Vendor ID (02h)	10B5	Hot Swap Control (4Ah)	00004C06
Subsystem ID (2Ch)	9054	Sub Vendor ID (2Eh)	10B5	Interrupt Line (08h)	01
Revision (08h)	01	Class Code (09h)	068000	Interrupt Pin (3Dh)	00
		Min_Gnt (09h)	00	Max_Lat (3Fh)	00

Local Configuration Registers

Range for PCI to Local Address Space 0 (00h)	FF000000	Local Base Address for Direct Master to PCI Memory (20h)	40000000
Remap for PCI to Local Address Space 0 (04h)	00000001	Local Bus Address for Direct Master to PCI ID/CFG (24h)	50000000
Local Arbitration Register (08h)	0101000C ->	PCI Base Address (Remap) for Direct Master to PCI (28h)	00000003 ->
Local Bus Big/Little Endian Descriptor Rgr (0Ch)	00305524 ->	PCI Config. Addr. Reg. for Direct Master to PCI/CFG (2Ch)	00000000 ->
Range for PCI to Local Expansion ROM (10h)	00000000	Range for PCI to Local Address Space 1 (1MB) (F0h)	FF000000
Remap for PCI to Local Expansion ROM (14h)	00000010	Remap for PCI to Local Address Space 1 (F4h)	00000001
Bus Region Descriptor for PCI to Local Access (18h)	8B430043 ->	Local Space1 for PCI to Local Accesses (F8h)	00000043 ->
Range for Direct Master to PCI (1Ch)	FF000000		

Runtime Registers

Mailbox 0 (User Defined) (78h)	00000000	Mailbox 1 (User Defined) (7Ch)	00000000
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Show Offset in: Serial EEPROM Offset
 Mapping to PCI Configuration Addr. and PCI Offset from Base Addr.

The EEPROM type you selected in the Configuration menu is NS93CS56.

Close Write Refresh

Figure A-1 Configuration EEPROM Settings for the PCI 9054RDK-860

CompactPCI 9054RDK-860:

The table below describes the memory requirements of the PCI SDK for the CompactPCI 9054RDK-860.

Item	CompactPCI 9054RDK-860
SDRAM Address	0x0000 0000 -> 0x01FF FFFF (32MB)
SBSRAM Address	0x2000 0000 -> 0x0007 FFFF (512KB)
FLASH Type	AT49LV040(default as shipped) AM29F040 also supported in software
FLASH Address	0xFFFF0 0000 -> 0xFFFF7 FFFF (512KB)
FLASH Image Base Address	0x0000 0000
Memory space used by ROM code	0x0000 0000 -> 0x0003 FFFF
Memory space used by RAM code (PCI SDK Samples)	0x0004 0000 -> 0x0007 FFFF
Direct Master to PCI memory space Address	0x4000 0000 -> 0x40FF FFFF (16MB)
Direct Master to PCI IO space Address	0x5000 0000 -> 0x50FF FFFF (16MB)
PCI 9054 Register Address	0x3000 0000 -> 0x3000 01FF
Memory space recommend for user's use.	0x0008 0000 -> 0x01FF FFFF (31.5MB)

User's who have upgraded the PCI SDK and intend to use it with an existing PLX RDK, must first reprogram the configuration EEPROM connected to the PLX chip. Skipping this step can cause unpredictable behavior of the PCI SDK. If you have purchased the PCI SDK with a PLX RDK then there is no need to upgrade the EEPROM because it was programmed at the factory before shipping. The following diagram shows the default settings for the RDK.

Displaying 93CS56 EEPROM values

PCI Configuration Registers

Device ID (00h)	C860	Vendor ID (02h)	10B5	Hot Swap Control (48h)	00004C06
Subsystem ID (2Ch)	9054	Sub Vendor ID (2Eh)	10B5	Interrupt Line (3Ch)	00
Revision (08h)	01	Class Code (09h)	068000	Interrupt Pin (3Dh)	01
		Max_Lat (3Fh)	00	Min_Gnt (3Eh)	00

Local Configuration Registers

Range for PCI to Local Address Space 0 (00h)	FF000000	Local Base Address for Direct Master to PCI Memory (20h)	40000000
Remap for PCI to Local Address Space 0 (04h)	00000001	Local Bus Address for Direct Master to PCI IO/CFG (24h)	50000000
Local Arbitration Register (08h)	0101000C	PCI Base Address (Remap) for Direct Master to PCI (28h)	00000003
Endian-Local Misc-VPD Boundary Register (0Ch)	00305524	PCI Config. Addr. Reg. for Direct Master to PCI/CFG (2Ch)	00000000
Range for PCI to Local Expansion ROM (10h)	00000000	Range for PCI to Local Address Space 1 (1MB) (F0h)	FF000000
Remap for PCI to Local Expansion ROM (14h)	00000010	Remap for PCI to Local Address Space 1 (F4h)	20000001
Bus Region Descriptor for PCI to Local Access (18h)	8B430043	Local Space1 for PCI to Local Accesses (F8h)	00000143
Range for Direct Master to PCI (1Ch)	FF000000		

Runtime Registers

Mailbox 0 (User Defined) (78h)	00000000	Mailbox 1 (User Defined) (7Ch)	00000000
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Show Offset in: Serial EEPROM Offset
 Mapping to PCI Configuration Addr. and PCI Offset from Base Addr.

The EEPROM type you selected in the Configuration menu is NS93CS56.

OK Write Refresh

Figure A-2 Configuration EEPROM Settings for the CompactPCI 9054RDK-860

PCI 9080RDK-401B:

The table below describes the memory requirements of the PCI SDK for the PCI 9080RDK-401B.

Item	PCI 9080RDK-401B
SDRAM Address	0x0000 0000 -> 0x00FF FFFF (16MB)
SRAM Address	0x1000 0000 -> 0x1007 FFFF (512KB)
FLASH Type	AM29F040
FLASH Address	0xFFFF8 0000 -> 0xFFFF FFFF (512KB)
FLASH Image Base Address	0x0006 0000
Memory space used by ROM code	0x1000 0000 -> 0x1003 FFFF
Memory space used by RAM code (PCI SDK Samples)	0x1004 0000 -> 0x1007 FFFF

Item	PCI 9080RDK-401B
Direct Master to PCI memory space Address	0xB800 0000 -> 0xBFFF FFFF (8MB)
Direct Master to PCI IO space Address	0xB000 0000 -> 0xB7FF FFFF (8MB)
PCI 9080 Register Address	0x2000 0000 -> 0x2000 01FF
Memory space recommend for user's use.	0x1008 0000 -> 0x1F8F FFFF (15.5MB)

User's who have upgraded the PCI SDK and intend to use it with an existing PLX RDK, must first reprogram the configuration EEPROM connected to the PLX chip. Skipping this step can cause unpredictable behavior of the PCI SDK. If you have purchased the PCI SDK with a PLX RDK then there is no need to upgrade the EEPROM because it was programmed at the factory before shipping. The following diagram shows the default settings for the RDK.

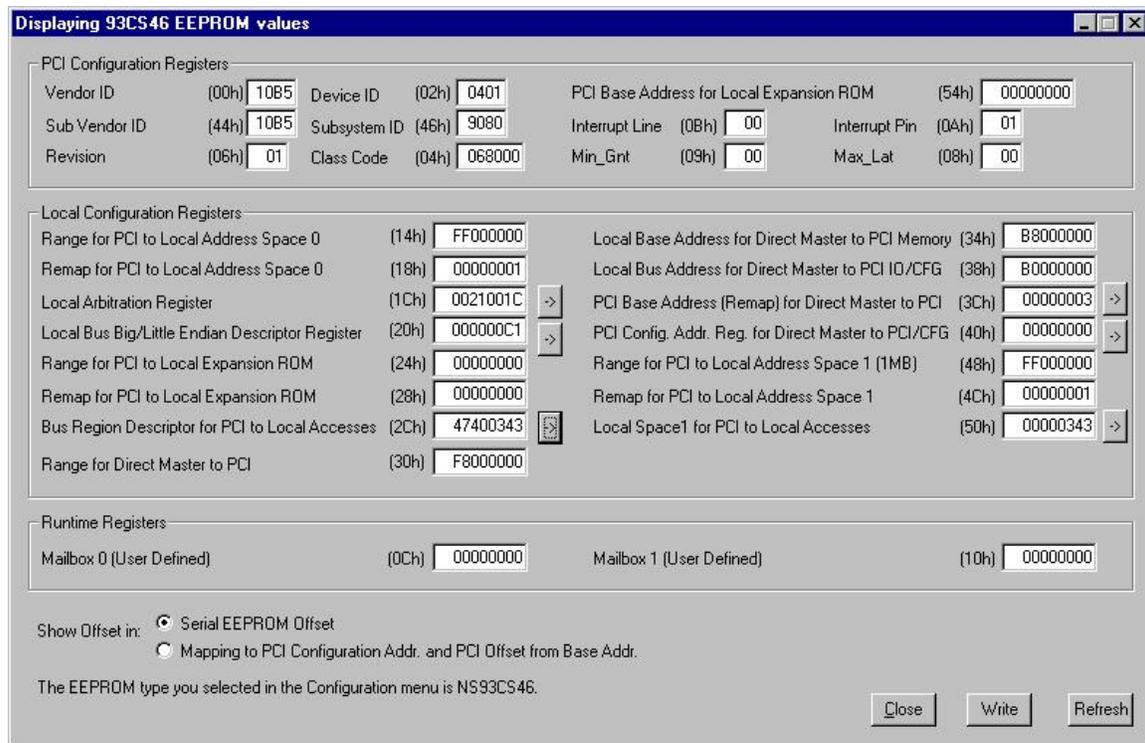


Figure A-3 Configuration EEPROM Settings for the PCI 9080RDK-401B



PCI 9080RDK-860:

The table below describes the memory requirements of the PCI SDK for the PCI 9080RDK-860.

Item	PCI 9080RDK-860
DRAM Address	0x1000 0000 -> 0x10FF FFFF (16MB)
SRAM Address	0x0000 0000 -> 0x0007 FFFF (512KB)
FLASH Type	AM29F040 (IOP programming only)
FLASH Address	0xFFFF8 0000 -> 0xFFFF FFFF (512KB)
FLASH Image Base Address	0x0000 0000
Memory space used by ROM code	0x0000 0000 -> 0x0003 FFFF
Memory space used by RAM code (PCI SDK Samples)	0x0004 0000 -> 0x0007 FFFF
Direct Master to PCI memory space Address	0x4000 0000 -> 0x40FF FFFF (16MB)
Direct Master to PCI IO space Address	0x5000 0000 -> 0x50FF FFFF (16MB)
PCI 9080 Register Address	0xC000 0000 -> 0xC000 01FF
Memory space recommend for user's use.	0x1000 0000 -> 0x10FF FFFF (16MB)

User's who have upgraded the PCI SDK and intend to use it with an existing PLX RDK, must first reprogram the configuration EEPROM connected to the PLX chip. Skipping this step can cause unpredictable behavior of the PCI SDK. If you have purchased the PCI SDK with a PLX RDK then there is no need to upgrade the EEPROM because it was programmed at the factory before shipping. The following diagram shows the default settings for the RDK.

Displaying 93CS56 EEPROM values

PCI Configuration Registers

Vendor ID (00h) 10B5 Device ID (02h) 0860 PCI Base Address for Local Expansion ROM (30h) 00000000
Sub Vendor ID (2Ch) 10B5 Subsystem ID (2Eh) 9080 Interrupt Line (3Ch) 01 Interrupt Pin (3Dh) 01
Revision (08h) 01 Class Code (09h) 068000 Max_Lat (3Fh) 00 Min_Gnt (3Eh) 00

Local Configuration Registers

Range for PCI to Local Address Space 0 (00h) FF000000 Local Base Address for Direct Master to PCI Memory (20h) 40000000
Remap for PCI to Local Address Space 0 (04h) 10000001 Local Bus Address for Direct Master to PCI IO/CFG (24h) 50000000
Local Arbitration Register (08h) 0101000C -> PCI Base Address (Remap) for Direct Master to PCI (28h) 00000583 ->
Local Bus Big/Little Endian Descriptor Register (0Ch) 00000024 -> PCI Config. Addr. Reg. for Direct Master to PCI/CFG (2Ch) 00000000 ->
Range for PCI to Local Expansion ROM (10h) 00000000 Range for PCI to Local Address Space 1 (1MB) (F0h) FF000000
Remap for PCI to Local Expansion ROM (14h) 00000010 Remap for PCI to Local Address Space 1 (F4h) 10000001
Bus Region Descriptor for PCI to Local Accesses (18h) 02430043 -> Local Space1 for PCI to Local Accesses (F8h) 00000043 ->
Range for Direct Master to PCI (1Ch) FF000000

Runtime Registers

Mailbox 0 (User Defined) (78h) 00000000 Mailbox 1 (User Defined) (7Ch) 00000000

Show Offset in: Serial EEPROM Offset
 Mapping to PCI Configuration Addr. and PCI Offset from Base Addr.

The EEPROM type you selected in the Configuration menu is NS93CS56.

OK Write Refresh

Figure A-4 Configuration EEPROM Settings for the PCI 9080RDK-860

PCI 9080RDK-SH3:

The table below describes the memory requirements of the PCI SDK for the PCI 9080RDK-SH3.

Item	PCI 9080RDK-SH3
DRAM Address for SH3 access	0x0C00 0000 -> 0x0CFF FFFF (16MB)
DRAM Address for PCI 9080 access	Not Supported
SRAM Address for SH3 access	0x0900 0000 -> 0x0903 FFFF (256KB)
SRAM Address for PCI 9080 access	0x4000 0000 -> 0x4003 FFFF (256KB)
EPROM Type	TMS27C010A-10
EPROM Address for SH3 access (if boot device)	0x0000 0000 -> 0x0001 FFFF (256KB)
EPROM Address for PCI 9080 access	Not Supported
FLASH Type	MBM29LV160B-90



Item	PCI 9080RDK-SH3
FLASH Address for SH3 access (if boot device)	0x0000 0000 -> 0x001F FFFF (2MB)
FLASH Address for SH3 access (if non-boot device)	0x0100 0000 -> 0x011F FFFF (2MB)
FLASH Address for PCI 9080 access	Not Supported
FLASH Image Base Address	0x0000 0000
Memory space used by ROM code	0x0C00 0000 -> 0x0C03 FFFF and 0x0900 0000 -> 0x0900 0FFF
Memory space used by RAM code (PCI SDK Samples)	0x0900 1000 -> 0x0900 FFFF
Direct Master to PCI memory space Address for SH3 access	0x0A00 0000 -> 0x0A0F FFFF (1MB)
Direct Master to PCI IO space Address for SH3 access	0x0B00 0000 -> 0x0B0F FFFF (1MB)
PCI 9080 Register Address for SH3 access	0x0800 0000 -> 0x0800 01FF
Memory space recommended for user's use for SH3 access.	0x0901 0000 -> 0x0903 FFFF (192KB)
Memory space recommended for user's use for PCI 9080 access.	0x4001 0000 -> 0x4003 FFFF (192KB)

User's who have upgraded the PCI SDK and intend to use it with an existing PLX RDK, must first reprogram the configuration EEPROM connected to the PLX chip. Skipping this step can cause unpredictable behavior of the PCI SDK. If you have purchased the PCI SDK with a PLX RDK then there is no need to upgrade the EEPROM because it was programmed at the factory before shipping. The following diagram shows the default settings for the RDK.

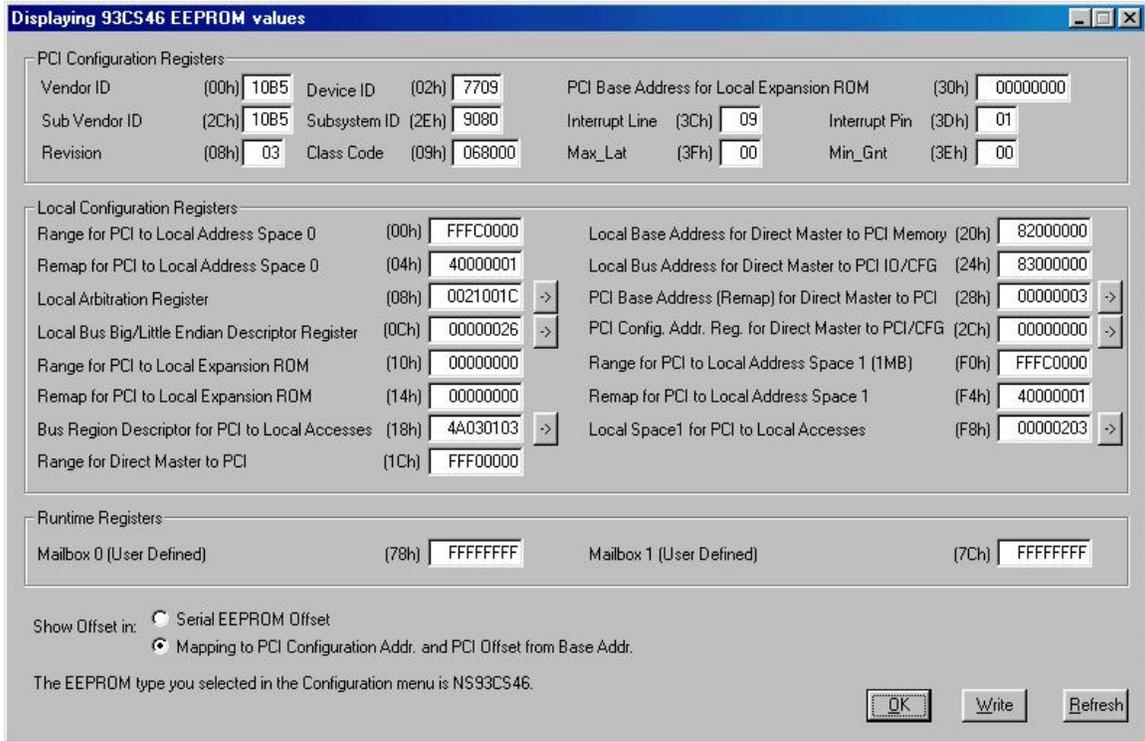


Figure A-5 Configuration EEPROM Settings for the PCI 9080RDK-SH3

PCI 9080RDK-RC32364:

The table below describes the memory requirements of the PCI SDK for the PCI 9080RDK-RC32364.

Item	PCI 9080RDK-RC32364
DRAM Virtual Address	0x0010 0000 -> 0x004F FFFF (4MB)
SRAM Virtual Address	0x0000 0000 -> 0x000F FFFF (1MB)
EPROM Type	M27C801-100
EPROM Virtual Address	0xBFC0 0000 -> 0xBFC7 FFFF (512KB)
EPROM Image Base Address	0x0000 0000
Virtual memory space used by ROM code	0x0000 0000 -> 0x0003 FFFF
Virtual memory space used by RAM code (PCI SDK Samples)	0x0004 0000 -> 0x0007 FFFF



Item	PCI 9080RDK-RC32364
Direct Master to PCI memory virtual space Address	0x1500 0000 -> 0x15FF FFFF (16MB)
Direct Master to PCI IO virtual space Address	0x1600 0000 -> 0x16FF FFFF (16MB)
PCI 9080 Register Virtual Address	0x1400 0000 -> 0x1400 01FF
Virtual Memory space recommend for user's use.	0x0008 0000 -> 0x004F FFFF (4.5MB)

The configuration EEPROM on this RDK is not removable and there is no need to reprogram it.