

# DRAFT

## Adapting the Liquid Argon Calorimeter SCA for use with CSC

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The Switched Capacitor Analog memory (SCA) used in the ATLAS LAr readout can also be used in the muon CSC system. The requirements of the two readout systems are different and this note describes how we plan to use the Nevis/Saclay SCA in the CSC.

### Summary of LAr Readout

LAr uses a three-gain structure to accommodate its large dynamic range. Each channel has a preamplifier and a 3-gain shaping amplifier before the SCA, as shown in Figure 1.

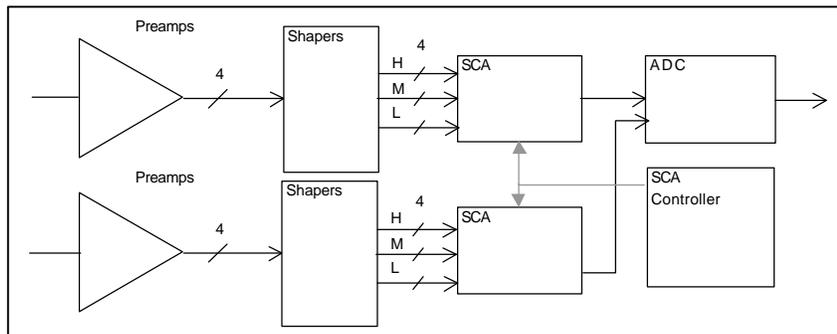


Figure 1. LAr tri-gain readout system

The SCAs each contain 16 "pipelines". Each pipeline is an array of 144 storage capacitors that can be connected to the read or write bus. The 12 shaped signals from 4 LAr channels are input to 12 of the pipelines and the remaining 4 pipelines are used as differential references (for subtraction of common mode noise.) All SCAs write to the same capacitor location in each pipeline. A new sample is written every 25 nsec. On readout, data from selected capacitors is multiplexed onto a common output bus. Only one sample at a time can be read out. The time required to read out a sample is limited by the settling time of the internal op-amp output buffer. A simplified block diagram of the SCA is shown in Figure 2.

Data can be simultaneously read and written to the SCA.

As shown in Figure 1, a pair of SCAs is read out by a dedicated 12 bit ADC. The same SCA pair has a dedicated readout controller (ALTERA FPGA) which controls the readout sequence. Write addresses are generated by a central controller (Xylinx FPGA.)

Upon receipt of a Level 1 trigger, the readout cycle is started. The SCA controller first reads out the peak sample in the mid-gain range of all channels to determine the proper gain for each channel. Then 5 samples from the proper gain range of all channels are read out. Hence the readout time is  $8 + 5 \times 8 = 48$  read clocks. With a readout clock of 5 MHz the read cycle can be completed in less than 10  $\mu$ s, allowing an average trigger rate of 100 kHz. This 5-sample readout cycle is shown in Figure 3 below.

# DRAFT

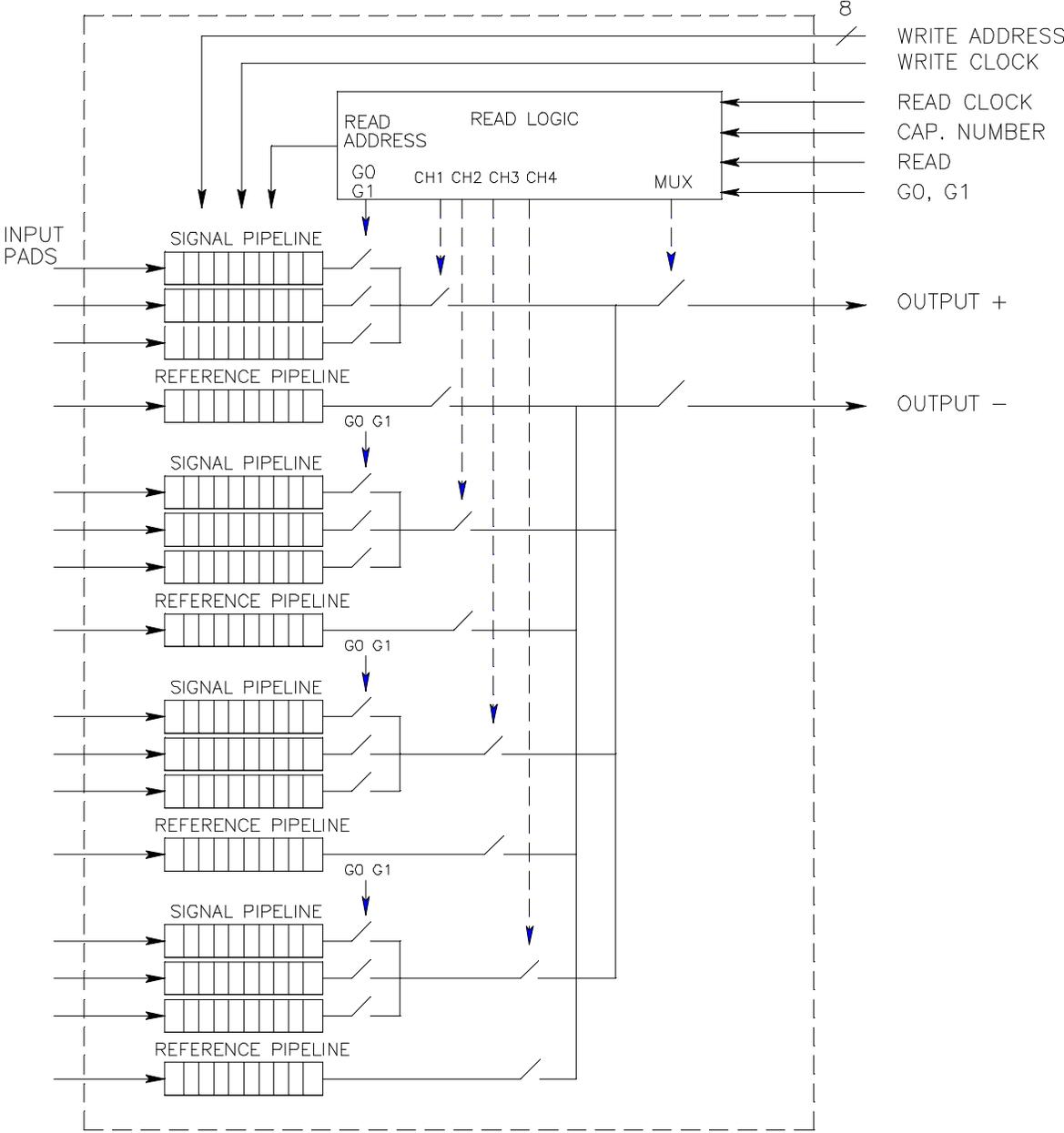


Figure 2. Simplified block diagram of the NEVMOD0 SCA chip.



# DRAFT

The SCA is the latest revision of an ongoing series of prototypes. The chip is fabricated in Hewlett-Packard's 1.2  $\mu\text{m}$  CMOS with 2 metal layers and a special implant to permit floating, linear MOS capacitors to be formed. The process was offered by the MOSIS multiproject service until January of 1998 and is no longer available. The SCA is packaged in a 100-lead QFP measuring approximately 17.8 x 25.4 mm. About 2000 chips have already been fabricated and tested. A portion of the FEB showing the top-side SCAs is shown in Figure 5.

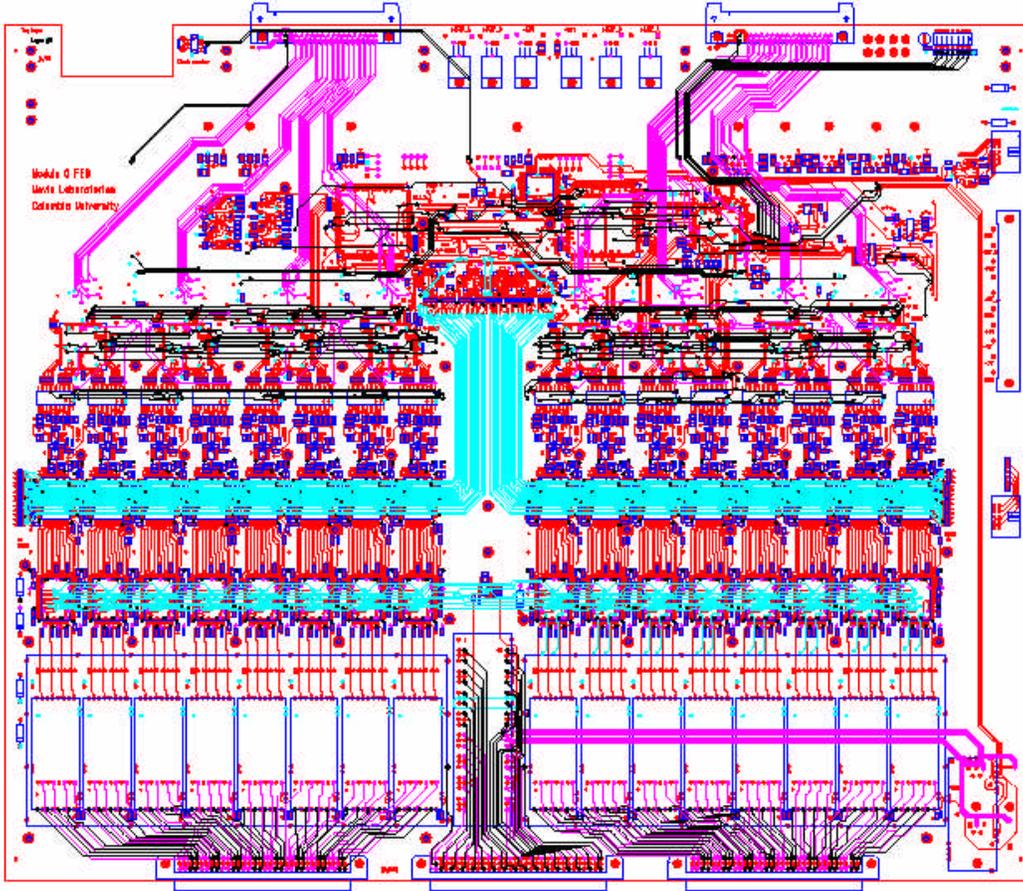


Figure 4. Layout of the LAr front-end board (FEB). Overall size: 49 x 41 cm.

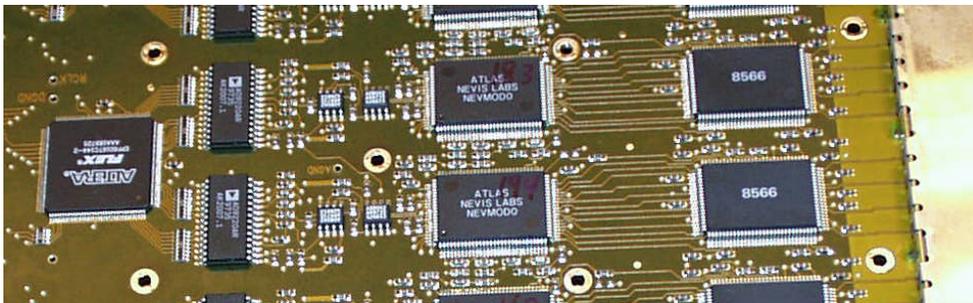


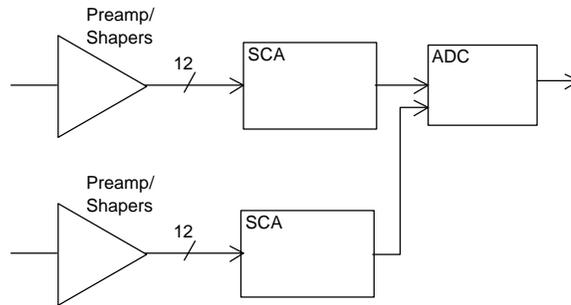
Figure 5. Photograph of a portion of FEB showing (right to left) shapers ("8566"), SCAs, ADCs, and SCA readout controller.

# DRAFT

## Proposal for CSC readout

The CSC readout electronics, while functionally similar to LAr, is denser, requires less precision, and must be produced at much lower cost. The preamp/shapers, SCAs, ADCs, and associated control logic are mounted along the edges of the CSC chambers (See Fig. 4.) The available board area totals about 0.24 m<sup>2</sup> per chamber for 920 channels. Unlike the LAr system, only a single gain range per channel is used.

We propose to use the Nevis SCA to read out 12 channels of CSC. The architecture of the system would otherwise resemble the LAr system (Fig. 6.) 12 channels of preamp/shaper signals are input to each SCA. Data is written to the SCA at 40 MHz as before. Since there is no gain selection, the readout sequence is simpler. Upon receipt of Level 1 trigger, the (common) readout controller reads out a sample from every channel into the ADC. *Note that the structure of the internal SCA logic makes it impossible to use one ADC for each SCA.* Instead we must multiplex two SCAs (24 channels) into one ADC. This is a factor of 3 higher multiplexing density than the LAr system.



**Figure 6. Proposed configuration of Nevis SCAs in the CSC system.**

The number of waveform samples per trigger  $N_{\text{samp}}$  is currently being investigated by Monte Carlo simulation. If we choose  $N_{\text{samp}}=5$ , then the readout time for a pair (24 channels) of SCAs will be  $5 \times 24 = 120$  clocks. In order to satisfy the 100 kHz trigger rate, the readout clock frequency must be at least  $120/10\mu\text{s} = 12$  MHz. The nearest available frequency which can be derived from the 40 MHz beam crossing clock is 13.3 MHz.

Tests are underway to determine if the Nevis SCA output multiplexer can settle to 10 bits within the available 75 nsec. If not, it may be possible to use fewer than 5 samples to read out the CSC waveform without degrading the position resolution. Alternatively, it may be possible to modify the SCA internal logic to allow each SCA to be read out by its own ADC. Table 1 shows the required readout clock rate for various values of  $N_{\text{samp}}$ .

$N_{\text{samp}}$	$N_{\text{RCLK}} = 24 \times N_{\text{samp}}$	$T_{\text{SAMP}}=10\mu\text{s}/N_{\text{RCLK}}$	$T_{\text{SAMP}}/25$	Divisor	$T_{\text{RCLK}}$	$F_{\text{RCLK}}$
1	24	417	16.7	16	400	2.5
2	48	208	8.32	8	200	5
3	72	139	5.56	5	125	8
4	96	104	4.16	4	100	10
5	120	83	3.32	3	75	13.3
8	192	52	2.08	2	50	20
Units	-	nsec	nsec	-	nsec	MHz

**Table 1. Readout clock (RCLK) rate for several values of  $N_{\text{samp}}$**

# DRAFT

The differences between the LAr and CSC readout systems are summarized in Table 1 below.

	LAr	CSC
Precision	12 bit	10 bit
Multiple gains	Yes	No
Channels per SCA	4	12
Simultaneous read/write	Yes	Yes
Write sampling rate	40 MHz	40 MHz
Read sampling rate	5 MHz	13.3 MHz
Number of readout samples/trigger	5	$\leq 5$
Readout board size	49.1 x 41.3 cm	24 x 12.5 cm
Channels per readout board	128	96
Area per channel	15.8 cm <sup>2</sup>	2.6 cm <sup>2</sup>

**Table 2. Differences between LAr and CSC readouts.**

## Board Layout

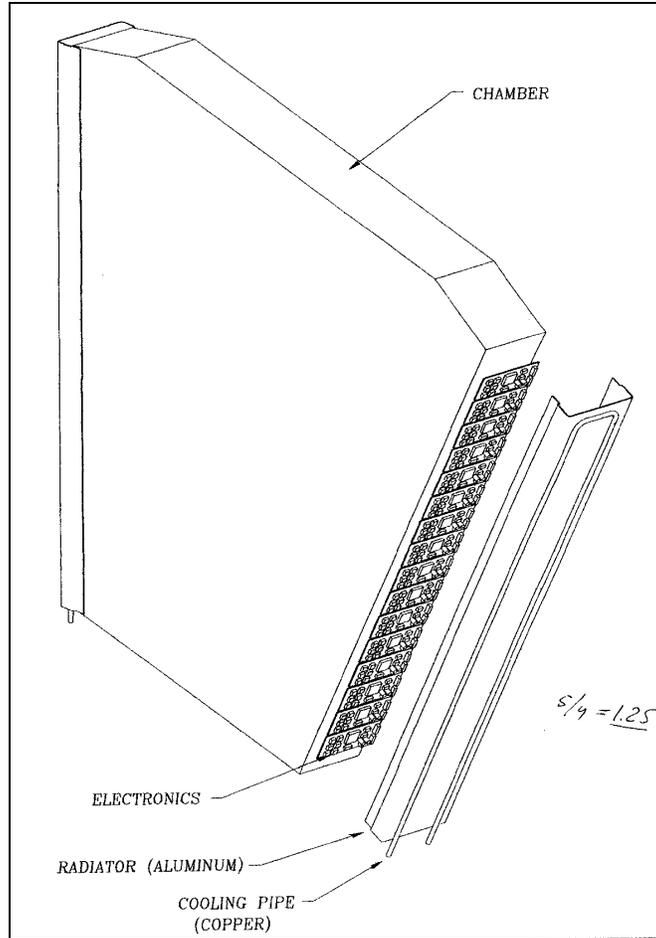
The CSC front-end readout electronics (preamp/shaper ASIC, SCA, digitizer) resides on a board called the ASM board which is mounted along the edges of the chamber (Figure 7.) The strips emerge from the chamber in 4 rows (layers) at 5mm pitch. There are 920 channels per chamber and 32 chambers per endcap.

The original ATLAS TDR proposal called for ASM boards to be mounted on only one edge of the chamber. Each ASM board served 48 channels and had an area of 6 x 10 cm, or 1.25 cm<sup>2</sup> per channel. This scheme can now be seen to be inefficient in consideration of the large area occupied by the circuits that support the SCAs. For example, in the LAr FEB for every 4 SCAs (2 back-to-back pairs) there are 2 ADCs, 4 dual op-amps, and one Altera CPLD for readout control. The area of this component group is about 10 x 5 cm = 50 cm<sup>2</sup>. For every board serving 32 SCAs total, 2 large Xilinx FPGAs are required along with numerous digital buffers. The area occupied by these circuits is about 30 x 8 = 240 cm<sup>2</sup>. The total area per SCA is  $\sim 50/4 + 240/32 = 20$  cm<sup>2</sup> per SCA, or 80 cm<sup>2</sup> for a 48-channel board. To this area we must add the area for the preamp/shapers, power conditioning, TTC and DCS interface, calibration, and connectors.

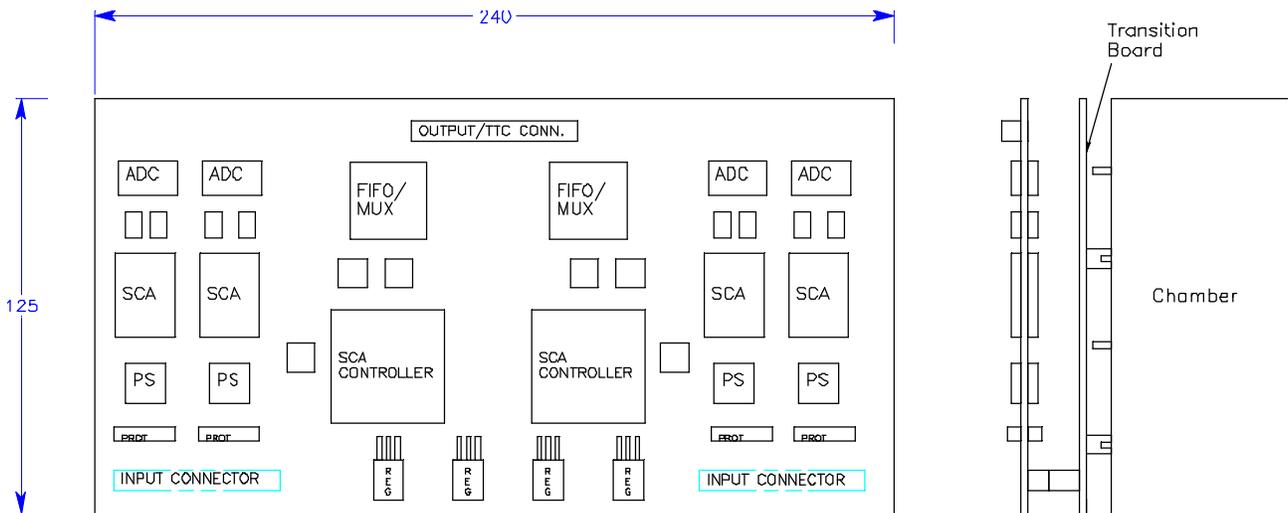
We can spread the area overhead of the SCA support circuitry by including more channels on the ASM board. In addition, we can populate both sides of the chamber with ASM boards to double the available area to 2400 cm<sup>2</sup>, or 2.6 cm<sup>2</sup> per channel. A possible layout of a 96-channel board is shown in Fig. 8. A total of 10 such boards (5 per side) would be needed per chamber.

In Fig. 8 the ASM board is not directly connected to the CSC cathode planes. There is a transition board with right angle board-to-board connectors on the bottom that mates with two planes of the CSC. The CSC strips may be terminated with mating gold plated fingers. The transition board re-maps the 96 strips into a single row connector on the long edge of the top side. The ASM board will have a mating connector on its bottom side as shown in the figure, and will require mechanical support on the opposite edge (not shown in Fig. 8.) The figure shows the ASM boards layout for the input connectors, protection networks, power conditioning, preamp/shapers, SCAs, ADCs, SCA support circuitry, output LVDS drivers, and output connector. Components are mounted on both sides of the ASM board. The component layout is arranged so that the high-speed digital bus to the SCAs is as straight and short as possible.

# DRAFT



**Figure 7. CSC readout electronics location on chamber**



**Figure 8. Proposed layout of 96-channel ASM board for CSC. This board would read out signals from 2 CSC planes. A similar board on the opposite face of the chamber would read out the other 2 planes.**

# DRAFT

## Data Volume and Sparsification

Table 3 below shows the output data rate in Mbits/sec from one 96-channel ASM board assuming a 100 kHz trigger rate for various combinations of  $N_{\text{SAMP}}$  and  $N_{\text{BITS}}$  where  $N_{\text{BITS}}$  is the resolution of the ADC. 10% overhead has been added to account for status and control words added to the data stream.

$N_{\text{SAMP}}$	$N_{\text{BITS}}$		
	8	10	12
1	84	106	127
2	169	211	253
3	253	317	380
4	338	422	507
5	422	528	634
8	676	845	1014

**Table 3. Data rate (Mbits/sec) from one 96-channel ASM board as a function of  $N_{\text{SAMP}}$  and  $N_{\text{BITS}}$**

The output from the ASM boards is sent as LVDS signals on twisted pair cable to the Data Concentrator Card (DCC) located on the large face of each chamber. Since the chamber occupancy is never expected to exceed 3% - 5%, it should be possible to reduce the data rate by a factor of 10 using appropriate sparsification algorithms. In addition we can use information from the anode wires to eliminate data that doesn't come from real tracks. The output from the DCC is then expected to be in the range of 200 - 500 Mbits/sec. This data will be sent off-chamber on optical fiber.