

Analog Signal Processing

ATLAS CSC Electronics

Conceptual Design Review

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Outline

- **Signals and noise - theory**
- **Implementation:**
 - **organization**
 - **mechanics**
 - **circuitry**

Signal formation, noise, and gain - 1

1. Chamber electrode configuration

- 4 gas gaps
- 192 precision strips
 - Readout pitch $d = 5.547\text{mm}$
 - Cstrip 20 – 50 pF
- 48 transverse strips (no interpolation)
- anode wires
- Outer "skin" of chamber is GROUND with firm connection to Faraday shields
- Each gap has perimeter ground
- Perimeter grounds linked across top of chamber, to skins

2. Signal size

- muon generates 75 electron-ion pairs (Landau peak)
- gas gain $\sim 10^5$
- 12% of charge is collected by the precision cathode in 100 ns
- => signal size is $\sim 900,000 e^-$ (144 fC) $\equiv Q_\lambda$
- central strip of cluster receives $\sim 1/2$ of charge => 72 fC ($Q_{\lambda,\text{cent}}$)

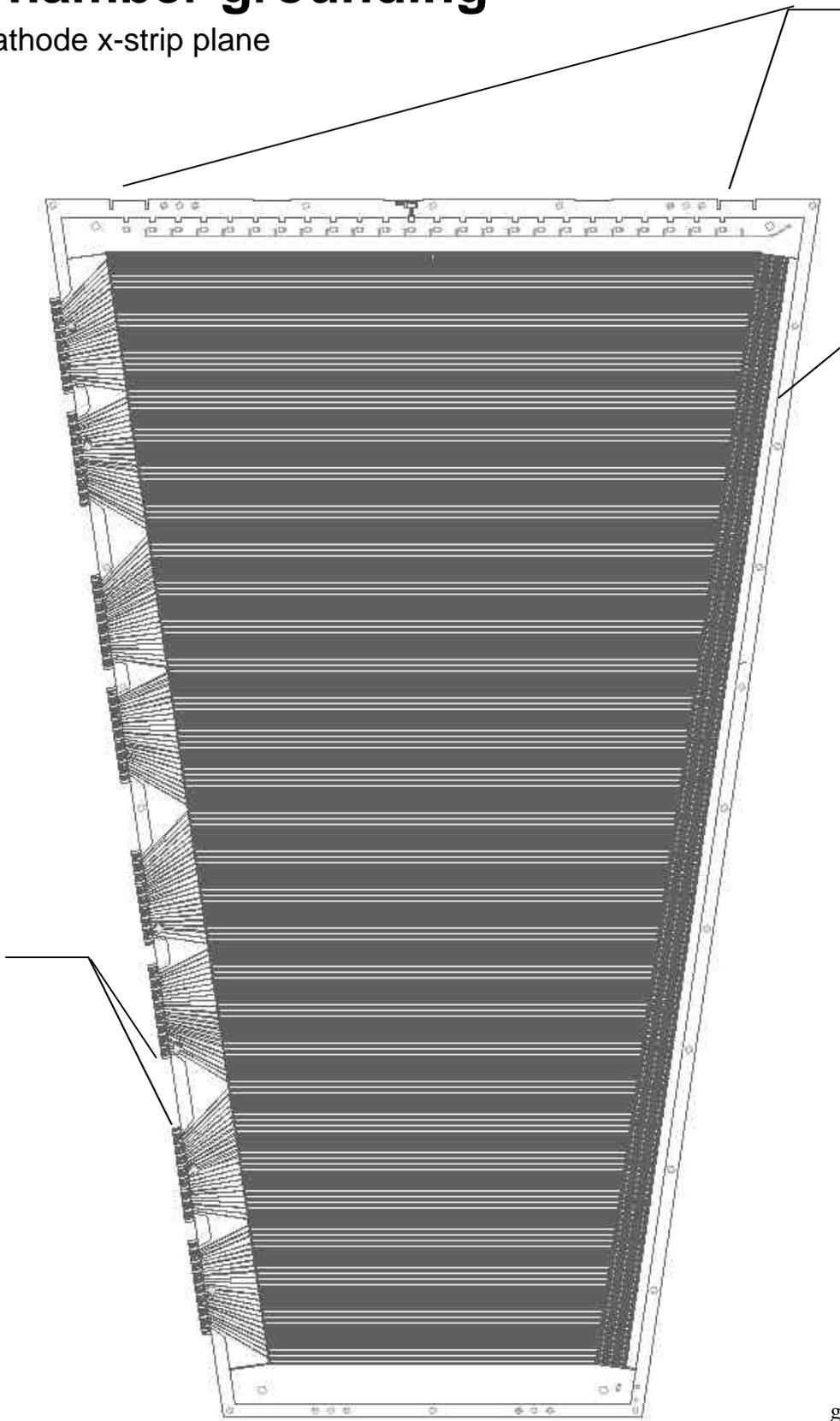
Chamber grounding

Cathode x-strip plane

Ground connection to other 3 x-strip planes

Continuous ground ring around outside edge of cathode planes

Ground connection to ASM-I's



Signal formation, noise, and gain - 2

3. Noise

- electronics noise shouldn't degrade position resolution

$$s_{x,elec} = \frac{\sqrt{3} \cdot d \cdot ENC}{Q_1} \leq 33mm$$

where d = strip pitch, ENC = equivalent input noise charge, Q = charge induced on cathode plane

$$ENC \leq 0.5 fC = 3100e^- \leftarrow \text{TOTAL input referred noise}$$

$$\text{Signal-to-noise (max. strip)} = \frac{Q_{1,cent}}{ENC} = \frac{72 fC}{3100e^-} = 145$$

4. Dynamic range and gain

for 98.5% efficiency,

$$\frac{Q_{FS}}{Q_1} \geq 5$$

$$\therefore Q_{FS} \geq 5 \cdot Q_1 = 725 \cdot ENC \cong 360 fC$$

for preamp/shaper $V_{FS} = 1.7$ V (positive lobe of bipolar waveform)

$$\therefore P/S \text{ gain} = \frac{V_{FS}}{Q_{FS}} = 4.7 mV / fC$$

5. Quantization

$$\frac{Q_{FS}}{2^{Nbits} \cdot \sqrt{12}} \ll ENC$$

$$2^{Nbits} \gg \frac{Q_{FS}}{\sqrt{12} \cdot ENC} = 209$$

$$Nbits \gg 7.7$$

$$Nbits = 10 (s_{Q,quant} = 20\% ENC) \text{ or } 12 (s_{Q,quant} = 5\% ENC)$$

12 bits preferred to accommodate negative lobe, gain and offset variations, etc.

High Rate / High Background Operation

- Overall background rate 10^7 Hz per chamber
- 50% charged particles, 50% neutron and γ
- Charged particle background is rejected by timing window around trigger or by pattern recognition of non-projective tracks
- Neutrals can deposit high charges:
 - 50% of neutrals above Q_{FS}
 - 1% of neutrals above $6 \times Q_{FS}$
- Neutrals produce short-range electrons so usually confined to 1 layer only
- But a neutral hit anywhere in chamber induces charge on all strips by anode-cathode crosstalk:

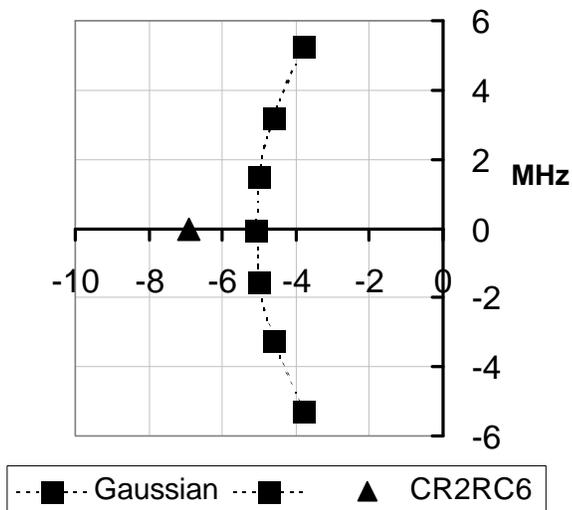
$$Q_{cross} = \frac{C_{ac}}{C_{filt}} \cdot Q_{anode} \cong 10^{-4} Q_{anode}$$

- This high-rate, low amplitude background behaves like electronic parallel noise (choice of shaping function)
- Within-chip crosstalk distorts signals in cluster, can systematically shift interpolated centroid position.

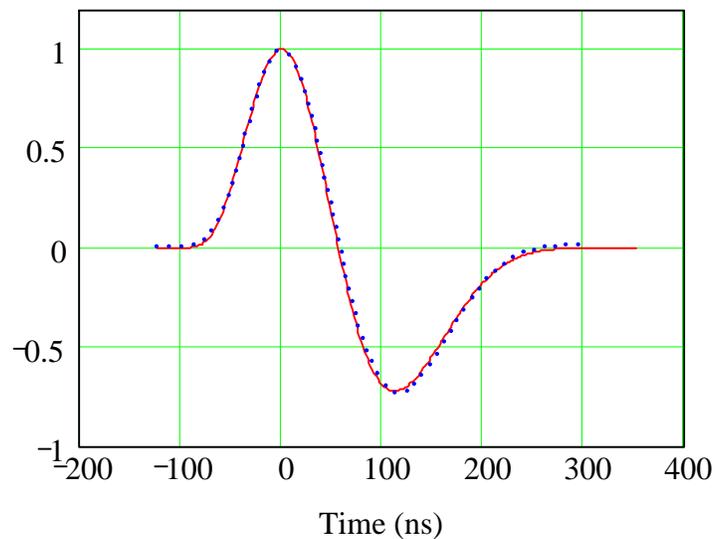
Rates and pulse shaping

- Optimal pulse shaping is a compromise between noise, which degrades position resolution, and pileup, which contributes to inefficiency.
- Bipolar pulse preferred in high-rate environment.
- From Monte Carlo study, peaking time should be ~ 100 ns and $FW1\%M < 430$ ns
- Bipolar 7th-order shaper using complex poles gives same return to baseline as 12th-order CR^2-RC^n configuration

Shaper Pole Positions

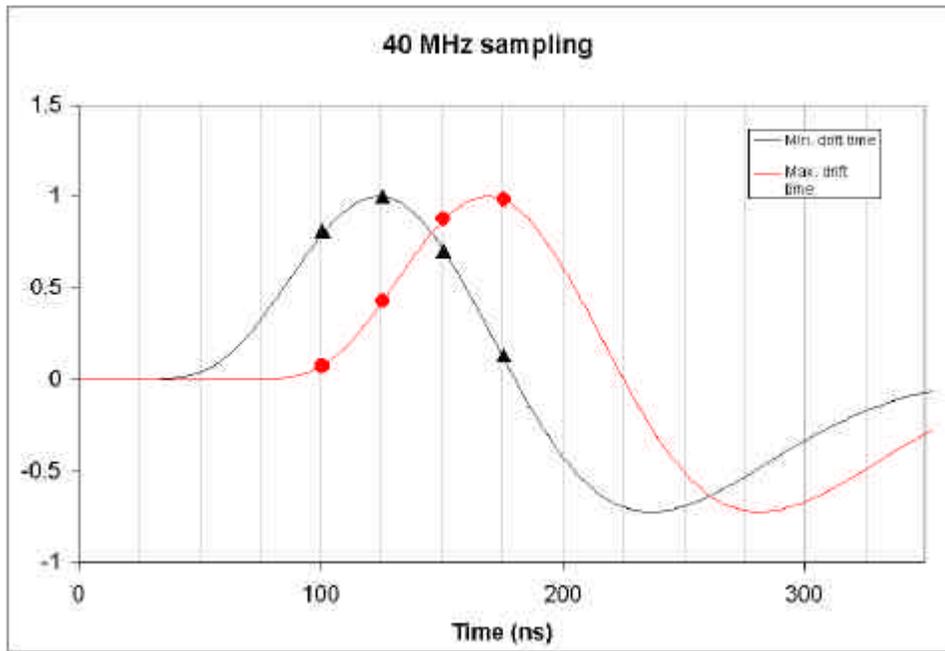


Waveform

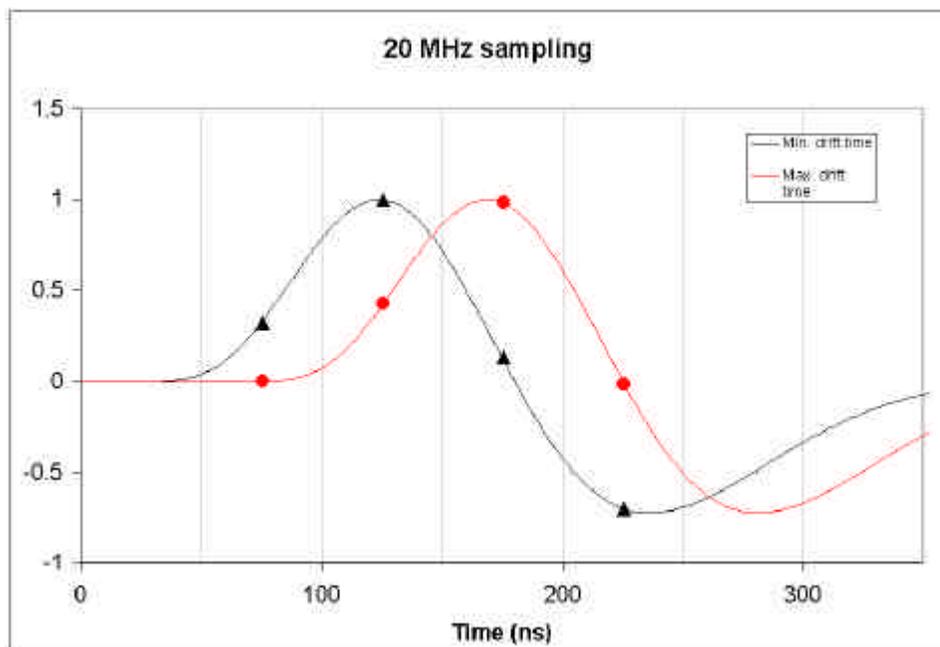


Sampling rate

- With 40 MHz sampling and only 4 samples, we can't always get the peak and both neighbors



- 20 MHz sampling/4 samples gives a wider window and doesn't degrade the resolution or efficiency



Calibration

- Precise (0.5%) calibration is necessary for interpolation
- Each plane has calibration circuit on ASM-II
- Pulse wire groups to induce charge on all strips simultaneously

$$0 \leq Q_{\text{cal}} \leq Q_{\text{FS}}$$

- Circuit still under development

Reliability

Goal: < 0.1% data lost due to hard or soft fails

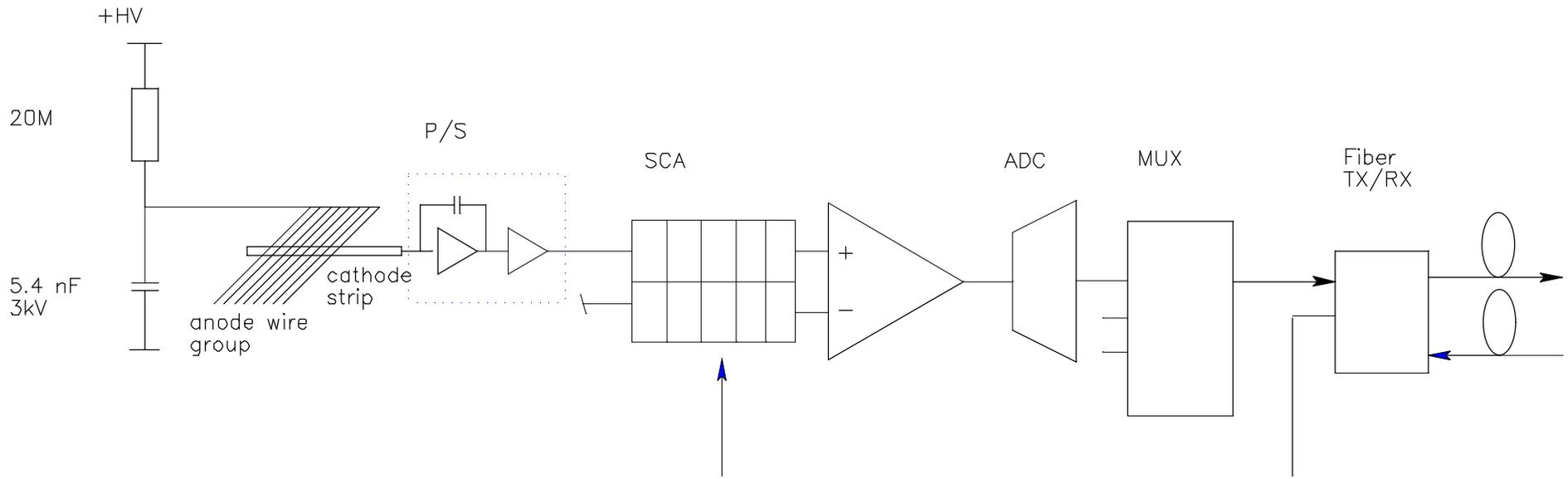
Strategy: on-detector electronics boards must be as simple and robust as possible

- Minimal parts list: B.O.M. for ASM-PACK active components:

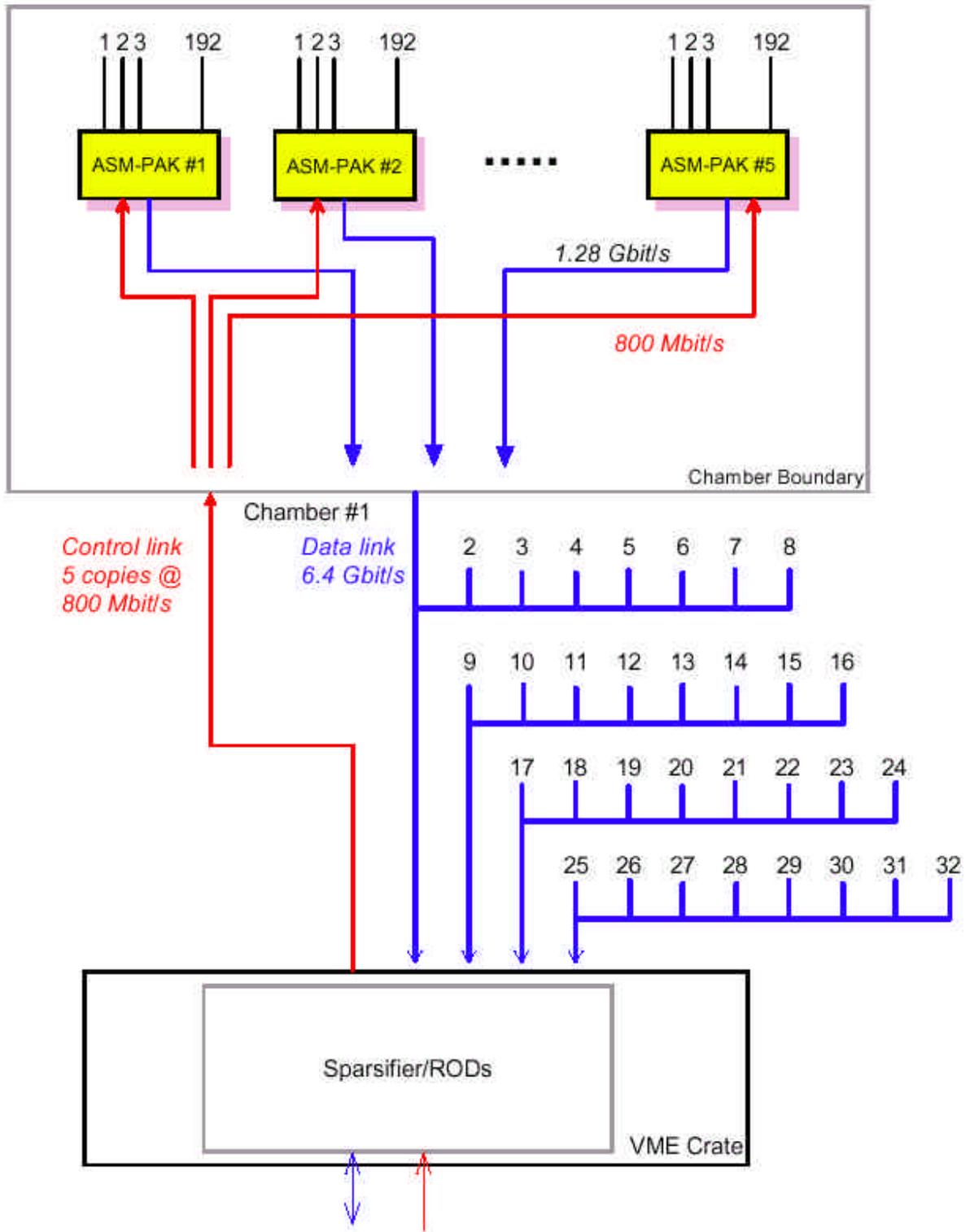
<i>3.3V (adj) regulator</i>	<i>AD 9042 12-bit ADC</i>
<i>5V fixed regulator</i>	<i>10H116 PECL driver</i>
<i>IC50 custom preamp/shaper</i>	<i>1N914 protection diodes</i>
<i>HAMAC v.4 custom SCA</i>	<i>G-link transceiver</i>
<i>AD8042 dual op-amp</i>	<i>HDMP 1022/1024 serializer/deserializer</i>
- All intelligence to reside on sparsifier/ROD
- ASM to have no

<i>Configuration registers</i>	<i>Programmable logic</i>
<i>FIFOs</i>	<i>RAM</i>
<i>Counters</i>	<i>State machines</i>
- Thorough radiation test of all components
- ESD protect inputs at board and chip level
- ATLAS policy on grounding and shielding
- Extra attention to amplifier stability
- No DCS
- Minimal monitoring

CSC Electronics Analog Signal Chain



CSC Electronics Overall Organization



CSC Electronics Numerology

SYSTEM

- 2 endcaps
- 64 chambers
- 61,440 channels
- 640 ASM-PACKs
- 32 Sparsifier/RODs

CHAMBER

- 4 layers
- 960 channels (768 precision, 192 transverse)
- 5 ASM-PACKs
- 15 optical links (10 data, 5 control)

ASM-PACK

- 192 channels
- 1 ASM-II board
- 2 ASM-I boards
- 3 fiber optic links

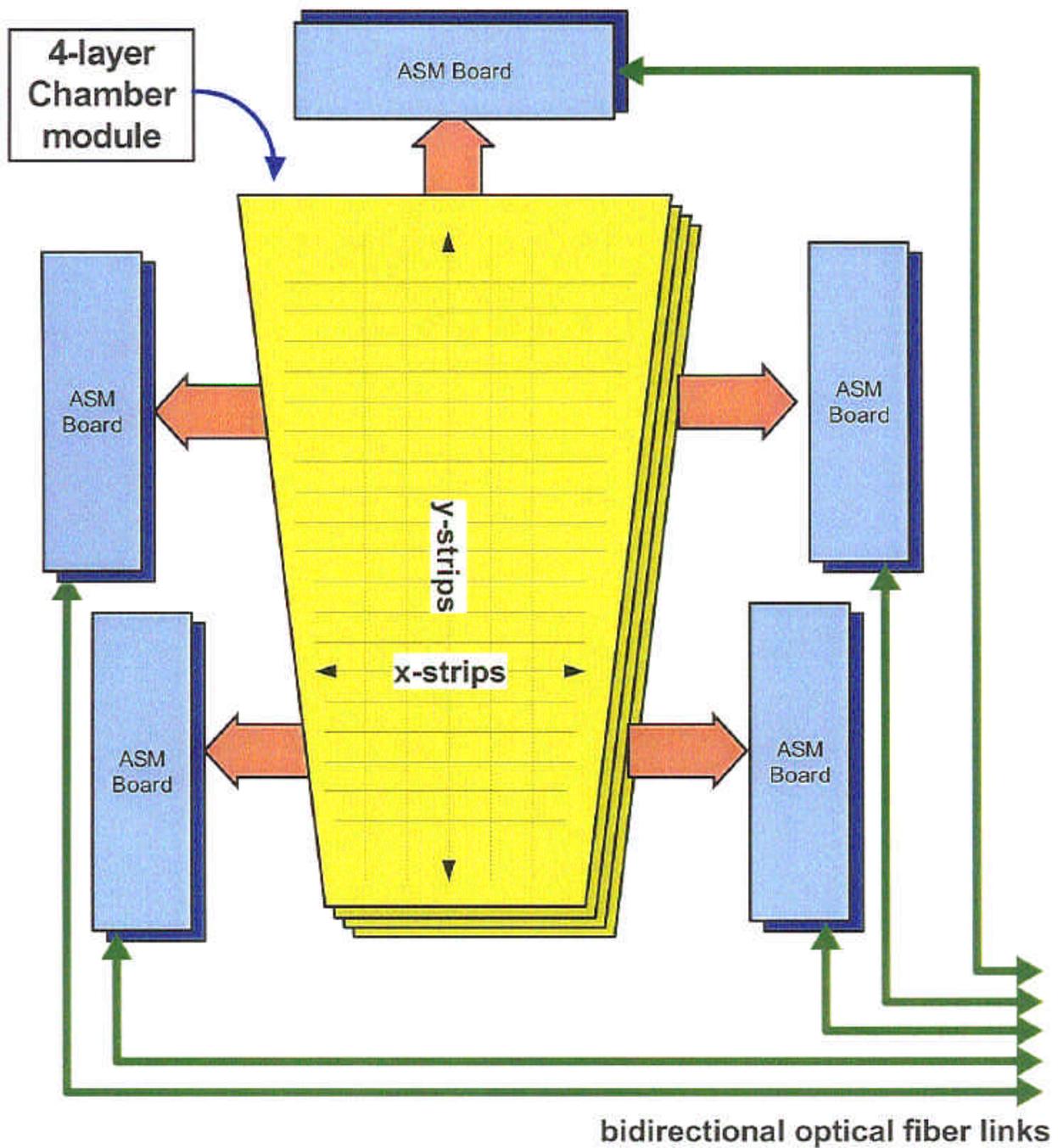
ASM-II

- 192 channels
- 2 ASM-I's
- 16 SCA ASICs
- 16 ADCs
- 2 serializer/transmitters
- 1 receiver/deserializer

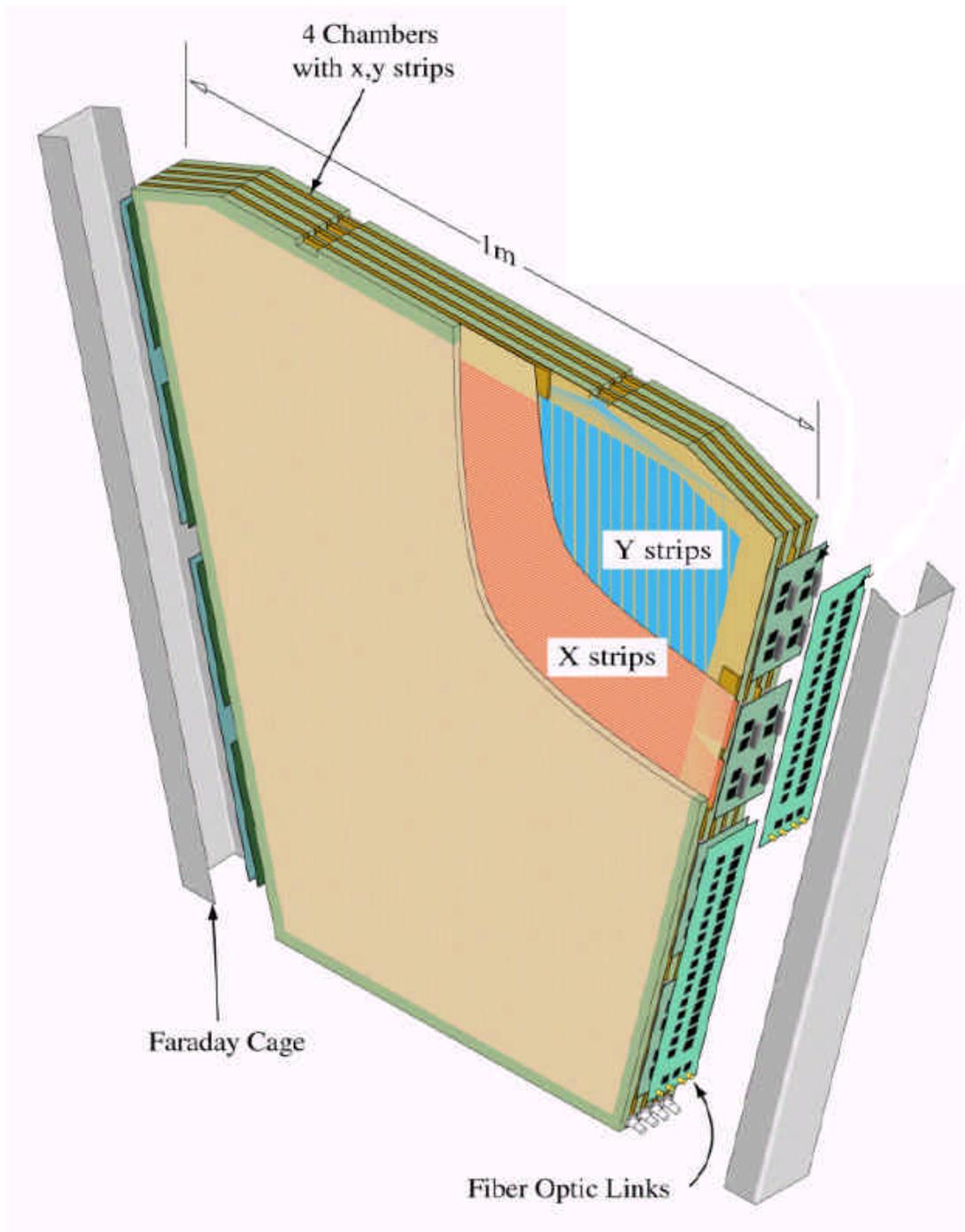
ASM-I

- 96 channels
- 16 Preamp/Shaper ASICs

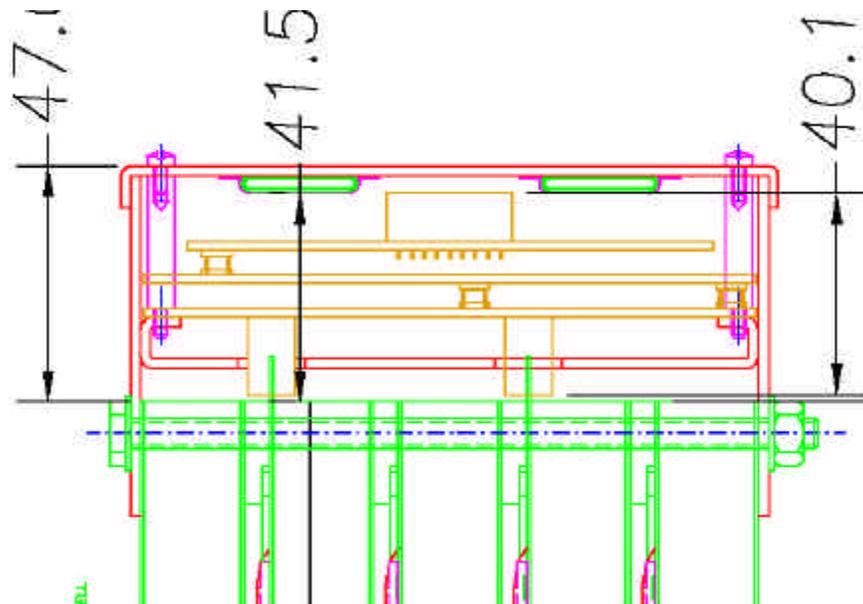
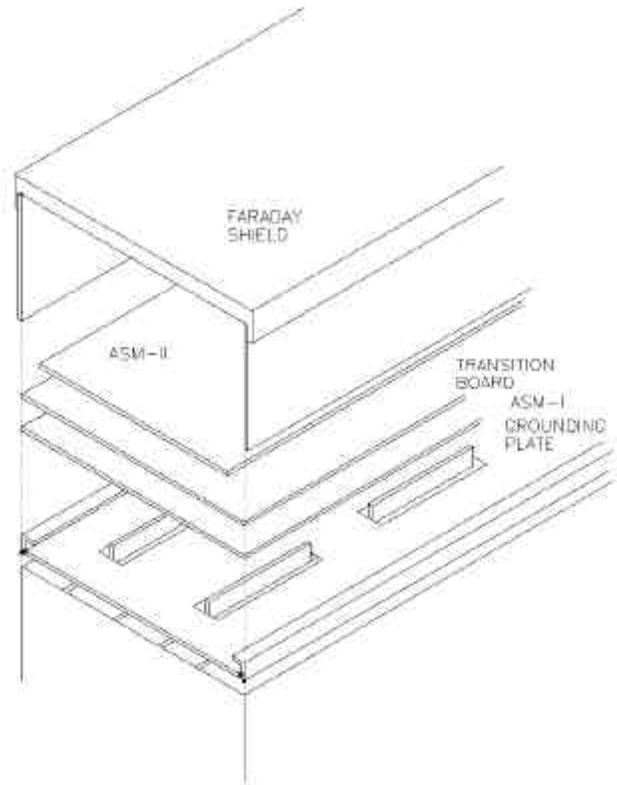
CSC On-Detector Electronics



CSC Mechanics

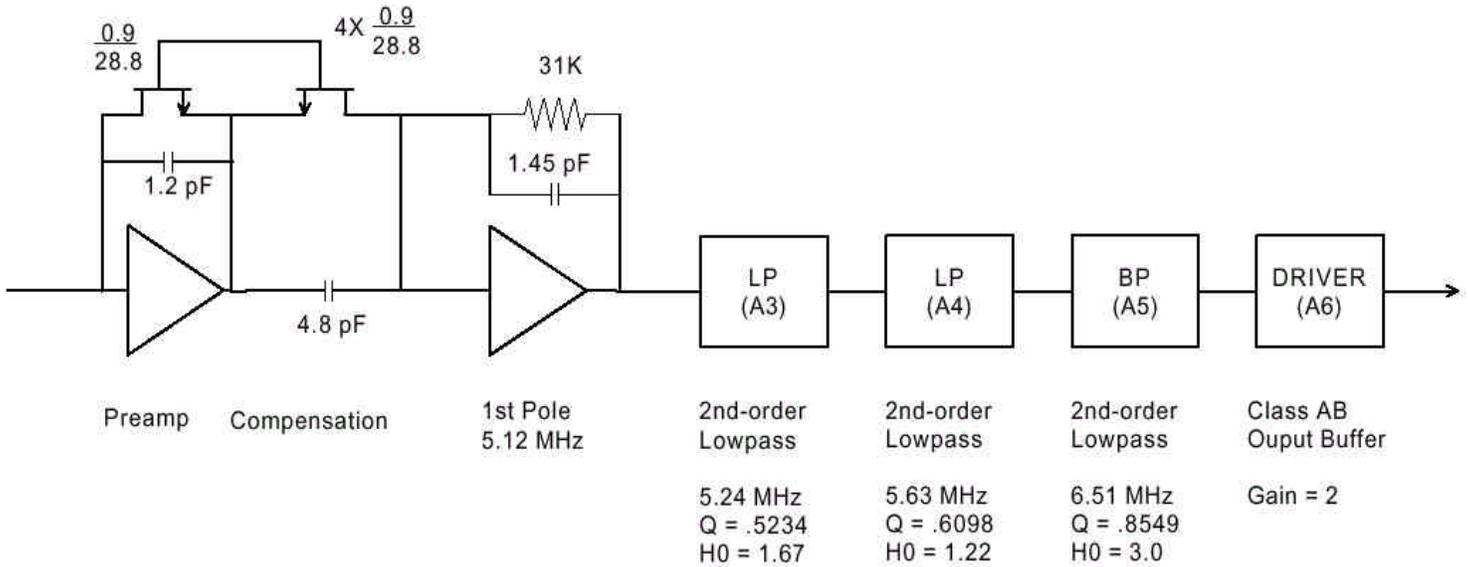


CSC On-detector Electronics Mounting



CSC Preamplifier/Shaper IC (IC50)

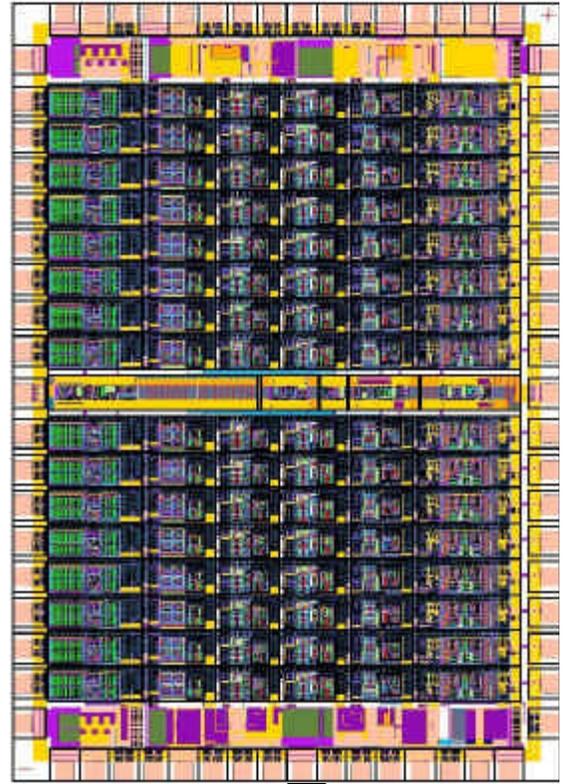
Block Diagram



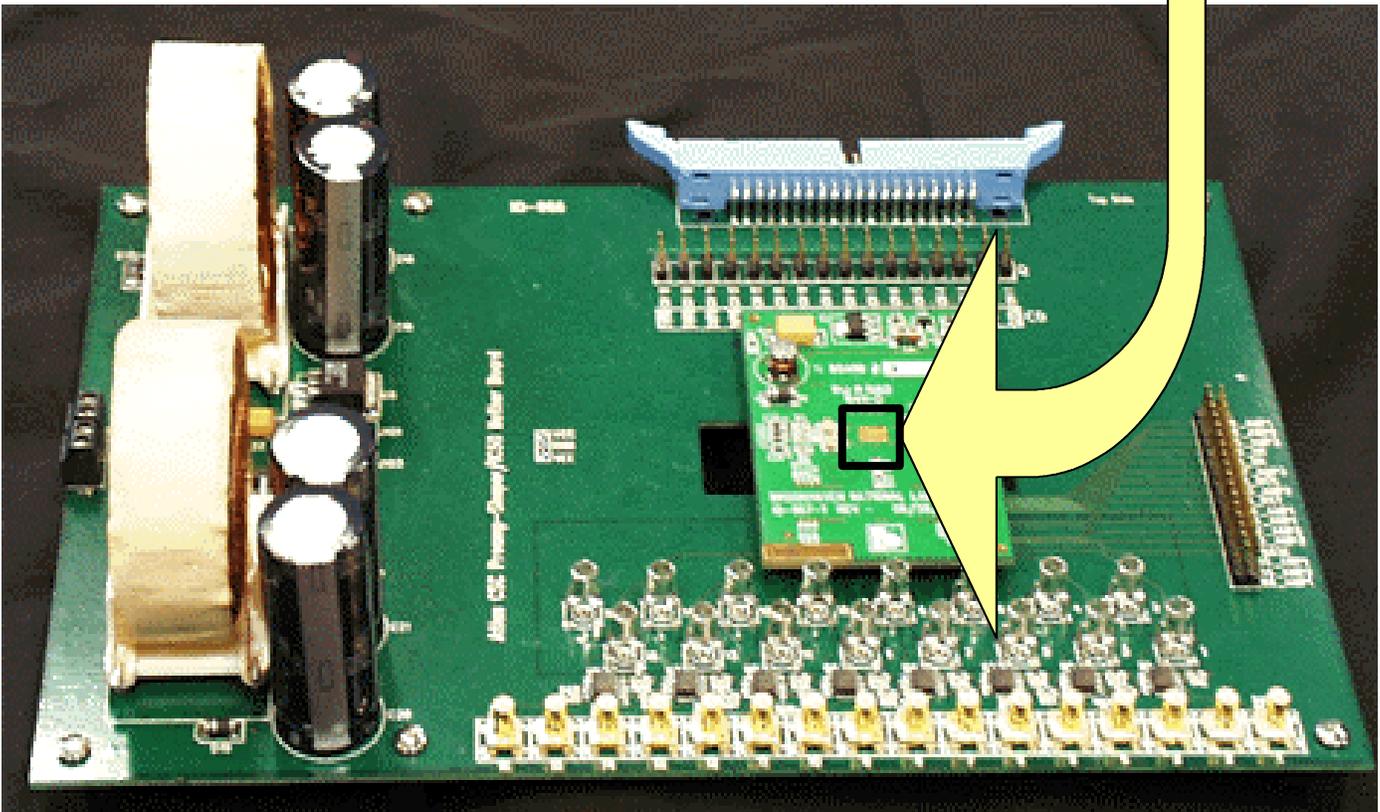
Technology	0.5 μ m CMOS
Channels	16
Die size	2.78 x 3.96 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 μ m, $I_d = 4$ mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7 th order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FW1%M	340 ns
Max. output loading (3% distortion)	500 Ω , 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent channel
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

CSC Preamp/shaper

Die Layout

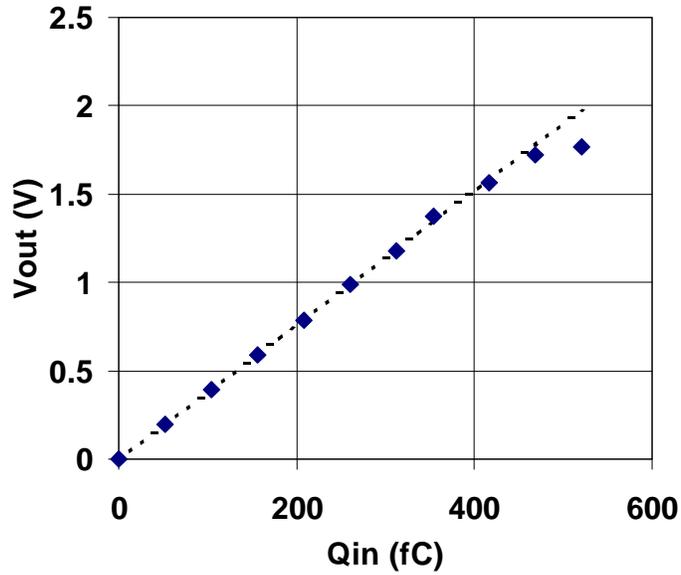


Test board

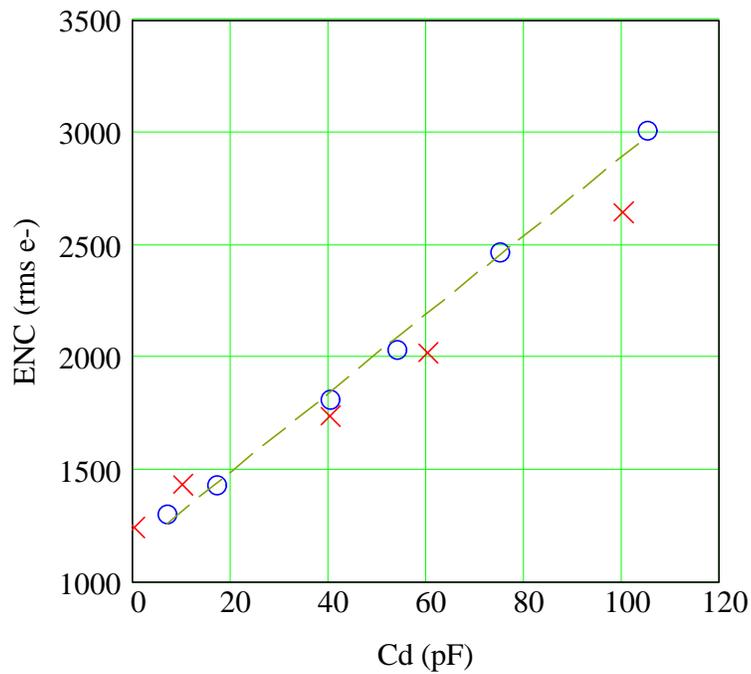


Preamp/Shaper Results

Linearity



Noise vs. capacitance



Simulated: ×

Measured: ○

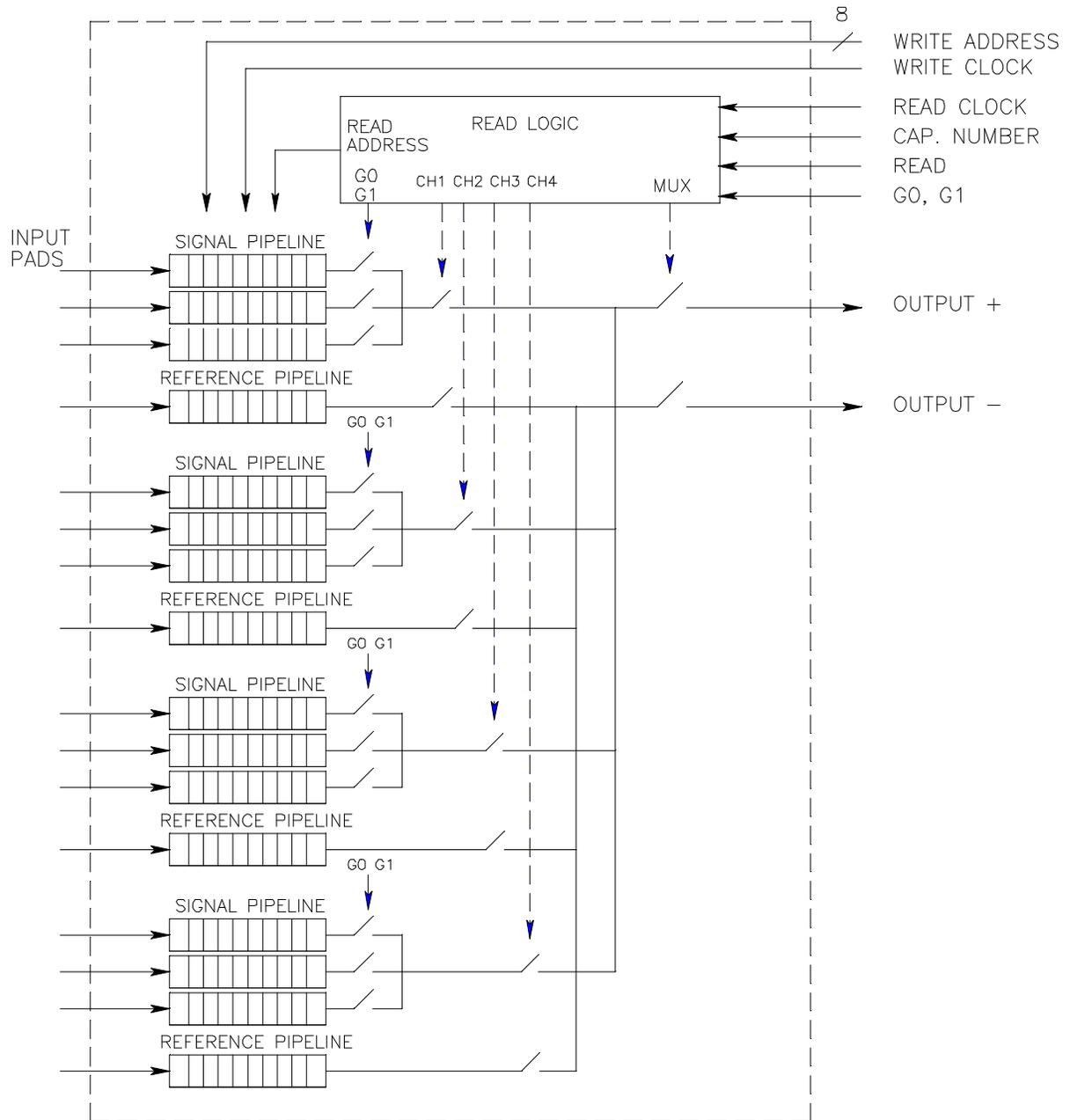
SCA Block Diagram

144 cells/channel

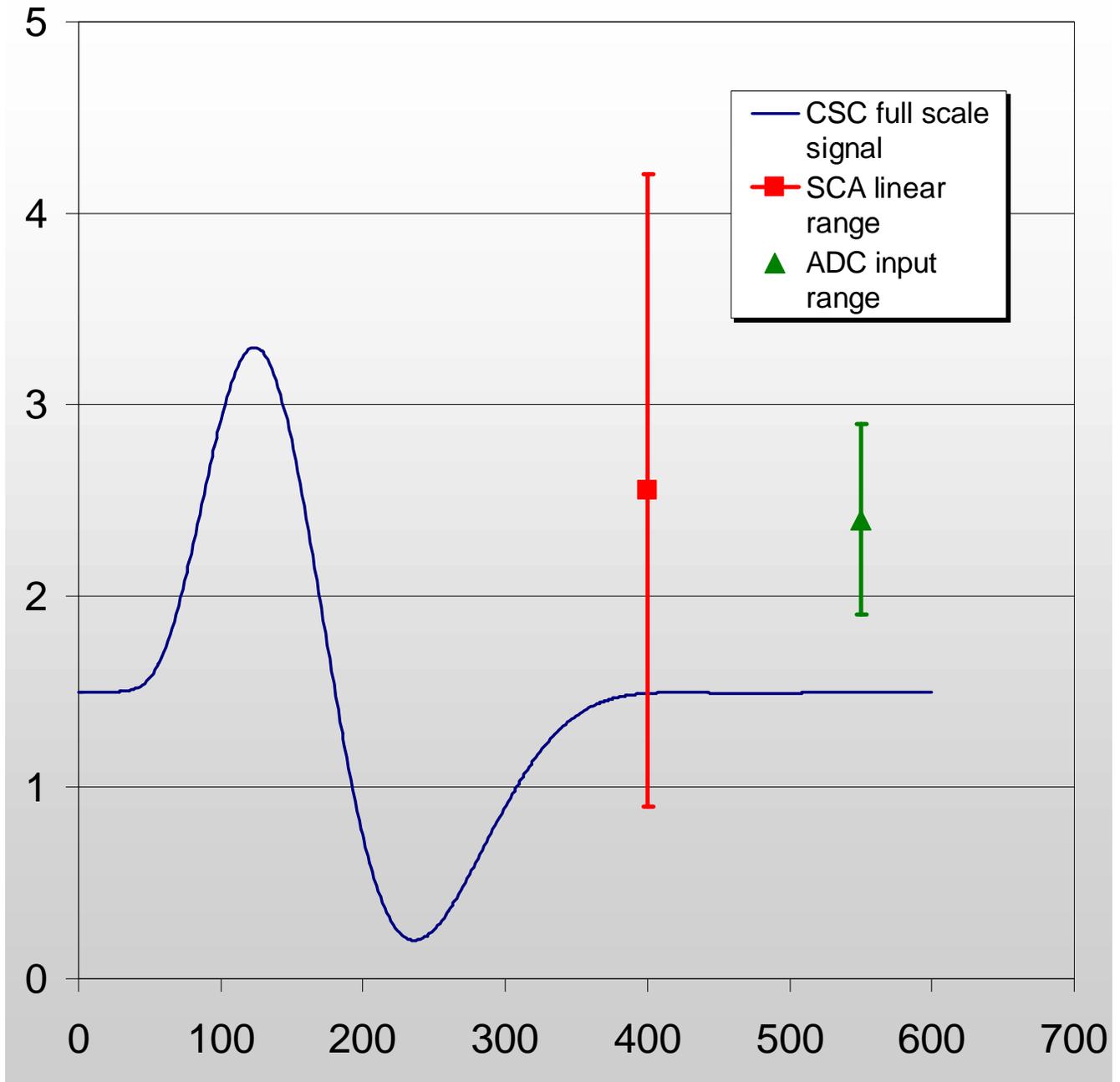
16 channels, organized as 4 groups of (3 + 1 reference)

Simultaneous read and write (deadtimeless)

Read logic modified 5/99 for CSC

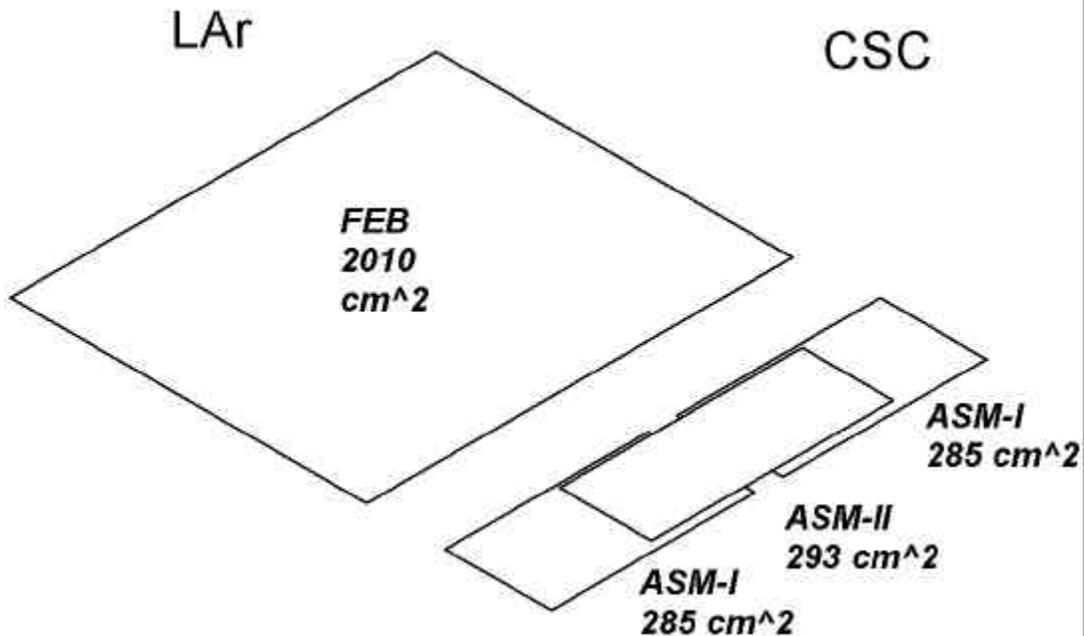


Signal levels in the CSC



Comparison of the LAr FEB and the CSC ASM-PACK

	LAr-FEB	CSC-ASM	Units
Channels	128	192	-
Gain ranges	3	1	-
Total board area	2010	580	cm ²
Signal levels:			
<i>baseline</i>	0.0	+1.5	V
<i>max.</i>	+2.5	+3.2	V
<i>min.</i>	-0.9	0.0	V
Power dissipation	85	35	W
Sampling rate	40	20	MHz
No. samples/trigger	5	4	-
Bits/sample	12	12	-
Raw data rate	896	922	Mbits/s



Summary – CSC On-detector Electronics

- Analog signal processing tuned for good S/N in ATLAS high rate, high background environment
- 10-b dynamic range
- Analog memory for data buffering with minimal deadtime
- SCA, digitization, data link based on LAr calorimeter system but with remote controller
- Engineered for robustness and reliability by minimizing hardware in this inaccessible, high radiation location