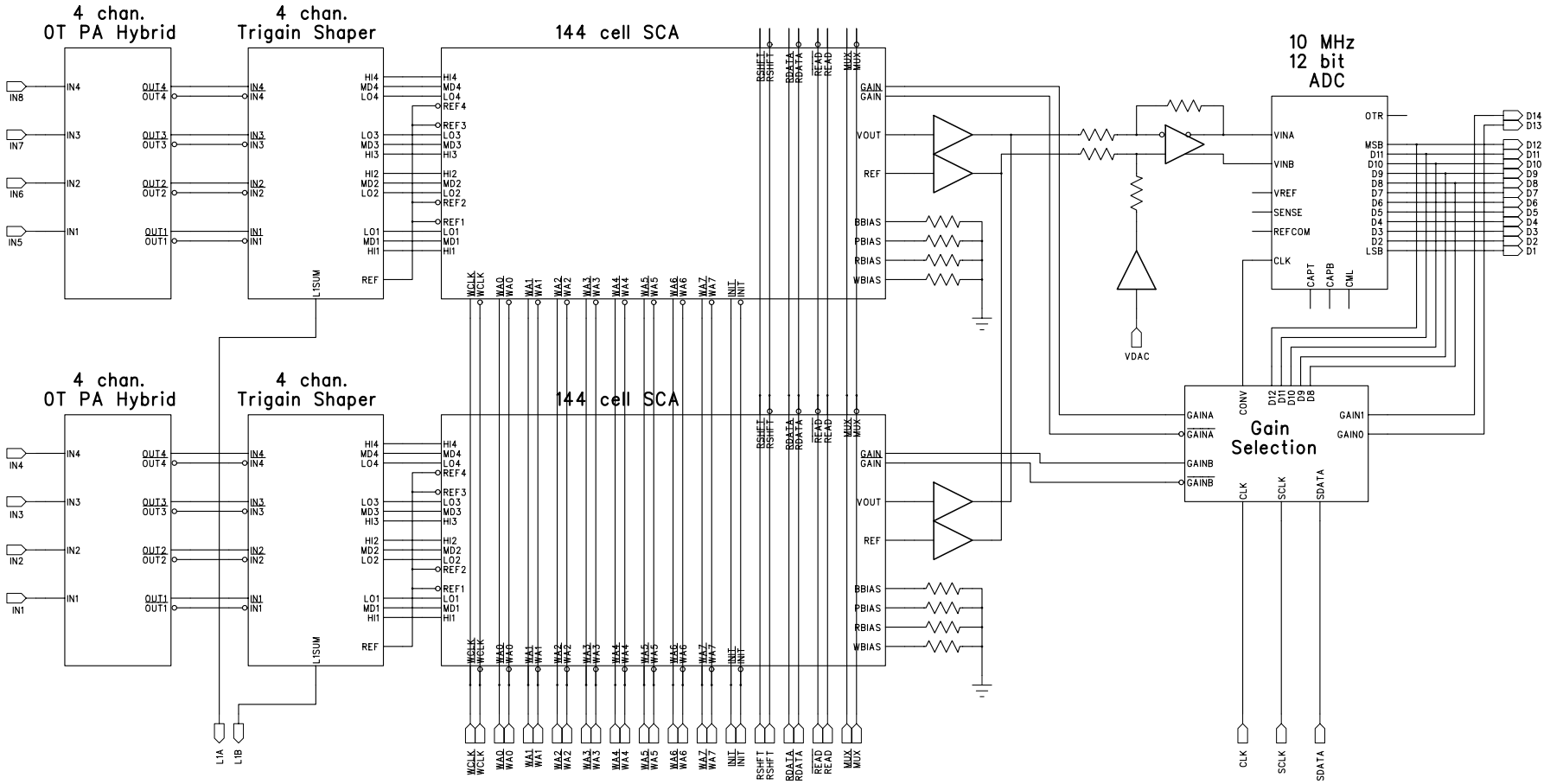
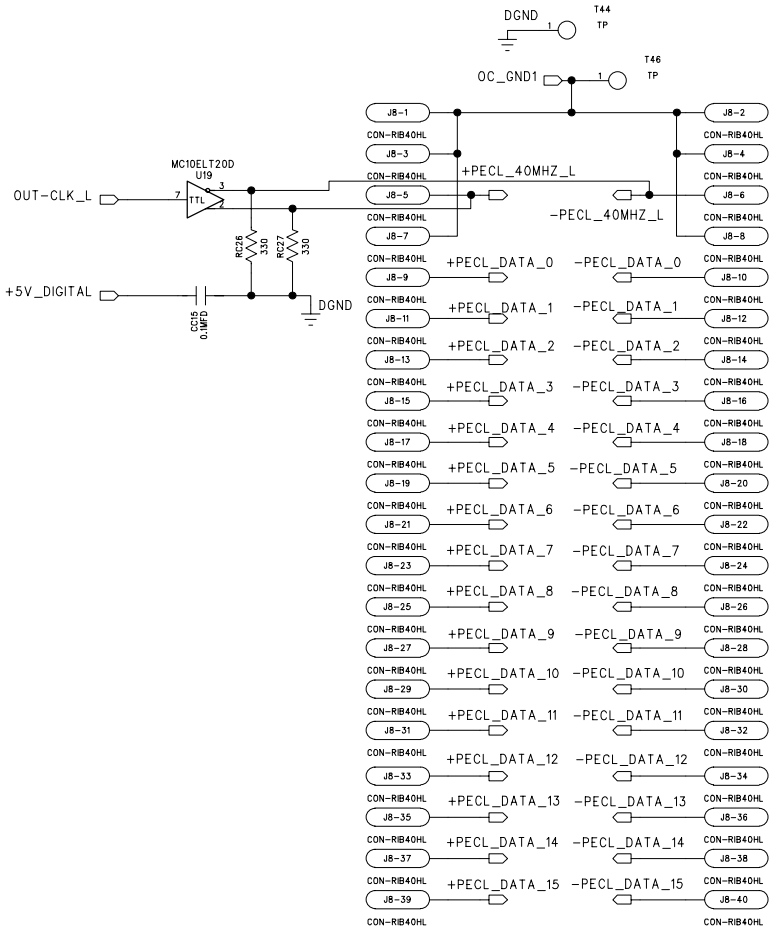

4 chan.
OT PA Hybrid
4 chan.
Trigain Shaper
144 cell SCA
10 MHz
12 bit
ADC
4 chan.
OT PA Hybrid
4 chan.
Trigain Shaper
144 cell SCA
Gain
Selection
VDAC
L1A
L1B
CLK
SCLK
SDATA

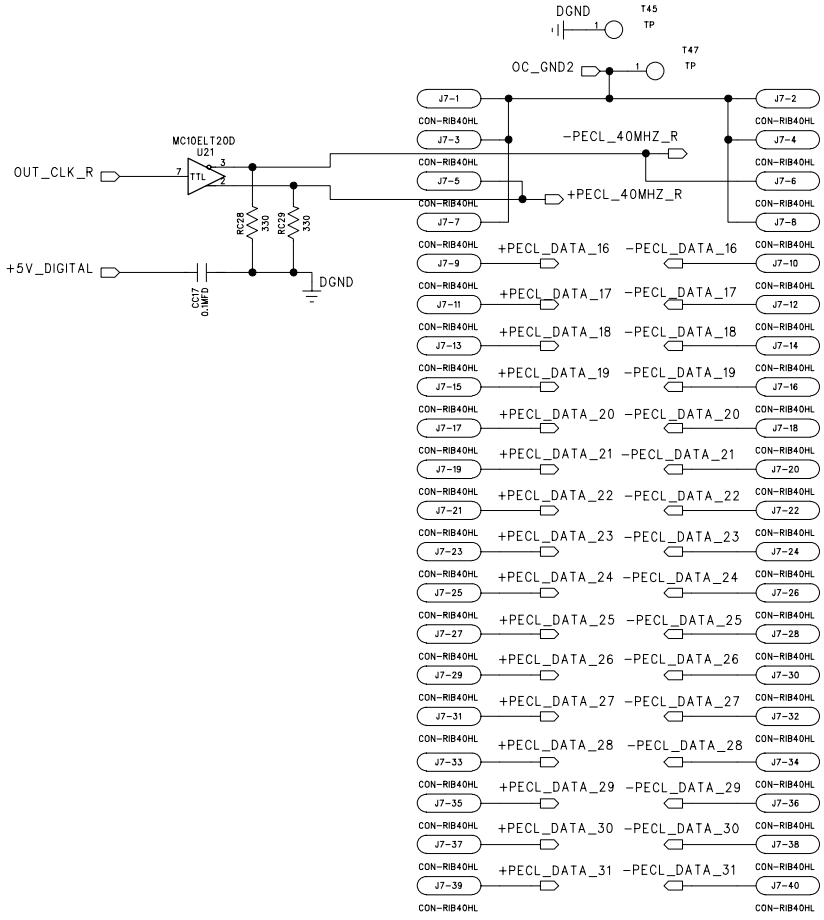
REVISION RECORD			
			DATE:

DRAWN:	DATED:	
CHECKED:	DATED:	
QUALITY CONTROL:	DATED:	
RELEASED:	DATED:	

COMPANY:			
TITLE:			
CODE:		DRAWING NO:	
SCALE:			

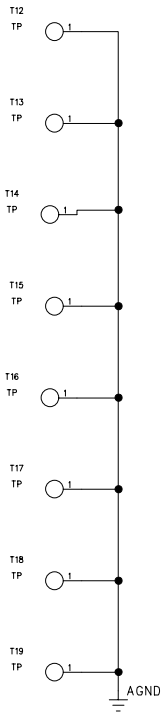
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

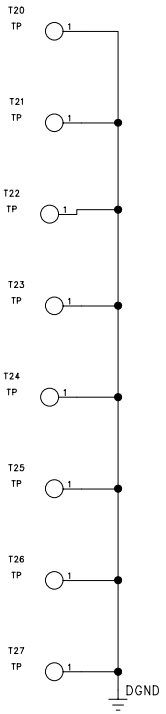


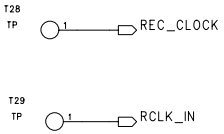


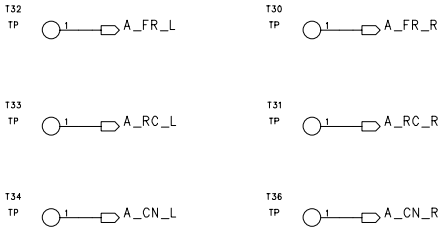
DRAWN:	DATED:	COMPANY: NEVIS LABS–COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Output connector	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED: jb	DATED: march/98	SCALE:	SHEET: OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

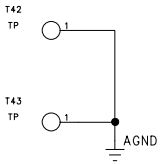


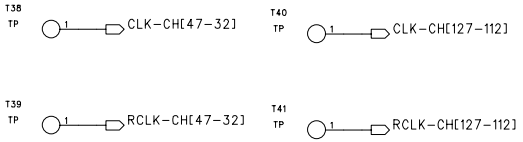




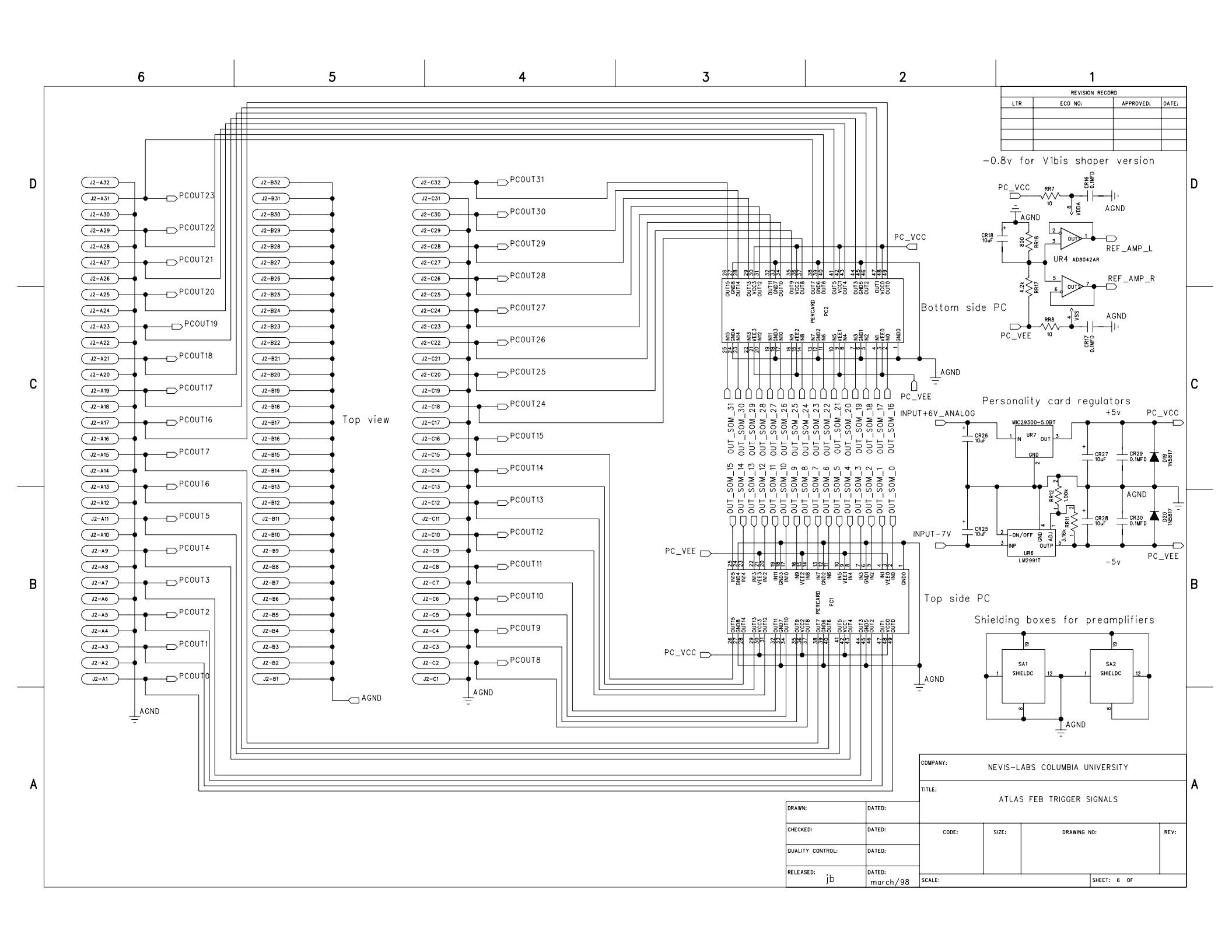


TP at the end of SCA busses



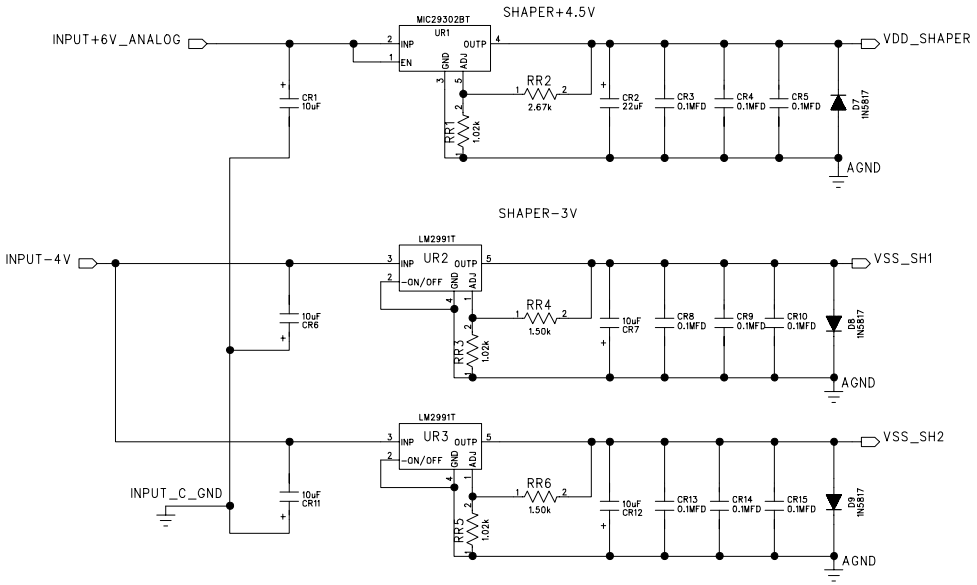


DRAWN:	DATED:	COMPANY: NEVIS LABS–COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Test points and misc	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO: / REV:	
RELEASED: jb	DATED: feb./98	SCALE:	SHEET: OF

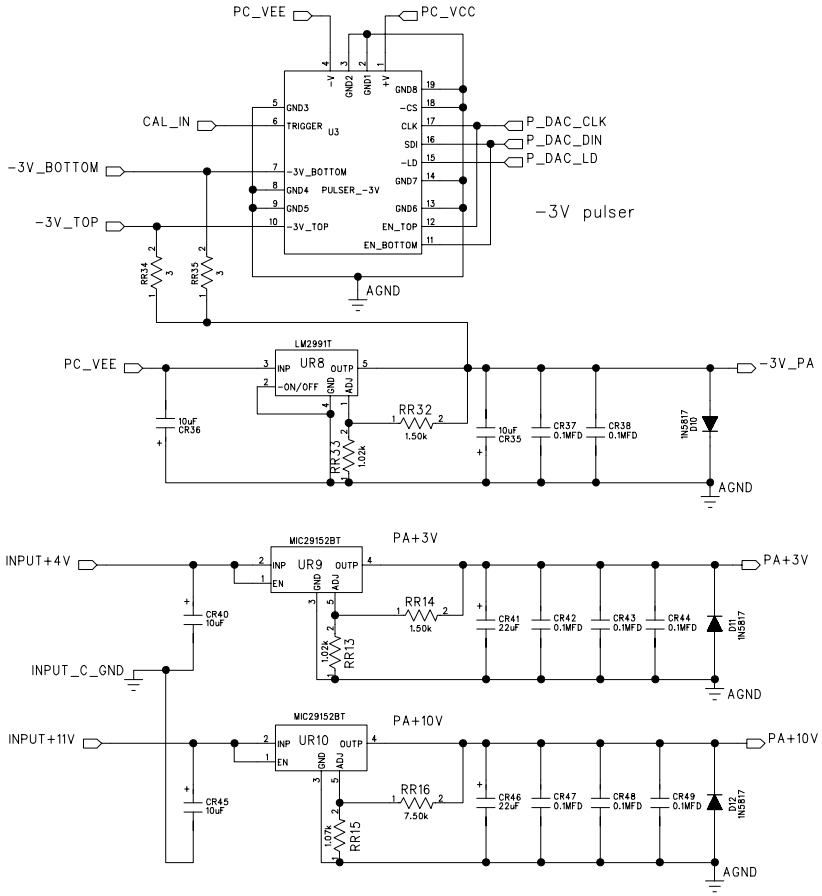

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
−0.8v for V1bis shaper version
Top view
Bottom side PC
Top side PC
Personality card regulators
Shielding boxes for preamplifiers
PERCARD
PC1
PC2
UR4 AD8042AR
UR6 LM2991T
UR7 MIC29300-5.0BT
REF_AMP_L
REF_AMP_R
INPUT+6V_ANALOG
INPUT−7V
+5v
−5v
PC_VCC
PC_VEE
AGND
SA1 SHIELDC
SA2 SHIELDC
COMPANY: NEVIS−LABS COLUMBIA UNIVERSITY
TITLE: ATLAS FEB TRIGGER SIGNALS
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED: jb
DATED: march/98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 6 OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Shaper regulators



Preamplifier regulators

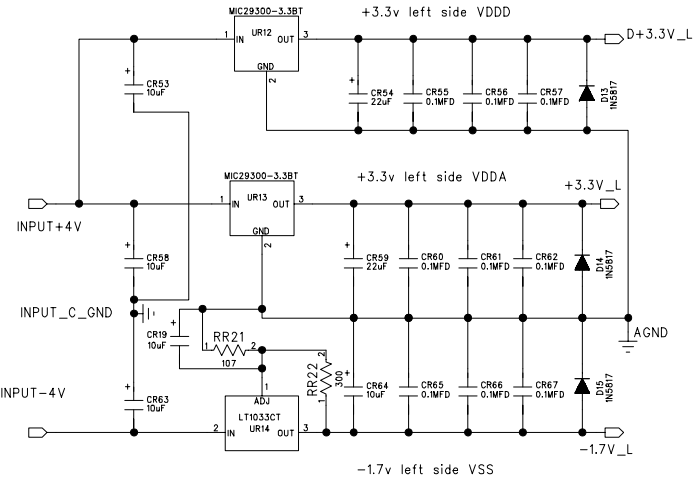


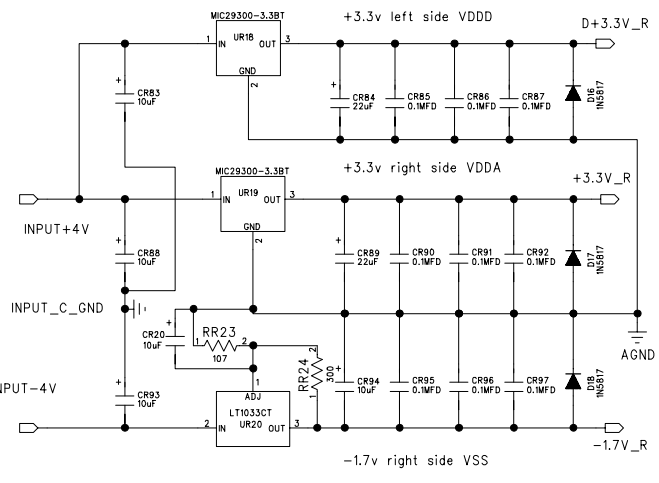
DRAWN:	DATED:	COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Shaper,preamp and PC regulators	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED: jb	DATED: march/98	SCALE:	SHEET: 4 OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

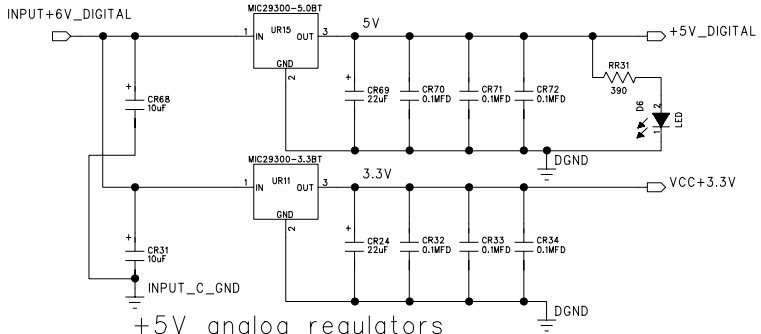
SCA regulators

(not populated for AC version)



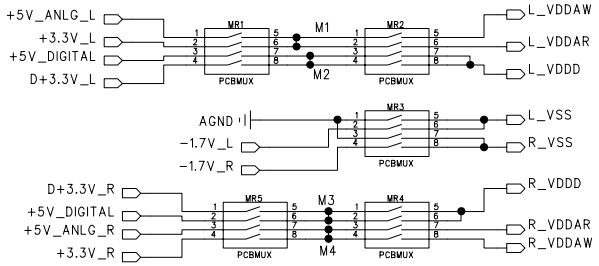


Digital regulators

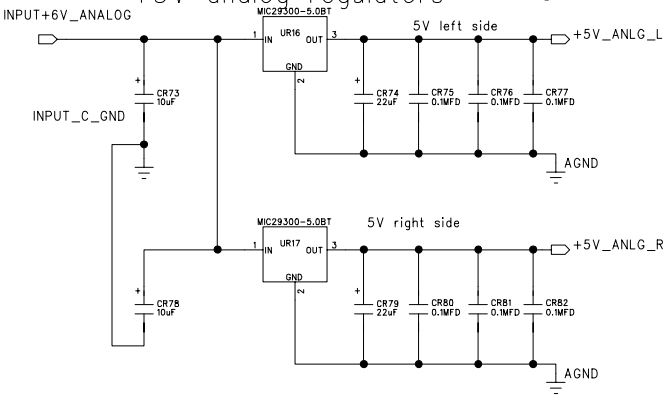


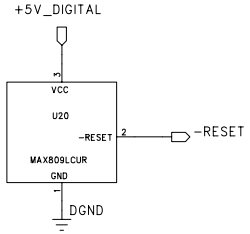
AC/DC voltage selection

PCBMUX are jumpers/printings on the board

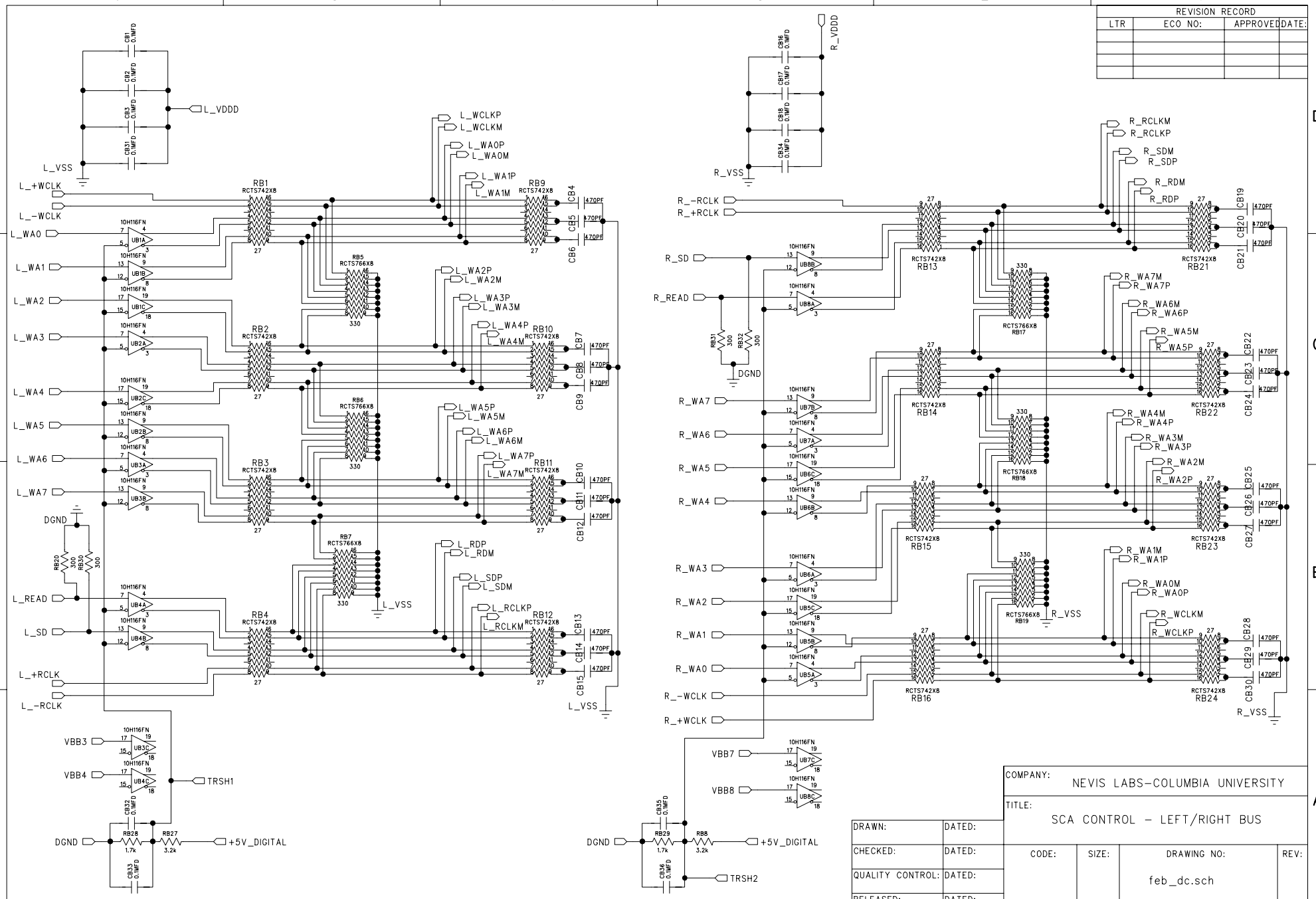


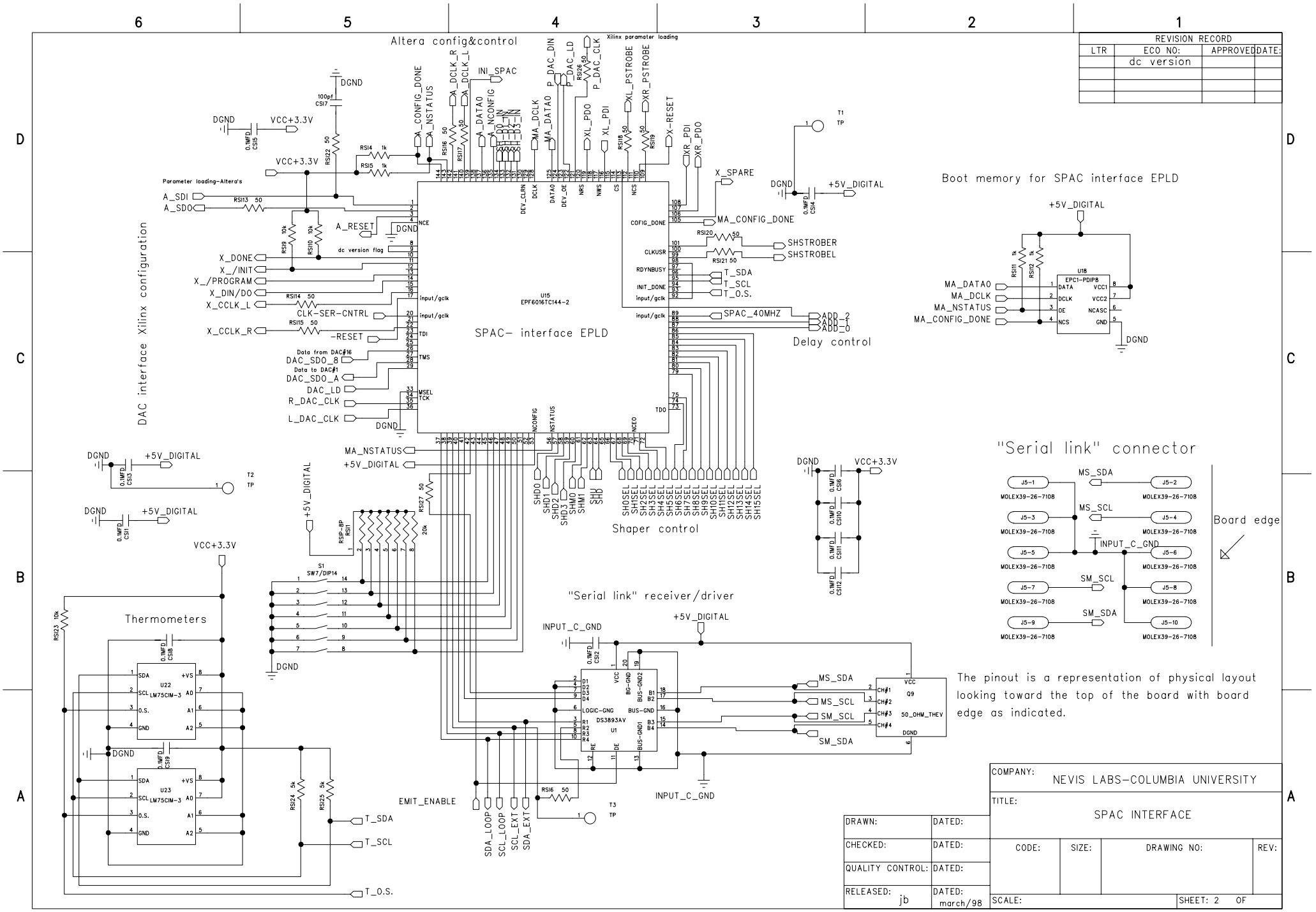
+5V analog regulators





COMPANY: NEVIS LABS–COLUMBIA UNIVERSITY			
TITLE: Back–end regulators			
DRAWN:	DATED:	CODE:	SIZE: DRAWING NO: REV:
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED: jb	DATED: march/98	SCALE:	SHEET: 5 OF

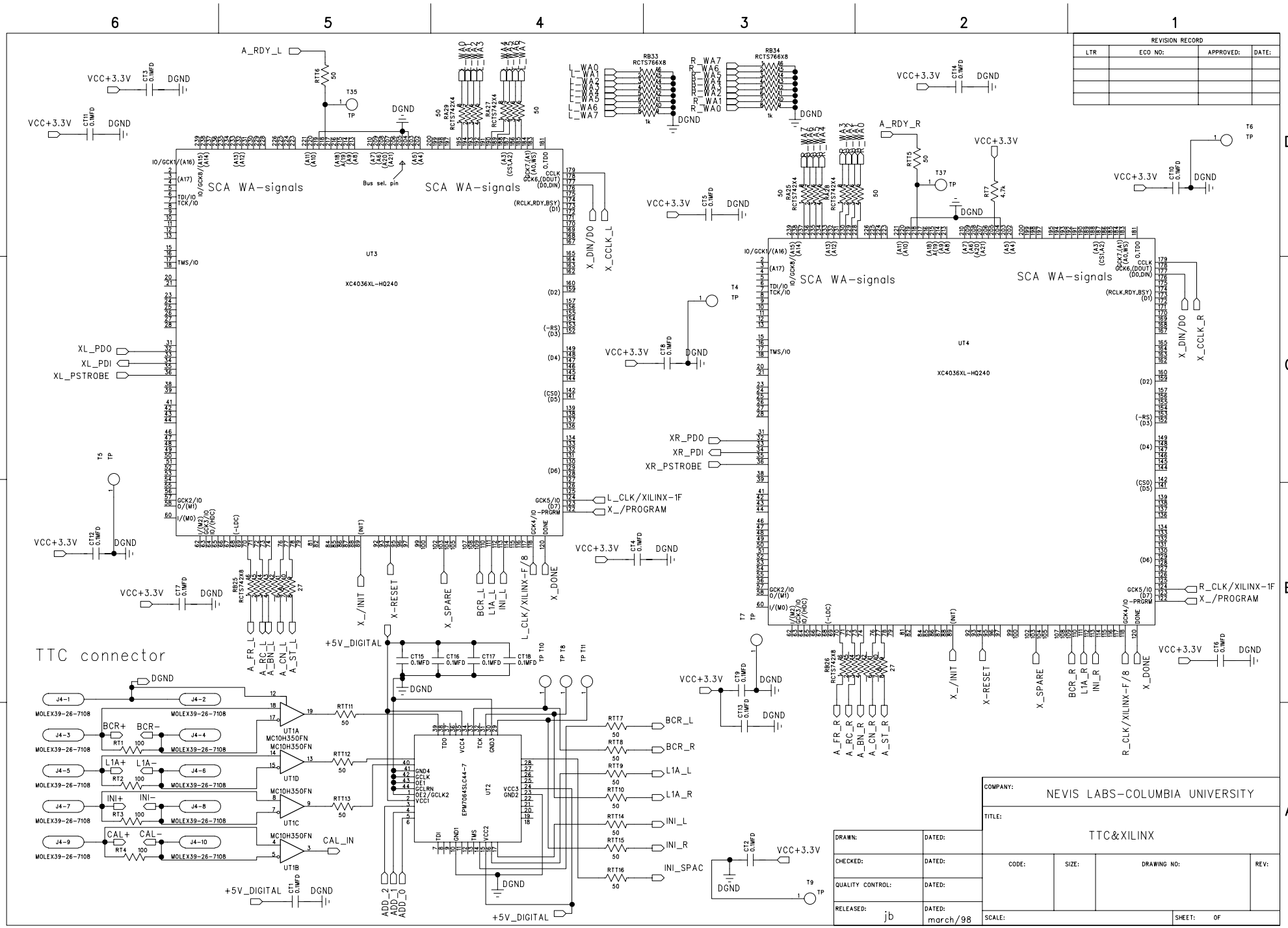

REVISION RECORD
LTR
ECO NO:
APPROVED
DATE:
L_VDDD
L_VSS
L_+WCLK
L_-WCLK
L_WA0
L_WA1
L_WA2
L_WA3
L_WA4
L_WA5
L_WA6
L_WA7
L_READ
L_SD
L_+RCLK
L_-RCLK
L_WCLKP
L_WCLKM
L_WA0P
L_WA0M
L_WA1P
L_WA1M
L_WA2P
L_WA2M
L_WA3P
L_WA3M
L_WA4P
L_WA4M
L_WA5P
L_WA5M
L_WA6P
L_WA6M
L_WA7P
L_WA7M
L_RDP
L_RDM
L_SDP
L_SDM
L_RCLKP
L_RCLKM
DGND
TRSH1
VBB3
VBB4
+5V_DIGITAL
R_VDDD
R_VSS
R_-RCLK
R_+RCLK
R_SD
R_READ
R_WA7
R_WA6
R_WA5
R_WA4
R_WA3
R_WA2
R_WA1
R_WA0
R_-WCLK
R_+WCLK
R_RCLKM
R_RCLKP
R_SDM
R_SDP
R_RDM
R_RDP
R_WA7M
R_WA7P
R_WA6M
R_WA6P
R_WA5M
R_WA5P
R_WA4M
R_WA4P
R_WA3M
R_WA3P
R_WA2M
R_WA2P
R_WA1M
R_WA1P
R_WA0M
R_WA0P
R_WCLKM
R_WCLKP
VBB7
VBB8
TRSH2
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SCA CONTROL - LEFT/RIGHT BUS
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
ban
DATED:
march/98
CODE:
SIZE:
DRAWING NO:
feb_dc.sch
REV:
SCALE:
SHEET: 1 OF

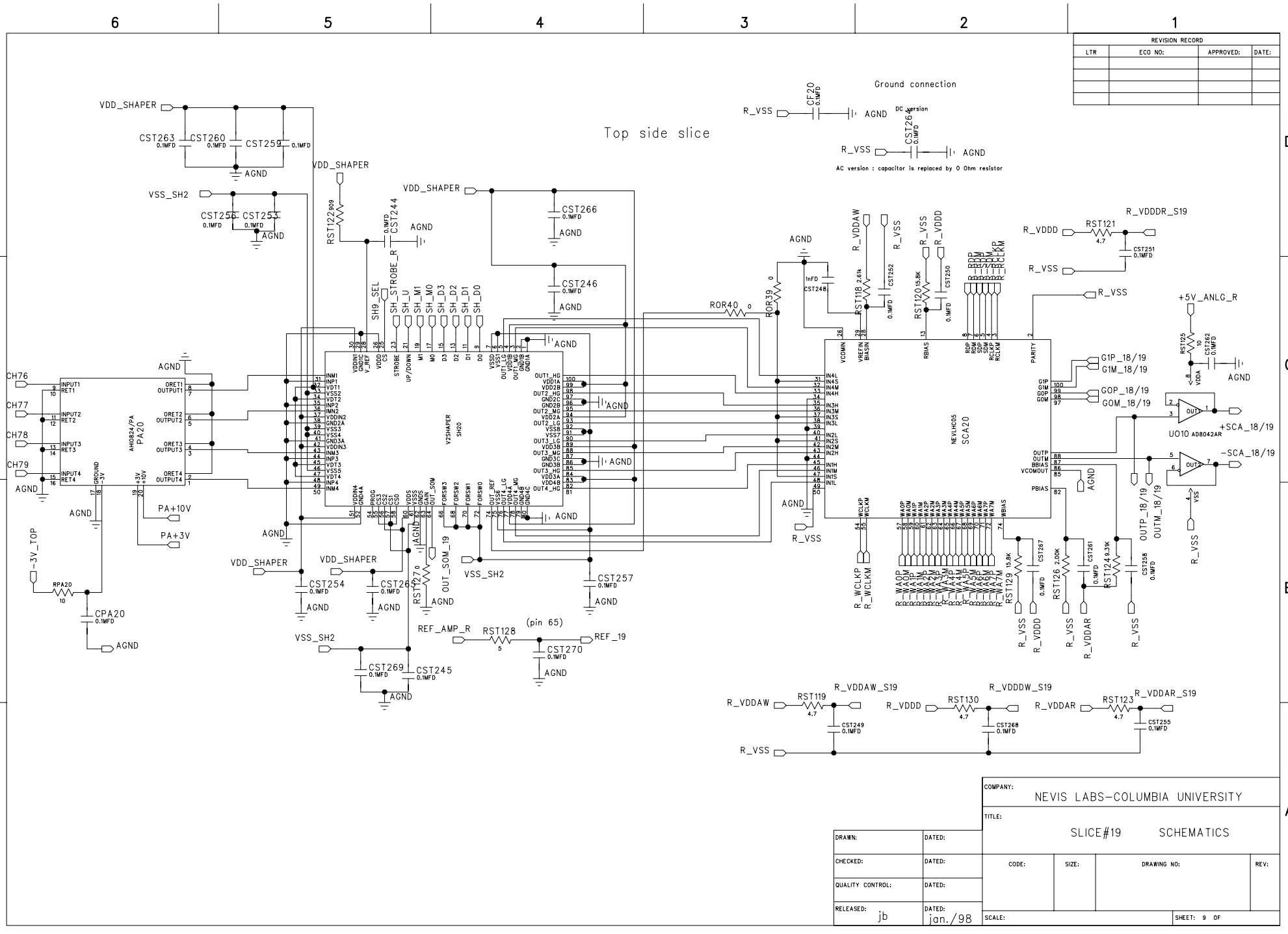


The pinout is a representation of physical layout looking toward the top of the board with board edge as indicated.

REVISION RECORD			
LTR	ECO NO:	APPROVED	DATE:
	dc version		

DRAWN:	DATED:	COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY			
CHECKED:	DATED:	TITLE: SPAC INTERFACE			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
RELEASED: jb	DATED: march/98	SCALE:		SHEET: 2 OF	


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
SCA WA-signals
SCA WA-signals
SCA WA-signals
UT3
XC4036XL-HQ240
UT4
XC4036XL-HQ240
TTC connector
UT1A
UT1B
UT1C
UT1D
UT2
EPM7064SLC44-7
A_RDY_L
A_RDY_R
XL_PDO
XL_PDI
XL_PSTROBE
XR_PDO
XR_PDI
XR_PSTROBE
X_DIN/DO
X_CCLK_L
X_CCLK_R
L_CLK/XILINX-1F
X_/PROGRAM
R_CLK/XILINX-1F
X_/INIT
X-RESET
X_SPARE
BCR_L
L1A_L
INI_L
L_CLK/XILINX-F/8
X_DONE
A_FR_L
A_RC_L
A_BN_L
A_CN_L
A_ST_L
+5V_DIGITAL
CAL_IN
BCR_R
L1A_R
INI_R
INI_SPAC
ADD_2
ADD_1
ADD_0
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
TTC&XILINX
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
march/98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF

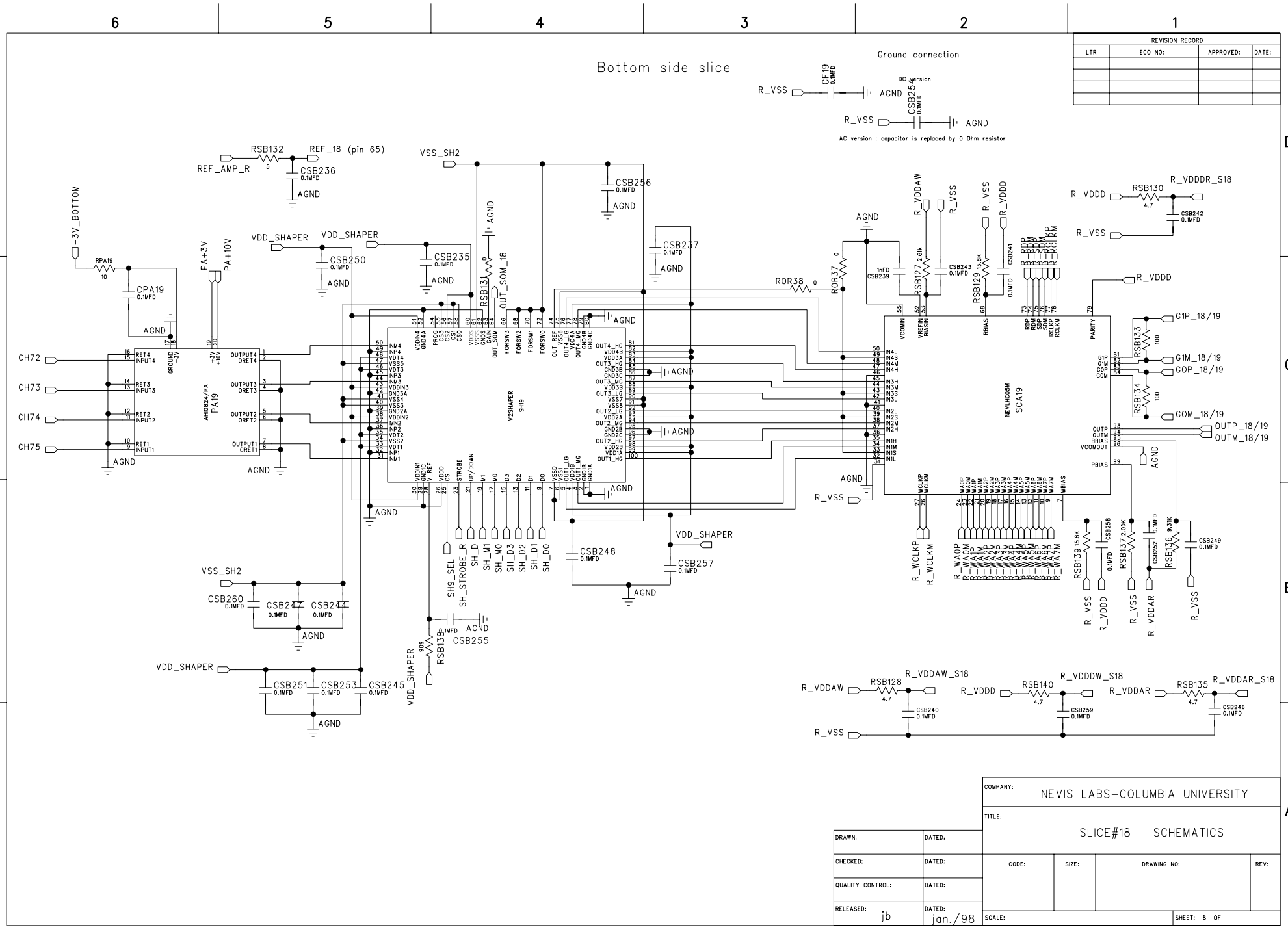


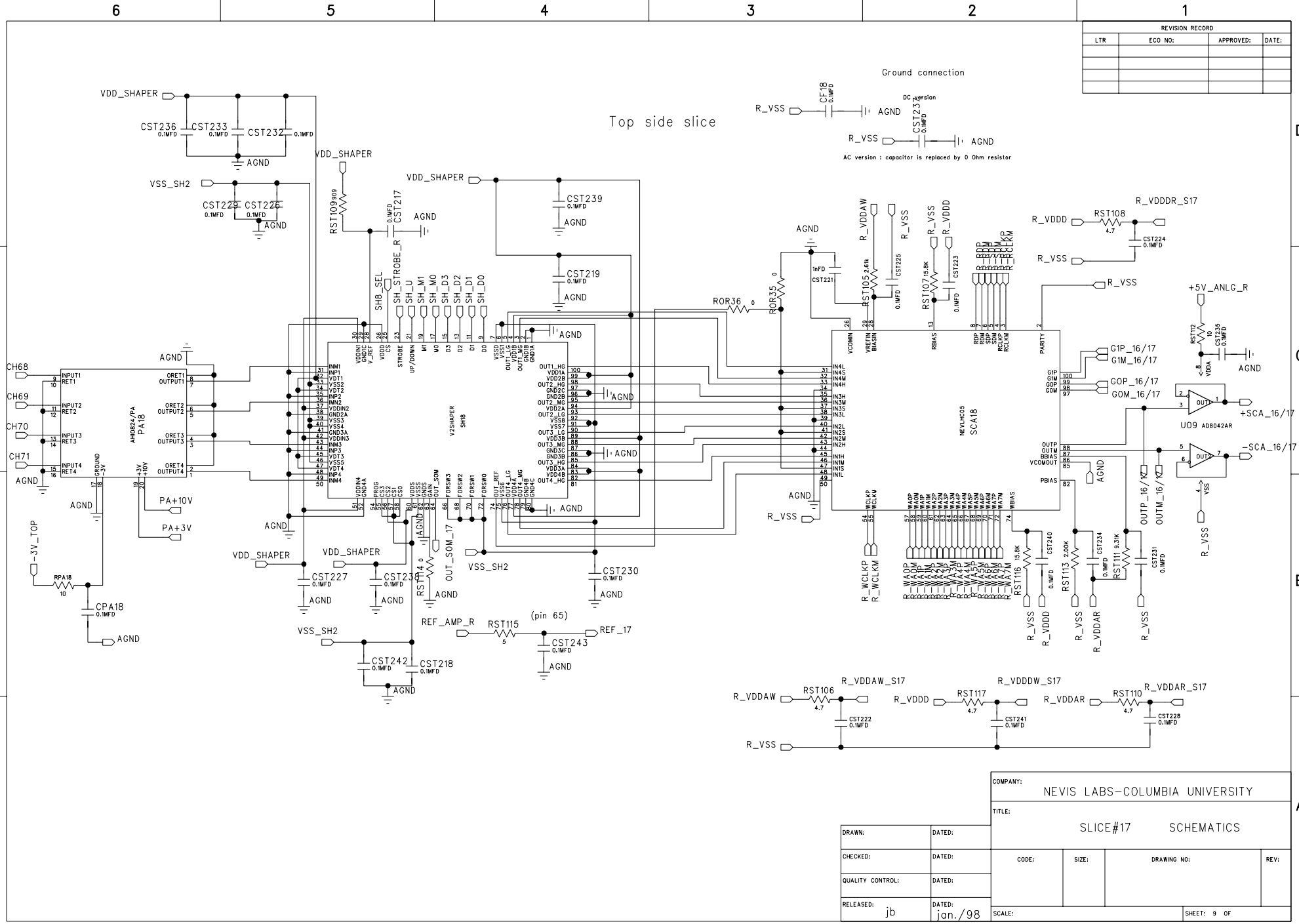
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY

TITLE: SLICE#19 SCHEMATICS

DRAWN:	DATED:				
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED: jb	DATED: jan./98	SCALE:		SHEET: 9 OF	


Bottom side slice
Ground connection
DC version
AC version : capacitor is replaced by 0 Ohm resistor
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
-3V_BOTTOM
PA+3V
PA+10V
REF_AMP_R
REF_18 (pin 65)
VSS_SH2
VDD_SHAPER
OUT_SOM_18
AGND
R_VSS
R_VDDD
R_VDDAW
R_VDDAR
R_VDDDR_S18
R_VDDAW_S18
R_VDDDW_S18
R_VDDAR_S18
R_WCLKP
R_WCLKM
R_WAOP
R_WAOM
CH72
CH73
CH74
CH75
AHH0824/PA
PA19
V2SHAPER
SH9
NEVLHCO5M
SCA19
G1P_18/19
G1M_18/19
GOP_18/19
GOM_18/19
OUTP_18/19
OUTM_18/19
SH9_SEL
SH_STROBE_R
SH_D
SH_M1
SH_M0
SH_D3
SH_D2
SH_D1
SH_D0
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SLICE#18 SCHEMATICS
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 8 OF

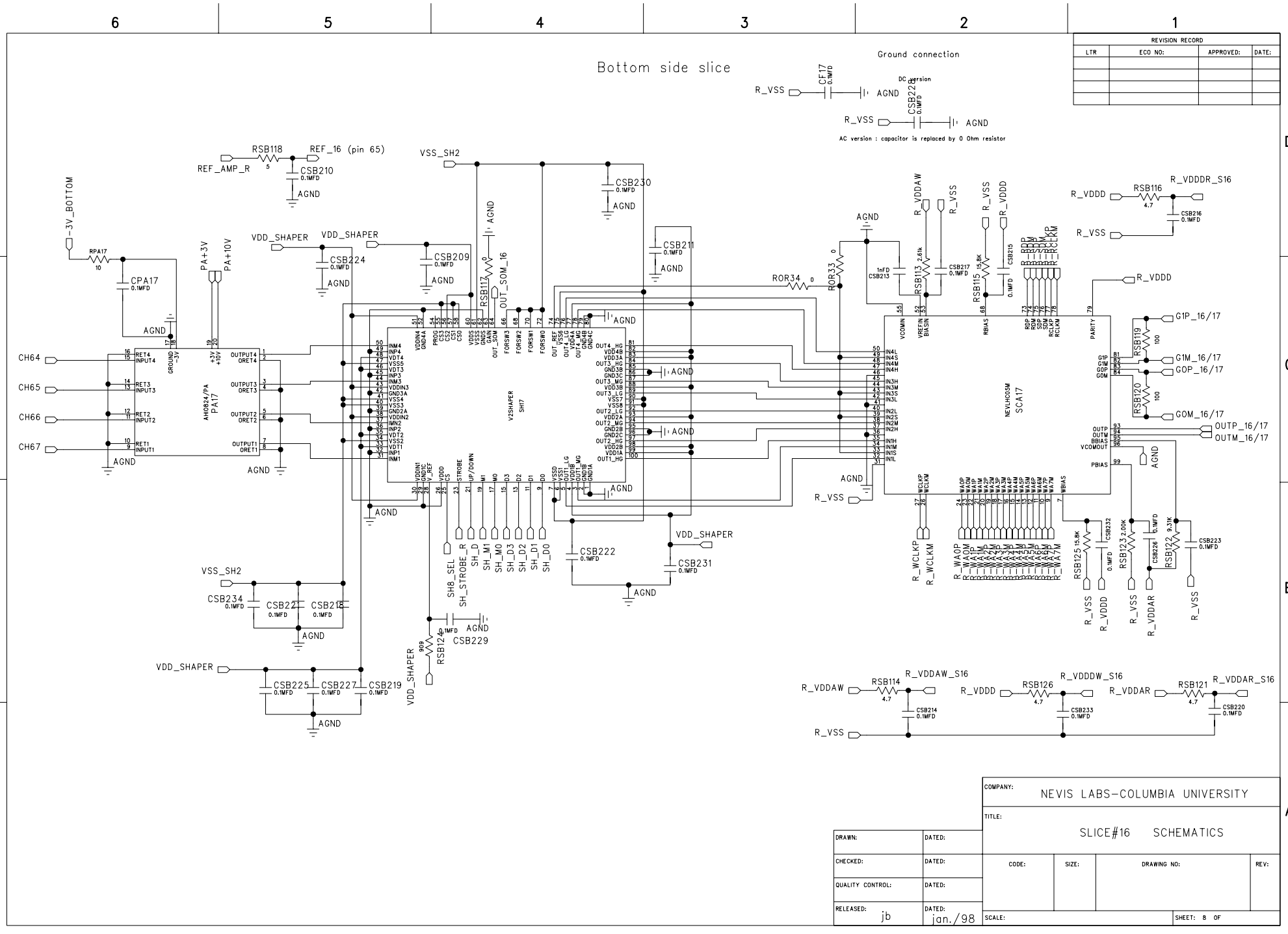


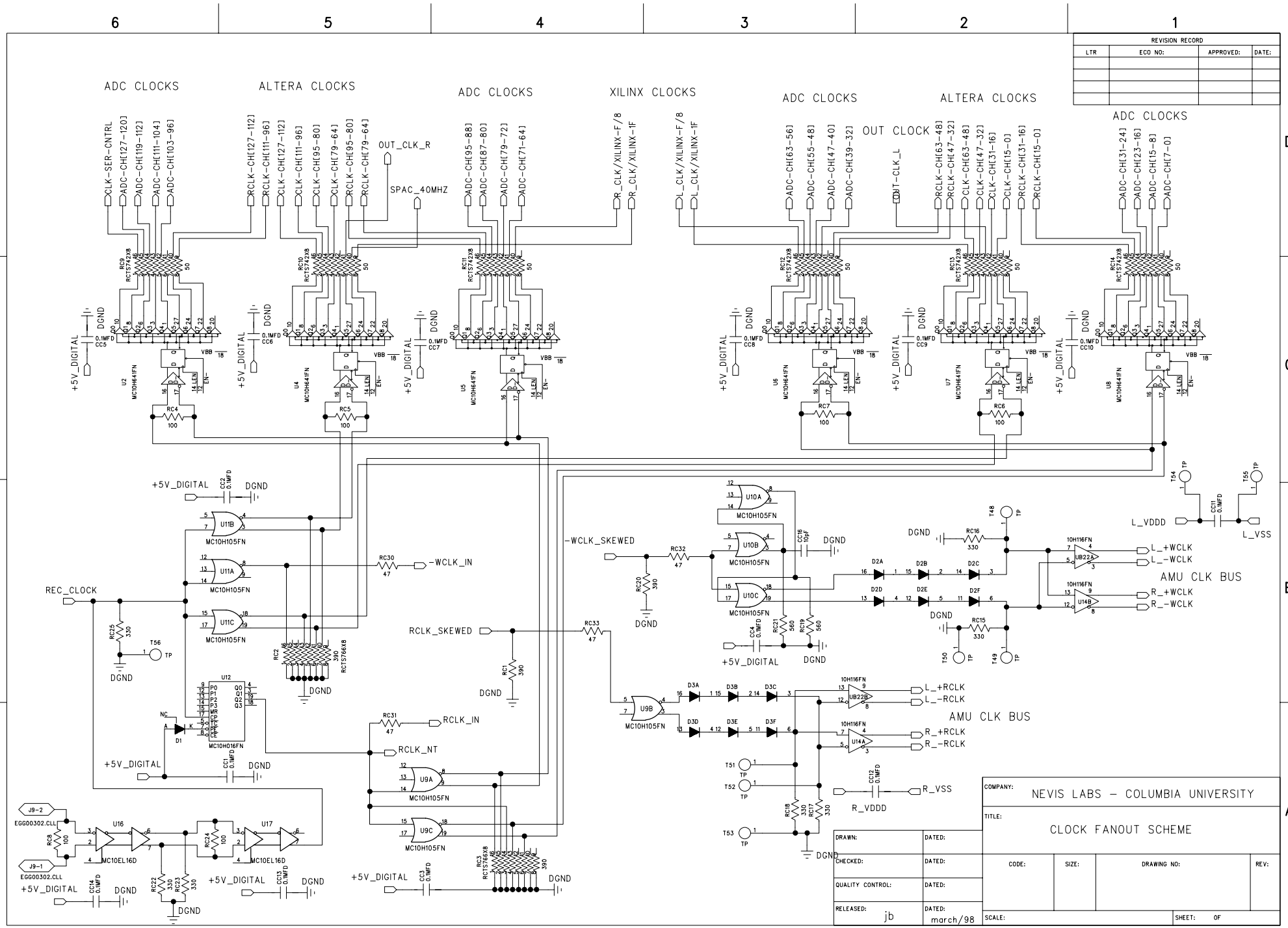
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

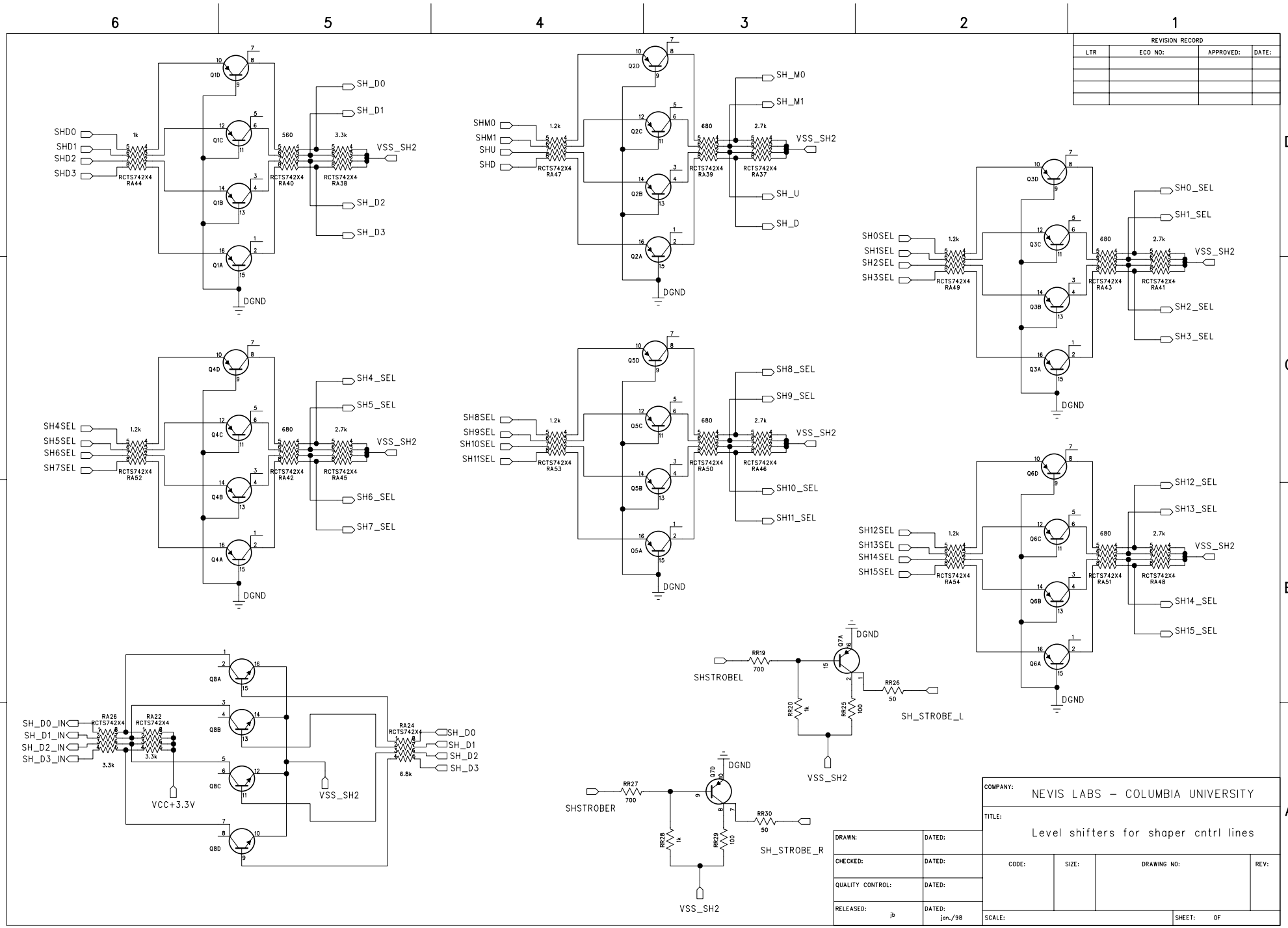
COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY

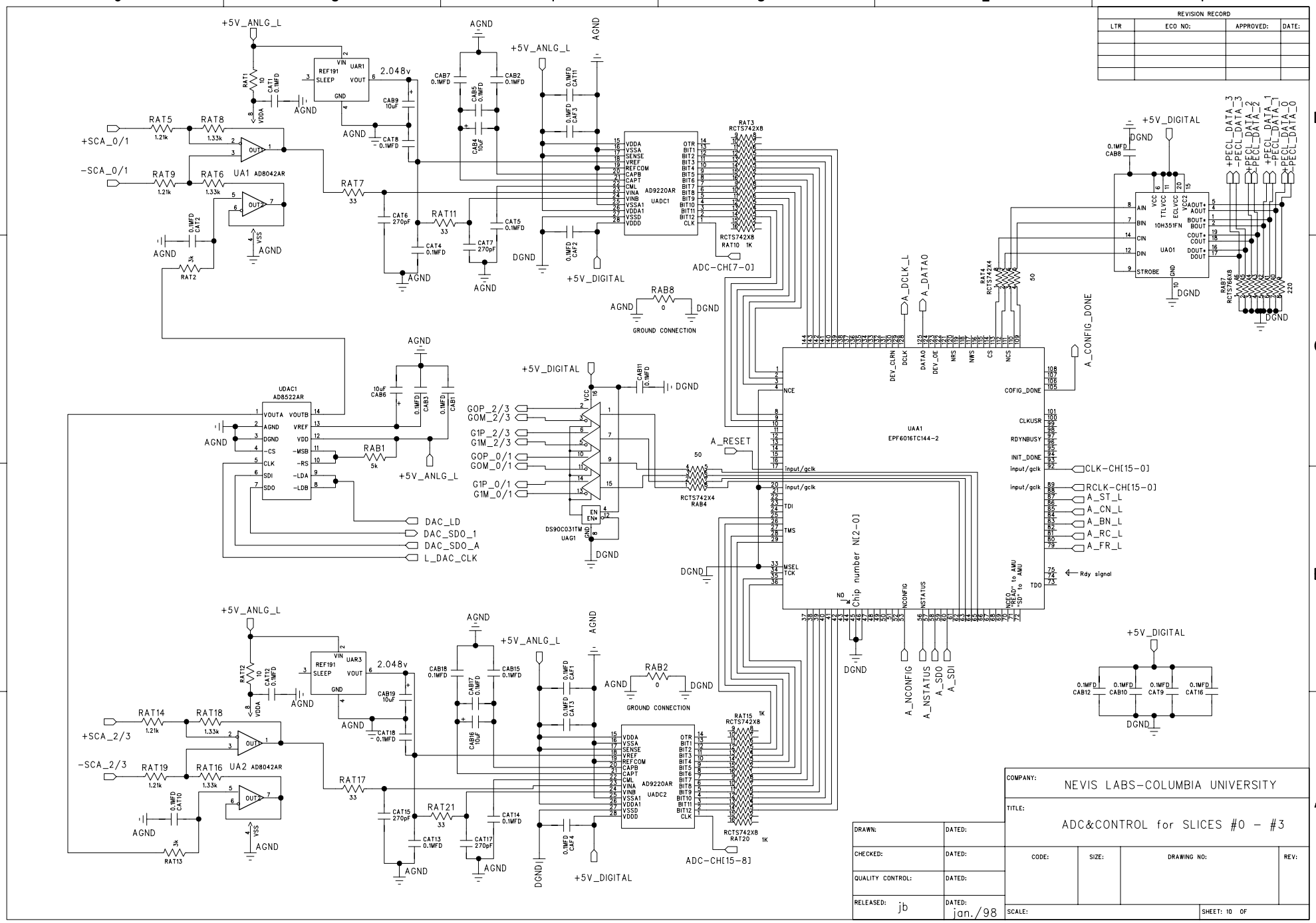
TITLE: SLICE#17 SCHEMATICS

DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED: jb	DATED: jan./98	SCALE:		SHEET: 9 OF	

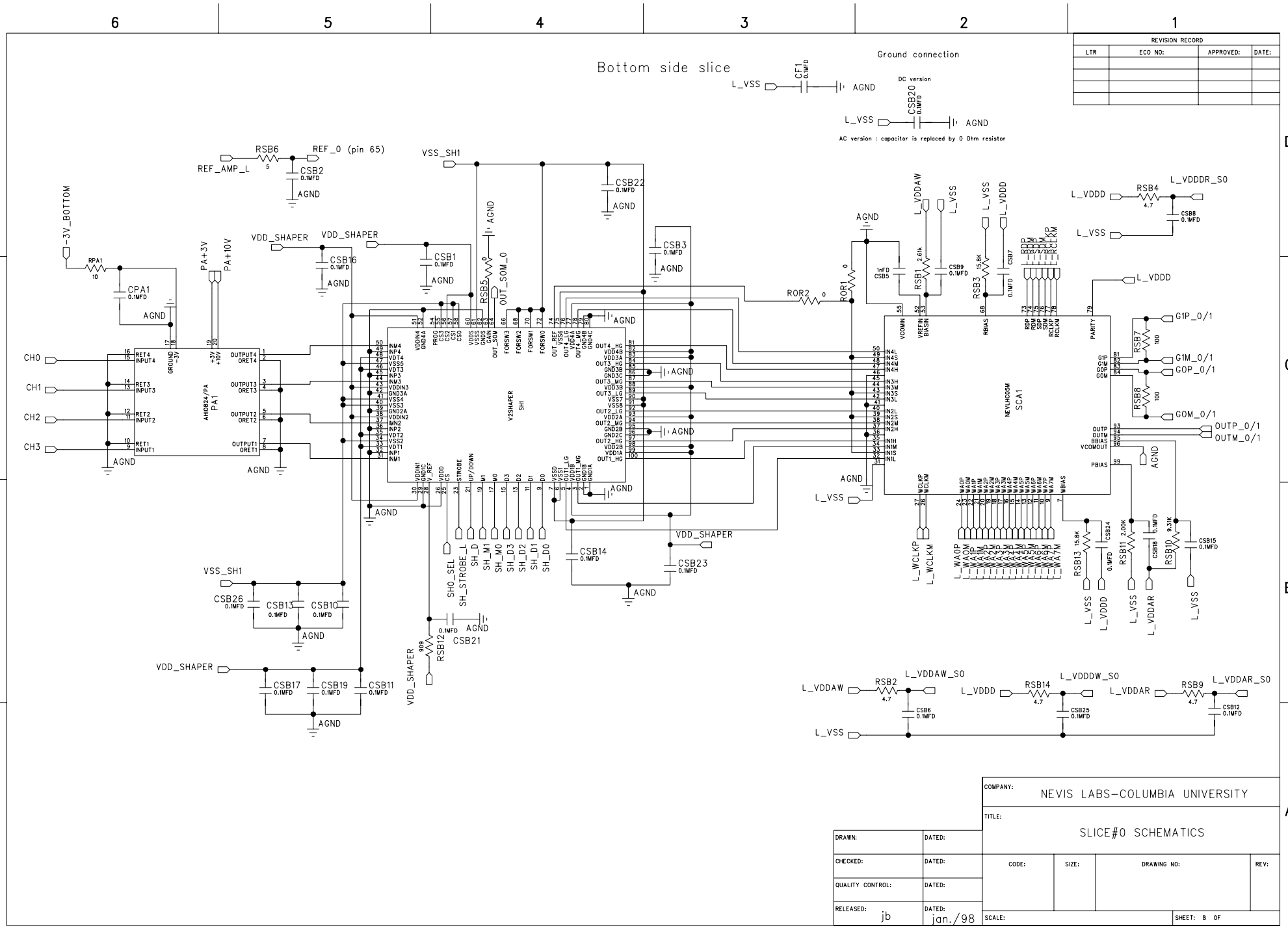

Bottom side slice
Ground connection
DC version
AC version : capacitor is replaced by 0 Ohm resistor
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
AH0824/PA
PA17
V2SHAPER
SH17
NEVLHC05M
SCA17
CH64
CH65
CH66
CH67
REF_AMP_R
REF_16 (pin 65)
VSS_SH2
VDD_SHAPER
-3V_BOTTOM
PA+3V
PA+10V
AGND
R_VSS
R_VDDD
R_VDDAW
R_VDDAR
R_VDDDR_S16
R_VDDAW_S16
R_VDDDW_S16
R_VDDAR_S16
G1P_16/17
G1M_16/17
GOP_16/17
GOM_16/17
OUTP_16/17
OUTM_16/17
SH8_SEL
SH_STROBE_R
SH_D
SH_M1
SH_M0
SH_D3
SH_D2
SH_D1
SH_D0
R_WCLKP
R_WCLKM
R_WAOP
R_WAOM
R_WA1P
R_WA1M
R_WA2P
R_WA2M
R_WA3P
R_WA3M
R_WA4P
R_WA4M
R_WA5P
R_WA5M
R_WA6P
R_WA6M
R_WA7P
R_WA7M
R_RDP
R_RDM
R_RCLKP
R_RCLKM
R_VDDAW
R_VDDD
R_VDDAR
R_VSS
CF17
CSB222
CSB230
CSB211
CSB209
CSB224
CSB234
CSB221
CSB218
CSB225
CSB227
CSB219
CSB229
CSB222
CSB231
CSB213
CSB217
CSB215
CSB216
CSB214
CSB233
CSB220
CSB232
CSB226
CSB223
RSB118
RSB117
RSB113
RSB115
RSB116
RSB119
RSB120
RSB125
RSB123
RSB122
RSB124
RSB114
RSB126
RSB121
RPA17
CPA17
RPA17
RSB117
OUT_SOM_16
RSB113
RSB115
RSB116
RSB119
RSB120
RSB122
RSB123
RSB124
RSB125
RSB126
RSB121
CSB210
CSB224
CSB209
CSB230
CSB211
CSB213
CSB215
CSB216
CSB217
CSB222
CSB231
CSB234
CSB221
CSB218
CSB225
CSB227
CSB219
CSB229
CSB232
CSB226
CSB223
CSB214
CSB233
CSB220
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SLICE#16 SCHEMATICS
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
jb
DATED:
jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 8 OF

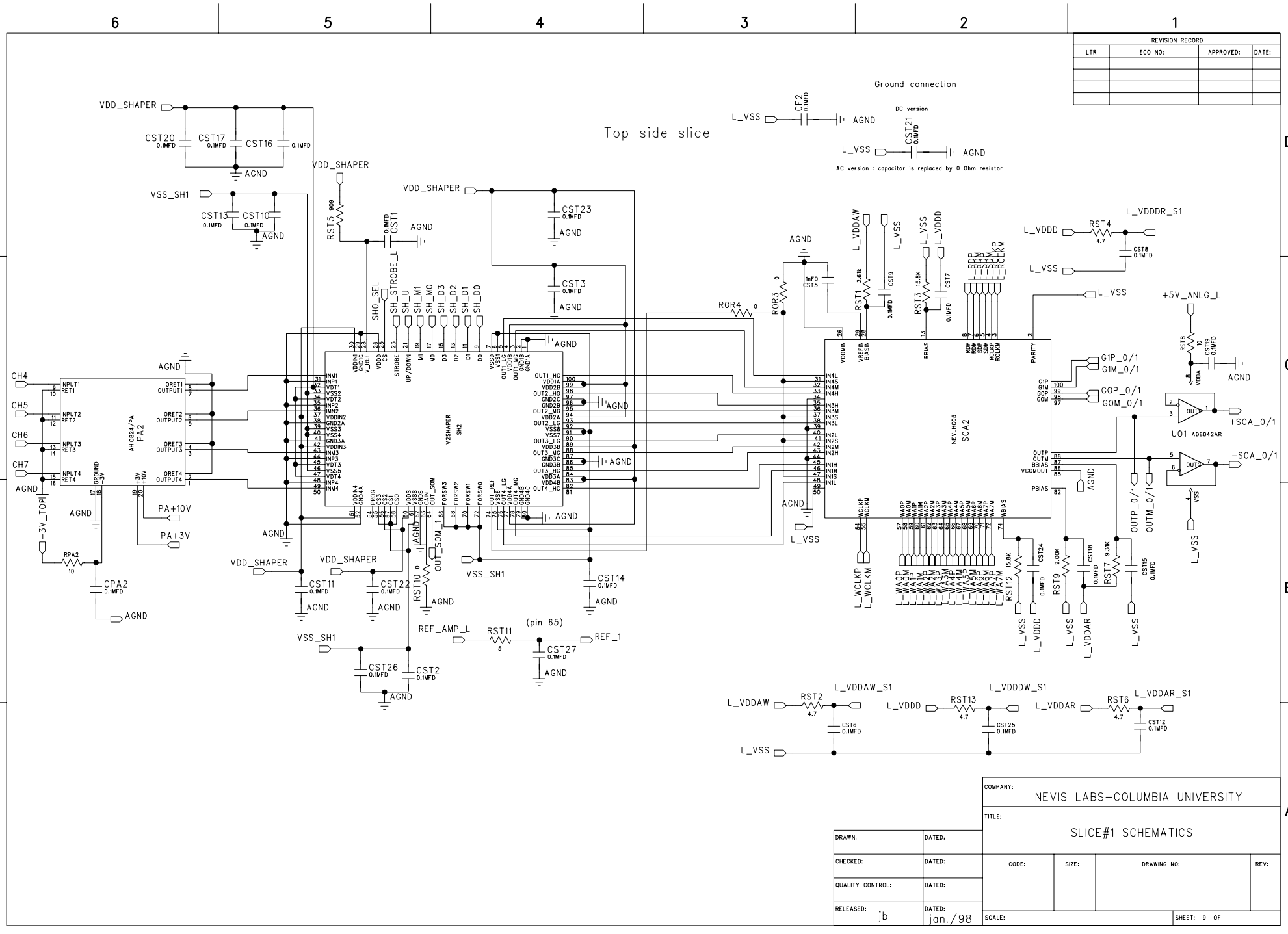

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
ADC CLOCKS
ALTERA CLOCKS
ADC CLOCKS
XILINX CLOCKS
ADC CLOCKS
ALTERA CLOCKS
ADC CLOCKS
OUT_CLK_R
SPAC_40MHZ
OUT CLOCK
OUT_CLK_L
CLK_SER_CNTRL
ADC_CH[127-120]
ADC_CH[119-112]
ADC_CH[111-104]
ADC_CH[103-96]
RCLK_CH[127-112]
RCLK_CH[111-96]
CLK_CH[127-112]
CLK_CH[111-96]
CLK_CH[95-80]
CLK_CH[79-64]
RCLK_CH[95-80]
RCLK_CH[79-64]
ADC_CH[95-88]
ADC_CH[87-80]
ADC_CH[79-72]
ADC_CH[71-64]
R_CLK/XILINX-F/8
R_CLK/XILINX-1F
L_CLK/XILINX-F/8
L_CLK/XILINX-1F
ADC_CH[63-56]
ADC_CH[55-48]
ADC_CH[47-40]
ADC_CH[39-32]
RCLK_CH[63-48]
CLK_CH[63-48]
CLK_CH[47-32]
CLK_CH[31-16]
RCLK_CH[47-32]
RCLK_CH[31-16]
RCLK_CH[15-0]
RCLK_CH[15-01]
ADC_CH[31-24]
ADC_CH[23-16]
ADC_CH[15-8]
ADC_CH[7-0]
+5V_DIGITAL
DGND
VBB
REC_CLOCK
-WCLK_IN
RCLK_SKEWED
RCLK_IN
RCLK_NT
-WCLK_SKEWED
L_VDDD
L_VSS
R_VDDD
R_VSS
AMU CLK BUS
L_+WCLK
L_-WCLK
R_+WCLK
R_-WCLK
L_+RCLK
L_-RCLK
R_+RCLK
R_-RCLK
EGG00302.CLL
MC10H105FN
MC10H641FN
MC10H016FN
MC10EL16D
RCTS742X8
RCTS766X8
COMPANY:
NEVIS LABS – COLUMBIA UNIVERSITY
TITLE:
CLOCK FANOUT SCHEME
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
jb
DATED:
march/98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: OF


6
5
4
3
2
1
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
SHD0
SHD1
SHD2
SHD3
1k
RCTS742X4 RA44
Q1D
Q1C
Q1B
Q1A
560
RCTS742X4 RA40
3.3k
RCTS742X4 RA38
SH_D0
SH_D1
SH_D2
SH_D3
VSS_SH2
DGND
SHM0
SHM1
SHU
SHD
1.2k
RCTS742X4 RA47
Q2D
Q2C
Q2B
Q2A
680
RCTS742X4 RA39
2.7k
RCTS742X4 RA37
SH_M0
SH_M1
SH_U
SH_D
VSS_SH2
DGND
SH0SEL
SH1SEL
SH2SEL
SH3SEL
1.2k
RCTS742X4 RA49
Q3D
Q3C
Q3B
Q3A
680
RCTS742X4 RA43
2.7k
RCTS742X4 RA41
SH0_SEL
SH1_SEL
SH2_SEL
SH3_SEL
VSS_SH2
DGND
SH4SEL
SH5SEL
SH6SEL
SH7SEL
1.2k
RCTS742X4 RA52
Q4D
Q4C
Q4B
Q4A
680
RCTS742X4 RA42
2.7k
RCTS742X4 RA45
SH4_SEL
SH5_SEL
SH6_SEL
SH7_SEL
VSS_SH2
DGND
SH8SEL
SH9SEL
SH10SEL
SH11SEL
1.2k
RCTS742X4 RA53
Q5D
Q5C
Q5B
Q5A
680
RCTS742X4 RA50
2.7k
RCTS742X4 RA46
SH8_SEL
SH9_SEL
SH10_SEL
SH11_SEL
VSS_SH2
DGND
SH12SEL
SH13SEL
SH14SEL
SH15SEL
1.2k
RCTS742X4 RA54
Q6D
Q6C
Q6B
Q6A
680
RCTS742X4 RA51
2.7k
RCTS742X4 RA48
SH12_SEL
SH13_SEL
SH14_SEL
SH15_SEL
VSS_SH2
DGND
SH_D0_IN
SH_D1_IN
SH_D2_IN
SH_D3_IN
RA26 RCTS742X4
3.3k
RA22 RCTS742X4
3.3k
VCC+3.3V
Q8A
Q8B
Q8C
Q8D
RA24 RCTS742X4
6.8k
SH_D0
SH_D1
SH_D2
SH_D3
VSS_SH2
SHSTROBEL
RR19
700
Q7A
DGND
RR20
1k
RR25
100
RR26
50
SH_STROBE_L
VSS_SH2
SHSTROBER
RR27
700
Q7D
DGND
RR28
1k
RR29
100
RR30
50
SH_STROBE_R
VSS_SH2
COMPANY:
NEVIS LABS – COLUMBIA UNIVERSITY
TITLE:
Level shifters for shaper cntrl lines
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
jb
DATED:
jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF



REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+5V_ANLG_L
AGND
DGND
+5V_DIGITAL
+SCA_0/1
-SCA_0/1
RAT5 1.21k
RAT8 1.33k
RAT9 1.21k
RAT6 1.33k
UA1 AD8042AR
RAT7 33
RAT11 33
RAT2 3k
REF191 UAR1
2.048v
CAB9 10uF
CAB7 0.1MFD
CAB2 0.1MFD
CAB5 0.1MFD
CAB4 10uF
CAT8 0.1MFD
CAT6 270pF
CAT4 0.1MFD
CAT7 270pF
CAT5 0.1MFD
AD9220AR UADC1
RAT3 RCTS742X8
RCTS742X8 RAT10 1K
ADC-CH[7-0]
RAB8 0
GROUND CONNECTION
UDAC1 AD8522AR
RAB1 5k
DAC_LD
DAC_SDO_1
DAC_SDO_A
L_DAC_CLK
GOP_2/3
GOM_2/3
G1P_2/3
G1M_2/3
GOP_0/1
GOM_0/1
G1P_0/1
G1M_0/1
DS90C031TM UAG1
A_RESET
RCTS742X4 RAB4
UAA1 EPF6016TC144-2
Chip number N[2-0]
A_DCLK_L
A_DATA0
A_CONFIG_DONE
CLK-CH[15-0]
RCLK-CH[15-0]
A_ST_L
A_CN_L
A_BN_L
A_RC_L
A_FR_L
Rdy signal
A_NCONFIG
A_NSTATUS
A_SDO
A_SDI
+PECL_DATA_3
-PECL_DATA_3
+PECL_DATA_2
-PECL_DATA_2
+PECL_DATA_1
-PECL_DATA_1
+PECL_DATA_0
-PECL_DATA_0
10H351FN UA01
RAB7 RCTS766X8
+SCA_2/3
-SCA_2/3
RAT14 1.21k
RAT18 1.33k
RAT19 1.21k
RAT16 1.33k
UA2 AD8042AR
RAT17 33
RAT21 33
RAT13 3k
RAB2 0
RAT15 RCTS742X8
RCTS742X8 RAT20 1K
ADC-CH[15-8]
COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY
TITLE: ADC&CONTROL for SLICES #0 - #3
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED: jb
DATED: jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 10 OF


Bottom side slice
Ground connection
DC version
AC version : capacitor is replaced by 0 Ohm resistor
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
-3V_BOTTOM
REF_AMP_L
REF_0 (pin 65)
VSS_SH1
VDD_SHAPER
PA+3V
PA+10V
OUT_SOM_0
L_VSS
L_VDDAW
L_VDDD
L_VDDDR_S0
L_VDDAW_S0
L_VDDDW_S0
L_VDDAR_S0
AGND
CH0
CH1
CH2
CH3
AHH0824/PA
PA1
VZSHAPER
SH1
NEVLHC05M
SCA1
SH0_SEL
SH_STROBE_L
SH_D
SH_M1
SH_M0
SH_D3
SH_D2
SH_D1
SH_D0
L_WCLKP
L_WCLKM
L_WAOP
L_WAOM
G1P_0/1
G1M_0/1
GOP_0/1
GOM_0/1
OUTP_0/1
OUTM_0/1
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SLICE#0 SCHEMATICS
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 8 OF

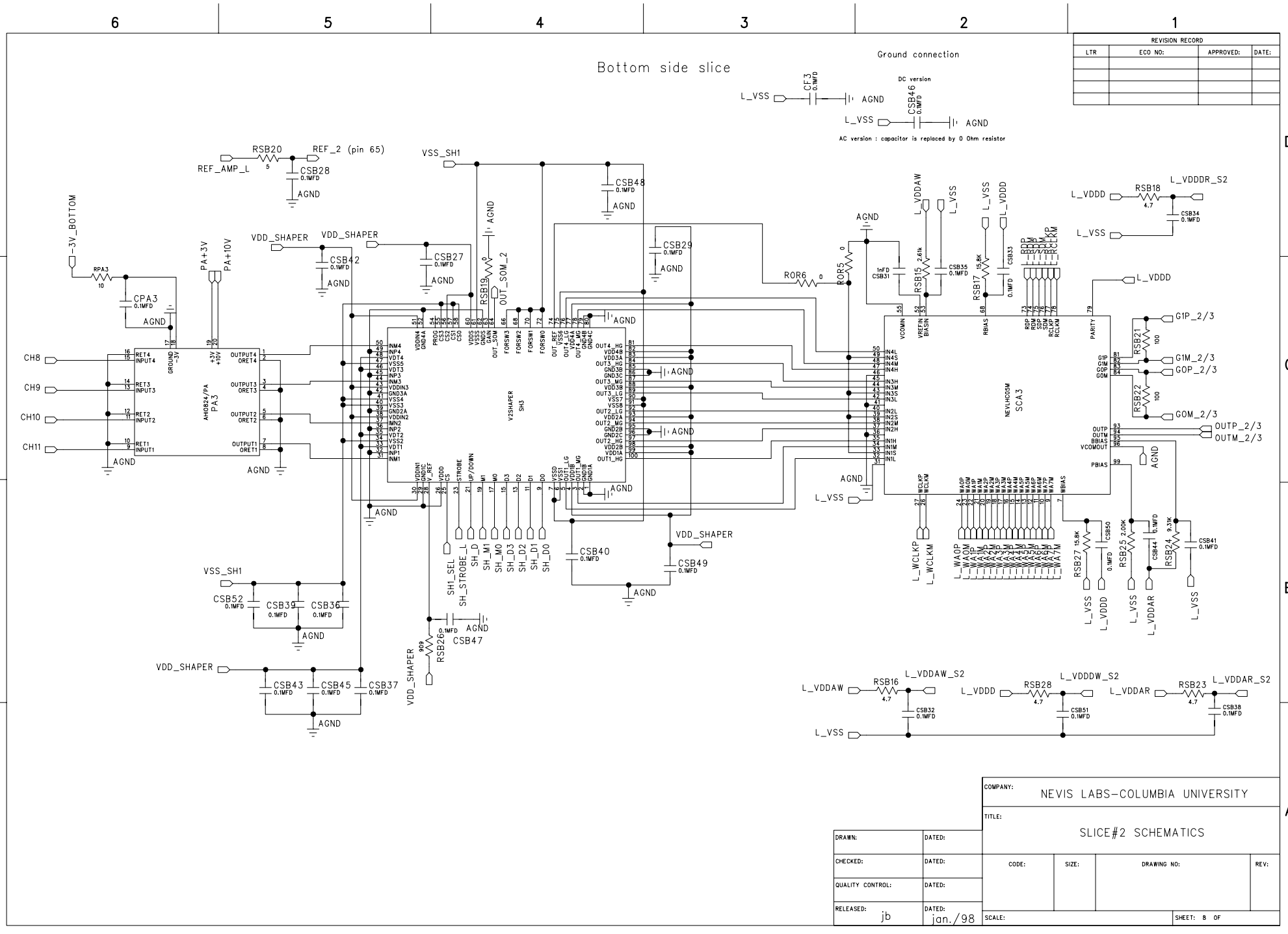


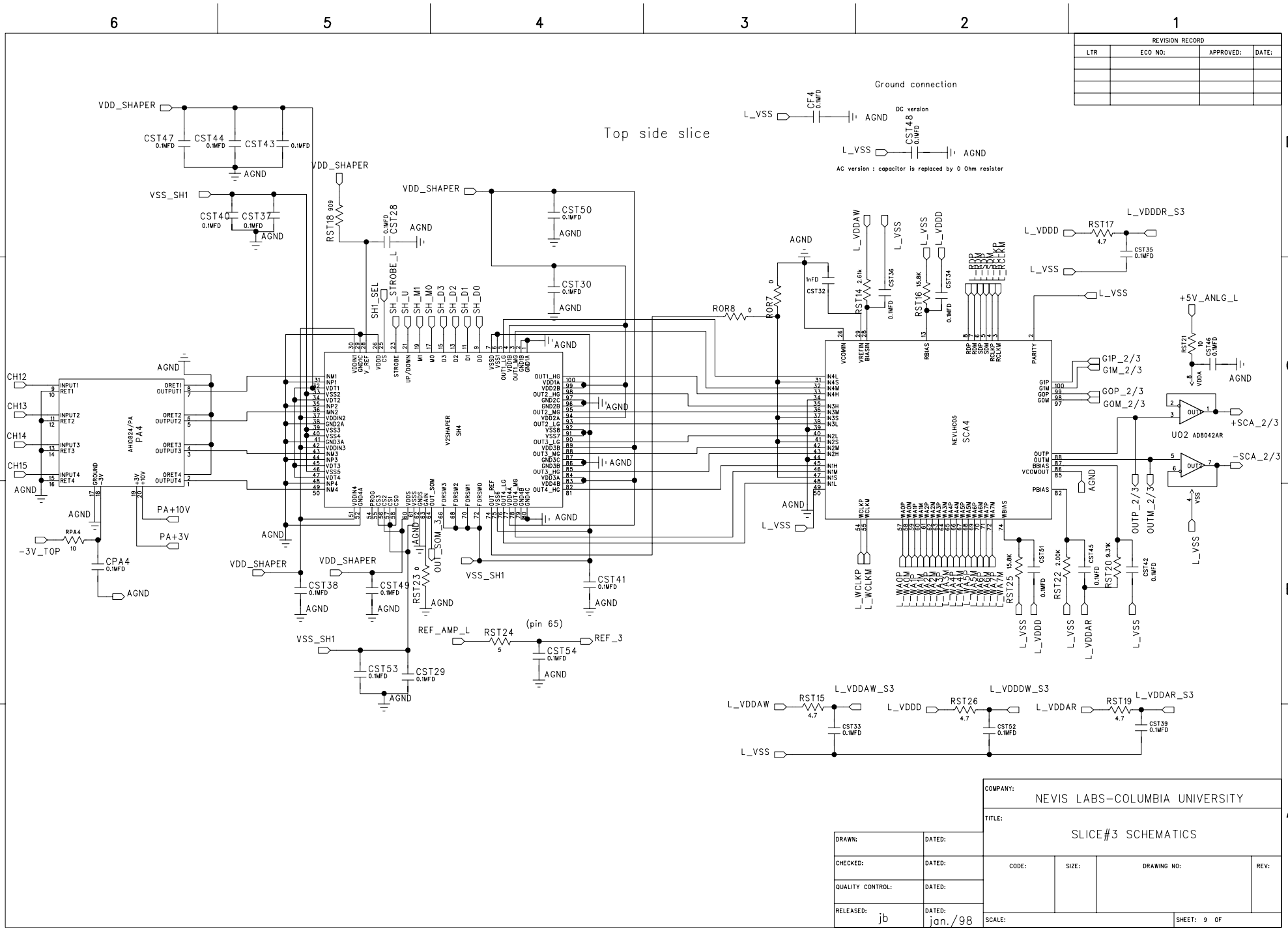
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY

TITLE: SLICE#1 SCHEMATICS

DRAWN:	DATED:				
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED: jb	DATED: jan./98	SCALE:		SHEET: 9 OF	


Bottom side slice
Ground connection
DC version
AC version : capacitor is replaced by 0 Ohm resistor
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
AH0824/PA
PA3
V2SHAPER
SH3
NEVLHC05M
SCA3
CH8
CH9
CH10
CH11
REF_AMP_L
REF_2 (pin 65)
VSS_SH1
VDD_SHAPER
-3V_BOTTOM
PA+3V
PA+10V
OUT_SOM_2
L_VSS
L_VDDD
L_VDDAW
L_VDDAR
L_VDDDR_S2
L_VDDAW_S2
L_VDDDW_S2
L_VDDAR_S2
G1P_2/3
G1M_2/3
GOP_2/3
GOM_2/3
OUTP_2/3
OUTM_2/3
SH1_SEL
SH_STROBE_L
SH_D
SH_M1
SH_M0
SH_D3
SH_D2
SH_D1
SH_D0
L_WCLKP
L_WCLKM
AGND
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SLICE#2 SCHEMATICS
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
jb
DATED:
jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 8 OF

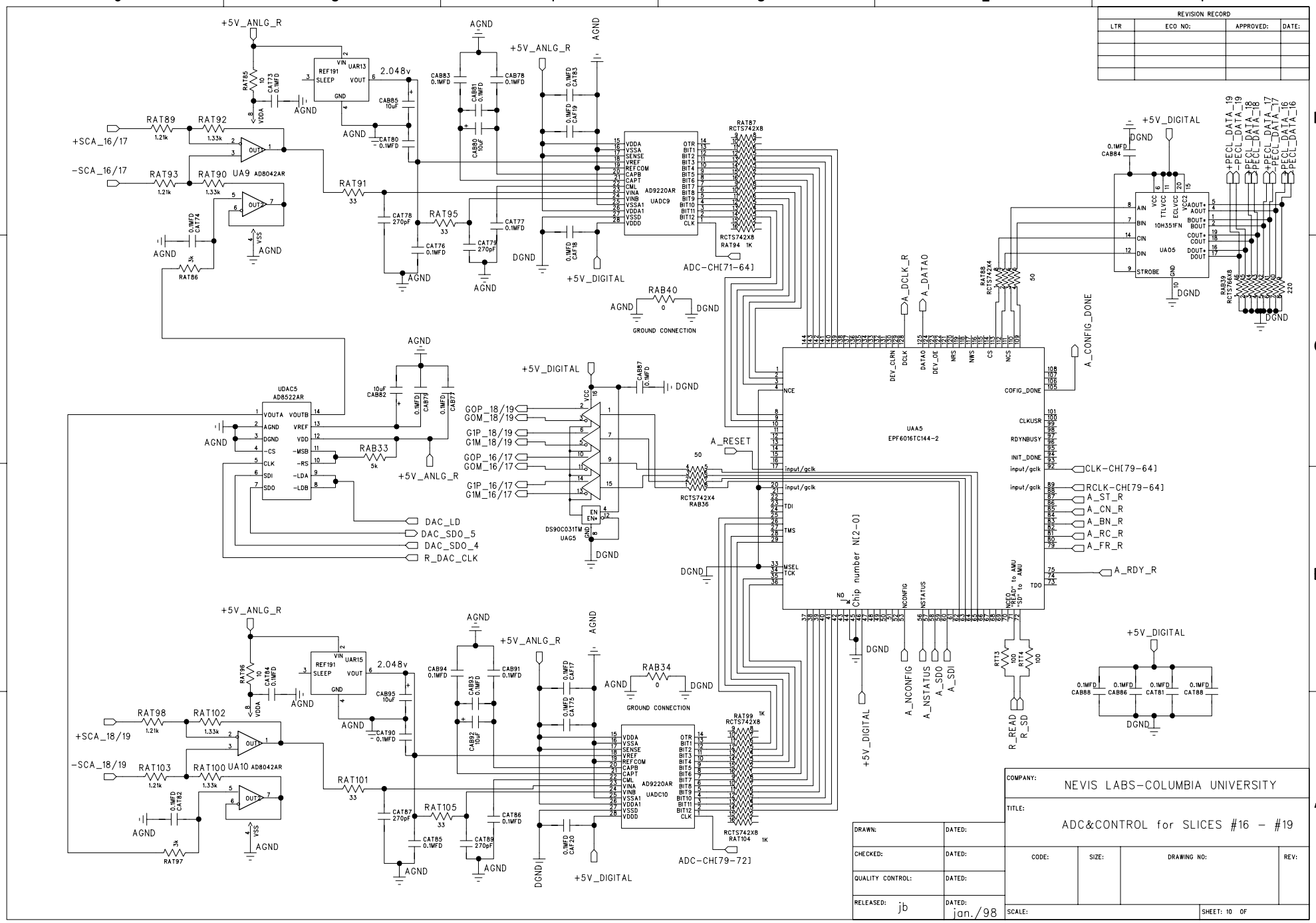


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY

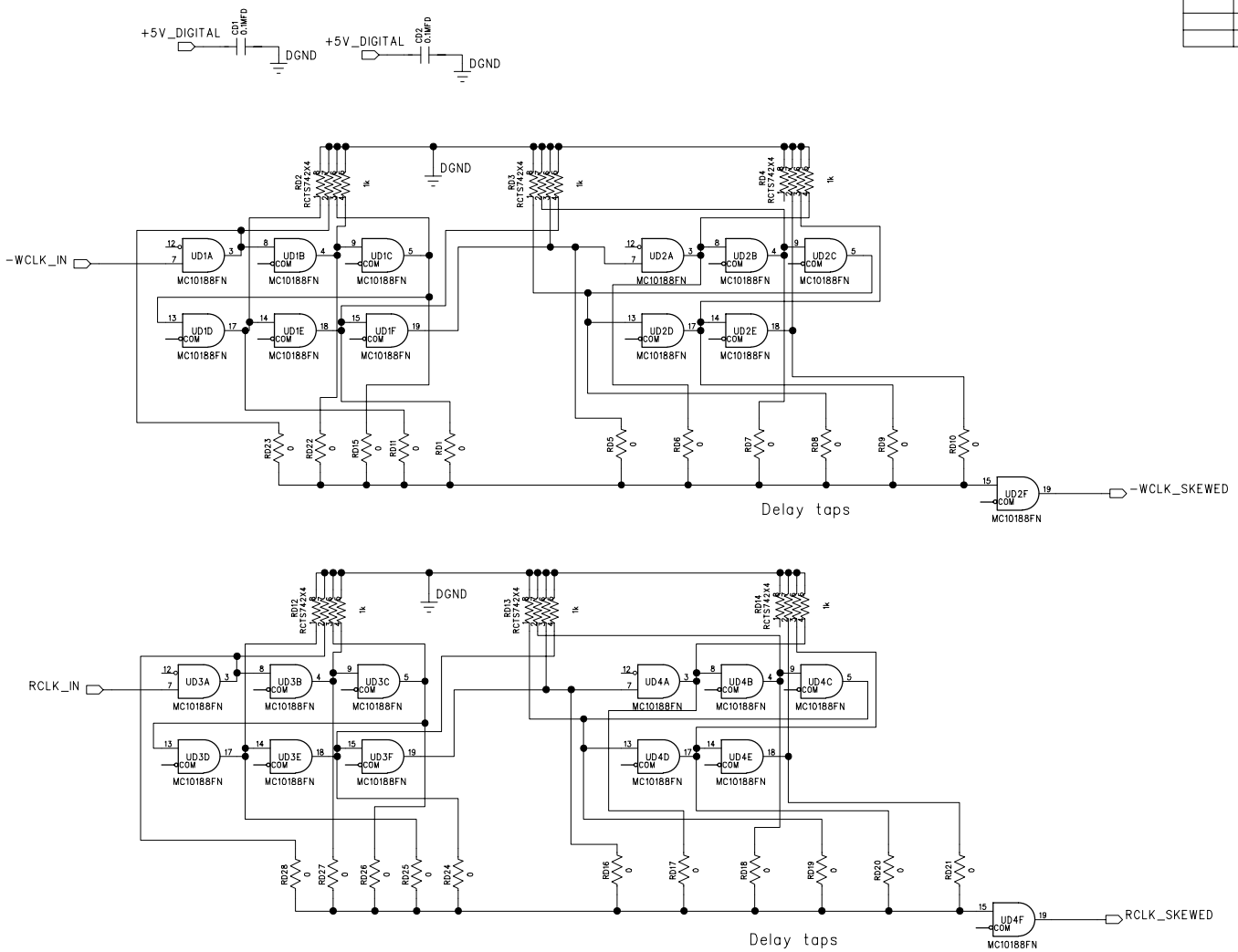
TITLE: SLICE#3 SCHEMATICS

DRAWN:	DATED:				
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED: jb	DATED: jan./98	SCALE:		SHEET: 9 OF	

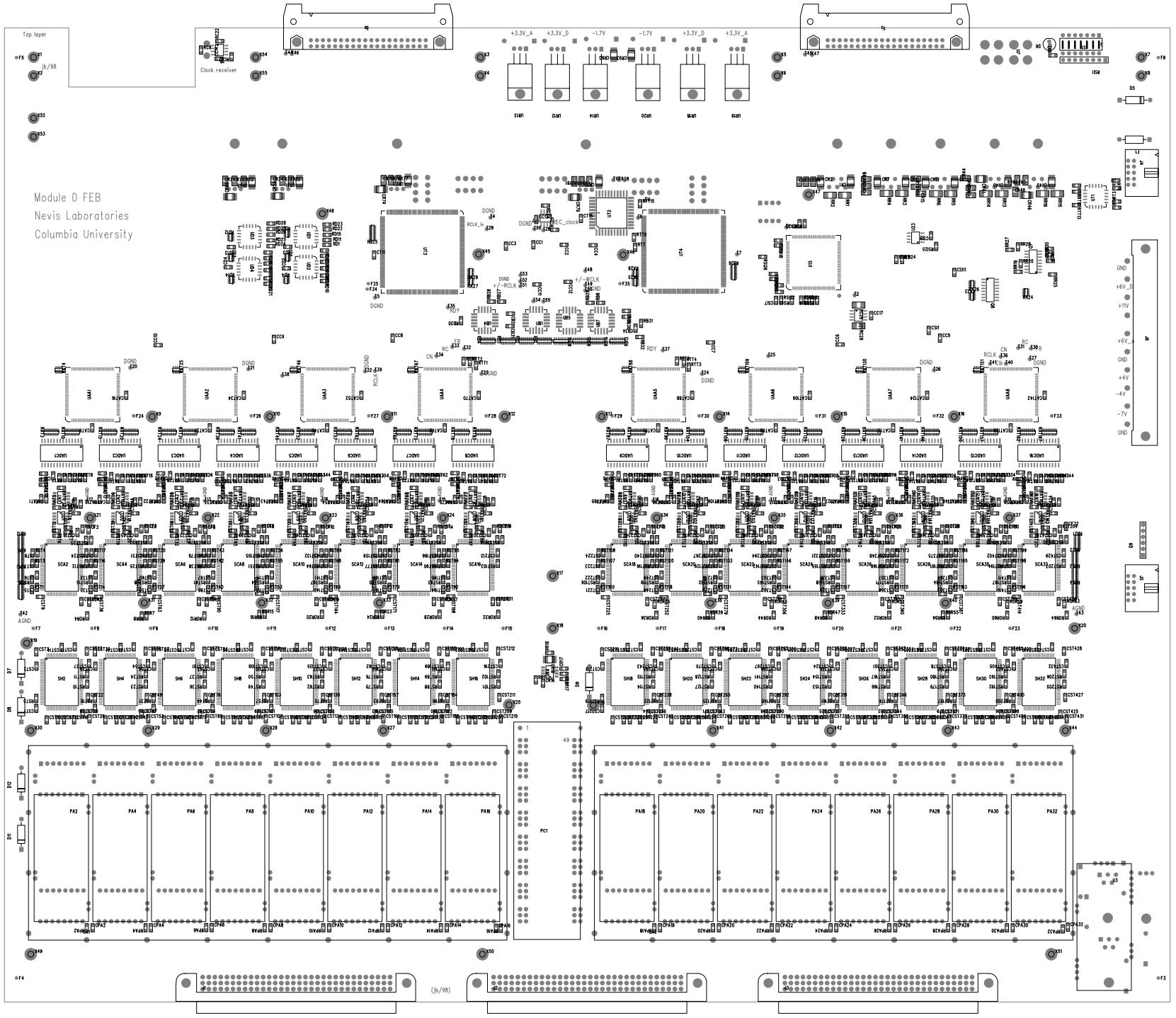


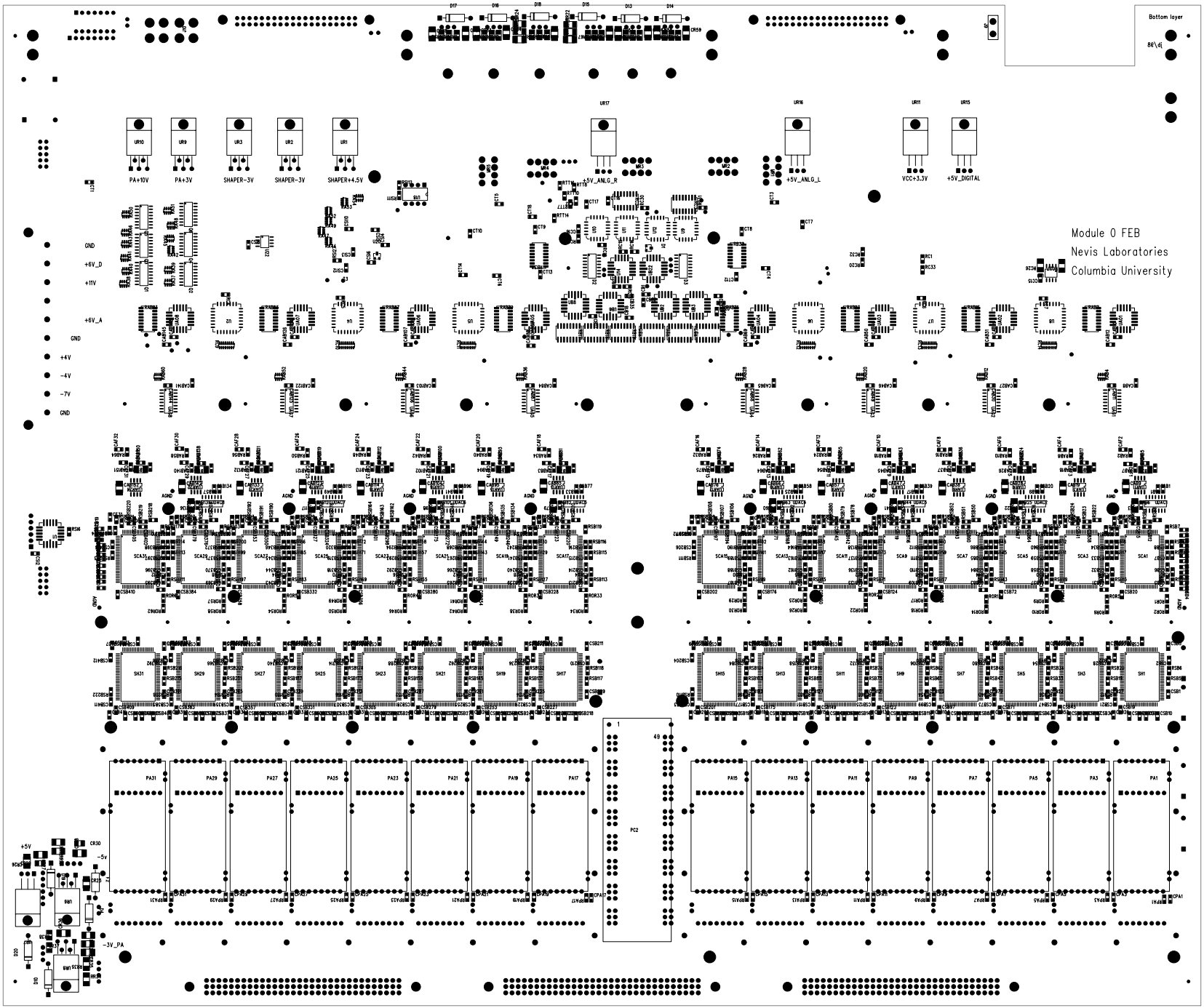
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+5V_ANLG_R
AGND
+5V_DIGITAL
DGND
+SCA_16/17
-SCA_16/17
RAT89
RAT92
RAT93
RAT90
UA9 AD8042AR
RAT91
RAT95
RAT86
RAT85
CAT73 0.1MFD
REF191
UAR13
SLEEP
VOUT
GND
2.048v
CAB85 10uF
CAT80 0.1MFD
CAB83 0.1MFD
CAB81 0.1MFD
CAB78 0.1MFD
CAB80 10uF
CAT83 0.1MFD
CAF19 0.1MFD
CAT78 270pF
CAT76 0.1MFD
CAT79 270pF
CAT77 0.1MFD
CAF18 0.1MFD
AD9220AR
UADC9
RAT87 RCTS742X8
RCTS742X8 RAT94 1K
ADC-CH[71-64]
RAB40
GROUND CONNECTION
UDAC5 AD8522AR
VOUTA
VOUTB
AGND
DGND
-CS
CLK
SDI
SDO
VREF
VDD
-MSB
-RS
-LDA
-LDB
RAB33
5k
CAB82 10uF
CAB79 0.1MFD
CAB77 0.1MFD
DAC_LD
DAC_SDO_5
DAC_SDO_4
R_DAC_CLK
GOP_18/19
GOM_18/19
G1P_18/19
G1M_18/19
GOP_16/17
GOM_16/17
G1P_16/17
G1M_16/17
DS90C031TM
UAG5
CAB87 0.1MFD
A_RESET
RCTS742X4 RAB36
UAA5
EPF6016TC144-2
input/gclk
TDI
TMS
MSEL
TCK
NCE
DEV_CLRN
DCLK
DATA0
DEV_OE
NRS
NWS
CS
NCS
COFIG_DONE
CLKUSR
RDYNBUSY
INIT_DONE
CLK-CH[79-64]
RCLK-CH[79-64]
A_ST_R
A_CN_R
A_BN_R
A_RC_R
A_FR_R
A_RDY_R
A_DCLK_R
A_DATA0
A_CONFIG_DONE
Chip number N[2-0]
NCONFIG
NSTATUS
A_NCONFIG
A_NSTATUS
A_SDO
A_SDI
RT73 100
RT74 100
R_READ
R_SD
+PECL_DATA_19
-PECL_DATA_19
+PECL_DATA_18
-PECL_DATA_18
+PECL_DATA_17
-PECL_DATA_17
+PECL_DATA_16
-PECL_DATA_16
CAB84 0.1MFD
10H351FN
UA05
AIN
BIN
CIN
DIN
STROBE
VCC
TTLVCC
ECLVCC
VCC2
AOUT+
AOUT
BOUT+
BOUT
COUT+
COUT
DOUT+
DOUT
RAB39 RCTS766X8
220
+SCA_18/19
-SCA_18/19
RAT98
RAT102
RAT103
RAT100
UA10 AD8042AR
RAT96
CAT84 0.1MFD
RAT97
CAT82 0.1MFD
RAT101
RAT105
CAB95 10uF
CAT90 0.1MFD
CAB94 0.1MFD
CAB93 0.1MFD
CAB92 10uF
CAB91 0.1MFD
CAF17 0.1MFD
CAF75 0.1MFD
CAT87 270pF
CAT85 0.1MFD
CAT89 270pF
CAT86 0.1MFD
CAF20 0.1MFD
RAB34
RAT99 RCTS742X8
RCTS742X8 RAT104 1K
ADC-CH[79-72]
CAB88 0.1MFD
CAB86 0.1MFD
CAT81 0.1MFD
CAT88 0.1MFD
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
ADC&CONTROL for SLICES #16 - #19
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED: jb
DATED: jan./98
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 10 OF

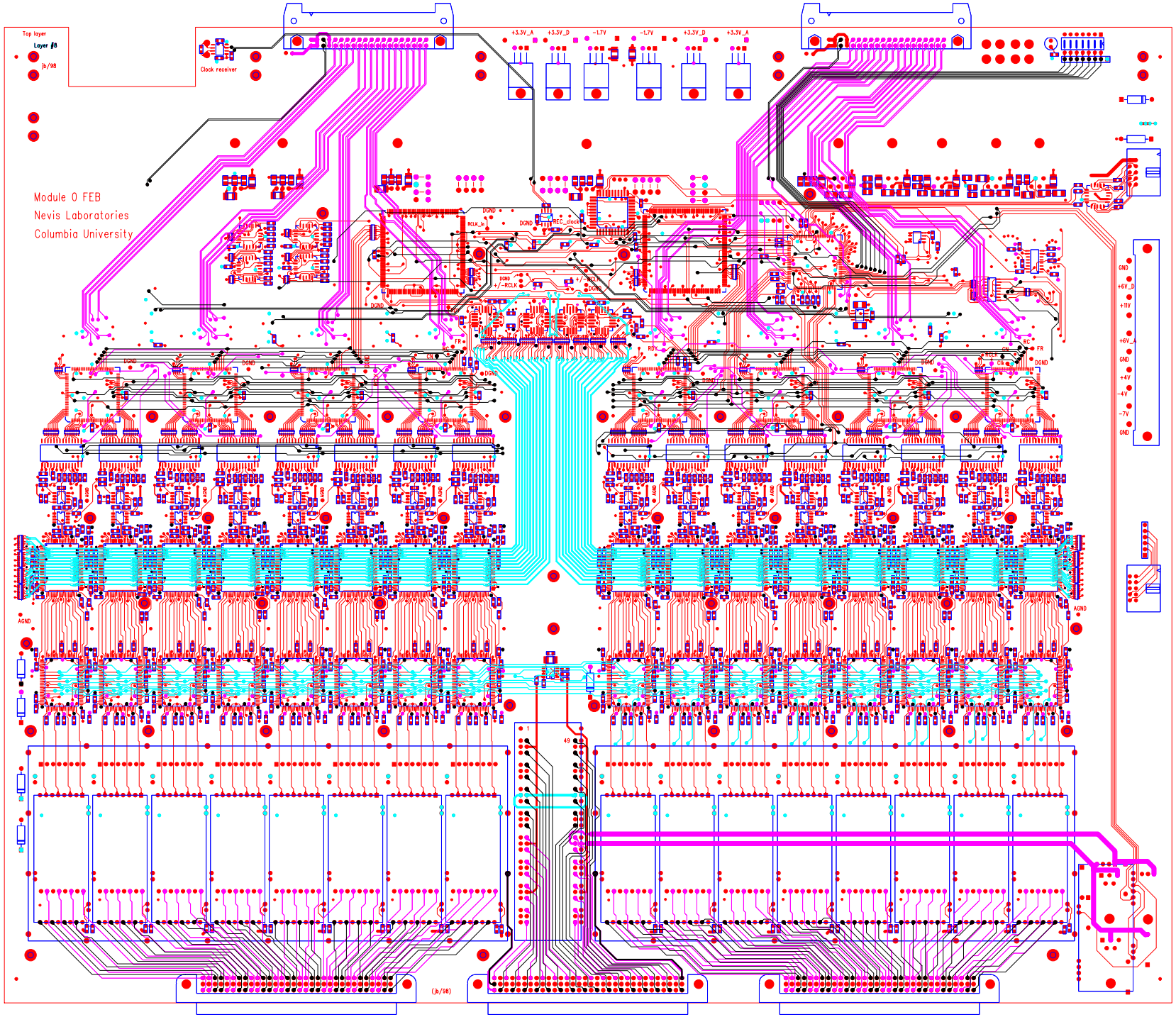
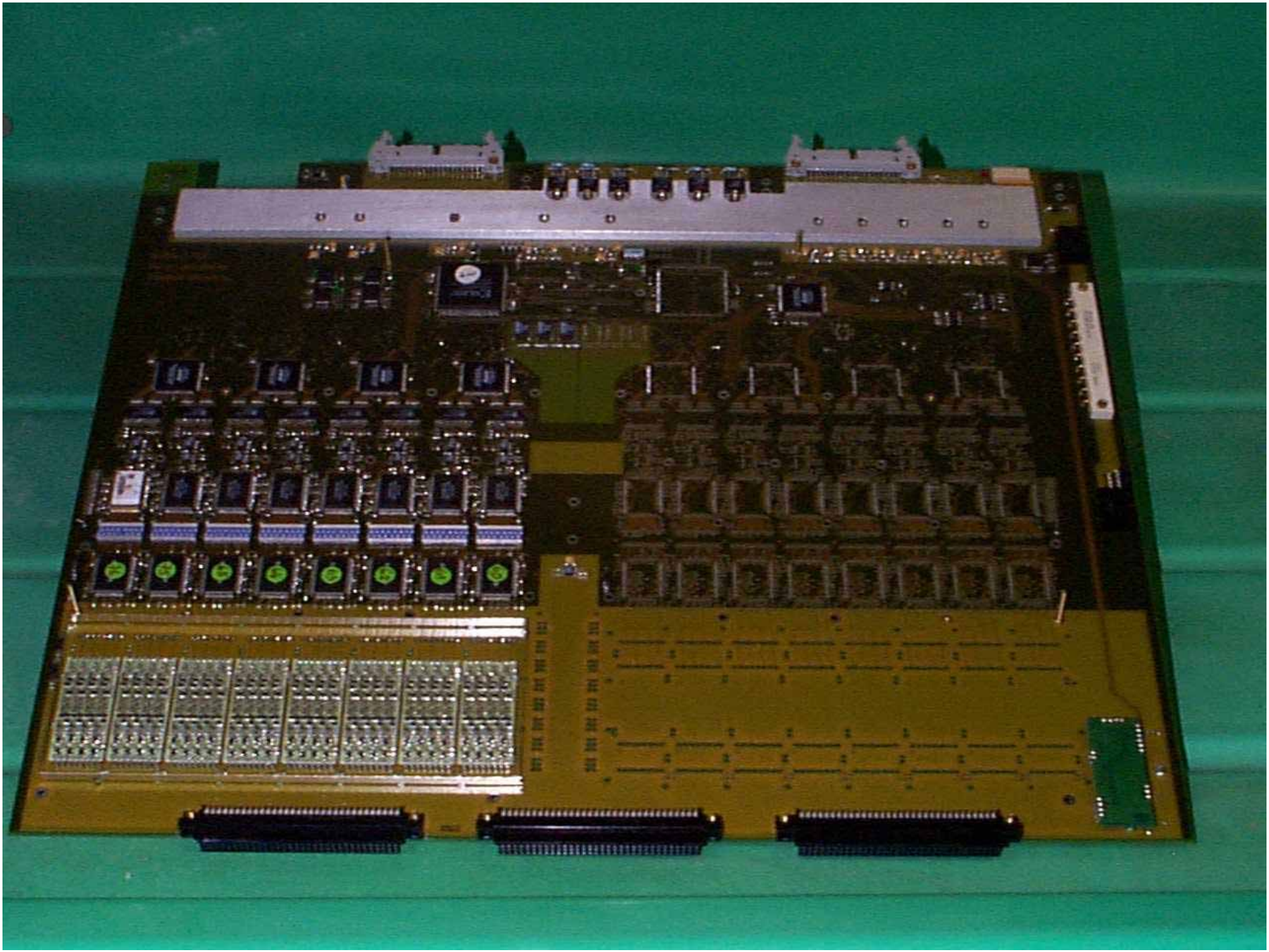
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN:	DATED:	COMPANY: NEVIS LABS – COLUMBIA UNIVERSITY			
CHECKED:	DATED:	TITLE: CLOCK delay			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
RELEASED:	DATED: march/98	SCALE:		SHEET: OF	


Top layer
jb/98
Clock receiver
Module 0 FEB
Nevis Laboratories
Columbia University
+3.3V_A
+3.3V_D
-1.7V
-1.7V
+3.3V_D
+3.3V_A
DGND
RCLK_in
SEC_clock
+/-RCLK
+/-WCLK
RDY
RC
CN
RCLK
AGND
+6V_D
+11V
+6V_A
+4V
-4V
-7V
PC1
(jb/98)


Bottom layer
Module 0 FEB
Nevis Laboratories
Columbia University
PA+10V
PA+3V
SHAPER-3V
SHAPER-3V
SHAPER+4.5V
+5V_ANLG_R
+5V_ANLG_L
VCC+3.3V
+5V_DIGITAL
GND
+6V_D
+11V
+6V_A
GND
+4V
-4V
-7V
GND
+5V
-5V
-3V_PA


Top layer
Layer #8
jb/98
Clock receiver
Module 0 FEB
Nevis Laboratories
Columbia University
+3.3V_A
+3.3V_D
-1.7V
-1.7V
+3.3V_D
+3.3V_A
DGND
RCLK_in
REC_clock
+/-RCLK
FR
RC
CN
RDY
GND
+6V_D
+11V
+6V_A
+4V
-4V
-7V
AGND
(jb/98)